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Continuous-Time Analog Filtering: Design Strategies and Programmability in CMOS Technologies for VHF Applications

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1. Introduction

The evolution of wireless applications (the performance as well as the number of users) has undergone explosive growth in the last years, resulting in an increasing demand for smaller, low-cost wireless transceivers with low power consumption. In order to meet this demand, continuous development must take place both in CMOS technology and in RF electronics, the goal of which should be to achieve a fully-integrated single-chip receiver in a low-cost CMOS process. This demand for complex read channel and multi-standard receiver ICs calls for the design and implementation of one category of analog interface chips as continuous-time (CT) filters, suitable for high speed with variable bandwidths over a wide frequency range, preferably using the G_m -C approach rather than other existing solutions.

Filters based on the G_m -C technique were used quite early on with bipolar technology and they have now become the dominant option to implement monolithic filters for very high frequency. The basic building block of a G_m -C filter is the integrator, which involves the use of transconductors and capacitors only and whose structure is therefore simpler than others, such as operational amplifiers. The simplicity of the transconductor coupled with the open-loop operation, which does not involve any complex frequency compensation schemes, point to this cell as the basic active element to be considered and the best option to operate in a VHF range with low supply voltages.

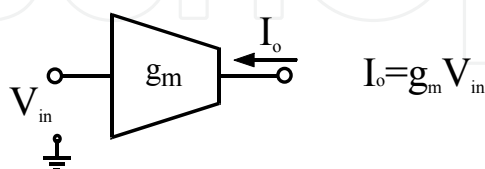


Fig. 1. Ideal transconductor V_{in} to I_o converter of transconductance g_m (conversion factor).

All the benefits of the G_m -C approach lie in the ideal behaviour of the transconductor. Nevertheless, its use as the basic element in the VHF active filter implementation forces one to consider some drawbacks related with the non-idealities of this fundamental cell: finite output resistance, finite bandwidth, noise, non-linearity, etc. The main disadvantages inherent to this technique are its high sensitivity to parasitic capacitors and the non-linear

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behaviour of the transconductor, to the extent of appearing a distortion brought about mainly by the non-linearities generated in the V-I conversion. Certain specific strategies require to be used to minimize these effects.

By taking differential or balanced transconductor structures into account, distortion is reduced (even non-linear components are cancelled) and better immunity to common-mode noise is obtained. Furthermore, the use of tuning techniques compensates parameter deviations due to process and temperature variations. These ideas, together with a careful layout, a detailed study of the technology and a deep analysis of the device, lead to an improvement in the transconductor behaviour, and consequently, in the filter performance. Thus, while developing the design of an active G_m -C filter, the effects of transconductor non-idealities must be analysed in depth to achieve optimum filter performance. The implementation of the transconductor should show a trade-off between dc-gain, linearity and low phase-error at the cut-off frequency.

Any pole or zero frequency in filters based on the G_m -C technique is of the G_m/C type. This means that there are two fundamental ways of programming the frequency response of the filter: keeping G_m constant and varying C , or vice versa. The choice of filter approach will affect noise and power dissipation (Pavan et al., 2000). The constant- C approach has the advantage of maintaining the noise specifications constant over the entire programming range while decreasing the power consumption for lower frequencies. Due to the above considerations, the constant- C scaling technique is the preferred approach for implementing filters operating in a very high frequency range, focusing on the design of tunable CMOS transconductors. On the other hand, discrete tuning is currently being more widely used than continuous tuning, both to preserve the dynamic range and take advantage of the digital system in mixed design to determine the control signal that calibrates and reconfigures the filter. A possible discrete tuning technique is based on a parallel connection of transconductors, where the desired time-constant can be digitally programmed (Pavan et al., 2000a). This approach succeeds in keeping the Q-factor constant and maintains an adequate dynamic range over the entire bandwidth setting.

The target is to implement a transconductor that is compatible with the latest low-cost pure digital CMOS technologies and programmable over a very high frequency range while maintaining an adequate dynamic range (DR). The concrete values of these specifications depend on each particular application. This work does not focus on a concrete application but on carrying out an overall analysis to seek the structure that provides the best trade-off between operation frequency, programmability, dynamic range and power consumption.

Considering all these points, an optimal solution for digitally programmable analog filters in the VHF/UHF range is to take advantage of current-mode pseudo-differential topologies and endow them with digital programmability. The design strategy is therefore as follows: after analysing the transconductor parameters that limit its ideal behaviour, a very well-known current-mode topology (Smith et al., 1996; Zele et al., 1996) will be characterized; starting from the Zele-Smith architecture, two different transconductors will be presented and in-depth analysis will be carried out, following which all the characteristic parameters of each active cell will be obtained; programmability will then be added to the VHF transconductors and the experimental results of a low-cost 0.35 μm CMOS implementation will be presented. As the active cell is based on a classical structure, a broad diversity of digitally programmable and continuously tunable CT filters can be obtained, where the programmability exhibited by the filter is achieved due to the design of a generic programmable transconductor. Due to the lack of special capacitor structures in standard digital technologies, the use of the MOS structure as

an intended passive device is probably as old as the MOS transistor concept itself. An alternative to implementing linear capacitors is to use the *gate-to-channel capacitance* of MOSFET devices as capacitors, where the gate-oxide thickness is a well-controlled variable in the process. This option will be considered in this work.

Therefore, in this chapter we will show the best way to implement key analog building blocks of a high-speed system in a CMOS technology with a wide programmable frequency range; considering new design techniques and uncovering potential problems associated with the design of high-speed analog circuits using short-channel and low-voltage devices. These are the challenges of CMOS filter design at very high frequencies and this study addresses the theoretical and practical problems encountered in the design of robust, programmable continuous-time filters with very high bandwidths implemented in low-cost digital CMOS technologies.

2. The Integrator: building-block in the G_m-C technique

The majority of continuous-time (CT) integrated filters, circuits where high frequency at low cost of silicon and power is required, present a frequency response controlled by time-constants, and one of the simplest implementations for these factors is taking advantage of the integrator structure. Therefore, the integrator is the dominant building block for many high-frequency active circuit design techniques, and its frequency response and linearity directly determine the filter performance.

Accordingly, systems based on the G_m-C technique are the first option for implementing CT filters, thanks to their acceptable performance over the VHF range. The active building element used by the G_m-C filter approach, based on an open-loop integrator, is the transconductor cell (Fig. 1), which ideally delivers an output current proportional to the input signal voltage:

$$I_o = g_m V_{in} \quad (1)$$

where g_m is the transconductance of the element. When a grounded capacitor is connected to the output node of the transconductor in order to take this current out, an integrator is obtained leading to V_{in} - V_o conversion, as shown in Fig. 2(a). It turns out that an ideal voltage-mode integrator has been obtained with a simple transconductance-capacitor combination. Nevertheless, a second structure can be considered taking into account the current-mode signal processing, whereby two different, yet completely equivalent, topologies are obtained. In this case, the input current is taken across the integration capacitance in order to obtain the transconductor input voltage and then, after the active cell, the output current. Thus, Fig. 2(b) shows the I_{in} - I_o conversion.

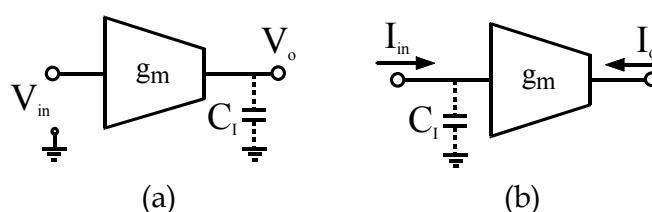


Fig. 2. Ideal integrator; (a) voltage-mode: $\frac{V_o}{V_{in}} = -\frac{g_m}{sC_1}$, (b) current-mode: $\frac{I_o}{I_{in}} = \frac{g_m}{sC_1}$.

Due to the grounded location of most parasitic capacitors of the active cell (the total output/input node effective parasitic capacitance, depending on the configuration), they must be considered by constituting a percentage of the total integration capacitance C_I , which is particularly significant at high frequencies. An extreme situation can be reached when considering the proposed transconductor as an integrator where total integration capacitance C_I is constituted only by these parasitic capacitances, with no need for any external capacitor. Nevertheless, these capacitances are not linear and, depending on their contribution, the total linearity of the system will be affected. As technological process variations will also affect the value of these parasitic capacitances, sensitivity to these capacitors requires a detailed study of the device models and integration technology together with a careful system layout.

The ideal integrator has an infinite dc-gain and no parasitic effects, thus obtaining a phase of $-\pi/2$ for all the frequencies. The unity-gain frequency is $\omega_t = g_m/C_I$. Nevertheless, a real integrator presents a non-zero transconductor output conductance g_{out} and parasitic poles and zeros, which distort the transfer function:

$$H(s) = A_{DC} \frac{\left(1 - s/\omega_2\right)}{\left(1 + s/\omega_1\right)} \quad (2)$$

where $A_{DC} = g_m/g_{out}$ is the dc-gain and $\omega_1 = \omega_t/A_{DC} = g_{out}/C_I$ is the frequency of the dominant pole. The effects of parasitic poles and zeros at frequencies much higher than the frequency range of the transconductor can be modelled with a single effective zero ω_2 : positive ω_2 results in an effective parasitic RHP-zero and negative ω_2 in an LHP-zero.

Non-zero transconductor output conductance g_{out} causes finite dc-gain in real integrators in the filter. In addition, parasitic poles and zeros in the integrator transfer function, together with finite A_{DC} , generate deviations of the inverter integrator phase response from $-\pi/2$, and it is well-known that phase error is the main source of misfunctions in filters. In particular, phase deviations around ω_t can cause significant errors in the filter transfer, depending on filter quality factors. The accuracy of the overall frequency response of the filter depends on how closely the individual integrators in the filter follow the ideal response. The filter remains very close to the ideal one if the integrator phase at its unity-gain frequency ω_t is equal to its ideal value $-\pi/2$; the amount by which the phase at ω_t deviates from this quantity will be called $\Delta\phi(\omega_t)$.

$$\phi(\omega_t) = -\frac{\pi}{2} + \tan^{-1}\left(\frac{\omega_1}{\omega_t}\right) - \tan^{-1}\left(\frac{\omega_t}{\omega_2}\right) \Rightarrow \Delta\phi(\omega_t) \approx \tan^{-1}\left(\frac{g_{out}}{g_m}\right) - \tan^{-1}\left(\frac{\omega_t}{\omega_2}\right) \quad (3)$$

Low dc-gain causes a leading phase error, and parasitic high-frequency poles and zeros in the integrator create lagging ($\omega_2 > 0$, RHP-zero) or leading ($\omega_2 < 0$, LHP-zero) phase errors. The acceptable worst case value of $\Delta\phi(\omega_t)$ depends on the specifications for the high-frequency response of the overall filter and the poles and quality factor of the transconductor transfer function. The integrator phase error can be modelled with a frequency-dependent integrator quality factor Q_{int} (Nauta, 1993), concluding that a high and accurate filter quality factor puts strong constraints on the integrators phase error, i.e. on Q_{int} .

$$\frac{1}{Q_{\text{int}}(\omega)} \approx \Delta\varphi(\omega) = \frac{\omega_1}{\omega} - \frac{\omega}{\omega_2} \tag{4}$$

The filter performance is dominated by the performance of the transconductors, since the filter specifications (dynamic range, dissipation and chip area) depend not only on filter properties (Q , cut-off frequency, impedance level) but also on transconductor properties (A_{DC} , ω_t , ω_1 , ω_2 , noise behaviour, linearity, area and power consumption). It is therefore useful to put effort into the study of a high-performance transconductor that would improve all its specifications, in order to obtain a proper design for these VHF filter building blocks.

3. Fully-balanced pseudo-differential transconductor cell

In this section, the development of a fully-balanced current-mode integrator based on a classical structure is described, which is characterized by low-power, high rejection of supply noise and VHF potential application. Fig. 3 shows the conceptual scheme of the Zele-Smith pseudo-differential integrator (Smith et al., 1996; Zele et al., 1996), a complete fully-balanced transconductance cell arranged for using a current-mode integrator.

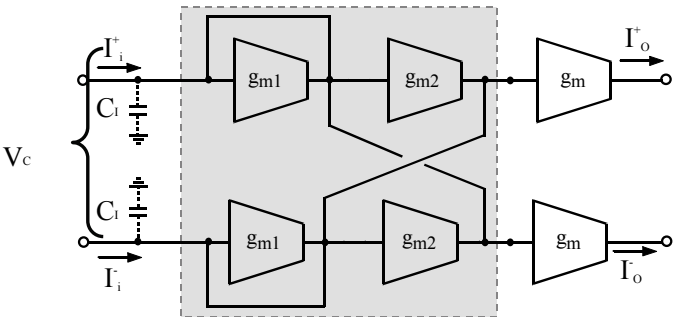


Fig. 3. Conceptual scheme of the complete fully-balanced current-mode transconductor.

To understand the basic operation we analyse the simple first-order model of the proposed transconductor, considering each unit cell as a simple transistor, i.e., single common-source stages as shown in Fig. 4. Under these conditions, the small-signal analysis gives the expression for the differential gain of the integrator (Eq. 5), where g_{mi} is the i -cell transconductance and $g_{o'}$ is the sum of output conductances g_{dsi} at the input node.

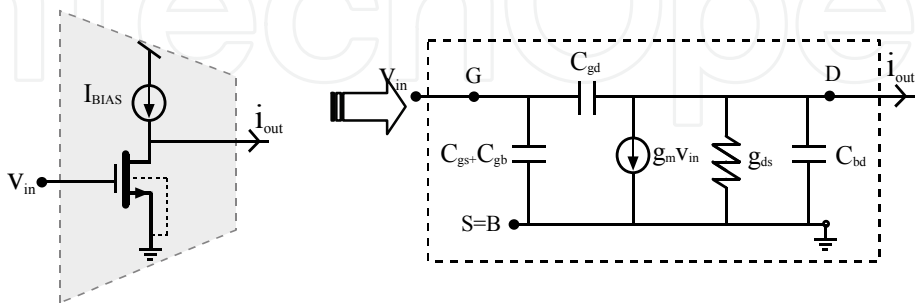


Fig. 4. Small-signal model for the common-source transconductor stage.

By analysing this expression and considering a first-order approximation, i.e., neglecting the g_{ds} effects of each transistor, an infinite dc-gain is achieved if perfect matching is obtained between g_{m1} and g_{m2} , so that $\delta g_m = g_{m1} - g_{m2} = 0$. Nevertheless, the effect of the output

conductances is not avoidable and the implementation of a negative resistance ($\delta g_m < 0$), inherent to this topology, provides the possibility of achieving dc-gain enhancement. Note that by making $\delta g_m + g_o' \rightarrow 0$, then $|A_{DC}| \rightarrow \infty$. In practice, mismatching between transistors limits the differential gain by up to 55 dB at most. Another equivalent way for analysing this improvement is to consider the differential-mode input resistance of the transconductor cell.

$$A_{DC} = \left| \frac{I_O^+ - I_O^-}{I_i^+ - I_i^-} \right| \approx \frac{g_m}{g_{m1} - g_{m2} + g_o'} \cong \frac{g_m}{\delta g_m + g_o'}; \quad R_D(in) \approx \frac{2}{g_{m1} - g_{m2} + g_o'} = \frac{2A_{DC}}{g_m} \quad (5)$$

As a result, this scheme shows the basic pseudo-differential structure obtained by considering two dual transconductor cells (g_m), leading to current integration through input capacitance C_i . Thanks to the additional negative resistance shown in grey in the same figure, dc-gain is increased by providing positive feedback compensation for the signal current and boosting the input resistance of the transconductor.

The approximate common-mode gain, which must be less than unity to guarantee stability in closed-loop configurations, is constrained by device ratios to a stable value over all frequencies (Eq. 6). Common-mode stability is assured by designing $(g_{m1} + g_{m2})/g_m > 1$. Common-mode behaviour analysis can be also carried out by calculating common-mode input resistance.

$$|A_{CM}| = \left| \frac{I_O^+ + I_O^-}{I_i^+ + I_i^-} \right| \approx \frac{g_m}{g_{m1} + g_{m2} + g_o'}; \quad R_{CM}(in) \approx \frac{1}{2(g_{m1} + g_{m2} + g_o')} = \frac{|A_{CM}|}{2g_m} \quad (6)$$

The common-mode feedback resulting from the interconnection of the negative resistance provides both a naturally high differential gain and low common-mode gain for the integrator, improving these limits attached to a real integrator structure. Consequently, the basic operation of the transconductor will be best understood by explaining, first, that the common-mode control and dc-enhancement circuitry is connected at the input of the circuit and then, that the linear V-I conversion mechanism occurs in the output stage.

The gain of the basic current integrator is independent of the supply voltage to the first-order approximation. When fully-differential current topologies are used, the small remaining supply noise feedthrough is common to both sides of the signal and thus has no direct effect, except through random device mismatch. Therefore, the integrator has good immunity to supply noise. Device mismatch can be minimized with careful layout and specific design techniques to around 0.1-1 %, in many applications (Croon et al., 2002; Otin et al., 2004; Otin et al., 2005).

The use of an integrator based on transconductance cells implemented by using single transistors (no internal nodes), results in a proper frequency response because the only nodes are at the inputs and at the outputs. To a first-order approximation, no parasitic poles or zeros exist in the differential ac-response of the basic integrator circuit. Both differential and common-mode gains can be independently set by the different values of g_{m1} and g_{m2} . The ideal integrator function is a result of setting $\delta g_m + g_o' = 0$ and the phase error at the unity-gain frequency, $\omega_t = g_m/C_L$, can be calculated by:

$$\Delta\phi(\omega_t) = \tan^{-1}\left(\frac{\omega_1}{\omega_t}\right) \approx \tan^{-1}\left(\frac{\delta g_m + g_o'}{g_m}\right) = \frac{\pi}{2} - \tan^{-1}\left(\frac{g_m}{\delta g_m + g_o'}\right) \quad (7)$$

To summarize, infinite differential input impedance can be obtained if $\delta g_m + g_o' \rightarrow 0$ while maximizing the differential dc-gain and minimizing the phase error at ω_t , and common-mode input impedance can be reduced by maximizing the sum of the transconductances ($g_{m1} + g_{m2}$). Consequently, the common-mode rejection ratio (CMRR) is improved. Nevertheless, an important concept should be borne in mind: as the dc-gain depends on the difference ($g_o' - |\delta g_m|$), the structure can lead to instability if this quantity becomes negative (total negative input conductance) due to overcompensation.

By analysing the small signal model of each common-source stage forming the complete transconductor topology (Fig. 4), the need to solve a frequency problem arises: the feedforward ac-current path from the gate (input) to the drain (output), through the overlap parasitic capacitance C_{gd} . When considering the stages forming the negative resistance, the repercussion of this effect is not important because the contribution to the total behaviour of the cell decreases as these capacitances are short-circuited with their respective g_{mi} . However, the feedforward current through C_{gd} in the fully-balanced output-stage g_m of the transconductor structure generates a transmission zero (g_m/C_{gd}) in the right complex half-plane. This parasitic RHP-zero modifies the integrator frequency response and creates a phase-lag at the unity-gain frequency. Furthermore, the Miller effect, also associated with this parasitic capacitor, introduces larger equivalent input capacitance ($C_{in} = C_{gs} + C_{gb} \Rightarrow C_{in} = C_{gs} + C_{gb} + (1+A)C_{gd}$) and an additional component to the equivalent output capacitance ($C_{out} = C_{bd} \Rightarrow C_{out} = C_{bd} + (1+A^{-1})C_{gd}$), where $A \approx g_m/g_{ds}$. Therefore, the neutralization of this effect will involve bandwidth enhancement.

Many methods have been proposed to minimize the Miller effect: the cascode technique (Gray et al., 2001), the inductor shunt peaking technique (Mohan et al., 2000), the capacitive compensation technique (Wakimoto et al., 1990; Vadipour, 1993), the distributed amplification technique (Ahn et al., 2002) and the active inductor technique (Säckinger et al., 2000). They all have the advantages of low-voltage compatibility and low area; however, the solutions considered in this work will be the use of cascode structures together with the capacitive compensation technique.

Differential systems allow the C_c -cancellation technique, using positive feedback to generate negative capacitances, which can cancel the positive ones to yield bandwidth increases. These C_c capacitors are the overlap C_{gd} parasitic capacitances of dummy compensation transistors used in a cross-coupled way to neutralize the feedback action of these Miller capacitors. The connection is between the output and the opposite sign input, available in a balanced configuration. Under these conditions, the RHP-zero is moved to infinity, i.e., the cause of phase lag is removed, thus expanding the bandwidth of the transconductor. At the same time, compensation capacitor C_c will cancel the Miller effect and a lower input node effective capacitance is obtained due to the reduction of the feedforward effect. This technique depends on feeding back a current that is precisely the same as the one flowing through the Miller capacitance C_{gd} and, in consequence, the neutralization capacitor must match precisely. However, it is remarkable that C_{gd} is voltage-dependent and compensation can only work with small signals. In the case of mismatch between C_{gd} and C_c , parasitic zero is not at infinity and can cause a small phase lag or lead.

However, this is not the full story of the high frequency behaviour of the transconductor cell and there are more frequency limits. Mismatch in common-mode feedback circuits can result in unexpected parasitic poles and zeros. In addition, high frequency models of the MOS transistor show that g_m is not independent of frequency, but has a finite delay $g_m(s)$

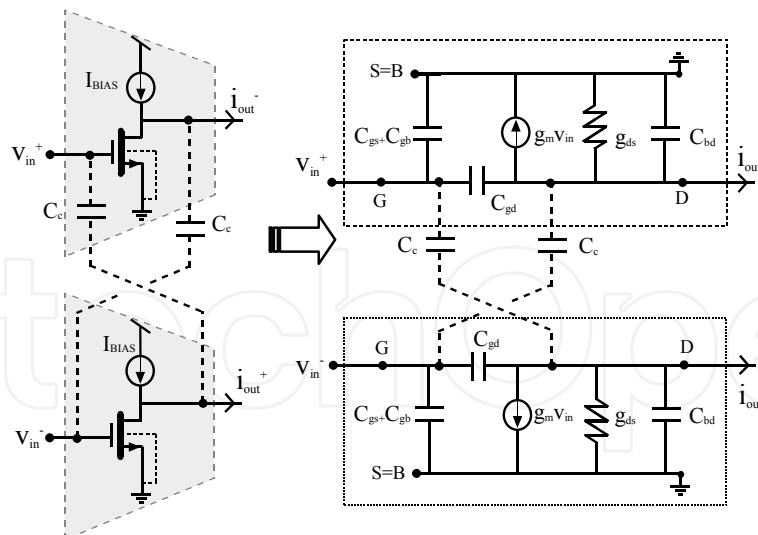


Fig. 5. Cancellation of transmission zero g_m/C_{gd} and neutralization of the Miller effect: C_c -cancellation technique.

and begins to roll off at very high frequencies. Although the frequency where this roll-off begins can be in the GHz range, the phase shift from this effect can become significant at much lower frequencies. Since most active filters are very sensitive to small phase changes in the integrator response, it is thus important to take this effect into account.

The first way to minimize these effects is to eliminate the internal nodes or, if this is not possible, to design them as low-impedance nodes. This procedure can be carried out by considering cascode topologies. Moreover, their use further prevents bandwidth reduction generated by transmission zero because one side of C_c is connected to the internal low-impedance node, i.e., to the low-gain point of the cascode transistor source.

Therefore, an enhancement of the integrator dc-gain has been obtained with this topology by means of the differential negative resistance, increasing the differential input resistance of the transconductor and keeping the common-mode gain lower than unity. With regard to frequency limit-related problems, transmission zero has been reduced by using C_c -capacitor compensation, taking advantage of the pseudo-differential topology. This solution can also be improved by considering cascode topologies, giving higher dc-gains in a natural way, which will also reduce the frequency drawbacks associated to the internal nodes of other topologies by avoiding internal high-impedance nodes in the signal path.

As a result, a low-voltage transconductor with high linearity, very high operation frequency and high power efficiency has been designed where cascode structures should be considered to obtain an improvement in the high-frequency behaviour of the basic topology. The main advantage of using cascode stages instead of single common-source stages is the higher dc-gain while maintaining a good frequency response. Hence, a higher quality factor of the integrator is expected due to the higher differential dc-gain (Abidi, 1988). Basic cascode circuits require high supply voltages to operate due to the large overhead bias from threshold voltages. However, variations of the cascode technique exist which can be used with lower voltage supplies. Two options are considered in this work, the so-called **high-swing cascode (HS)** stage and the **folded cascode (FC)** stage (Baker et al., 1998; Sansen et al. 1999; Sedra et al., 2004). The unit cells replacing the common-source stages previously used are shown in Fig. 6. The complete fully-balanced current-mode transconductance cells implemented by using these cascode stages are described in the following sections.

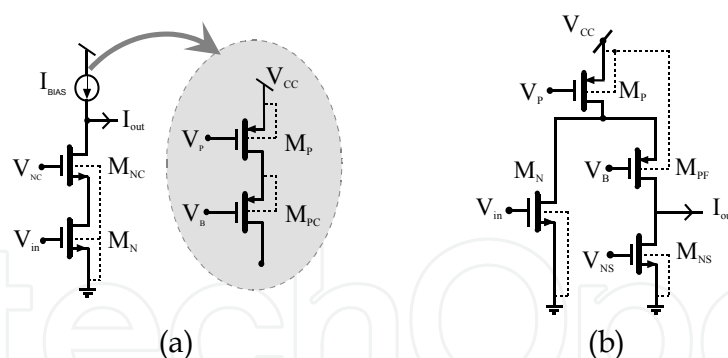


Fig. 6. Unit transconductance cell: (a) high-swing (HS) and (b) folded cascode (FC) topology.

3.1 High-swing cascode section: HS topology

Fig. 7(a) shows the transconductor arranged for using the current-mode integrator described in Fig. 3, where the unit cells have been implemented by using high-swing cascode stages (Baker et al., 1998; Sansen et al. 1999; Sedra et al., 2004). As illustrated in the corresponding HS unit cell (Fig. 6(a)), current sources are also implemented by using high-swing cascode elements. The substrate terminals of NMOS transistors are connected to the reference voltage as usual, and those of the PMOS transistors are connected to the corresponding source node of each transistor.

The use of high-swing cascode elements offers as high accuracy as using basic cascode stages to implement each unit cell of the transconductor but, because of the slightly different connection between transistors, needs lower supply voltage and has fewer internal parasitic poles, generating nodes between the input and the output, giving a better frequency response of the integrator. The main disadvantage of the improved cascode topology is that due to biasing constraints, the gate-source voltages must be kept small, resulting in larger devices for a bias current level.

3.2 Folded cascode section: FC topology

In order to obtain an improvement in biasing flexibility and further reduction of the supply voltage in the design of the transconductor cell, we can also take advantage of folded-cascode sections (Sansen et al. 1999; Sedra et al., 2004). The schematic used to describe the complete integrator based on the proposed current-mode pseudo-differential transconductor is shown in Fig. 7(b), where the unit cells have been implemented by using FC stages illustrated in Fig. 6(b). In this case, current sources are implemented by using single elements, both bias sources I_{BIAS} and cascode sources M_{NSi} . The substrate terminals of NMOS transistors are connected to the reference voltage as usual, and those of PMOS transistors, both those used to implement current sources I_{BIAS} and those implementing folded transistors M_{PFi} , are connected to the V_{CC} node.

The use of folded cascode elements exhibits a substantial improvement in biasing flexibility, because of the increased drain-voltage of the transistors, at the cost of additional current sources and bias voltages. Another significant benefit of using these stages is that by avoiding the biasing constraints associated to the high-swing cascode structure, we obviate the need to keep gate-source voltages low, which results in smaller and simpler devices for a given bias current level, lower voltage supply and larger unity-gain frequencies.

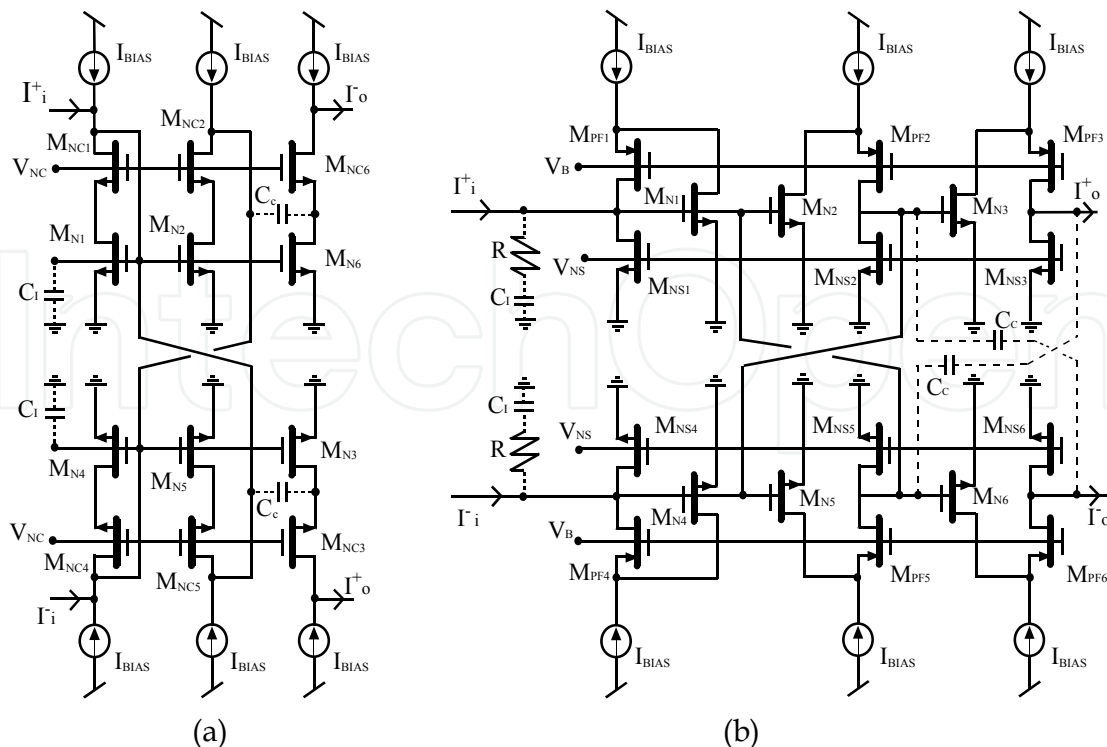


Fig. 7. Fully-balanced pseudo-differential current-mode cell, based on (a) high-swing cascode unit stages: **HS transconductor**; (b) folded-cascode unit stages: **FC transconductor**.

3.3 General considerations: basic principle

A similar notation and index-linking have been adopted in both transconductor implementations in order to simplify the description of the basic principle and to unify the topology analysis. Assuming ideal behaviour for the integrator, the balanced input current flows entirely into integration capacitance C_i . Diode-connected stages $M_{1,4}$ adequately bias cascode output $M_{3,6}$, whilst transistors $M_{2,5}$ provide positive feedback compensation for the signal current flowing into $M_{1,4}$ and boost the input resistance of the integrator.

Regarding the gain enhancement by means of the negative resistance formed by transistors $M_{2,5}$, this technique is absolutely necessary for Zele-Smith topologies and other voltage-mode transconductors (Nauta, 1993), in order to obtain reasonably high dc-gain values. Theoretically, the dc-gain could be infinity by adjusting the equivalent negative resistance, but in practice mismatching limits the dc-gain by about 40 dB in single transistor stages. However, the use of cascode topologies leads to a natural enhancement of this parameter and differential dc-gain values of up to 55 dB can be reached with identical transistors under identical bias conditions by means of a lower mismatching sensitive design. Nevertheless, there is a key difference between the HS and the FC cascode structure:

- The high output resistance is directly guaranteed thanks to the true cascode output stage exhibited by the HS transconductor. Therefore, positive feedback compensation is not necessary to boost differential resistance or enhance the dc-gain.
- On the other hand, the output-node for the FC transconductor is not a very high impedance node, and the negative resistance proves necessary to obtain real input resistance enhancement. In this approach, positive feedback compensation for the signal current flowing into $M_{3,6}$ is essential, boosting the input resistance of the integrator and increasing dc-gain.

The reason for this difference is that the FC unit cell considered and shown in Fig. 6(b) is a pseudo-cascode topology. To obtain similar output impedance to that of the HS approach, the M_{NS} current source would have to be implemented by using a cascode current source. Nevertheless, even if the HS implementation undergoes an immediate dc-gain/input resistance improvement, both topologies require positive feedback compensation (negative resistance) to reduce common-mode gain (common-mode input resistance) and stabilize common-mode voltages. On the other hand, the use of pseudo-differential structures requires careful and efficient control over the common-mode behaviour of the circuit. It is worth noting that this structure not only stabilises the common-mode voltage, but also rejects common-mode signals by means of partial positive feedback. This idea has already been used for high-frequency transconductors in (Nauta, 1993) and for a class of current-mode filters (Smith et al., 1996; Zele et al., 1996).

Thus, considering this topology implemented by using cascode stages, dc-gains of about 55 dB and CMRR of 60 dB can be obtained with inherent stability of common-mode voltages. Note that the propagation of common-mode (CM) signals in balanced circuits can cause instability and distortion. Further, current consumption, linearity and transconductance value are strongly dependent on the CM input signals. Additional techniques can be used in the proposed topology if a greater CMRR is needed, such as feedforward cancellation of the input CM signal. Balanced transconductors with high-input common-mode rejection that are capable of operating with low-voltage supplies are obtained by using an additional transconductor that is only sensitive to CM signals (Baschiroto et al., 1994; Wyszynski et al., 1994). Considering this technique, CMRR values up to 70 dB could be obtained.

4. High frequency response

In this section, the bandwidth of the transconductor will be analysed. Note that if single transistor stages and unrealistic simplified models are used in the proposed topology (Fig.3), the bandwidth could be infinite owing to the absence of internal nodes influencing the transfer function of the integrator. A more complete model of the MOS transistor does predict a finite bandwidth due to the second-order frequency effects such as the transmission zero associated to overlap parasitic capacitance C_{gd} , frequency dependence of the transconductance $g_m(s)$ and mismatch in common-mode feedback circuits. A closer explanation of MOS behaviour at high-frequencies (splitting it into an **intrinsic** and an **extrinsic** part) is required before starting the study of the complete integrator. Taking into account a non-quasistatic model (Tsividis, 1996), the high-frequency behaviour of the current mode integrator will be calculated.

When analysing transconductor bandwidth, several general factors must be considered:

- The output of the complete transconductor may be assumed to be short-circuited for ac-signals when calculating the frequency response of the integrator.
- In all the equations: g_m is the transconductance, g_{ds} the output conductance, g_{mb} the bulk-transconductance and C_{gd} , C_{gs} , C_{ds} , C_{bs} and C_{bd} the parasitic capacitances.
- All the unit cells are designed to seek perfect matching between them. Therefore, all similar transistors have the same properties except for transconductance g_m of the N-transistor processing the signal (M_N transistor in both unit cells shown in Fig. 6). In this way, considering the notation and index-linking previously used in Fig. 3: $g_m(N_1)=A_N g_m(N)$; $g_m(N_2)=A_P g_m(N)$; $g_m(N_3)=g_m(N)$. Consequently, $\delta g_m=(A_N-A_P)g_m$

- represents the difference between M_1 and M_2 , or, M_4 and M_5 due to the difference in dimensions and bias currents of N-transistors, which gives rise to the negative resistance that enhances the dc-gain of the system.
- Total integration capacitance C_I comprises not only the external capacitance, but also the contribution of parasitic capacitors ($C_I=C_{ext}+C_p$). Intrinsic capacitance C_{gs} is the main contribution of these parasitic capacitances C_p and consideration of it as a great percentage of total integration capacitance acquires great significance.
 - External capacitor C_{ext} can be implemented by using double-poly, metal-metal or MOS capacitors, depending on the technological process.
 - Current source is modelled with a Norton equivalent circuit, where G_s and C_s are the admittance and capacitance components. The external capacitance C_{ext} connected to the transconductor input is in parallel with C_s . For purposes of simplicity, from now on, C_s will include the equivalent capacitance of the current source and the external capacitance ($C_s\equiv C_s+C_{ext}$). Therefore, total integration capacitance can be expressed as: $C_I=C_s+C_p$, including parasitic effects, the external capacitance and the equivalent-model of the non-ideal current source.

Firstly, a model for the V-I conversion of the unit cell is derived, in both implementations to show the calculation process of the bandwidth of the complete transconductance cell.

4.1 High-frequency model of the HS unit cell

The following circuit represents the high frequency model for the HS unit cell previously shown in Fig. 6(a), where $X(N)$ denote the parameters associated to the M_N -transistor, $X(NC)$ those associated to the cascode transistor, $X(P)$ those associated to current sources I_{BIAS} and $X(PC)$ those associated to the cascode current sources as shown in Fig. 6(a). Table 1 summarizes the parameters associated to the impedances shown in the small-signal equivalent circuit. The rest of the elements: $g_m(N)$, $g_{ds}(N)$, $g_{ds}(NC)$, $g_{ds}(PC)$, $g_m(PC)$, $C_{gd}(N)$ and $C_{ds}(NC)$ directly represent the parameters of the respective transistor.

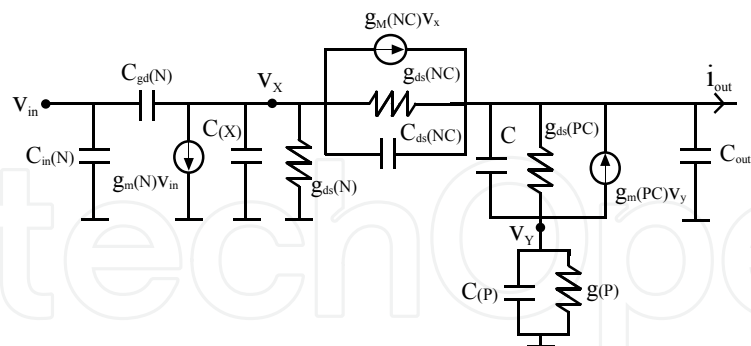


Fig. 8. Equivalent high-frequency circuit for the HS unit cell.

$g_M(NC) = g_m(NC) + g_{mb}(NC)$	$g(P) = g_{ds}(P)$
$C_{in}(N) = C_{gs}(N) + C_{gb}(N)$	$C(x) = C_{ds}(N) + C_{bd}(N) + C_{gs}(NC) + C_{bs}(NC)$
$C = C_{ds}(PC) + C_{bd}(PC)$	$C_{out} = C_{gb}(NC) + C_{bd}(NC) + C_{gd}(PC)$
$C(P) = C_{gd}(P) + C_{ds}(P) + C_{bd}(P) + C_{gb}(PC) + C_{gs}(PC)$	

Table 1. Small-signal parameters for the HS unit cell.

4.2 High-frequency model of the FC unit cell

The following circuit represents the high frequency model for the FC unit cell previously shown in Fig. 6(b), where X(N) are the parameters associated to the M_N-transistor, X(PF) those associated to the folded transistor, X(P) those associated to the current sources I_{BIAS} and X(NS) those associated to the current source of the folded transistor, which is implemented with a single NMOS transistor as previously illustrated.

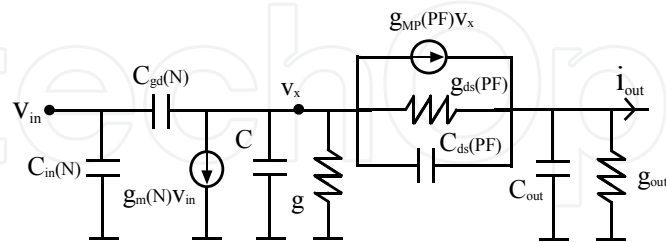


Fig. 9. Equivalent high-frequency circuit for the FC unit cell.

Table 2 summarizes the parameters associated to the impedances shown in the small-signal equivalent circuit. The rest of the elements: g_m(N), g_{ds}(PF), C_{gd}(N) and C_{ds}(PF) directly represent the parameters of the respective transistor.

$g = g_{ds}(N) + 2g_{ds}(P)$	$C_{in}(N) = C_{gs}(N) + C_{gb}(N)$
$g_{out} = g_{ds}(NS)$	$C = C_{ds}(N) + C_{bd}(N) + 2C_{gd}(P) + 2C_{ds}(P) + 2C_{bd}(P) + C_{gs}(PF) + C_{bs}(PF)$
$g_{MP}(PF) = g_m(PF) + g_{mb}(PF)$	$C_{out} = C_{gd}(PF) + C_{bd}(PF) + C_{gd}(NS) + C_{ds}(NS) + C_{bd}(NS)$

Table 2. Small-signal parameters for the FC unit cell.

Great similarity is obtained in the description of both unit cells. Even the FC capacitive parameter C will be equivalent to C+C(x) in the HS description. This parallelism will also appear in the complete transconductor analysis.

4.3 High-frequency model of the complete transconductance cell

Under these conditions, the differential gain of the proposed transconductor cell (in both implementations) can be calculated by:

$$H(s) = k \frac{(s - s_0)(s + s_1)}{s^2 + x_1s + x_2} \approx K \frac{(s - s_0)}{(s + \delta_1)(s + \delta_2)} \tag{8}$$

where:

$$K = \frac{-A_{DC} \delta_1 \delta_2}{s_0}; \quad x_1 = \frac{\beta}{\gamma}; \quad x_2 = \frac{\alpha}{\gamma}; \quad \delta_1 = \frac{\alpha}{\beta} = \frac{x_2}{x_1}; \quad \delta_2 = \frac{\beta}{\gamma} - \delta_1 \approx \frac{\beta}{\gamma} = x_1 \tag{9}$$

Denominator factorization of Eq.(8) leads to obtain two parasitic poles, -δ₁ and -δ₂, but only if the approximation (α·γ/β²)<<1 is verified. Furthermore, parasitic zero -s₁ must be negligible in the frequency range of interest. Both considerations will be demonstrated, either in the HS or in the FC approach (s₁>>s and s₁>>s₀: s₁(HS)=1600 s₀=1100 GHz, s₁(FC)=30 s₀=1900 GHz).

Due to the use of a pseudo-differential structure, a careful study of the common-mode behaviour is mandatory. Thanks to the topology proposed, the common-mode voltage is

stabilized by means of partial positive feedback as previously explained. Under these assumptions:

$$A_{CM}(s) = k_{CM} \frac{(s - s_0)(s + s_1)}{s^2 + y_1s + y_2} \approx K_{CM} \frac{(s - s_0)}{s^2 + y_1s + y_2} \quad (10)$$

$$K_{CM} = \frac{-A_{CM} y_2}{s_0}; \quad y_1 = \frac{\beta_{CM}}{\gamma_{CM}}; \quad y_2 = \frac{\alpha_{CM}}{\gamma_{CM}} \quad (11)$$

Eq.(10) once more shows the need to neglect parasitic zero $-s_1$, leading to the same consideration as in the differential gain equation. In this analysis, denominator factorization is more difficult to accomplish. However, the approximate equations are easily derived and, making use of the figures obtained in each particular design, the possibility of using the approximate common-mode transfer function will be analysed. Therefore, if $(\alpha_{CM} \cdot \gamma_{CM} / \beta_{CM}^2) \ll 1$ is verified, the common-mode gain can be expressed as:

$$A_{CM}(s) = K_{CM} \frac{(s - s_0)}{(s + \xi_1)(s + \xi_2)} \quad (12)$$

$$\xi_1 = \frac{\alpha_{CM}}{\beta_{CM}} = \frac{y_2}{y_1}; \quad \xi_2 = \frac{\beta_{CM}}{\gamma_{CM}} - \xi_1 \approx \frac{\beta_{CM}}{\gamma_{CM}} = y_1 \quad (13)$$

Both transfer functions are characterized by two parasitic poles and one RHP-zero; the differential-mode by $-\delta_1$, $-\delta_2$, and s_0 ; and the common-mode by $-\xi_1$, $-\xi_2$, and s_0 (zero s_0 is the same in both transfer functions)¹. Consequently, in order to obtain a transconductor design that is compatible with all the requirements of the active G_m -C filter implementation, a proper analysis and characterization of these parasitic elements becomes a top-priority challenge. From this study, their origin and frequency location may lead to some design considerations to improve the integrator frequency response.

Differential dc-gain, common-mode dc-gain, s_0 and s_1 are summarized in table 3 for both implementations. The parasitic poles can be calculated by using α , β , γ , α_{CM} , β_{CM} , γ_{CM} , as shown in Eqs.(9) and (13). As the resulting relations are very complicated, it is necessary to look for the dominant terms and obtain approximate expressions to draw conclusions. They can be simplified to analyse and understand the behaviour of the transconductance cell and its frequency limits that are associated to second order effects, which differentiate between the frequency behaviour of the proposed topology and the expected ideal response.

4.4 HS transconductance cell frequency response

Considering the previous study of the HS unit cell, a detailed analysis of the frequency response of the complete HS integrator is carried out. The dominant terms of these expressions are subsequently obtained in this section. In order to simplify the notation, the small-signal parameters are redefined in table 4.

¹ According to stable systems, negative poles $-\delta_1$, $-\delta_2$, $-\xi_1$ and $-\xi_2$ have been obtained in the transfer functions for both implementations. For purposes of simplicity, when referring to these poles, their associated frequency (δ_1 , δ_2 , ξ_1 , ξ_2) will be the considered magnitude.

	HS transconductor	FC transconductor
S_0	$s_0 = \frac{g_m(N)}{C_{gd}(N)}$	$s_0 = \frac{g_m(N)}{C_{gd}(N)}$
S_1	$s_1 = \frac{g_M(NC) + g_{ds}(NC)}{C_{ds}(NC)}$	$s_1 = \frac{g_{MP}(PF) + g_{ds}(PF)}{C_{ds}(PF)}$
A_{DC}	$A_{DC} = \frac{g_m(N)(g_M(NC) + g_{ds}(NC))}{\alpha}$	$A_{DC} = \frac{g_m(N)(g_{MP}(PF) + g_{ds}(PF))}{\alpha}$
A_{CM}	$A_{CM} = \frac{-g_m(N)(g_M(NC) + g_{ds}(NC))}{\alpha_{CM}}$	$A_{CM} = \frac{-g_m(N)(g_{MP}(PF) + g_{ds}(PF))}{\alpha_{CM}}$

Table 3. Summary of the high-frequency parameters.

$G = g_{ds}(N) + g_M(NC) + g_{ds}(NC)$
$C_{IN} = C_s + 2C_{in}(N) + C_{out} = C_s + 2C_{gs}(N) + 2C_{gb}(N) + C_{gb}(NC) + C_{bd}(NC) + C_{gd}(PC)$
$C_{\beta} = C_{out} + C_{in}(N) = C_{gs}(N) + C_{gb}(N) + C_{gb}(NC) + C_{bd}(NC) + C_{gd}(PC)$

Table 4. Impedance parameters for the HS integrator.

By analysing in detail the small-signal equivalent model for the complete HS integrator, the value of total integration capacitance C_I can be calculated by Eq.(14). This definition will lead to a simplification of the parasitic pole expressions.

$$C_I = C_{IN} + C_{\beta} = C_s + 3C_{in}(N) + 2C_{out} \tag{14}$$

Firstly, the differential and common-mode gain can be expressed as follows:

$$A_{DC} \approx \left[(A_N - A_P) + \frac{2g_{ds}(NC)g_{ds}(N)}{g_m(N)(g_M(NC) + g_{ds}(NC))} \right]^{-1} \tag{15}$$

$$A_{CM} \approx - \left[(A_N + A_P) - \frac{2g_{ds}(NC)g_{ds}(N)}{g_m(N)(g_M(NC) + g_{ds}(NC))} \right]^{-1} \approx \frac{-1}{A_N + A_P} \tag{16}$$

In these expressions, the differential negative resistance obtained by the partial positive feedback compensation is shown by means of the difference $\delta g_m = (A_N - A_P)g_m(N)$. The existence of this negative resistance allows the differential dc-gain to be enhanced. Parasitic poles δ_1 and δ_2 can be calculated by means of ratios between α , β and γ . Final expressions are summarized in table 6. The origin of second order effects can be better understood by focusing on their dependence.

$$\alpha \approx ((A_N - A_P)g_m(N))(g_M(NC) + g_{ds}(NC)) + 2g_{ds}(NC)g_{ds}(N) \approx 2g_{ds}(NC)g_{ds}(N) \tag{17}$$

$$\beta \approx G(C_s + 3C_{in}(N) + 2C_{out}) = G C_I \tag{18}$$

where considering the dominant term in the transconductance G , the expression can be written as:

$$\beta \approx (g_{ds}(N) + g_M(NC) + g_{ds}(NC))C_I \approx g_M(NC)C_I \quad (19)$$

Therefore, the parasitic pole δ_1 can be expressed as:

$$\delta_1 = \frac{\alpha}{\beta} \approx \frac{2g_{ds}(NC)g_{ds}(N)}{g_M(NC)C_I} \quad (20)$$

Following the same process for the other pole δ_2 , we obtain:

$$\gamma \approx C_I (C_{gd}(N) + C_{ds}(NC) + C(x)) \approx C_I C(x) \approx C_I C_{gs}(NC) \quad (21)$$

$$\delta_2 = \frac{\beta}{\gamma} \approx \frac{G}{C(X)} = \frac{g_{ds}(N) + g_M(NC) + g_{ds}(NC)}{C_{ds}(N) + C_{bd}(N) + C_{gs}(NC) + C_{bs}(NC)} \approx \frac{g_M(NC)}{C_{gs}(NC)} \quad (22)$$

Similar results can be obtained for the common-mode frequency response:

$$\alpha_{CM} \approx ((A_N + A_P)g_m(N))(g_M(NC) + g_{ds}(NC)) \approx (A_N + A_P)g_m(N)g_M(NC) \quad (23)$$

$$\beta_{CM} \approx \beta \approx g_M(NC)C_I; \quad \gamma_{CM} \approx \gamma \approx C_I C_{gs}(NC) \quad (24)$$

$$\xi_1 = \frac{\alpha_{CM}}{\beta_{CM}} \approx \frac{(A_N + A_P)g_m(N)g_M(NC)}{G C_I} \approx \frac{(A_N + A_P)g_m(N)}{C_I}; \quad \xi_2 = \frac{\beta_{CM}}{\gamma_{CM}} \approx \delta_2 \approx \frac{G}{C(X)} \approx \frac{g_M(NC)}{C_{gs}(NC)} \quad (25)$$

4.5 FC transconductance cell frequency response

Considering the previous study of the FC unit cell, a detailed analysis of the frequency response of the complete FC integrator is carried out. The dominant terms of these expressions are obtained in this section. In order to simplify the notation, two small-signal parameters are redefined in table 5.

$G_I = G_s + 2g_{out}$
$C_I = C_s + 3C_{in}(N) + 2C_{out} = C_s + 3C_{gs}(N) + 3C_{gb}(N) + 2C_{gd}(PF) + 2C_{bd}(PF) + 2C_{gd}(NS) + 2C_{ds}(NS) + 2C_{bd}(NS)$

Table 5. Impedance parameters for the FC integrator.

In accordance with the analysis of the small-signal equivalent model for the complete FC integrator, parameter C_I , defined in table 5, directly represents the total integration capacitance, the expression of which is the same as in the HS integrator. Therefore, the total integrator capacitance of both integrator implementations can be calculated by Eq.(26).

$$C_I = C_s + 3C_{in}(N) + 2C_{out} \quad (26)$$

For the FC integrator, the differential and common-mode gain can be expressed as follows:

$$A_{DC} \approx \left[(A_N - A_P) + \frac{2g_{ds}(NS)(g_{MP}(PF) + 2g_{ds}(P))}{g_m(N)(g_{MP}(PF) + g_{ds}(PF))} \right]^{-1} \approx \left[(A_N - A_P) + \frac{2g_{ds}(NS)}{g_m(N)} \right]^{-1} \quad (27)$$

$$A_{CM} \approx - \left[(A_N + A_P) + \frac{2g_{ds}(NS)}{g_m(N)} \right]^{-1} \approx \frac{-1}{A_N + A_P} \quad (28)$$

In these expressions, the negative resistance obtained by the partial positive feedback compensation is shown again by means of the difference $\delta g_m = (A_N - A_P)g_m(N)$. Parasitic poles, δ_1 and δ_2 , are obtained by means of ratios among α , β and γ , as in the HS implementation. The final expressions are summarized in table 6. Consequently, parasitic poles δ_1 and δ_2 can be expressed as:

$$\alpha \approx ((A_N - A_P)g_m(N))(g_{MP}(PF) + g_{ds}(PF)) + 2g_{ds}(NS)(g_{MP}(PF) + 2g_{ds}(P)) \approx 2g_{ds}(NS)(g_{MP}(PF) + 2g_{ds}(P)) \quad (29)$$

$$\beta \approx (g + g_{ds}(PF) + g_{MP}(PF))C_I \approx (g_{MP}(PF) + 2g_{ds}(P))C_I \quad (30)$$

$$\delta_1 = \frac{\alpha}{\beta} \approx \frac{2g_{ds}(NS)}{C_I} \quad (31)$$

$$\gamma \approx C_I (C_{ds}(PF) + C_{gd}(N) + C) \approx C_I C \approx C_I (2C_{gd}(P) + 2C_{ds}(P) + C_{gs}(PF) + C_{bs}(PF)) \approx 2C_I C_{gd}(P) \quad (32)$$

$$\delta_2 = \frac{\beta}{\gamma} \approx \frac{g_{MP}(PF) + 2g_{ds}(P)}{2C_{gd}(P) + 2C_{ds}(P) + C_{gs}(PF) + C_{bs}(PF)} \approx \frac{g_{MP}(PF) + 2g_{ds}(P)}{2C_{gd}(P)} \quad (33)$$

Similar results can be obtained for the common-mode frequency response:

$$\alpha_{CM} \approx ((A_N + A_P)g_m(N))(g_{MP}(PF) + g_{ds}(PF)) + 2g_{ds}(NS)(g_{MP}(PF) + 2g_{ds}(P)) \approx (A_N + A_P)g_m(N)(g_{MP}(PF) + g_{ds}(PF)) \quad (34)$$

$$\beta_{CM} \approx \beta \approx (g_{MP}(PF) + 2g_{ds}(P))C_I; \quad \gamma_{CM} \approx \gamma \approx 2C_I C_{gd}(P) \quad (35)$$

$$\xi_1 = \frac{\alpha_{CM}}{\beta_{CM}} \approx \frac{(A_N + A_P)g_m(N)}{C_I}; \quad \xi_2 = \frac{\beta_{CM}}{\gamma_{CM}} \approx \delta_2 \approx \frac{g_{MP}(PF) + 2g_{ds}(P)}{2C_{gd}(P)} \quad (36)$$

4.6 Comments and discussion

A full analysis has been developed in previous sections in order to draw some design strategies and implement a competitive and robust transconductor cell. Great similarity was found between the two topologies, as reflected in table 6.

The first conclusion regards total integration capacitance, C_I , which has the same definition in both implementations: $C_I = C_s + 3C_{in}(N) + 2C_{out}$ (Eq. 26), where C_s represents the equivalent

	S_0	S_1	δ_1	δ_2	ξ_1	ξ_2
HS	$\frac{g_m(N)}{C_{gd}(N)}$	$\frac{g_M(NC) + g_{ds}(NC)}{C_{ds}(NC)}$	$\frac{2g_{ds}(NC)g_{ds}(N)}{g_M(NC)C_I}$	$\frac{g_M(NC)}{C_{gs}(NC)}$	$\frac{(A_N + A_P)g_m(N)}{C_I}$	$\frac{g_M(NC)}{C_{gs}(NC)}$
FC	$\frac{g_m(N)}{C_{gd}(N)}$	$\frac{g_{MP}(PF) + g_{ds}(PF)}{C_{ds}(PF)}$	$\frac{2g_{ds}(NS)}{C_I}$	$\frac{g_{MP}(PF) + 2g_{ds}(P)}{2C_{gs}(P)}$	$\frac{(A_N + A_P)g_m(N)}{C_I}$	$\frac{g_{MP}(PF) + 2g_{ds}(P)}{2C_{gs}(P)}$

Table 6. Parasitic poles and zeros for the integrator topology.

parallel capacitance between the external capacitance and the Norton capacitance of the input current source. This definition can easily be obtained by taking two different ideas into account. Considering the proposed integrator topology (Fig. 3), the expected integration capacitance will be the external capacitance in addition to the contribution of parasitic capacitors to the input node. For example, looking at the positive branch (the upper one) in this figure, there are three transconductor cell inputs ($g_m(1+)$, $g_m(2+)$ and $g_m(-)$) and two outputs ($g_m(1+)$, $g_m(2-)$) connected to the integrator input and contributing to C_I . Each unit cell forming the complete integrator has been studied in detail and their corresponding models obtained (tables 1 and 2). From this analysis, $C_{in}(N)$ and C_{out} are the equivalent input and output capacitance respectively for each unit cell; which, combined with the previous consideration, leads directly to the definition obtained for C_I .

The low-impedance internal node strategy combined with the use of a negative resistance to enhance the differential dc-gain of the system, while increasing the differential input resistance and reducing the phase error, suggested the use of cascode topologies to us, also taking advantage of their inherent transmission zero reduction. The differential dc-gain obtained in both structures, shown in Eq.(15) and (27) respectively, reflects the existence of this positive feedback compensation, making the ideal infinite dc-gain of the integrator possible. Regarding the common-mode behaviour of the circuit, both implementations are described with the same expression complying with the stability requirement $|A_{CM}| < 1$: $A_{CM} \sim -1/(A_N + A_P) \sim -1/2$.

Variations on the negative resistance value are equivalent to considering a mismatching between $M_N(1)$ and $M_N(2)$, which generates a difference between the drain currents of these transistors. Furthermore, the same effect can also be achieved by modifying bias currents I_{BIAS} in these two branches of the circuit. In consequence, the tuning of the value of this negative resistance allows for correction in process deviations and mismatching between the transistors M_N that process the signal.

Finally, cascode stages introduce two dominant parasitic poles and a dominant zero as shown in Eq.(8), which stem from parasitic capacitances mainly associated with the source nodes of cascode transistors. In consequence, an excess phase shift $\Delta\phi(\omega_t)$ takes place at unity-gain frequency (Eq. 37). Theoretically, by using the minimum length for cascode transistors and minimizing source and drain diffusion areas, the parasitic poles and zero can be located further away from the unity-gain frequency. This consideration will also minimize distributed-channel effects, which cannot be ignored at high frequencies (Tsividis, 1999). However, the minimum channel length is conditioned by the required transistor matching (Pelgrom et al., 1989).

$$\Delta\phi(\omega_t) \approx \frac{\pi}{2} - \tan^{-1}\left(\frac{\omega_t}{\delta_1}\right) - \tan^{-1}\left(\frac{\omega_t}{\delta_2}\right) - \tan^{-1}\left(\frac{\omega_t}{s_0}\right) \quad (37)$$

These general considerations reflect the benefits of the topology and its frequency limits. Nevertheless, both integrators have been implemented, and the real values drawn from these designs allow a better study of the frequencies related to parasitic effects to be carried out and a comparison to be made between both topologies.

Second-order frequency dependence. The previous study for the frequency behaviour of the integrator was summarized in Eq.(8), and, taking into account the definition for the integrator quality factor (Eq. 4), the general relation in both approximations can be reported as:

$$\frac{1}{Q_{\text{int}}} = \frac{\delta g_m + g_o'}{g_m(N)} - \frac{C_{gd}(N)}{C_I} - \frac{C_p(C)}{C_I} \frac{g_m(N)}{g_m(C)} \quad (38)$$

where g_o' is the sum of output conductances at the input node, C_I is the total integration capacitance, $g_m(C)$ is the transconductance of the cascode element ($g_m(\text{NC})$ and $g_m(\text{PF})$ for the HS and FC approach respectively), and $C_p(C)$ the parasitic capacitance at the low-impedance node associated to the cascode structures (node X in Figs. 8 and 9).

The second-order frequency dependence can be analysed when considering the M_N transistor mismatch $A_N - A_P = \delta g_m / g_m$ and including the frequency dependence for their transconductance $g_m(s)$ (Eq. 39) in the transfer function (Smith et al., 1996; Zele et al., 1996). In this way, the non-quasistatic model for the MOS transistor, required for operation at very high frequencies, is included.

$$g_m(s) = \frac{g_m(N)}{1 + s\tau} \quad ; \quad \tau = \frac{2 C_{gs}(N)}{5 g_m(N)} \quad (39)$$

By simplifying the result obtained to draw some conclusions, the frequency behaviour of the integrator is described (Eq. 40) reflecting the effect of these additional second-order dependencies.

$$\frac{1}{Q_{\text{int}}} = \left(\frac{g_o'}{g_m(N)} \right)^2 + \frac{\delta g_m}{g_m(N)} - \frac{3C_{gs}(N)}{7C_I} - \frac{C_{gd}(N)}{C_I} - \frac{C_p(C)}{C_I} \frac{g_m(N)}{g_m(C)} \quad (40)$$

From this study, a set of parasitic poles and zeros appear at frequencies higher than 15 GHz in the proposed designs, the effect of which is considered negligible in a first-order approximation.

5. Noise

In general, the range of signals that can be accurately driven by electronic devices is limited. For low-signals, electrical noise restricts the minimum amplitude that can be processed. Noise is considered as all the unwanted electrical signals generated within the device or externally and coupled to the output of the system. These signals appear in the system whether input signals are applied or not. Noise signals interfere with the incoming signal and make it impossible to detect with sufficient quality the signals presenting an amplitude comparable to the noise level. Moreover, signals below this level are almost impossible to detect. So, noise in the system represents the lowest level for the incoming signal (Silva-

Martínez et al., 2003). The origins of noise can be classified as intrinsic and extrinsic transistor noise sources, following a similar notation to that used for the parasitic elements of the MOS transistor. There are two dominant intrinsic noise sources in CMOS transistors: channel thermal noise and $1/f$ or flicker noise. Extrinsic noise is mainly due to the signals produced by the surrounding circuitry and coupled to the device or to the system. The only noise considered in this work is noise generated by the transistor.

The noise of a G_m -C filter is caused by the noise output currents of the transconductors and the mean square noise currents are generally proportional to the corresponding transconductance. Considering the model of a noisy transconductor, the output mean square noise current over a certain frequency interval df is given by:

$$\overline{i_n^2} = 4 k T NF g_m df \quad (41)$$

where k is the Boltzmann constant, T the absolute temperature and NF a noise factor determined by the electronic design of the transconductor. $NF=1$ corresponds to a transconductor output noise current equal to the thermal noise current of a resistor of value $R=1/g_m$.

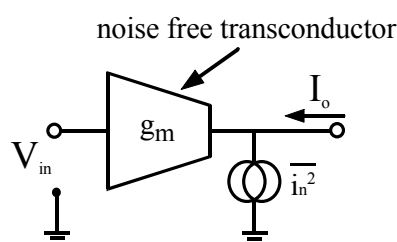


Fig. 10. Transconductor noise model.

To investigate the latter effect in the frequency design of VHF filters, calculating the noise factor and its frequency dependence becomes necessary in both HS and FC transconductor implementations, because filter noise behaviour not only depend on the filter parameters but also on the transconductor noise behaviour. Therefore, the NF -factor appears as a useful quantity to translate the transconductor noise properties to the filter noise properties and, likewise, the properties of each unit cell to the complete transconductor implementation. In consequence, transconductor output noise is determined by the noise properties of the unit cell and by the properties of the transconductor topology.

The transconductor topology analysed is the balanced structure shown in Fig. 3. First, the noise behaviour of each single unit cell is calculated ($H_{HS}(s)$ and $H_{FC}(s)$) and then the noise factor of the complete transconductor in both implementations, $F_{HS}(s)$ and $F_{FC}(s)$.

5.1 Noise model for the unit cell

For high and very-high frequencies, the $1/f$ or flicker noise can be neglected. Assuming only thermal noise, the drain-current noise of a single transistor can be written as:

$$\overline{i_n^2} = 4 k T c g_m df \quad (42)$$

where k is the Boltzmann constant, T the absolute temperature, g_m the small-signal transconductance of the transistor, and df the frequency interval over which the noise is

measured. The constant c value is 2.5 for a short-channel transistor working in the saturation region² (Tsividis, 1999). The noise output current of the HS unit cell (Fig. 6(a)) is:

$$\overline{i_n^2}(HS) = 4 k T H_{HS} df \quad (43)$$

where:

$$H_{HS} = (1 - \sqrt{\alpha})^2 c(PC) g_m(PC) + \alpha c(P) g_m(P) + (1 - \sqrt{\beta})^2 c(NC) g_m(NC) + \beta c(N) g_m(N) \quad (44)$$

$$\sqrt{\alpha} = \frac{g_m(PC) + g_{ds}(PC)}{g_m(PC) + g_{ds}(PC) + g_{ds}(P)}; \quad \sqrt{\beta} = \frac{g_m(NC) + g_{ds}(NC)}{g_m(NC) + g_{ds}(NC) + g_{ds}(N)} \quad (45)$$

For the FC approach, the noise output current of the unit cell (Fig. 6(b)) can be written as:

$$\overline{i_n^2}(FC) = 4 k T H_{FC} df \quad (46)$$

where:

$$H_{FC} = (1 - \sqrt{\alpha})^2 c(PF) g_m(PF) + 2\alpha c(P) g_m(P) + c(NS) g_m(NS) + \alpha c(N) g_m(N) \quad (47)$$

$$\sqrt{\alpha} = \frac{g_m(PF) + g_{ds}(PF)}{g_m(PF) + g_{ds}(PF) + 2g_{ds}(P) + g_{ds}(N)} \quad (48)$$

As a result, certain conclusions can be drawn from this study. The main noise sources in both topologies are transistors M_N processing the signal and bias current sources, to which the main contribution applies. The FC unit cell presents a noise factor 2.5 times higher than the HS topology, which is due to the additional current sources required in this topology.

5.2 Noise model for the complete transconductor cell

The noise factor of the complete transconductor can be calculated using the model obtained for the unit cells (Nauta, 1993), or by calculating the complete noise model of the proposed transconductance cell from the start. We use this second option to obtain a more accurate result, modelling the output noise currents of the transistors with noise current sources in parallel with the outputs as in the previous section. The two noise output currents of the differential transconductor are $\overline{i_{n,plus}^2}$ and $\overline{i_{n,minus}^2}$. Following a similar process as in the noise study on the unit cells, the noise output current of the complete HS transconductor can be written as:

$$\overline{i_{n,plus}^2}(HS) = \overline{i_{n,minus}^2}(HS) = 4 k T F_{HS} df \quad (49)$$

² The constant c , which models transistor noise behaviour, depends on both its operation region and its dimensions. A theoretical derivation for the transistor working in the linear region leads to $1 < c < 2$; however, $c = 2/3$ for a long-channel device and $c = 2.5$ for a short-channel device are obtained in the saturation region (Tsividis, 1999).

where:

$$F_{HS} = c(PC) F_{HS}(PC) + c(P) F_{HS}(P) + c(NC) F_{HS}(NC) + c(N) F_{HS}(N) \quad (50)$$

$$F_{HS}(PC) = x_1^2 [(A_N + A_P - 2)g_m(N) \cdot (g_m(NC) + g_{ds}(NC)) \cdot x_2 + 2g_{ds}(P)g_{ds}(PC)x_3 + 2g_{ds}(N)g_{ds}(NC)x_2]^2 g_m(PC) \quad (51)$$

$$F_{HS}(P) = \frac{F_{HS}(PC)}{g_m(PC)} \left(\frac{g_m(PC) + g_{ds}(PC)}{g_{ds}(P)} \right)^2 g_m(P) \quad (52)$$

$$F_{HS}(NC) = \left(g_{ds}(N) + \frac{x_2 g_m(N)(g_m(NC) + g_{ds}(NC))(g_m(NC) + g_{ds}(NC) - g_{ds}(N))}{\alpha} \right)^2 x_2^2 g_m(NC) \quad (53)$$

$$F_{HS}(N) = \left(1 + \frac{x_2^2 (g_m(NC) + g_{ds}(NC))^2 (A_N + A_P) g_m^2(N)}{\alpha^2} \right) x_2^2 (g_m(NC) + g_{ds}(NC))^2 g_m(N) \quad (54)$$

$$x_1 = \frac{g_{ds}(P) x_3}{\alpha}; \quad x_2 = \frac{1}{g_{ds}(N) + g_m(NC) + g_{ds}(NC)}; \quad x_3 = \frac{1}{g_{ds}(P) + g_m(PC) + g_{ds}(PC)} \quad (55)$$

$$\alpha = x_2 (g_m(NC) + g_{ds}(NC)) ((A_N + A_P) g_m(N) - 2g_{ds}(NC)) + 2g_{ds}(NC) + 2g_{ds}(P)g_{ds}(PC)x_3 \quad (56)$$

The noise output current of the complete transconductor implemented with FC unit cells can be written as:

$$\overline{i_{n,plus}^2(FC)} = \overline{i_{n,minus}^2(FC)} = 4kT F_{FC} df \quad (57)$$

where:

$$F_{FC} = c(PF) F_{FC}(PF) + c(P) F_{FC}(P) + c(NS) F_{FC}(NS) + c(N) F_{FC}(N) \quad (58)$$

$$F_{FC}(PF) = \left(1 - \alpha - \frac{2\alpha(1-\alpha)}{\chi} \right)^2 g_m(PF); \quad F_{FC}(P) = 2\alpha^2 \left(1 - \frac{2\alpha}{\chi} \right)^2 g_m(P) \quad (59)$$

$$F_{FC}(NS) = \left(1 - \frac{2\alpha}{\chi} \right)^2 g_m(NS); \quad F_{FC}(N) = \left(1 + \frac{\alpha^2}{\chi^2} (A_N + A_P) \right) \alpha^2 g_m(N) \quad (60)$$

$$\alpha = \frac{g_m(PF) + g_{ds}(PF)}{g_m(PF) + g_{ds}(PF) + 2g_{ds}(P) + g_{ds}(N)}; \quad \chi = 2(1-\alpha) \frac{g_{ds}(PF)}{g_m(N)} + 2 \frac{g_{ds}(NS)}{g_m(N)} + \alpha(A_N + A_P) \quad (61)$$

From this study, the major noise contributions are those due to NMOS transistors in the signal path, M_N , representing almost the total contribution for the FC implementation. The contribution of the bias current sources, which was relevant in the noise analysis of the unit cells, becomes negligible when implementing the complete fully-balanced current-mode

topology. A significant benefit of this structure is that the previous noise-related difference existing between the two unit cells disappears in the complete transconductor, with the same value being obtained mostly for F_{HS} and F_{FC} . Another important conclusion is that the output noise current is independent of the value of the negative resistance δg_{mv} inherent characteristic of the topology.

Hence, the noise is dominated by the M_N transistors involved in the V to I conversion, with similar noise contributions being achieved for both transconductor implementations. The post-layout simulation results corroborate this idea, with a total input-referred noise of 11 nA_{rms} being obtained for the HS topology and 8 nA_{rms} for the FC approach. This is a very important design conclusion and requires be further considered in the design of high-performance filters.

6. Distortion

The ability to handle large signals with minimum distortion is an important consideration in most linear applications. In this section, the large signal characteristics of the current mode integrator for differential inputs are analysed using first-order square-law MOSFET models, which can provide a sufficiently accurate description of the large signal behaviour for design purposes. The proposed transconductor topology (Fig. 3) has been implemented by using two different cascode architectures: the HS and the FC approach. Transconductor V-I conversion is obtained in the output stage g_{mv} and a negative resistance, shown in grey in the same figure, is connected at the input in order to improve the topology characteristics.

A theoretical distortion analysis including all the non-linearities would be too complex and provides no practical benefit. Consequently, a separate study of each factor affecting linearity has been developed to obtain simple and efficient design strategies. There are two main contributions to transconductor distortion, the first one will be non-linearities in V to I conversion, and the second non-linearities in the negative resistance. Each effect is analysed separately. The effects of capacitor non-linearities are not taken into account here.

6.1 Non-linearities in V-I conversion

For this study, only the output stage will be considered, i.e., the transconductor cell without the negative resistance. This differential structure will present good linearity in V-I conversion if both paths are perfectly matched. Using a simple model of the MOS transistor, the drain currents of the N- and P-channel MOS transistor in strong inversion can be written as:

$$I_{dn} = \beta_n (V_{gsn} - V_{tn})^2; \quad I_{dp} = \beta_p (V_{gsp} - V_{tp})^2 \quad \text{with} \quad \beta_n = \frac{\mu_n C'_{ox} W_n}{2L_n}; \quad \beta_p = \frac{\mu_p C'_{ox} W_p}{2L_p} \quad (62)$$

Considering $V_{IN}^+ = V_C + v_{in}/2$, $V_{IN}^- = V_C - v_{in}/2$ and v_{in} the differential input voltage of the transconductor cell, the differential output current can be written as:

$$I_{out} = i_{out}^+ - i_{out}^- = 2\sqrt{I_{BIAS}\beta_n(N)} v_{in} \quad (63)$$

where I_{BIAS} is the bias current per branch and $\beta_n(N)$ the factor associated to the M_N transistor in both implementations. The same result has been obtained with the two possible transconductor structures, the HS and the FC topologies, leading to the same distortion

analysis in both situations. This equation is valid as long as the transistors operate in strong inversion and saturation, and show that the differential voltage to current conversion of the transconductor is perfectly linear, making use of the square-law and matching properties of the MOS transistors. However, mobility reduction will cause deviations from the transistor square-law behaviour, generating distortion. The mobility of the NMOS and PMOS transistors can be expressed in the first-order approximation as:

$$\mu_n = \frac{\mu_{on}}{1 + \theta_n (V_{gsn} - V_{tn})}; \quad \mu_p = \frac{\mu_{op}}{1 - \theta_p (V_{gsp} - V_{tp})} \quad (64)$$

Considering again the output stage of the complete cell (Fig. 3), driven balanced around the common-mode voltage level V_C as previously explained, the differential output current can be calculated as:

$$I_{out} = i_{out}^+ - i_{out}^- \quad (65)$$

Using the previous expressions for mobility reduction and assuming equal transistors operating in saturation, the differential output current can be expanded into Taylor series:

$$I_{out} = \frac{k_{on} V_{on} \left(1 + \frac{1}{2} \theta_n V_{on}\right)}{(1 + \theta_n V_{on})^2} v_{in} - \frac{\theta_n k_{on}}{(1 + \theta_n V_{on})^4} \frac{1}{8} v_{in}^3 - \frac{\theta_n^3 k_{on}}{(1 + \theta_n V_{on})^6} \frac{1}{32} v_{in}^5 + \dots; \quad (66)$$

where: $V_{on} = V_C - V_{tn} = \sqrt{\frac{I_{BIAS}}{\beta}} > 0$ and $k_{on} = \frac{\mu_{on} C'_{ox} W_n}{L_n}$.

The fifth and higher order distortion terms can be neglected, giving the following as a result for distortion calculation:

$$I_{out} = C_1 v_{in} + C_3 v_{in}^3; \quad \text{with} \quad C_1 = \frac{k_{on} V_{on} \left(1 + \frac{1}{2} \theta_n V_{on}\right)}{(1 + \theta_n V_{on})^2}; \quad C_3 = \frac{-\theta_n k_{on}}{(1 + \theta_n V_{on})^4} \frac{1}{8} \quad (67)$$

$$HD_3 = \frac{C_3}{C_1} = \frac{-\theta_n}{8 V_{on} (1 + \theta_n V_{on})^2 \left(1 + \frac{1}{2} \theta_n V_{on}\right)} \approx \frac{-\theta_n}{8 V_{on}} \quad (68)$$

The expression for HD_3 can be simplified as $\theta_n V_{on} \ll 1$. This expression is the same for both implementations of the transconductor cell. The main conclusion from Eq.(68) is that increasing V_{on} , i.e., the common-mode voltage V_C or the bias current I_{BIAS} , lowers the distortion in the V-I transfer.

6.2 Non-linearities in the negative resistance

Non-linearities in V-I conversion and non-linearities in the negative resistance will introduce non-linear effects in the input resistance of the differential transconductor (Nauta, 1993). The effect of these non-linearities is a signal dependent integrator quality factor, i.e., a phase error; and can cause distortion in filters, especially high-Q filters. As long as the value

of the input impedance is high enough and an enhancement of the dc-gain is obtained, the effect of non-linearities will be slight. Considering the equations for a single transistor reported in Eq.(62) and analysing the structure shown in Fig. 3, the differential input voltage can be written as:

$$v_{in} = \sqrt{\frac{I_{BIAS}}{\beta_n}} \left(\sqrt{1 + \frac{i}{I_{BIAS}}} - \sqrt{1 - \frac{i}{I_{BIAS}}} \right) \quad (69)$$

where $(2i)$ is the differential input current, i.e., $I_i^+ = i$ and $I_i^- = -i$, considering the description shown in Fig. 3. The same relation has been obtained in both implementations, leading again to the same distortion analysis. This expression can be expanded into Taylor series, where $A=i/I_{BIAS}$, $\alpha_1=1$ and $\alpha_3=1/8$.

$$v_{in} = \alpha_1 A \cos(\omega t) + \alpha_2 A^2 \cos^2(\omega t) + \alpha_3 A^3 \cos^3(\omega t); HD_2 = \frac{\alpha_2 A}{2\alpha_1}; HD_3 = \frac{\alpha_3 A^2}{4\alpha_1} \Rightarrow HD_3 = \frac{1}{32} \left(\frac{i}{I_{BIAS}} \right)^2 \quad (70)$$

The large signal output characteristics of the current mode integrator present a similar form to that of the standard MOS differential pair. On the other hand, the distortion generated in positive feedback compensation through negative resistance is only dependent on the ratio between the input current and the bias current I_{BIAS} . This analysis is the same for both implementations of the transconductor topology.

6.3 Matching and harmonic-distortion

The process that causes time-independent random variations in physical parameters of identically designed devices is called mismatch, and is a limiting factor in general-purpose analog signal processing. The impact of MOS transistors mismatching becomes very important because the dimensions of the devices are reduced and the available signal swings decrease. To obtain a better circuit design, the physical origin of this effect has been discussed in several studies (Pelgrom et al., 1989), not only for its random but also for its systematic contribution (Gregor, 1992), and also possible measurements for its characterization (Felt et al., 1994).

Thanks to the use of a fully-balanced pseudo-differential topology, with this inherent positive feedback compensation providing the system with an enhancement of the differential dc-gain, distortion resulting from mismatch is small. As mentioned above, the existing negative resistance enables small variations in dimensions of M_N transistors and bias current sources I_{BIAS} to be controlled. In order to obtain a good matching, the minimum channel length related to the considered CMOS technology must be avoided. However, high frequency operation requires short channels, relying on the negative resistance to obtain the adequate matching between transistors in the signal path. In addition, channel length modulation is not considered, as it only has a substantial effect on integrator response linearity at low frequencies, where distortion is suppressed by feedback (Smith et al., 1996; Zele et al., 1996). In consequence, transistors are assumed to be well matched, which will be achieved by means of a lower mismatching sensitive design while obtaining the final layout.

Mismatching between transistors also degrades the outstanding benefits provided by balanced structures, since they depend strongly on the symmetry of the circuit. Therefore, mismatching can also be reflected in unbalanced signal paths. Post-layout simulations have been accomplished regarding sensitivity to this unbalance for both HS and FC transconductor implementations. The starting point was an input signal of 10 MHz and 45 dB of THD. Subsequently, variations of 10% and 20% in magnitude and phase between the input currents I_i^+ and I_i^- were considered while analysing the effect on the THD. Regarding the variations in magnitude: with a shift of 10% between the magnitude of I_i^+ and I_i^- , the THD changes by 1 dB (HS) and 0.5 dB (FC), and for a shift of 20%, the THD changes by 2 dB and 1.5 dB respectively. For deviations between the phase of I_i^+ and the phase of I_i^- , with a shift of 10%, the THD changes by 1 dB for both topologies; and for a shift of 20%, the THD changes by 8 dB (HS) and 6 dB (FC).

As a result, we can conclude that the proposed topology is quite insensitive to transistor mismatching. In addition to this, the effect of common-mode signal mismatching is alleviated by means of feedback compensation, as previously explained, thus supporting the proposed design strategy.

7. Digital programmability

Apart from the usual requirements associated with high frequency CMOS filter design, the issue of programmability brings to the forefront the considerable problem of maintaining performances such as frequency response accuracy, noise and dynamic range across the entire tuning range. Requirements of robust and precise implementation of filtering systems in the VHF range point to programmable G_m -C continuous-time filters as the best option for obtaining a wide programming range (usually 1:5). Due to process and temperature variations, G_m/C time-constants are liable to vary by as much as $\pm 30\%$. The fact of considering both effects at the same time means that the unity-gain frequency ω_t of each integrator in the filter should be electronically variable over a wide range.

Lower supply voltages required by current digital CMOS technologies make the use of conventional continuous tuning techniques over a wide frequency range very difficult due to their effect on dynamic range and non-linear distortion. These techniques are based on the variation of the transistors biasing points, limiting their application to compensate the inherent changes due to temperature and the technological process. Therefore, discrete tuning is the best option to preserve the dynamic range (DR).

There are three different ways of achieving this wide range of variability: the capacitor, the transconductor or both can be made programmable. At high frequencies, the integrating capacitances are relatively small. If they are replaced by capacitor arrays to obtain C-programmability, the net parasitic capacitances at the terminals of the array can be quite large when the array is implementing the lowest effective capacitance, which is a very difficult problem to solve. In addition to this, switchable array of capacitors provides high precision on filters though the existence of switches in the signal path. So, the constant-C scaling technique is the option considered, leading to the desired programmability by varying G_m discretely while maintaining the noise specifications over the entire frequency range. Furthermore, lower power consumption is achieved at low frequency values of the

programming range. This is the best option for maintaining a trade-off between noise specifications, power consumption and programming range (Pavan et al., 2000).

Two different strategies can be used to extend the tuning range and preserve DR: switchable array of degenerating MOS resistors and parallel connection of identical transconductors switched by a digital word. The first one uses the same transconductor and capacitor throughout the whole frequency range whilst the degeneration resistor R is formed by a parallel connection of MOS triode transistors (Bollati et al., 2001). This technique involves variations over the entire frequency range of the noise factor, which is proportional to the degenerated resistor, generating dynamic range variations. Phase errors will also appear, achieving the worst situation for both undesirable parameters in the opposite ends of the frequency range: minimum DR (maximum R) for the lowest frequency f_{\min} , and maximum phase error for the highest frequency f_{\max} . However, this strategy leads to the simplest structure, with a small active area and lower power consumption. The second strategy consists of a parallel connection of identical transconductors obtaining a programmable array where the desired time-constant can be digitally tuned (Pavan et al., 2000). This solution is the best option for VHF applications. However, its main drawbacks are power consumption and area, proportional to the number of connected active cells.

Considering all these ideas, the latter strategy is the technique selected for achieving the desired programmability for the proposed topology. Programmability using a parallel connection of conventional differential pairs has been published previously (Pavan et al., 2000); however, these structures are not directly suitable for low-voltage supply. It is worth noting that obtaining a programming range for a transconductor also includes an additional gap of $\pm 30\%$ for the extreme transconductance values G_{\min} and G_{\max} , in order to compensate the deviation due to temperature and technological process variations. Therefore, the total tunable range will be greater than the nominal one.

7.1 Principle of programmability

Our proposal is to achieve a digitally programmable transconductor, specifically designed for a wide programmability range comprised of parallel connection of unit cells. Fig. 11 shows the conceptual scheme of a 3-bit programmable cell. This topology presents two main drawbacks; the need for additional transistors in the signal path and the variation of parasitic capacitances C_{pin} and C_{pout} depending on the digital word. However, it is necessary to keep the dynamic range constant for each g_m value and the total node parasitic capacitances over the entire programming range.

This solution is adopted for the proposed transconductor topology, giving a HS implementation with a programmable range from 1:7 (Fig. 12(a)) and a FC implementation with a varying range from 1:5 (Fig. 12(b)). Each cascode unit cell (Fig. 6), i.e., cascode amplifier and biasing current source, consists of a parallel connection of equal cells switched by a digital word. The connecting lines of the substrate terminals are not shown on these schematics as the explanation has already been given in previous sections. By driving the gates of the cascode transistors (M_{NC} and M_{PC} in the HS approach, and M_{PF} and M_{NS} in the FC) with modulated digital voltages we can obtain the desired transconductance with no switches in the signal path and power consumption proportional to total transconductance.

The other disadvantage inherent to this topology can be also alleviated with an additional design strategy. When a change in the digital word occurs, some transistors change from saturation to cut-off region and *vice versa*, and different contributions to total input node

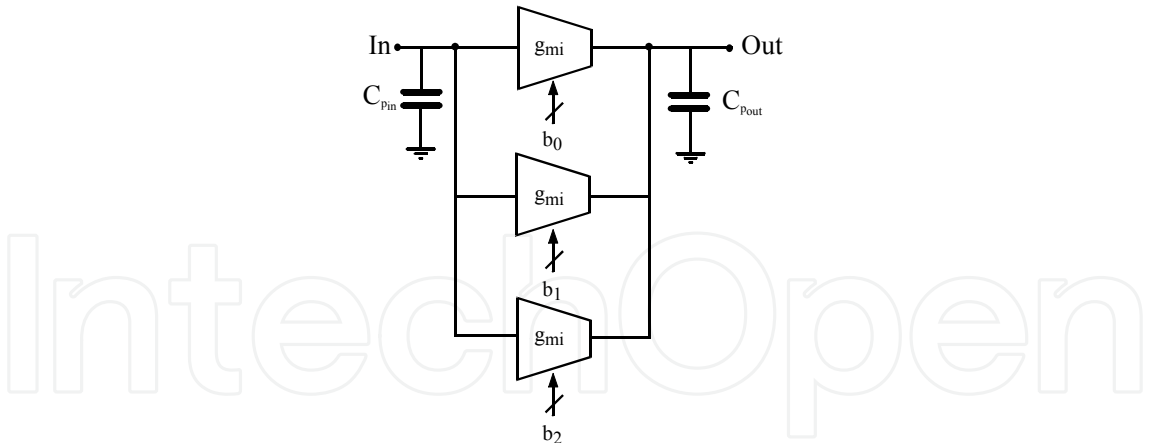


Fig. 11. Topology of the 3-bit programmable transconductor.

parasitic capacitance C_{pin} are obtained. This change can generate a shift in the desired frequency and Q-factor variations, limiting the integrator and filter performance. In consequence, the implementation of each unit cell has been modified by using dummy elements connected at the input, which allow us to make the input capacitance independent of the digital word, maintaining the same parasitic capacitances on the signal processing nodes (Pavan et al., 2000). Note that the total output parasitic capacitance –junction extrinsic capacitance– is also constant because it has almost the same value for cut-off or saturation transistors (Tsividis, 1996; Tsividis, 1999).

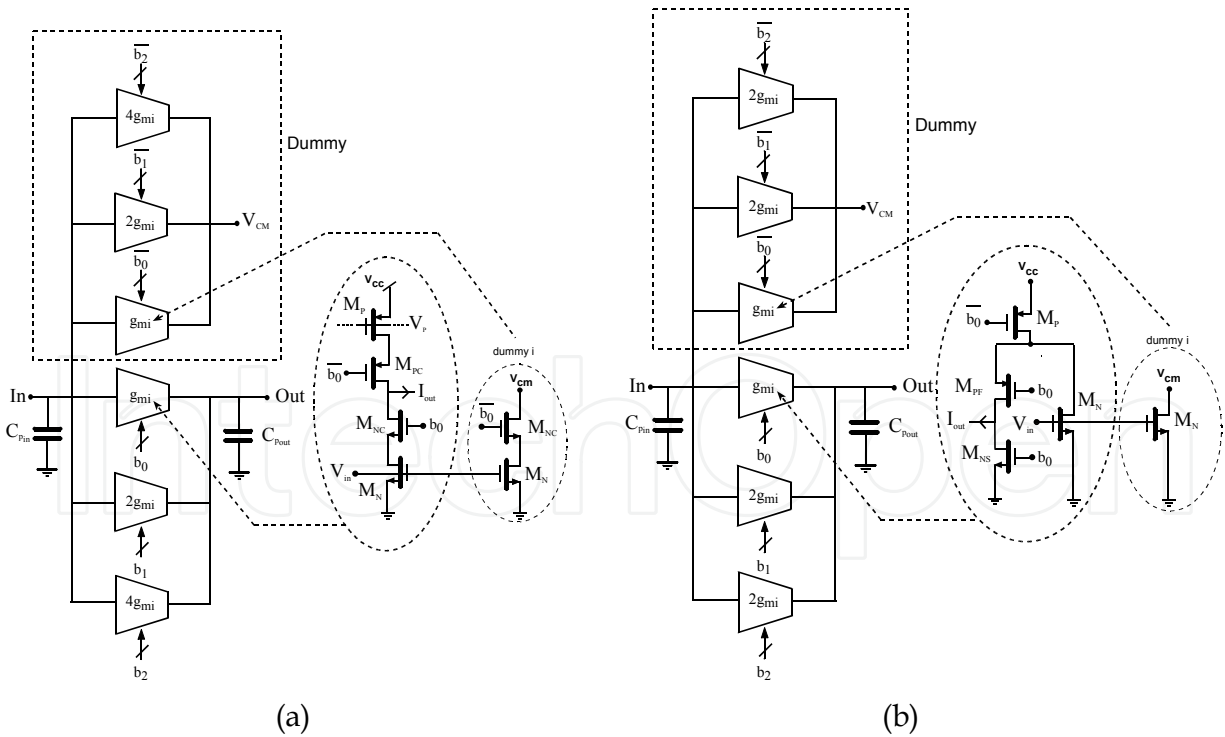


Fig. 12. Implementation of 3-bit programmable topology: (a) HS and (b) FC transconductor. As the output conductance is proportional to the transconductance, the differential dc-gain is maintained irrespective of the digital word. Consequently, the relative shape of the frequency response, output noise power and dynamic range are independent of the digital

word. Therefore, we obtain the desired programmable transconductor with no switches in the signal path by driving the gates of bias and cascode transistors with a digital word modulated with the adequate analog value. The power consumption is proportional to the necessary transconductance in each frequency range. The digital control word for programming the transconductor is $b_2b_1b_0$, controlling transconductance value from $001 \equiv g_m$ to $111 \equiv 7g_m$ in the HS topology and from $001 \equiv g_m$ to $111 \equiv 5g_m$ in the FC topology.

7.2 Implementation results

Two different integrators have been implemented. The first one is based on the HS topology, considering the total input node parasitic capacitance –basically gate-source capacitances– as the total integration capacitance with no need for any external capacitors, in order to reach the maximum operation frequency with moderate power consumption. Therefore, for this situation, maintaining the integration capacitance constant becomes essential and its value can be controlled by means of the dummy-based system.

Fig. 13(a) plots the post-layout simulation results for HS implementation and shows the variation of unity-gain frequency versus digital word value. The expected linear dependence of the transconductance and the constant integration capacitance are observed, and a programming range from 28 to 185 MHz is obtained by varying the digital word. However, a marked phase lag due to parasitic effects (parasitic zero s_0) at high frequency was detected, as expected. A possible compensation scheme, is based on two capacitors, C_C , implemented with dummy MOS transistors and connected in a cross-coupled manner as shown in Fig. 7(a). Consequently, by using this compensating scheme, the phase shift error is effectively reduced and a very efficient scheme endowed with a phase error of less than 3° over the entire frequency range is obtained.

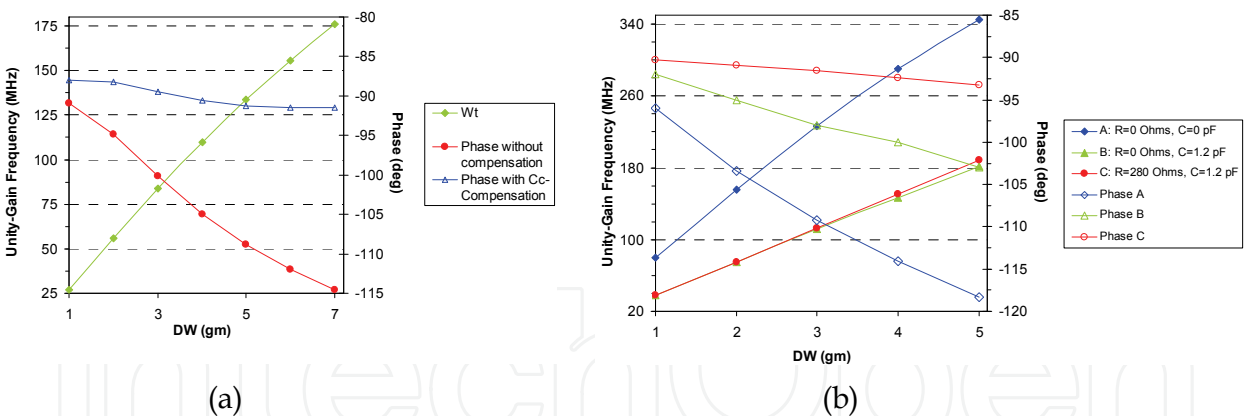


Fig. 13. Unity-gain frequency and phase vs. digital word value for the: (a) HS integrator with and without compensation scheme; (b) FC integrator with various compensation schemes.

The second implementation is based on the FC topology, considering integration capacitance in this case as the total input node parasitic capacitance together with an additional one ($C_{ext}=1.2$ pF). Total integration capacitance is once more maintained constant by means of the dummy-based system and Fig. 13(b) plots the post-layout simulation results. The first curve plots the variation of the transconductance as a function of the digital word when no external capacitance is connected at the input; a non-linear response is obtained, due to the expected parasitic poles and zeros. When connecting the external capacitance, the expected linear dependence is obtained, providing the system with coarse

tuning. Nevertheless, a phase shift is obtained even when the compensation scheme based on the two cross-coupled capacitors C_C is used.

Next step involves a resistance R being connected at the input in series with the external capacitance, as shown in Fig. 7(b). This resistor is implemented with a transistor working in the linear region and is the best option to compensate this phase error. Therefore, by varying the digital word, the unity-gain frequency is controlled and the phase error is effectively reduced over the entire programming range. Then, to control the operation frequency and to reduce the phase error, a shunt connection is made at the input between a resistance and the integration capacitance C_I . We obtain a compensation scheme for the FC transconductor based on an RC circuit at the input, leading to a programming range from 40 to 200 MHz by varying the digital word with a phase error of less than 3° over the entire frequency range.

We can define the transconductor input voltage variations around the bias point (V_C) as shown in Fig. 3. The linear input range is constant for digital scaling of the transconductance as shown in Fig. 14. The variation of the g_m as a function of the digital word is presented, providing the system with coarse tuning. In consequence; for the HS topology, ω_t is controlled from 28 to 185 MHz by varying the digital word from 1 to 7; and for the FC topology, ω_t varies from 40 to 200 MHz by varying the DW from 1 to 5. Therefore, by means of a parallel connection of equal transconductors switched by a digital word we guarantee that the DR for each g_m value and the total external node capacitances will be kept constant.

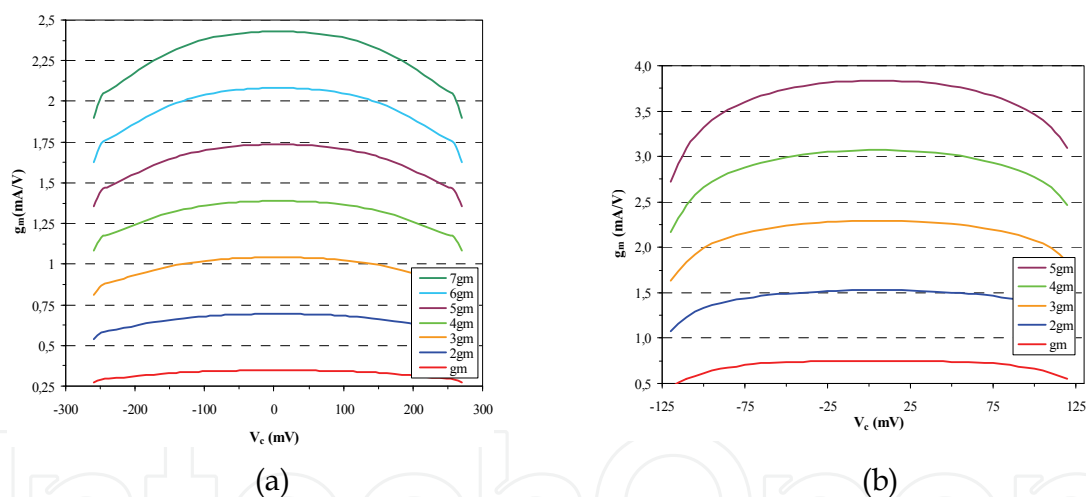


Fig. 14. Transconductance as a function of the digital word (coarse tuning) for the: (a) HS implementation; (b) FC implementation.

On the other hand, fine tuning can be achieved if necessary, as the transconductance value can be controlled by varying the bias current source for a fixed digital word. Hence, discrete steps are swept by varying the bias current while maintaining the same dynamic range. At the same time, an additional control over the dc-gain can be achieved by modifying the ratio between the bias currents of the negative resistance: M_1/M_2 and M_4/M_5 in both topologies, solving problems associated to mismatching between transistors. Therefore, a complete control of the frequency response can be obtained. The trade-off between transconductance and linear input range is shown in Fig. 15 for both topologies. These figures can also be seen as the fine tuning for the proposed structure since the transconductance value is controlled by varying the bias current source for a fixed digital word: I_{bias} changes from 45 to 180 μA

control the HS transconductance from 270 to 452 $\mu\text{A/V}$, and changes from 40 to 100 μA in the FC topology control the transconductance from 550 to 800 $\mu\text{A/V}$.

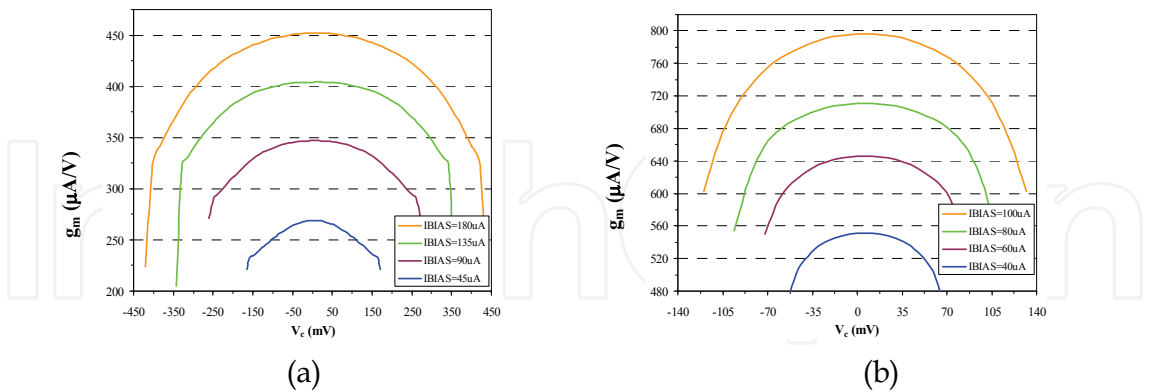


Fig. 15. Transconductance versus biasing currents (fine tuning) for the: (a) HS implementation; (b) FC implementation.

To conclude, the proposed structure is a balanced topology aimed at improving immunity to digital noise and linearity. A digitally programmable transconductor has been designed, maintaining the same dynamic range over the entire frequency range. Therefore, it can be used in the design of programmable filters, as the expected characteristics of a programmable cell will be obtained: to maintain Q-factor, noise power and maximum signal swing constant over the entire programming range, leading to a DR independent on the operation frequency. The expected linear dependence of the unity-gain frequency is obtained and the phase error is effectively reduced over the entire programming range in both implementations, with a compensation scheme based on two cross-coupled capacitors for the HS topology and the classical RC circuit connected at the input for the FC approach.

8. Results and discussion

To demonstrate the theoretical advantages of this approach for a programmable transconductor suitable for VHF, two 3-bit programmable integrators have been designed. The HS transconductor has been implemented by using the design kit of an AMI Semiconductor (AMIS) 0.35 μm CMOS technology (P-substrate, N-well, 5-metal, 2-poly) with a 3 V power supply and a nominal bias current of 90 μA per branch; whereas the FC transconductor has been implemented by using the design kit of an AMS (C35B4C3) 0.35 μm CMOS technology (P-substrate, N-well, 4-metal, 2-poly) with a 2 V power supply and a nominal bias current of 100 μA per branch.

The dimensions of the transistors were chosen in order to cover all the design requirements obtained in this chapter, leading to a complete sweep of the discrete step by varying the bias current. In this way, for the HS implementation, the operation point is located at 90 μA and the bias current adjustment is possible from 45-180 μA . However, for the FC implementation, the operating point is located at 100 μA , covering the digital step by varying the bias current from 20-110 μA . In this way, the discrete tunability requirement is obtained but the FC transconductance value at the operation point is maximised.

8.1 Layout strategy

A careful layout has been drawn out to obtain all the characteristics associated with the proposed design accurately and demonstrate the feasibility of the intended approach. As

stated below, we have taken special care to get rid of the unwanted effects related to parasitic elements and mismatching (Baker et al., 1998; Hastings, 2001). All the designs have been carried out taking into account the specific design rules for high frequency operation, which are highly appropriate for obtaining good matching between components. Interdigitized and common-centroid layout techniques have been considered to reduce the variations of threshold voltage, which are associated with gradients in gate-oxide thickness. Guard rings have been included in the design with the aim of reducing substrate noise. Bond-pads have also been carefully laid out and, in this way, input and output pins have been placed as far as possible between them. Balanced structures provide outstanding benefits, but they are strongly dependent on the symmetry of the circuit. Consequently, special care has been taken to outline the paths of the balanced signals, in an attempt to ensure the best matching between them. MOS devices have fragile gates seeing that electrostatic discharges may cause destruction of the device if the oxide breakdown voltage is exceeded. Considering this point, we concluded that it would be advisable to provide the transistors that control the quality factor of the circuit with a path protection system. The scheme chosen to achieve this goal was the anti-parallel diodes configuration. This circuit is very straightforward and simple but is sufficient for the purposes of this work.

Fig. 16(a) shows the drawn layout of the HS test chip with an active area of 0.10 mm^2 . Fig. 16(b) shows the microphotograph of the programmable FC transconductor, with an active area of 0.04 mm^2 including the compensation RC circuit, where the integration capacitance has been implemented with a double-poly capacitor. The area of the FC active element is 0.03 mm^2 and a regular and compact arrangement of transistors can be observed.

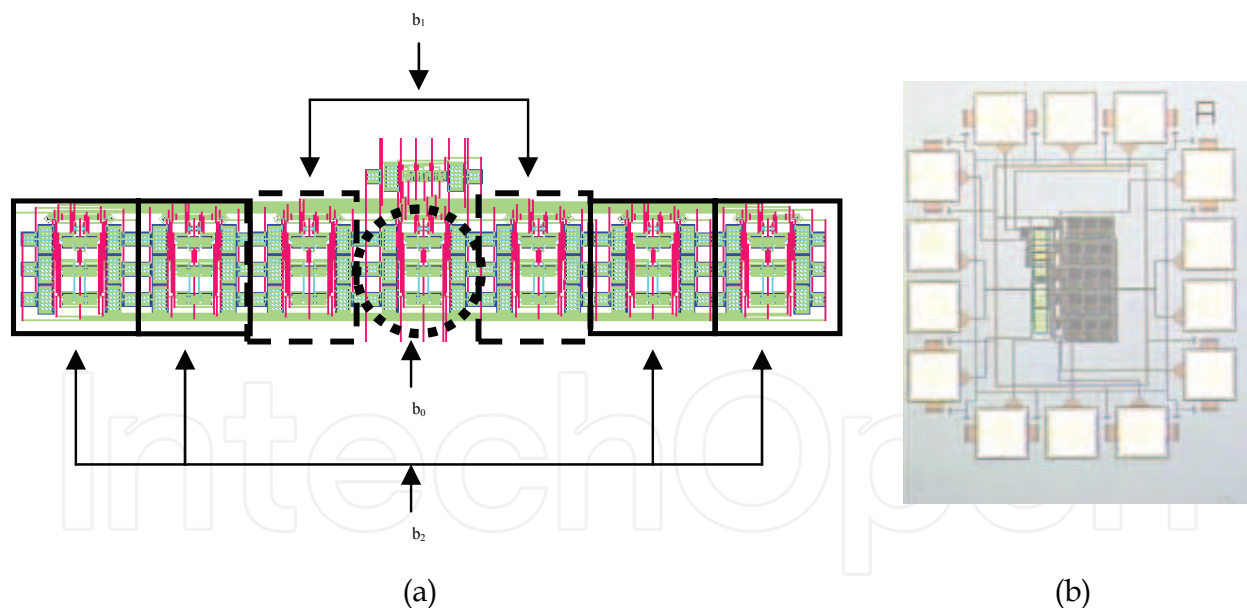


Fig. 16. (a) Layout of the fully-balanced 3-bit programmable HS integrator.
(b) Microphotograph of the FC integrator, by using double-poly capacitors.

8.2 Experimental results

For the HS approach, a unity-gain frequency of 28 MHz was achieved with a power dissipation of 1.62 mW using a 3 V supply. By varying the digital word from 1 to 7, we expected to control the unity-gain frequency from 28 to 185 MHz and the experimental results lead to a variation between 25 and 185 MHz, as shown in Fig. 17(a). Focusing on the

same figure, by varying the bias current source from 45 to 180 μA for a fixed digital word, the transconductance value is modified, providing complementary fine tuning of the frequency. All discrete steps are covered and, in consequence, a frequency span of 25-185 MHz can be provided. The maximum frequency error is obtained at the maximum digital word where a deviation of 6 % is obtained from the 7:1 ratio.

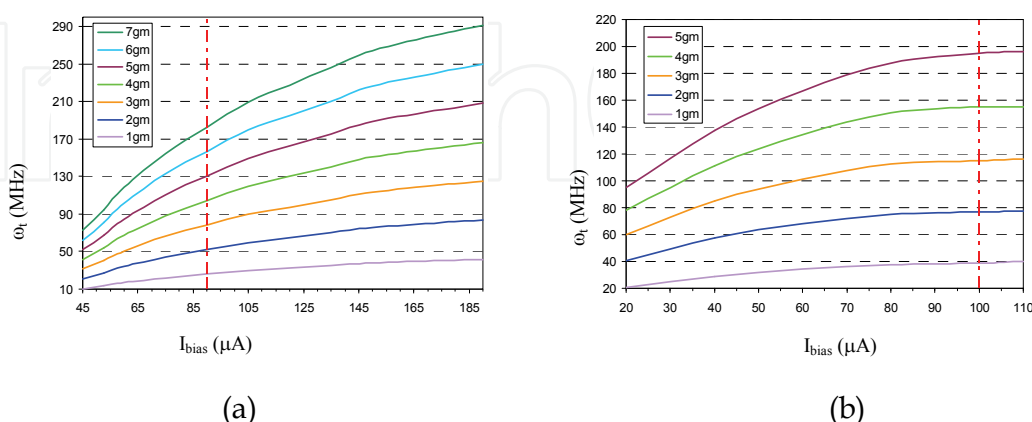


Fig. 17. Experimental results for coarse and fine tuning of the (a) HS and (b) FC topology. Variation of the unity-gain frequency versus bias currents for all the digital words.

For the FC approach, a unity-gain frequency of 40 MHz is achieved with a power dissipation of 2.4 mW using a 2 V supply, as expected from the post-layout simulation results. By varying the digital word from 1 to 5, the unity-gain frequency is controlled from 40 to 190 MHz, as shown in Fig. 17(b). All discrete steps are swept by varying the bias current from 20 to 110 μA . The maximum frequency error is obtained at the maximum digital word where a deviation of 5 % is obtained from the 5:1 ratio.

The next step is to demonstrate constant linearity by means of a constant THD over the entire programming range. Figs. 18 and 19 show the THD variation as a function of the differential output current for all the digital words. THD was measured for a sine input current of 10 MHz (a) and for the unity-gain frequency (b) in both topologies. These figures show the expected THD dependence, studied above in section §6: lower bias currents or higher input signal amplitudes lead to higher THD values. A corner parameter analysis was carried out following the guidelines provided by the design kit manufacturer of the 'AMI Semiconductor C035M Design-Kit' and the worst-case analysis for the HS integrator was obtained. This distortion study gave 1 % of THD for a differential input signal of 56 μA and 10 MHz. Experimental results for the design, shown in Fig. 18, lead to a differential input current of 50 μA in the same situation. For the FC approach, the expected value for 1 % of THD was a differential input signal amplitude of 37 μA and 10 MHz; and the experimental results (Fig. 19), give an amplitude of 35 μA .

The post-layout simulated result for the input-referred noise integrated from 0 to 30 MHz in the HS topology was 11.2 nA_{rms} . Hence, the dynamic range, defined as the input signal amplitude at 1 % THD divided by the total noise level integrated over 30 MHz, is 70 dB. In the FC structure, the input-referred noise integrated from 0 to 40 MHz was 8 nA_{rms} . Hence, the dynamic range, defined as the input signal amplitude at 1 % THD divided by the total noise level integrated over 40 MHz, is also 70 dB.

In summary, frequency is adjusted in a coarse discrete way by connecting identical transconductors in parallel and with fine continuous tuning by varying the biasing current.

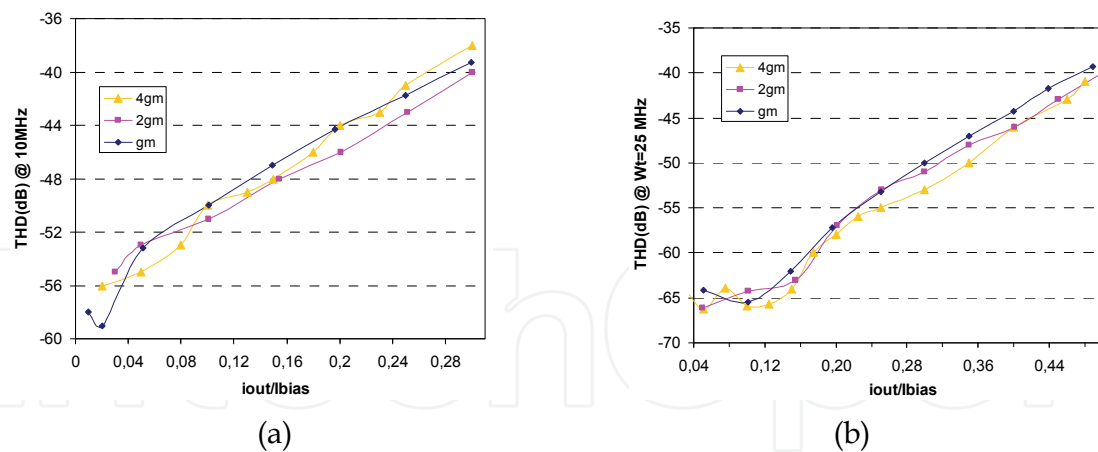


Fig. 18. THD versus differential output current in the HS integrator for three different digital words: (a) $\omega(\text{input})=10$ MHz, (b) $\omega(\text{input})=\omega_t$ (25 MHz for $1g_m$).

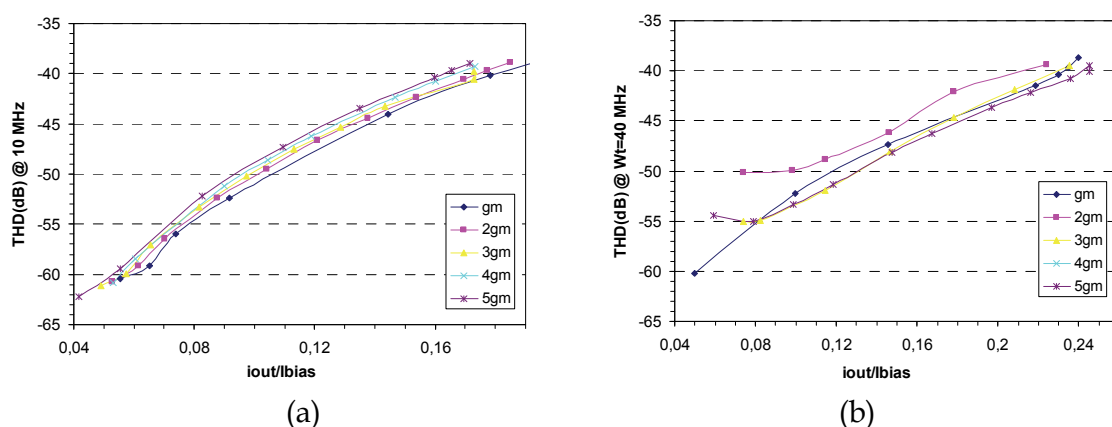


Fig. 19. THD versus differential output current in the FC integrator for all the digital words: (a) $\omega(\text{input})=10$ MHz, (b) $\omega(\text{input})=\omega_t$ (40 MHz for $1g_m$).

The feasibility of the programmable array of transconductors has been proven in a 3-bit programmable integrator obtaining frequency scaling as expected. All the specifications in both transconductor implementations are summarized in table 7. The main advantage of the topology proposed was the inherent enhancement of the dc-gain, provided through the existing positive feedback compensation (negative resistance).

The HS design condition was very difficult to achieve because technological process and temperature variations are expected to be greater than the small changes required in this topology. As expected, by varying the external control for this negative resistance, no change was obtained for the dc-gain. The post-layout simulated dc-gain was a variation of 15 dB between the minimum (40 dB) and the maximum (55 dB), with a maximum CMRR of 60 dB. The experimental results lead to a differential dc-gain of 30 dB with no change with the value of the negative resistance and a CMRR greater than 35 dB over the entire frequency range. Therefore, in this case, there is no control on the dc-gain of the system.

The design condition for the FC topology is less restrictive and two different implementations have been fabricated. The post-layout simulation results in both cases showed a dc-gain control of 15 dB from 30 to 45 dB and a maximum CMRR of 50 dB. The first implementation has been designed with the same dimensions for the M_N transistors

involved in the negative resistance, and similar results are obtained as in the HS topology. There is no external dc-gain control and an experimental value of 26 dB and CMRR of 33 dB are obtained. In the second one, where a pre-designed mismatching is included between M_N transistors involved in the negative resistance, a variation of 12 dB (from 26 to 38 dB) for the dc-gain is obtained by modifying the value of the negative resistance (Fig. 20). The CMRR is greater than 46 dB over the entire frequency range.

	HS topology	FC topology
Power supply voltage	3 V	2 V
Unity-gain frequency	25 MHz	40 MHz
Power dissipation	1.62 mW	2.4 mW
CMRR over the entire pass-band	>35 dB	>46 dB
Active area	0.10 mm ²	0.04 mm ²
Total rms input-referred noise (sim.)	11.2 nA _{rms}	8 nA _{rms}
Maximum differential input signal current at 1 % THD @ 10 MHz	50 μ A (peak)	35 μ A (peak)
Dynamic range	70 dB	70 dB

Table 7. Summary of the experimental results for the integrator (1 LSB).

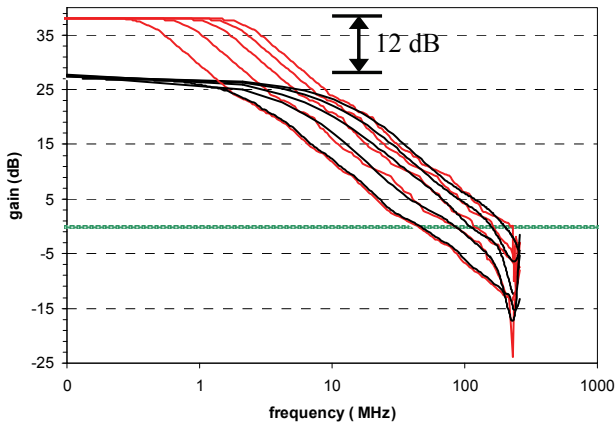


Fig. 20. Experimental dc-gain control for the FC transconductor with a pre-designed mismatching between M_N transistors involved in the negative resistance.

9. Conclusion

This work describes a new approach for implementing digitally programmable and continuously tunable VHF/UHF transconductors compatible with pure digital CMOS technologies and suitable for HDD read channel applications. The cell is suitable for low-voltage operation over an extended frequency range. The programmability exhibited by the transconductor is due to the use of a generic programmable structure that gives a G_m digital control as a parallel connection of unit cells, and the total parasitic capacitances are maintained constant thanks to the specific design of the unit cell: a cascode stage with

dummy elements. This transconductor could be used in any kind of G_m -C filter, thus providing a very wide range of programmable CT filters. The fully-balanced current-mode G_m -C integrator based on this topology exhibits a unity-gain frequency programmability from 25-185 MHz in the HS implementation and 40-200 MHz in the FC approach; with a phase error of less than 4° in both topologies throughout the entire operating frequency range. Total harmonic distortion (THD) of less than 1 % (-40 dB) for a differential input signal of 50 and 35 μ A in the HS and FC topology respectively is obtained. The integrator operates over the programming range with 70 dB of dynamic range for 1 % of THD. The cell has been fabricated in a 0.35 μ m CMOS process.

The experimental results confirm this approach as an excellent choice to achieve filters exhibiting a good trade-off between tuning capability and dynamic range working in the very high frequency range. The proposed technique can be easily adapted to lower power supply voltages by using folded cascode structures and, in addition, better frequency ranges of operation can be achieved considering current CMOS digital technologies.

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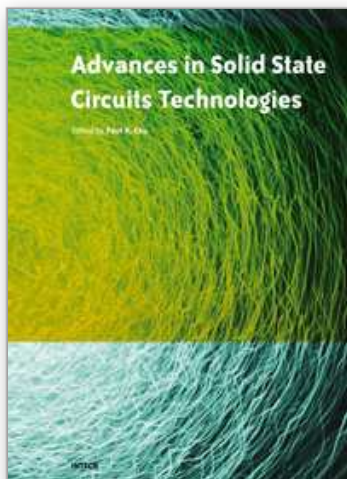
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