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GaN-based metal-oxide-semiconductor devices

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1. Introduction

Si-based semiconductors-related technologies are well developed for their applications in electronic devices and integrated circuits (ICs). However, the properties of Si-based semiconductors are seldom being applied in high-frequency and high-power systems. In comparison, the GaN-based semiconductors have also aroused huge interests in recent years owing to their advantages, such as wide and direct energy bandgap, better thermal and chemical stability, and high-electron drift velocity. Therefore, GaN-based semiconductors are widely utilized in electronic devices, including field-effect transistors (FETs) (Khan et al., 1993; Zolper et al., 1996; Klein et al., 1999; Yoshida & Suzuki, 1999; Johnson et al., 2000; Zhang et al., 2000; Jiménez et al., 2002; Binari et al., 2002; Braga et al., 2004; Wallis et al., 2005; Horio et al., 2005; Hong & Kim, 2006; Saripalli et al., 2007) and high-electron mobility transistors (HEMTs) (Egawa et al., 2000; Karmalkar & Mishra, 2001; Vetury et al., 2001; Islam et al., 2002; Koley et al., 2003; Khan et al., 2003; Mizutani et al., 2003; Lu et al., 2003; Meneghesso et al., 2004; Fareed et al., 2005; Inoue et al., 2005; Seo et al., 2008). Among the devices mentioned above, GaN-based HEMTs possess high electron mobility larger than $1000\text{cm}^2/\text{Vs}$ at room temperature and large operating current due to the formation of two dimensional electron gases (2DEGs). In addition, the GaN-based optoelectronic devices, such as light-emitting diodes (LEDs) (Han et al., 1998; Chang et al., 2004; Fujii et al., 2004; Wierer et al., 2004; Shen et al., 2006; Lee et al., 2006; Chang et al., 2006; Lee et al., 2007; Chen et al., 2007; Chuang et al., 2007), photodetectors (PDs) (Kuksenkov et al., 1998; Walker et al., 1998; Katz et al., 2001; Rumyantsev et al., 2001; Sheu et al., 2002; Seo et al., 2002; Pau et al., 2004; Su et al., 2005; Vardi et al., 2006; Navarro et al., 2009), and laser diodes (LDs) (Nakamura et al., 1996; Nakamura et al., 1996; Saitoh et al., 2003; Suski et al., 2004; Schoedl et al., 2005; Peng et al., 2006; Laino et al., 2007; Braun et al., 2008; Rossetti et al., 2008), have also been investigated and developed extensively for display, lighting, memory system, and communication system in recent years.

It has been reported that utilizing Schottky contact gate could substantially improve the performances of GaN-based metal-semiconductor field-effect transistors (MES-FETs) and metal-semiconductor high-electron mobility transistors (MES-HEMTs) in high-frequency applications (Chumbes et al., 2001; Ohno et al., 2001; Javorka et al., 2002; Okita et al., 2003; Endoh et al., 2004). However, these devices are not suitable for high-power applications because of large gate leakage current, small gate voltage swing (GVS) and small breakdown

voltage. To conquer these aforementioned drawbacks, GaN-based metal-oxide-semiconductor field-effect transistors (MOS-FETs) and metal-oxide-semiconductor high-electron mobility transistors (MOS-HEMTs) are proposed by featuring promising structures and their immense potential in high-power and high-frequency applications (Hu et al., 2001; Kao et al., 2005; Simin et al., 2005; Endoh et al., 2006; Higashiwaki et al., 2006). For MOS devices, the gate insulator plays an important role, since the good quality dielectric layers would yield these devices with outstanding performances. Up to now, several dielectrics, such as SiO_2 , Pr_2O_3 , Si_3N_4 , AlN , Ta_2O_5 , MgO , $\text{Ga}_2\text{O}_3(\text{Gd}_2\text{O}_3)$, Sc_2O_3 , Al_2O_3 , and stack dielectric materials, etc. (Arulkumaran et al., 1998; Ren et al., 1999; Hong et al., 2000; Therrien et al., 2000; Rumyantsev et al., 2000; Gaffey et al., 2001; Chen et al., 2001; Lay et al., 2001; Kim et al., 2001; Cho et al., 2003; Ma et al., 2003; Mehandru et al., 2003; Bas & Lucovsky, 2004; Irokawa et al., 2004; Cico et al., 2007) have been used in GaN-based MOS devices and the corresponding electrical characteristics have also been reported. In this chapter, after presenting a brief introduction of the working principle of MOS devices, various dielectric film deposition methods are summarized with a particular emphasis in the photoelectrochemical (PEC) oxidation method. At the same time, the different performances of GaN-based MOS-HEMTs with different insulators are also compared and discussed.

2. Operation principle of metal-oxide-semiconductor devices

2.1 The metal-oxide-semiconductor (MOS) diodes

The metal-oxide-semiconductor (MOS) diodes are key parts of MOS transistors. Fig. 1 shows the cross-sectional schematic configuration of conventional MOS diodes. An oxide film as the insulator layer was deposited on the surface of a semiconductor and then the gate electrode was deposited thereafter on the surface of the oxide film. An ohmic metal contact was formed at the bottom surface of the semiconductor.

Fig. 1. The cross-sectional schematic configuration of conventional MOS diodes.

Three typical situations are normally occurred at the semiconductor surface, including accumulation, depletion, and inversion, depending on the applied bias between the two electrodes. Fig. 2 shows the energy band diagrams of an ideal MOS diode with n-type semiconductor at different operating conditions (Neaman, 1997). When a positive voltage is applied on the gate electrode of the MOS diode, the free electrons in conduction band of the semiconductor are driven towards the oxide/semiconductor interface, where electrons are accumulated. Accordingly, the energy band at the semiconductor surface is bent downward and

the conduction band edge becomes closer to Fermi level. This is so-called accumulation case, as shown in Fig. 2 (a). When a small negative voltage is applied, the electrons are driven away from the oxide/semiconductor interface by the surface electric field which results in the formation of a depletion region. This case is called depletion case, as shown in Fig. 2 (b). When a larger negative bias is applied, a large number of minority carriers (hole) were induced at oxide/semiconductor interface. Therefore, the energy bands bent upward even more so that the intrinsic level at the surface crosses over the Fermi level. The number of holes (minority carriers) at the semiconductor surface is larger than the number of electron (majority carriers), and in which case it is called inversion and shown in Fig. 2 (c). However, the situation is different for GaN-based MOS diodes, within which the inversion layer is hard to form because the GaN-based material is a wide energy gap semiconductor. The reported results showed that the generation rate of the minority carriers (holes) is extremely low at room temperature (Casey et al., 1996; Hashizume et al., 2000). For an n-type GaN-based material with a carriers concentration of $1.2 \times 10^{17} \text{cm}^{-3}$, the generation time of minority carriers is $t \cong 4.2 \times 10^{18} \text{s}$. However, it is impossible to form an inversion layer with an extremely long generation time. When a negative bias is applied, there are an insufficient number of minority carriers present at the interface and the depletion region extends into GaN to maintain electric neutrality. Consequently, the n-type GaN-based MOS diodes show a deep depletion characteristic at negative bias.

Fig. 2. The energy band diagrams of ideal MOS diode at different operating conditions: (a) accumulation, (b) depletion, and (c) inversion.

2.2 GaN-based metal-oxide-semiconductor field-effect transistors

The GaN-based metal-oxide-semiconductor field-effect transistors (MOS-FETs) is a device which consists of two ohmic electrodes and a MOS diode. Those two ohmic electrodes, located at the two sides of the gate electrode, are connected to GaN-based semiconductor through doped regions. One of the contacts is called the source as it implies that the charge carriers entering the channel originate from this contact, while the other is the drain where the carriers leave the channel. The conductance of the semiconductor near the interface under the gate electrode can be modulated by applying gate bias, as mentioned above for the MOS diode. By applying gate bias, one can modify the effective channel thickness by varying the width of the depletion region, and this in turn varies the output current. If a negative gate voltage is applied on n-channel, the carriers are then depleted from the channel, causing a decrease of the channel conductance; in this case the device behaves as a normally-on (depletion) GaN-based MOS-FETs.

Figure 3 (a) and (b) show the cross-sectional schematic configuration of an n-channel depletion GaN-based MOS-FETs and MES-FETs, respectively. The prior one has better electrical performances due to small gate leakage current, large gate voltage swing and high breakdown field than those of the later one. Fig. 4 shows the depletion layer and the output characteristics of MOS-FETs under various bias conditions (Sze, 2002). As shown in Fig. 4 (a), when gate voltage is zero and drain voltage is small, a small drain current flows from drain to source in the channel and varies linearly with the drain voltage. When the drain voltage increases, the width of depletion layer extends while the cross-sectional area of channel reduces. If the drain voltage is further increased, the depletion layer touches the semi-insulating substrate and the channel became pinch-off, as shown in Fig. 4 (b). The corresponding value of the drain voltage and drain current are called saturation voltage and saturation current, respectively. In Fig. 4 (b), the location P is called the pinch-off point. If the drain voltage increases further, the depletion region widens and pinch-off point then shifts toward the source, as shown in Fig. 4 (c). As the voltage at point P equals to saturation voltage, the current flow in the channel remains fixed. When the drain voltage is larger than the saturation voltage, the drain current becomes independent of the drain voltage. In addition, when a negative voltage is applied to the gate electrode, the electrons are driven away from semiconductor surface, which reduces the electron concentration and forms the depletion layer. Consequently, as the effective channel thickness decreases, and the drain current becomes lower. When the negative gate voltage increases over a certain value, the depletion layer touches the semi-insulating substrate and the channel then operates in a cut-off mode, as shown in Fig. 4 (d). Consequently, the depletion of n-channel depletion-mode MOS-FETs at semiconductor surface can be achieved by applying a sufficient gate bias to inhibit the device current. The GaN-based MES-FETs have similar behaviors. When Schottky gate metal contacts to semiconductors as shown in Fig. 3 (b), the depletion region forms at the metal/semiconductor interface and its width can be controlled by gate bias as mentioned above.

Fig. 3. The cross-sectional schematic of an n-channel depletion (a) MOS-FETs and (b) MES-FETs.

Fig. 4. The depletion layer width and output characteristic of MOS-FETs at various bias conditions. (a) $V_G=0$ and a small V_D voltage (b) $V_G=0$ and at pinch-off (c) $V_G=0$ and at post pinch-off ($V_D>V_{Dsat}$) (d) a negative V_G voltage and at cut-off case.

2.3 GaN-based metal-oxide-semiconductor high-electron mobility transistors

Metal-oxide-semiconductor high-electron mobility transistors (MOS-HEMTs), namely metal-oxide-semiconductor heterojunction field-effect transistors (MOS-HFETs) (Sze, 2002), are another kind of field effect transistor, which is similar to the MOS-FETs but with its semiconductor layer replaced by a semiconductor heterostructure. Figure 5 shows the energy band diagram of the AlGaN/GaN heterostructure. The band gap of AlGaN (low electron affinity) is wider than the bandgap of GaN (high electron affinity). When they form junctions, both the conduction band and valence band at the AlGaN/GaN interface bend and the conduction band of GaN drops below the Fermi level. Consequently, a triangular potential well is formed at the GaN side of the interface, owing to the conduction band discontinuity. The electrons are confined in this well, and forming a two dimensional electron gas (2DEG). In addition, the spontaneous polarization (Ambacher et al., 1999; Ambacher et al., 2000) and piezoelectric polarization (Smorchkova et al., 1999; Sacconi et al., 2001) effects, which are large in the wurtzite GaN-based semiconductor materials (Johnson et al., 2001; Lu et al., 2001), provide a further improvement in the sheet carrier concentration of the 2DEG, which is typically up to 10^{13}cm^{-2} . Furthermore, the 2DEG are located in the region of the undoped GaN, where the carrier mobility is high as the scattering effect is reduced.

Fig. 5. The energy bandgap diagram of AlGaN/GaN heterostructure.

Figure 6 (a) and (b) shows the schematic configuration of AlGaN/GaN MOS-HEMTs and MES-HEMTs grown on sapphire substrates (Al_2O_3) using metalorganic chemical vapor deposition (MOCVD) system or molecular-beam epitaxy (MBE) system. The carbon-doped GaN layer has high resistance and can confine the carriers transport in the AlGaN/GaN channel (Webb et al., 2001). The electrons transport occurs in the 2DEG channel between two ohmic contacts of source and drain electrode. The insulators are deposited in the drain-source region for surface passivation and gate insulation. The source is usually grounded and the voltage applied between the drain and source is called V_{DS} , while the gate-source voltage is called V_{GS} . The current flowing from source to drain is called I_{DS} and I_{GS} is the current entering the gate through the oxide film. This is the reason why the MOS-HEMTs have small gate leakage current and large breakdown voltage compared to those of MES-HEMTs. The ability of the gate electrode to modulate the source-drain current is expressed as the extrinsic transconductance $g_m = \partial I_{\text{DS}} / \partial V_{\text{GS}}$. The conductance of the channel varies with the sheet carrier concentration, which is modulated by the gate bias. When the gate bias is positive, more electrons accumulate in the 2DEG channel and the operation current of

AlGaN/GaN MES-HEMTs will be larger. The current decreases with the decrease of the gate bias. The 2DEG channel will be fully depleted and the drain-source current will drop to zero when the gate bias reaches a negative threshold value, which is called cut-off voltage or threshold voltage. This corresponds to the case of which the MOS-HEMTs operating in the depletion mode.

Fig. 6. The schematic configuration of AlGaN/GaN (a) MOS-HEMTs and (b) MES-HEMTs.

3. Obstacle to further improving transistor performances

For GaN-based MES-HEMTs and MOS-HEMTs, there are still some problems to be solved, which limit their performances ultimately. Among them, the self-heating (Gaska et al., 1997; Gaska et al., 1998; Ahmad et al., 2006) and current collapse (Klein et al., 2001; Mittereder et al., 2003; Kuzmik et al., 2004; Zheng et al., 2008) are the most serious effects that degrade the high-frequency and high-power performances of the transistors.

The self-heating effect occurs usually when the transistor operates at high drain-source voltage. Fig. 7 gives a typical example where the drain current decreases at high DC drain-source voltage (Fan et al., 2004). This is related to the fact that the electrons flowing in the device transfer part of their energy to the lattice via trap-related scattering and electron-phonon interaction (Bhaskar et al., 1997), which raises the channel temperature of the devices. This effect is induced by the poor thermal conductivity of the sapphire substrates which are commonly used for fabricating GaN-based transistors. The self-heating effect can be suppressed by using highly thermal conductive SiC substrates in stead of sapphire substrates (Morkoc et al., 1994).

During epitaxial processes, traps exist in GaN buffer layer, AlGaN layer and AlGaN surface. Traps on the semiconductor surface capture electrons and form lots of virtual gates. Those virtual gates deplete the channel and make the drain-source current is smaller than ideal value. In addition, when high drain-source electrical field is applied, some hot electrons transfer from 2DEG channel to adjacent layer with high concentration of traps. Those factors cause the drain-source current decrease and this phenomenon is called the current collapse. The simple schematic configuration of current collapse of transistors is shown in Fig. 8 (Zheng et al., 2008). It can be suppressed by surface passivation and gate insulation by depositing dielectrics on AlGaN surface (Tan et al., 2002; Arulkumaran et al., 2004) or using

confinement layer underlying 2DEG channel (Palacios et al., 2006). For obtaining better radio-frequency (rf) performances and power performances, suppressing those two unideal effects is urgent.

Fig. 7. Self-heating in an AlGaIn/GaN MOS-HEMT.

Fig. 8. Current collapse in an Al₂O₃/AlGaIn/GaN MOS-HEMT (dashed lines: Before stress; solid lines: After stress).

In addition, the low frequency noises, such as flicker noise, and generation-recombination noise, mean the inevitable disturbances of output signals when devices operated at a low frequency. Fig. 9 shows the spectra of flicker noise and generation-recombination noise. The prior one is proportional to inverse frequency but the later one has Lorentzian distribution. Flicker noise is an important indicator for judging the transistors whether they are suitable for communicating applications or not, because a large level of flicker noise limits the phase noise characteristics and causes the performance degradation of the electronic systems (Balandin et al., 1999). The interface-state densities, defects, and phonons are possible sources of flicker noise. Furthermore, it is a useful tool for confirming crystal quality, and manufacture techniques (Balandin et al., 1999; Balandin et al., 2000). In general, MOS-HEMTs have better behavior in flicker noise than MES-

HEMTs, because the interface-state densities in MOS-HEMTs are well passivated (Vertiatchikh & Eastman, 2003; Chiu et al., 2008). Fabricating transistors with low flicker noise is a vital issue for developing high performance electronic devices and systems.

Fig. 9. Low temperature noise characteristics of the GaN MES-HEMTs in the subsaturation regime. Generation-recombination (g-r) bulges are clearly seen in spectra of the doped channel device (P1) at frequency $f \approx 3\text{--}4$ kHz.

4. Method of growing gate insulators of GaN-based MOS devices

For fabricating GaN-based MOS devices with excellent performances, an important task is, as with the other MOS devices, to find suitable right methods to form a proper insulator layer on the semiconductor. Many efforts have been focused on the exploration of insulator materials and deposition methods. In most of cases reported in the literature, the insulator layers of the GaN-based MOS devices were deposited externally onto the semiconductor surface by physical vapor deposition (PVD) and chemical vapor deposition (CVD) methods. The main results reported in the literatures will be reviewed first. Then, we will give a more detailed discussion on photoelectrochemical (PEC) oxidation method, with which the oxide layer is formed via a chemical reaction with the semiconductors, instead of relying on an external deposition.

4.1 Electron-beam deposition method

The electron beam evaporation employs an electron-beam emitted by a filament of the electron gun to bombard the target in a high vacuum chamber. The kinetic energy of the electron-beam transforms into the thermal energy upon contact of the target, which in turn melts the target. The e-beam evaporation has good thermal translation efficiency and high evaporation rate. In addition, the current can be controlled, so as to judiciously control the evaporation rate. There are basically no limits to which the materials can be evaporated with the electron-beam evaporation method. The materials can easily be evaporated irrespective of their purity and chemical compounds. The target is placed into a crucible with an adequate cooling through proper arrangement. High thermal melt zone is localized around a position of the target which is bombarded directly by an electron-beam.

Several conventional gate oxides such as $\text{Ga}_2\text{O}_3(\text{Gd}_2\text{O}_3)$, SiO_2 , TiO_2 , AlN , MgO , Ta_2O_5 , Pr_2O_3 and stack dielectrics have been deposited using e-beam deposition system for gate insulators of GaN-based MOS devices (Hong et al., 2000; Arulkumaran et al., 2005; Kikuta et al., 2006; Yagi et al., 2006; Chiu et al., 2008). Figure 10 shows the typical capacitance-voltage characteristics of GaN MOS diode with $\text{Ga}_2\text{O}_3(\text{Gd}_2\text{O}_3)$ as the gate insulator, measured at various frequencies. The capacitance measured at forward bias is originated by capacitance of oxide films. The smaller capacitance at reverse bias is due to the capacitances in series originated from the oxide layer and the depletion region. The frequency dispersion observed in accumulation mode is attributed to the traps existed in the inner oxide layer. This phenomenon is induced from the Maxwell-Wranger effect (Hippel, 1954). The obtained density state (D_{it}) is less than $10^{11}\text{cm}^{-2}\text{eV}^{-1}$. The $\ln(J)$ v.s. V characteristics of the GaN MOS diodes are shown in Fig. 11. It can be seen that the $\text{Ga}_2\text{O}_3(\text{Gd}_2\text{O}_3)$ insulator grown using the electron-beam deposition method exhibits good insulation properties.

Fig. 10. The capacitance-voltage characteristics of $\text{Ga}_2\text{O}_3(\text{Gd}_2\text{O}_3)/\text{GaN}$ MOS diodes.

Fig. 11. The current-voltage characteristics of $\text{Ga}_2\text{O}_3(\text{Gd}_2\text{O}_3)/\text{GaN}$ MOS diodes.

The drain-source current-drain-source voltage ($I_{DS}-V_{DS}$) characteristics of $\text{SiO}_2/\text{AlGaIn}/\text{GaN}$ MOS-HEMTs and AlGaIn/GaN MES-HEMTs are reported by Arulkumaran and Egawa, et al., and shown in Fig. 12 (a) and (b), respectively (Arulkumaran et al., 2005). It can be seen

that the $I_{DS(max)}$ of MOS-HEMTs is about 856mA/mm which is larger than that of MES-HEMTs. Fig. 13 (a) and (b) show the gate leakage current (I_g) as a function of gate-source voltage and the transfer characteristics of MOS-HEMTs and MES-HEMTs, respectively. At reverse voltage of 40V, the I_g of MOS-HEMTs is about three orders smaller than that of MES-HEMTs The $g_{m(max)}$ of MOS-HEMTs and MES-HEMTs are 160mS/mm and 145mS/mm, respectively. Better direct-current (dc) performance can be obtained with the improvement of the extrinsic transconductance of transistors. These results show that the electrical performance can be enhanced through the surface passivation and gate insulation. The similar behaviors of AlGaIn/GaN MOS-HEMTs with different gate insulators can be observed in other reports (Kikuta et al., 2006; Yagi et al., 2006).

Fig. 12. The I_{DS} - V_{DS} characteristics of (a) $SiO_2/AlGaIn/GaN$ MOS-HEMTs and (b) $AlGaIn/GaN$ MES-HEMTs.

Fig. 13. The dc electric performance of MOS-HEMTs and MES-HEMTs (a) the gate leakage current as a function of gate-source voltage and (b) the transfer characteristics.

Investigating dielectrics with high permittivity is an interesting issue for better high-frequency and high-performances due to the suppression of gate leakage current and

current collapse by applying gate dielectrics in AlGaIn/GaN MOS-HEMTs. However, the decrease of the transconductance (Ye et al., 2005) and the large shift of the threshold voltage are obvious expenses. Using dielectrics with high permittivity (high-k) is helpful to solve these problems. A larger dielectric constant could translate to an efficient gate modulation (Liu et al., 2006); thus, a smaller decrease in transconductance and a moderate increase in the threshold voltage could be expected in MOS-HEMTs with high-k gate insulators. The Pr₂O₃ high-k dielectrics (k=30) have also been deposited using an electron-beam evaporator for gate insulation and surface passivation of AlGaIn/GaN MOS-HEMTs (Chiu et al., 2008). Fig. 14 shows the flicker noise spectra of MES-HEMTs and MOS-HEMTs, respectively. It can be seen that the level of flicker noise of the MOS-HEMTs is smaller than that of the MES-HEMTs. It means that the lower surface states and gate leakage current is achievable with high-k Pr₂O₃ films grown using an electron-beam evaporator. The microwave-power characteristics of both devices are shown in Fig. 15. The maximum output-power density and PAE are 753mW/mm and 36.8% for MOS-HEMTs at an input power of 15dBm, which are better than those of the MES-HEMTs with corresponding values of 698mW/mm and 32.1%, respectively.

Fig. 14. Flicker noise spectra of MES-HEMTs and MOS-HEMTs, respectively.

Fig. 15. The microwave-power characteristics of MES-HEMTs and MOS-HEMTs.

4.2 Atomic layer deposition (ALD) deposition method

The atomic layer deposition (ALD) deposition is a technique for growing thin films on various substrates with atomic scale precision based on alternate saturated surface reaction in each cycle of deposition. ALD is a chemical gas phase deposition process. The growth of thin film is self-limited and based on surface reaction. The deposition of conformal thin-films onto substrates of varying compositions via sequential surface chemistry enables controllable atomic scale deposition. ALD reaction divides the CVD reaction into two half-reactions. The ALD deposition has several advantages over other techniques, including high quality deposited films, excellent conformity and reproducibility. A variety of thin films can be deposited utilizing ALD deposition with high density and low impurity at a low deposition temperature.

The Al₂O₃ and HfO₂ dielectrics are common insulators grown using ALD system and have been applied in AlGaIn/GaN MOS-HEMTs (Park et al., 2004; Ye et al., 2005; Wu et al., 2006; Kim et al., 2007; Medjdoub et al., 2007; Yue et al., 2008; Feng et al., 2009; Chang et al., 2009). The qualities of Al₂O₃ films gauged by several important figures of merit including uniformity, defect density and stoichiometric ratio of the deposited films, are comparably better, when ALD is chosen over the other deposition methods such as sputtering and electron-beam deposition methods. The I_{DS}-V_{DS} and effective electron mobility characteristics of GaN MOS-HEMTs are shown in Fig. 16 (a) and (b), respectively. The I_{DS(max)} of MOS-HEMTs at V_{GS}=6V is 375mA/mm and the off-state breakdown voltage is 145V. In addition, the negative output conductance under high drain bias is due to self-heating effect. The effective carrier mobility (μ_{eff}) of insulator/AlGaIn/GaN structure as a function of effective electric field (E_{eff}) is larger compared to the other semiconductors, which implies devices sharing this kind of structure do possess excellent high-frequency and high-power performances.

Fig. 16. The measured (a) I_{DS}-V_{DS} and (b) effective electron mobility of AlGaIn/GaN MOS-HEMTs.

The HfO₂ insulator is a promising candidate because of its high dielectric constant (20~25) and large bandgap (5.6~5.8eV). Al₂O₃ is also a potential candidate for the above application, which has a good passivation effect and low interface state density. The Al₂O₃ is a better insulator for interfacial passivation layer (IPL) application in high-k gate process of

AlGaIn/GaN MOS-HEMTs because it has better chemical and thermal stabilities against AlGaIn compared to HfO_2 films (Gusev et al., 2006). The $\text{HfO}_2/\text{Al}_2\text{O}_3$ stack gate dielectrics deposited using ALD system utilized in AlGaIn/GaN MOS-HEMTs are reported by Yue and Hao, et al. (Yue et al., 2008). The $g_{m(\max)}$ of MES-HEMTs and MOS-HEMTs are 165mS/mm and 150mS/mm, respectively. The decay of the transconductance is due to the increase of the distance between the channel and Schottky gate of the MOS-HEMT structure. Furthermore, the negative shift in threshold voltage from -4V of MES-HEMTs to -5V of MOS-HEMTs is caused by the same reason. The decrease of $g_{m(\max)}$ is only 9% and therefore is better compared with the deterioration degree of transconductance in MOS-HEMTs with low-k gate insulators (Kordos et al., 2005). The gate voltage swing (GVS) of MES-HEMTs and MOS-HEMTs are 2.4V and 1.8V, respectively. MOS-HEMTs not only have better linear operation because of large GVS compared to HEMTs, but also have a smaller intermodulation distortion, a smaller phase noise, and a larger dynamic range. These advantages ultimately render them suitable for practical amplifier applications (Khan et al., 2006). The pulse current-voltage performances of Al_2O_3 passivated MES-HEMTs and stack gate MOS-HEMTs are shown in Fig. 17. The current collapse phenomenon ascribed to the interface state density can not be observed in both devices and therefore it is reasonable to assume the surface states are well passivated in both transistors. Moreover, the unity current gain cut-off frequency and the maximum frequency of oscillation are 12GHz and 34GHz, respectively, as depicted in Fig. 18. According to the results mentioned above, the MOS-HEMTs not only have excellent dc and pulse mode electrical performances than those of passivated MES-HEMTs, but also exhibit outstanding high-frequency properties.

Fig. 17. The pulse current-voltage characteristics of Al_2O_3 passivated MES-HEMTs and stack gate MOS-HEMTs.

Fig. 18. The short-circuit current gain (H_{21}) and unilateral power gain (U) versus frequency of MOS-HEMTs operated at $V_{DS}=10V$ and $V_{GS}=-3V$.

4.3 Sputter deposition method

Usually, a sputtering deposition involves two electrical plates in the vacuum chamber and one of them is used to accommodate a target material. When a negative voltage is applied to the target (i.e. cathode) by an external power supply, a number of free electrons are accelerated toward the anode. While on their way to anode these free electrons would expect to hit other gas molecules and then ionize them in the chamber, if the energy of the accelerated electrons is sufficiently high enough. Due to the negative voltage applied on target, the energy of these positive ions attracted toward the target surface depend on the applied voltage. When accelerated positive ions collide with the surface atoms of the target material, their energy are imparted to the target molecules, so that they can be ejected or sputtered out from the surface of the target material. Sputtering of target material is a possible outcome only, when the bombarding ion energy is large enough to disrupt the target molecules. Sometimes the ions bombarding the cathode may knock the electrons out from it, causing them to accelerate under the influence of applied field to enhance a chain of reactions involving the necessary ionization of molecules and the sputtering process. Magnetron sputtering is a powerful and flexible technique and the sputtering process almost places no restriction in the choice of the target materials; these include using a dc power to sputter pure metals and a rf power or pulsed dc power source to sputter semiconductors and isolators.

The performances of GaN-based MOS devices with insulators grown by sputtering technology are demonstrated (Nakano & Kachi, 2003; Liu et al., 2007; Jhin et al., 2008; Shih et al., 2009). Liu and Chor, et al. have reported the performances of AlGaIn/GaN MOS-HEMTs with HfO_2 high-k dielectrics deposited using sputtering system (Liu et al., 2006). The $I_{DS}-V_{DS}$ and transfer characteristics are shown in Fig. 19 (a) and (b), respectively. The $I_{DS(max)}$ of 830mA/mm is obtained at $V_{DS}=6V$. In addition, the self-heating effect does not be found under the high drain-source current operation, because the Si substrate has better thermal conductivity. The G_{VS} and $g_{m(max)}$ of MOS-HEMTs are 2.91V and 115mS/mm, respectively. The negative shift in threshold voltage from -4V of MES-HEMTs to -6V of MOS-HEMTs is

caused by the increase in distance between gate and channel. Figure 20 shows the dc and pulse mode measurement of MES-HEMT and MOS-HEMT respectively. The V_{DS} bias is held at 8V and the frequency of pulsed V_{GS} is 100kHz. There is 60% drain current discrepancy between the dc and pulsed modes associated with MES-HEMTs. However, a significant drain current recovery is observed in MOS-HEMTs. This phenomenon clearly indicates that the HfO_2 layer can passivate the traps on AlGaN surface that otherwise would create a depletion region and suppress the current collapse.

Fig. 19. The (a) I_{DS} - V_{DS} of MOS-HEMTs and (b) transfer characteristics of MES-HEMTs and MOS-HEMTs.

Fig. 20. The dc and pulse mode measurement of AlGaN/GaN (a) MES-HEMTs and (b) MOS-HEMTs.

The relationship between gate insulation and high-frequency performances are also investigated (Liu et al., 2007). The high-frequency performances of AlGaN/GaN HEMTs with and without HfO_2 gate insulator are shown in Fig. 21 (a) and (b), respectively. The improvement of f_T and f_{max} is attributed to the increase of transconductance.

Fig. 21. The S-parameter measurement of AlGaIn/GaN (a) MES-HEMTs and (b) MOS-HEMTs.

4.4 Jet vapor deposition (JVD) method

The jet vapor deposition (JVD) is a novel process for synthesizing wide variety of thin films of metals, semiconductors, and insulators (Ma, 1998). It relies on supersonic jets of a light carrier gas such as helium to transport depositing vapor from the source to the substrate. Because of the separation of the constituent depositing species, and their short transit times, there is very little chance for gas-phase nucleation. In contrast to the conventional CVD silicon nitride, the high-field I-V characteristics of the JVD silicon nitride fit the Fowler-Nordheim (F-N) tunneling theory over 4-5 orders of magnitude in current, but do not fit at all with the Frenkel-Poole (F-P) transport theory. This is consistent with a much lower concentration of electronic traps in the JVD silicon nitride.

The JVD is a novel and interesting technology. The SiO₂/Si₃N₄/SiO₂ stack gate insulators of GaN MOS devices grown using JVD system were reported (Gaffey et al., 2001; Ma et al., 2003). Figure 22 (a) shows the measured and theoretical capacitance-voltage characteristics performed at a room temperature and a frequency of 10kHz. The open circle and solid line indicate the measured data and theoretic value of capacitance-voltage (C-V) characteristics, respectively. It can be seen that the measured data are fitted well to theoretic data with out any translation along the voltage axis. This phenomenon indicates that the net density of fixed charges within the insulator is very low. Fig. 22 (b) shows the C-V performances at different frequency at 450°C. The near ideal curve means that the devices work well up to 450°C. The interface-state density (D_{it}) of devices should be low because of weak frequency dependence. The inset shows a magnified view of this C-V curve with respect to a particular voltage region and note that the small frequency dependence is observed.

Fig. 22. (a) The measured and theoretic C-V characteristics of GaN MOS devices at room temperature. (b) The C-V characteristics of GaN MOS devices at varied testing frequency and 450°C.

The extracted D_{it} values using conductance method (Schroder, 1998) as a function of energy separation from conduction band edge are shown in Fig. 23 (a). Those values are on the order of mid-to-high $10^{11}\text{cm}^{-2}\text{eV}^{-1}$, which are deemed reasonable. The relationships between gate leakage current (J) and oxide electrical field (E) are measured at 27°C, 150°C, 250°C, 350°C, and 450°C and shown in Fig. 23 (b), respectively. The electrical field is defined as V_g/t_{ox} , where V_g is the gate voltage and t_{ox} is the equivalent oxide thickness. It can be seen that the leakage currents are very low and with weak temperature dependence. In addition, an acute breakdown is observed when electrical field is larger than 12MV/cm over the entire range of temperatures. The observed phenomena demonstrate the realization of the high quality stack gate insulators.

Fig. 23. (a) The estimated D_{it} values as a function of energy separation from conduction band edge at 450°C. (b) The gate leakage current density as a function of oxide electrical field of GaN MOS devices measured at various temperatures.

The MOS-FETs using $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ stack as gate insulators demonstrate reliable performance up to the working temperature as high as 450°C (Ma, 2003). Fig. 24 (a) and (b) shows the I-V characteristics of a typical GaN MOS-FET on 6H-SiC substrate before and after accelerated lifetime test stress. In this experiment, a device was declared “dead” when its gate oxide leakage current exceeded $0.25\text{mA}/\text{cm}^2$, as measured from an otherwise well-functioned device shown in Fig. 24 (b). The inversion layer electron mobility obtained from this device is around $40\text{cm}^2/\text{Vs}$ both before and after the accelerated lifetime test. In this case, the effective channel mobility is reduced by the high source and drain contact resistances.

Fig. 24. I-V characteristics of a typical GaN MOS-FETs on 6H-SiC substrate (a) before and (b) after accelerated lifetime test stress.

4.5 Chemical vapor deposition (CVD) method

Traditional CVD deposition systems include atmospheric pressure CVD (APCVD), low-pressure CVD (LPCVD), and plasma-enhanced CVD (PECVD). Among the three systems, PECVD appears more advantages due its comparatively low deposition temperature and a good step surface coverage. The power source of a CVD system is usually a radio-frequency (RF) power with frequency of 13.56MHz applied to the vacuum deposition chamber. It induces the gas molecules situated between the parallel electrodes to collide with electrons, and thereby to trigger the dissociation of molecules. Several free radicals, gas ions, electrons, and nuclear gas molecules, called cold plasma, are thus generated due to the increase of internal energy which enhances to induce excitation, ionization, relaxation, and recombination reactions to take place. The undisturbed RF power provides energy to the gas plasma and the collisions among gas species lead to the chemical reactions. Since the dissociation of the gas plasma provides the energy needed for the chemical vapor deposition directly, the process could therefore take place under a low temperature. It is the most frequently used technique for low temperature deposition.

There are reports about the electrical performances of AlGaN/GaN MOS-HEMTs with gate oxide layers grown using PECVD system (Casey et al., 1996; Arulkumaran et al., 1998; Khan et al., 2000; Simin et al., 2002; Marso et al., 2002; Misstele et al., 2003; Onojima et al., 2007; Higashiwaki et al., 2009). As shown in Fig. 25 (a), the $g_{m(\text{max})}$ of passivated MES-HEMTs is improved compared to the traditional MES-HEMTs (Marso et al., 2002). The threshold voltage of passivated MES-HEMTs is not affected by SiO_2 layer, because the metalized gate makes direct contact with the

semiconductor surface of the unpassivated MES-HEMTs as well as that of the passivated MES-HEMTs. The SiO_2 passivation layer of the passivated MES-HEMTs cannot influence the channel in the active region under the gate contact, however, it can reduce the resistance of the source and the drain, thereby improving the dc performances (Higashiwaki et al., 2005). For MOS-HEMTs, the large negative shift of the threshold voltage is observed and it is mainly caused by an increase in gate-to-channel separation due to the presence of the dielectric layer. Besides, in the Fig. 25 (b), the cutoff frequency (f_T) of unpassivated MES-HEMTs, passivated MES-HEMTs and MOS-HEMTs are 16.5GHz, 18.2GHz, and 24.0GHz, respectively.

Fig. 25. The (a) transfer characteristics and (b) small-signal performances of traditional MES-HEMTs, passivated MES-HEMTs and MOS-HEMTs.

The power performance of $\text{SiO}_2/\text{AlGaIn}/\text{InGaIn}/\text{GaIn}$ MOS-HEMTs are investigated (Simin et al., 2002). Figure 26 shows the power performance and the stability of power performance of MOS-HEMTs. A maximum power of 6.1W/mm in CW mode and 7.5W/mm of in pulse mode can be obtained, when the MOS-HEMTs are operated at $V_{DS}=30V$ and 2GHz. It is worth noting that the power degrades at about 0.5~0.6W/mm in the first 2~3 hours and this stabilization is irreversible.

Fig. 26. The (a) power performances and (b) CW mode power performances of MOS-HEMTs.

In general, the PECVD system is not perfect and there is a concern on the degree of plasma damage or charge-induced damage which would affect the devices during fabrication process. In some cases, such as the passivation of compound semiconductor devices, the plasma damage is serious that it would even affect the throughput of device production. The catalytic chemical vapor deposition (Cat-CVD) method was developed to overcome these problems encountered during the deposition process of PECVD. It is expected that vary low-damage process using the Cat-CVD system can be realized (Wiesmann et al., 1979; Matsumura et al., 1986), which is a low-temperature method being developed without using the plasma. The Cat-CVD method, also known as the hot-wire CVD (HWCVD) method, the deposition gases are decomposed by catalytic cracking reaction with a heated catalyzer placed near the substrate, so that the films are deposited at a low substrate temperatures around 300°C without any plasma. The Cat-CVD apparatus consists mainly of three parts: a gas inlet which feed gas into the low-pressure deposition chamber, an arrangement for gas decomposition via catalytic cracking reaction at the surface of a heated catalyzer, and the substrate for film deposition where decomposed species are transported from the catalyzer. In most cases, a tungsten (W) wire or a W ribbon is used as the catalyzer, because the melting point of W is as high as 3382°C, and also can sustain the temperature as high as 2165°C (Poate et al., 1978) even when the surface of W is converted to silicide by the reaction with SiH_4 gas.

The performances of AlGaIn/GaN MOS-HEMTs with SiN_x films for gate insulation and surface passivation grown using Cat-CVD system are demonstrated by Higashiwaki and Mimura, et al. (Endoh et al., 2006; Higashiwaki et al., 2006; Yamashita et al., 2006). The output and transfer characteristics are shown in Fig. 27 (a) and (b), respectively. The $I_{DS(\max)}$ and $g_{m(\max)}$ are 1.49A/mm at $V_{GS}=1\text{V}$ and 402mS/mm at $V_{DS}=2\text{V}$, respectively. A large reduction of the transconductance occurs as the V_{DS} is increased from 2 to 6V, mainly due to the self-heating effect. The off-state gate-drain breakdown voltage is about -18V at a gate leakage current density of 1mA/mm.

The maximum f_T and $f_{\max}$ are obtained at different bias voltages, as shown in Fig. 28 (a) and (b). The maximum f_T is 181GHz. The maximum $f_{\max}$ is also a very high value, 186GHz or 183GHz obtained from the maximum stable gain (MSG) or unilateral gain (U_g) extrapolation.

Fig. 27. The dc performances of MOS-HEMTs (a) output characteristics (b) transfer characteristics.

Fig. 28. The small-signal RF characteristics of MOS-HEMTs with $L_G=30\text{ nm}$ at $V_{GS}=-4.2\text{ V}$, (a) $V_{DS}=4.0\text{ V}$ and (b) $V_{DS}=6.0\text{ V}$.

In recent years, the photochemical vapor deposition (photo-CVD) method has been developed to grow high-quality SiO_2 layers on various MOS devices (Chiou et al., 2003). In this method, a deuterium (D_2) lamp is used as the excitation source. The D_2 lamp emits strong ultraviolet and vacuum ultraviolet radiation, which can effectively decompose SiH_4 and O_2 . The O_2 can absorb photons in the wavelength region from 133 nm to 175 nm and SiH_4 can absorb photons below 147 nm (Chang et al., 2003). Therefore, the energy can be directly transferred from the D_2 lamp to the excited Si and O atoms. It has been reported that the quality of oxide layers grown by photo-CVD system is close to that of grown by thermal oxidation. Consequently, the better electrical properties of MOS devices with oxide films

grown using photo-CVD system can be obtained (Wang et al., 2003; Chiou et al., 2003; Chiou et al., 2004; Wang et al., 2005; Liu et al., 2007).

The current-voltage characteristics and transfer performances of MOS-HEMTs, in which the SiO₂ film is grown using photo-CVD method, operated at room temperature and 300°C are shown in Fig. 29 (a) and (b), respectively. It can be found that the values of I_{DS} decrease as the transistors are operated at high temperature. The I_{DS(max)} values of MOS-HEMTs operated at room temperature and 300°C are about 755mA/mm and 323mA/mm, respectively. The g_{m(max)} and GVS of transistors biased at V_{DS}=10V and V_{GS}=-5V at room temperature are 95mS/mm and 8V, respectively. The electrical performance of transistors at 300°C is poor compared to those operated at room temperature due to the decrease of the electron mobility in the 2DEG channel.

Fig. 29. The (a) output characteristics and (b) transfer performances of fabricated SiO₂/AlGaIn/GaN MOS-HEMTs.

The flicker noise of transistors is an important indicator when they are applied as mixers and oscillators in communication systems. The flicker noise performance of AlGaIn/GaN MOS-HEMTs with SiO₂ grown by photo-CVD is investigated (Liu et al., 2007). The diagram of noise sources of MOS-HEMTs is shown in Fig. 30. The possible noise sources of transistors are originated from the resistance of gate-region and series resistance of ungated-region. The prior resistance can be modulated by gate voltage while the later remains constant. The normalized noise power spectra of MOS-HEMTs, in which the SiO₂ layer is deposited using Cat-CVD method, operated in saturation region are shown in Fig. 31. It can be seen that the noise are fitted well by 1/f law, when V_{GS} is closed to threshold voltage. However, the exponent of 1/f fitting line increases when gate bias becomes positive. This phenomenon is attributed to the spatial distribution of interfacial traps states (Reimbold et al., 1984).

Fig. 30. The diagram of noise sources of MOS-HEMTs.

Fig. 31. The normalized noise power spectra of MOS-HEMTs operated in saturation region.

4.6 Metalorganic chemical vapor deposition (MOCVD) method

The metalorganic chemical vapor deposition (MOCVD) is a form of CVD utilizing metalorganic compounds as precursors. Essentially all III-V and II-VI semiconductors and most of their alloys can be successfully grown using MOCVD system, making this possibly the most versatile growth technique for compound semiconductors. Mechanism of MOCVD system growth process in general is governed by thermodynamics, reaction kinetics, flow dynamics, and chemical composition of the gas species in the MOCVD system. Thermodynamics provide the driving force for the reactions, i.e. the equilibrium condition. The kinetic reaction describes the speed of the reaction and dynamic flow control the transport of the reactants to the surface. The chemical composition of the atmosphere determines the reactions involved in the growth, which includes the pre-reactions as well. MOCVD process relies on the vapor transport of the group III alkyls combined with group V hydrides to the heated substrate. At the heated substrate, the molecules pyrolyze to produce the group III and the group V elements needed for formation of the desired III-V semiconductors and subsequent reaction that comes after. Because these precursor molecules are so unstable at the growth temperature and the III-V solid is so stable, the thermodynamic driving force for MOCVD typically is enormous. Up to now, many works dedicated to study the electrical performance of AlGaIn/GaN MOS-HEMTs with dielectrics deposited using MOCVD system are reported (Kawai et al., 1998; Ren et al., 1998; Mehandru et al., 2002; Rai et al., 2006; Pozzovivo et al., 2007; Gregušová et al., 2007; Kordoša et al., 2007; Kuzmik et al., 2008). The performances of

AlGaN/GaN MOS-HEMTs with 4-nm-thick Al₂O₃ gate insulators grown using MOCVD are reported by Gregušová and Stoklas, et al. (Gregušová et al., 2007). Fig.32 (a) and (b) show the static and dynamic output characteristics of fabricated MES-HEMTs and MOS-HEMTs, respectively. The $I_{DS(max)}$ of the MES-HEMTs and MOS-HEMTs are 440mA/mm and 630mA/mm, respectively. The threshold voltages of MES-HEMTs and MOS-HEMTs are -3.14V and -4.26V, respectively. The $g_{m(max)}$ of MES-HEMTs and MOS-HEMTs are 67mS/mm and 116mS/mm, respectively. The larger g_m value of MOS-HEMTs compared to that of MES-HEMTs may be attributed to the incorporation of very thin gate insulators (Gregušová et al., 2007). In Fig. 32 (b), it can be seen that the MOS-HEMTs have less current collapse but the self-heating effect is still found at large drain-source voltage.

Fig. 32. The (a) static and (b) dynamic output performances of AlGaN/GaN MES-HEMTs and MOS-HEMTs.

The Si₃N₄/AlGaN/GaN MOS-HEMTs with field-plate structure for power application are investigated (Rai et al., 2006). The schematic configuration of MOS-HEMTs and power performances of MES-HEMTs and MOS-HEMTs are shown in Fig. 33 (a) and (b), respectively. When both devices operated at 2GHz and 50V, the output power of MES-HEMTs and MOS-HEMTs are 12 W/mm and 14.32 W/mm, respectively.

Fig. 33. The (a) schematic configuration of MOS-HEMTs and (b) power performances of AlGaN/GaN MES-HEMTs and MOS-HEMTs.

4.7 Photoelectrochemical (PEC) oxidation method

The dielectrics of AlGaIn/GaN MOS-HEMTs are often deposited externally using electron-beam evaporator, sputtering system, MOCVD system, CVD system and others. However, the performances of these MOS devices are still affected by the natures of aforementioned deposition techniques involving particular growth conditions and contaminants inevitably brought to the semiconductor surface. In recent years, a photoelectrochemical (PEC) method has been successfully developed to either etch (Youtsey & Adesida, 1997) or oxidize (Rotter et al., 2000) GaN semiconductor. The PEC oxidation method can oxidize GaN and AlGaIn semiconductors directly for gate insulators and surface passivation and it is similar to the formation of SiO₂ film on Si wafer directly using thermal or wet oxidation method. The PEC oxidation technique has many advantages including large growth rate, low cost, plasma damage-free, and oxide/semiconductor interface with few contaminants. Compared with external deposition methods, the PEC oxidation method is able to deliver high quality oxide/semiconductor interface with low interface state density and high insulation layer (Lee et al., 2005). In the PEC experiment, the chemical solution with appropriate pH value and light source with appropriate wavelength are needed. The purpose of using a laser beam with a wavelength shorter than the wavelength corresponding to the energy bandgap of semiconductors is to create more electron-hole pairs for enhancing the PEC oxidation reactions. When n-type GaN semiconductor makes contact with chemical solution, a Schottky contact is formed at the interface owing to the difference in the work function between semiconductor and chemical solution (Lee et al., 2005). The induced holes are moved up toward the interface owing to the built-in electrical field.

Figure 34 illustrates the photoelectrochemical oxidation system. A chemical aqueous solution of H₃PO₄ with a pH value of 3.5 was used as the electrolytic solution. An ampere meter and a pH meter were used to measure the current and pH value, respectively. The work function W_E of electrolytic solution as a function pH value can be expressed as (Finklea, 1988):

$$W_E(\text{eV}) = 4.25 + 0.059 \times \text{pH value} \quad (1)$$

Since the pH value of 3.5 was used, the work function of the electrolytic solution is 4.457 eV. The work function W_s of n-type GaN is expressed as:

$$W_s(\text{eV}) = \chi + (E_C - E_F) \quad (2)$$

Where $\chi = 4.1 \text{ eV}$ is the electron affinity of n-type GaN, and $E_C - E_F = 0.039 \text{ eV}$ is the energy difference between the conduction band E_C and Fermi level E_F for the n-type GaN with an electron concentration of $5.0 \times 10^{17} \text{ cm}^{-3}$. The schematic energy-band diagram for the electrolytic solution/n-type GaN is shown in Fig. 35. A built-in electric field was induced within the depletion region due to the work function difference between the electrolytic solution and the n-type GaN. By using a He-Cd laser with a wavelength of 325 nm, electron-hole pairs were generated on the n-type GaN layer. The built-in electric field transported the generated electrons and holes to the n-type GaN and the electrolytic solution/n-type GaN interface, respectively. Since holes were accumulated at the interface, the n-type GaN was oxidized via the following reaction:

where h^+ is hole. Not only was the Ga₂O₃ formed, but also the Ga₂O₃ was etched by the electrolytic solution. When the oxidation rate is larger than the etching rate, the Ga₂O₃ layer can be grown directly. Therefore, we can deduce that the growth rate of the Ga₂O₃ depends on the

pH value of the electrolytic solution and the intensity of the He-Cd laser. By using a He-Cd laser, the growth rate of the Ga oxide film as a function of the laser intensity is shown in Fig. 36. The dependence of the induced current on the He-Cd laser intensity is also shown in Fig. 36. It can be seen that the growth rate and induced current are almost linearly proportional to the laser intensity. Because the generation rate of electron-hole pairs depends on the laser intensity, the increase in growth rate is attributable to the accumulation of more holes on the interface between the electrolytic solution and the n-type GaN. Oxidation was the process by which a layer of Ga oxide was formed on the n-type GaN surface. The oxidizing species diffused through the already grown Ga oxide to react with the GaN. For a grown Ga oxide thickness t_{ox} etched with KOH solution, we found the Ga oxide surface to be $0.67t_{ox}$ above the original n-type GaN surface, while the Ga oxide/n-type GaN interface was $0.33t_{ox}$ below.

Fig. 34. Photoelectrochemical oxidation system.

Fig. 35. Schematic energy band structure for H_3PO_4 solution/n-type GaN.

Fig. 36. Dependences of growth rate and induced current on He-Cd laser intensity.

For the p-GaN semiconductors, the schematic energy band diagram for H₃PO₄ solution/p-type GaN is shown in Fig. 37 (a). The flat-band potential energy W_s of p-GaN with a hole concentration of 3×10¹⁷cm⁻³ can be calculated from the following equation:

$$W_s(\text{eV})=q\chi + E_g - (E_F - E_V) \tag{4}$$

where $q\chi=3.3\pm0.2\text{eV}$ (Wu & Kahn, 1999) and $E_g=3.4\text{eV}$ are the electron affinity and the energy bandgap of the p-GaN, respectively. The separation between the Fermi level E_F and the valance band edge E_V of p-GaN is 0.106eV. Owing to the difference between the flat-band potential energy of p-GaN and the work function of the H₃PO₄ solution, a Schottky contact is consequently formed; its schematic energy band diagram is shown in Fig. 37 (a). The holes and electrons ionized in the space-charge layer can move toward the p-GaN layer and H₃PO₄/p-GaN interface, respectively, due to the built-in electric field. These induced holes would move into the bulk layer under the influence of the built-in electrical field if p-GaN is made contact with electrolytic solution (Huang et al., 2009). This may explain why oxidizing p-GaN using traditional PEC oxidation is considered difficult. As shown in Fig. 37 (a), p-GaN is known to have a very large downward band bending in the dark. However, when laser light with enough intensity illuminates the p-GaN surface, the band bending is flattened owing to the surface photovoltage (SPV) effect (Long & Bermudez, 2002) The SPV effect may cause upward band bending to bring a small density of holes up to the surface. To push more holes toward the H₃PO₄/p-GaN interface to effectively oxidize the p-GaN, an applied forward bias is needed to counteract the effect of the built-in electric field. Figure 37 (b) shows the energy band diagram of the bias-assisted H₃PO₄ solution and p-GaN. The grown oxide thickness as a function of forward bias for an oxidation time of 10min is shown in Fig. 38. It is found that the oxidation occurs when the forward bias is larger than 2V, and the oxide thickness is proportional to the net forward bias.

Fig. 37. Schematic energy band diagram for H_3PO_4 solution/p-type GaN (a) without bias assistance and (b) with bias assistance.

Fig. 38. Grown oxide thickness as a function of forward bias.

It can be found that the etching and oxidative reaction occur concurrently at the interface. Whichever the reaction is dominant could usually be determined using the appropriate PH value of the electrolytic solution in the PEC experiment. Furthermore, these reactions also reveal that the holes play an important role in the PEC oxidation process. The properties of oxide films grown by oxidizing GaN semiconductor directly using PEC oxidation method is reported by Lee and Chen, et al. (Lee et al., 2005). Figure 39 shows the $\text{Ga}2\text{P}_{3/2}$ core-level and $\text{O}1\text{s}$ core-level x-ray photoelectron spectroscopy (XPS) spectra of oxide films grown using PEC oxidation method. It can be seen that the XPS peaks related to Ga-O, O-Ga, and O-P bonds are observed at 1118.9eV, 530.8eV and 532.7eV. We can deduce that the GaN is oxidized successfully and the existence of O-P bonds is caused by H_3PO_4 chemical solution utilized in PEC experiment. The energy-dispersive spectrometer (EDS) measurement is used to analyze the composition of the Ga oxide films and is hereby shown

in Fig. 40. The composition of oxide layer is determined to be Ga:O:P=36.8%:62.4%:0.8%. Therefore, the composition of Ga oxide film is determined to be Ga₂O₃. The XRD measurement is utilized to verify the crystalline phases of oxide films annealed at different temperature. The XRD patterns of as grown oxide film and annealed oxide film at various temperatures are shown in Fig. 41. It can be found that the α-Ga₂O₃ (104) corresponded to 33.78% appears after the annealing treatment. According to the results observed in this work, the PEC oxidation method could grow Ga₂O₃ by oxidizing GaN semiconductor directly.

Fig. 39. (a) Ga2P_{3/2} core-level and (b) O1s core-level XPS spectra for grown Ga oxide Films.

Fig. 40. The EDS spectra of grown Ga oxide films.

Fig. 41. The Diffraction patterns of as-grown Ga₂O₃ and annealed Ga₂O₃ films measured by x-ray diffraction.

Figure 42 shows the cross-sectional TEM micrograph of the oxidized samples. It is evident that the hexagonal pinholes originated from the defects of the n-type GaN. Using EDS measurement, similar Ga_2O_3 composition was found for the oxidation layers in the flat surface and pit region of the GaN. It is obvious that not only the flat surface of the n-type GaN was oxidized, but that the defect region was also oxidized into Ga oxide.

Fig. 42. Cross-sectional TEM micrograph of oxidized n-type GaN.

For PEC oxidation of n-AlGaN semiconductors (Huang and Lee, 2007), a He-Cd laser with a power density of $10.0\text{mW}/\text{cm}^2$ and a wavelength of 325nm were used as the light source. An H_3PO_4 chemical solution with a pH value of 3.5 was used as the electrolytic solution. The work function W_E of the H_3PO_4 solution can be calculated as (Finklea, 1988):

$$W_E(\text{eV}) = 4.25 + 0.059 \times \text{pH value} = 4.457\text{eV} \quad (5)$$

The work function W_S of the n-type AlGaN is expressed as:

$$W_S(\text{eV}) = 3.985 + (E_C - E_F) \quad (6)$$

where 3.985eV is the electron affinity of the n-type AlGaN, and $E_C - E_F = 0.021\text{eV}$ is the energy difference between the conduction band E_C and Fermi level E_F of the n-type AlGaN with an electron concentration of $1.2 \times 10^{18}\text{cm}^{-3}$. By illuminating a He-Cd laser, electron-hole pairs were generated on the surface of the n-type AlGaN layer. The energy band structure for the electrolytic solution and the n-type AlGaN is shown in Fig. 43. An induced built-in electric field resulted in the surface of the n-type AlGaN layer. The generated electrons and holes were transported to the n-type AlGaN layer and the interface between the H_3PO_4 electrolytic solution and the n-type AlGaN by the induced built-in electric field, respectively. Because the generated holes were accumulated at the interface, the surface of the n-type AlGaN layer was gradually oxidized via the following reaction

where h^+ is holes. Not only was the oxidized film formed, but it was etched by the H_3PO_4 electrolytic solution. The PEC method is a diffuse procedure similar to thermal oxidation of Si in O_2 ambient. Even oxide films were grown; electrolytic solution continuously diffused through the grown oxide film to the interface and gradually formed oxide films. Figure 44 shows the XRD pattern of the grown oxidized film without thermal annealing. The peak of

ϵ - Al_2O_3 (32.63°) and Ga_2O_3 (43.08° and 47.61°) can be found, except for the peaks of Al_2O_3 , GaN, and AlGaN which originated from the sapphire substrate, undoped GaN nucleation layer and buffer layer, and AlGaN layer, respectively. Because a 200nm thick Ti metal was deposited on a part of the surface of the sample to assist the oxidation process, a peak of Ti (36.37°) was also found in Fig. 44. Because the oxidized film without thermal annealing can be easily dissolved in developer, acid solution, and alkaloid solution, it is difficult to use in the fabrication process of related devices. When the oxidized film was annealed in O_2 ambient at 700°C for 2h, the thickness was reduced from 400 to about 280nm. To clearly illustrate the oxidized film with the annealing process, the difference in the resulting XRD pattern between the original sample and the annealed oxidized sample is shown in Fig. 45. It can be seen that Ga_2O_3 was transferred to β - Ga_2O_3 (57.56° and 59.23°). Furthermore, the ϵ - Al_2O_3 crystal phase was transferred to α - Al_2O_3 (52.55°). Both β - Ga_2O_3 and α - Al_2O_3 crystalline phases show a better stability and ability of antietching in developer, acid solution, and alkaloid solution. This phenomenon indicates that the oxidized AlGaN films have a better quality after the annealing treatment. Figure 46 shows the XPS spectra and associated curve-fitting spectra for the core level O1s of the oxidized AlGaN without and with annealing treatment, respectively. As shown in Fig. 46, the binding energies of 530.8, 531.4, and 532.7eV are related with O-Ga, O-Al, and O-P bonds, respectively (Tourtin et al.,). It can be found that the main composition of the oxidized AlGaN film consists of Ga_2O_3 and Al_2O_3 . However, O-P existed in the oxidized AlGaN film. The content of P originated from the H_3PO_4 chemical solution. Because the composition related with O-P binding structure was not found in the XRD pattern as shown in Fig. 44, it can be deduced that the content of P is very small. For the XPS spectra of core level O1s for the oxidized AlGaN film annealed in O_2 ambient at 700°C for 2h as shown in Fig. 46, the signal intensity of O-P bonds, O-Ga bonds, and O-Al bonds is enhanced. It can be deduced that more oxygen would bind with P, Ga, and Al atoms and form more PO_x , Ga_2O_3 , and Al_2O_3 bonds during the annealing process in O_2 ambient. The components of the oxidized AlGaN layer were measured using SIMS. Figure 47 shows the associated SIMS depth profiles. The source used in SIMS measurement is Cs^+ . The depth profiles shown in Fig. 47 indicate that the AlGaN was oxidized.

Fig. 43. Schematic energy band structure for H_3PO_4 solution/n-type AlGaN.

Fig. 44. XRD pattern of an oxidized AlGaN oxide layer without annealing treatment.

Fig. 45. The comparison of the different XRD patterns of the original sample and an oxidized AlGaN layer annealed at 700°C in O_2 ambient for 2h.

Fig. 46. The XPS spectra of oxidized AlGaN layer with and without annealing treatment.

Fig. 47. The SIMS depth profile of oxidized AlGaN layer.

The electrical performance of GaN MOS diodes with as-grown Ga₂O₃ films grown by PEC oxidation method are also demonstrated by Lee and Chen, et al. (Lee et al., 2003). The schematic configuration of GaN MOS diodes is shown in Fig. 48. The inner radius, outer radius, and oxide thickness of gate insulators are 150μm, 400μm, and 100nm, respectively. Figure 49 shows the current-voltage characteristics of MOS diodes. The forward breakdown field and reverse breakdown field of GaN MOS diodes with 100-nm-thick as-grown Ga₂O₃ films are 2.8MV/cm and 5.7MV/cm, respectively. In addition, by applying the forward bias, many electrons are accumulated at the interface. When a reverse bias is applied, there are an insufficient number of holes to be supplied to accumulate at the interface. Since inducing minor carriers with only an applied bias in GaN-based semiconductors is very difficult, hence the deep-depletion phenomenon can easily be observed from the capacitance-voltage characteristics of GaN-based MOS diodes. Figure 50 shows the photoassisted C-V characteristics of the GaN MOS diodes. With forward bias applied, the total capacitances are predominantly attributed to the oxide film. The dielectric constant of 10.6 can be obtained using following equation:

$$C_{ox}=\epsilon_{ox}\epsilon_0A/t_{ox} \tag{8}$$

where C_{ox} is the capacitance of oxide film, ε_o is the permittivity in a vacuum, A and t_{ox} are the measured area and thickness of oxide films. The interface state density can be calculated using the following:

$$D_{it}=C_{ox}\Delta V/AqE_g \tag{9}$$

where ΔV is the shift of threshold voltage, and E_g is the energy bandgap of GaN. The interface state density estimated from the above is 2.53×10¹¹cm⁻²eV⁻¹. So, the PEC oxidation method potentially could render high insulating oxide film and oxide/semiconductor interface with low interface state density.

Fig. 48. The schematic configuration of GaN MOS diodes.

Fig. 49. The current-voltage characteristics of the MOS devices at room temperature.

Fig. 50. The photoassisted C-V characteristics of the MOS devices.

The electrical performance of GaN-MOS diodes with SiO₂/Ga₂O₃ stack gate dielectrics is reported by Lee, et al. (Lee et al., 2003). The MOS devices with insulating layer of as-grown Ga₂O₃ (80nm) and SiO₂-as-grown Ga₂O₃ (20–80nm) are referred to as device 1 and device 2, respectively. The devices 3, 4, 5, and 6 are referred to as GaN MOS devices with oxide films of SiO₂ and Ga₂O₃ annealed at 300°C, 500°C, 700°C, and 900°C, respectively. The thickness of as-grown oxide films decreases with an increase in annealing temperature, making the oxide films gradually become denser. Figure 51 shows the cross-sectional schematic configuration of MOS diodes with stack gate oxide films. The current-voltage characteristics of MOS diodes depicted in normal scale and a magnified scale are shown in Fig. 52 and 53 respectively. It can be seen that the forward leakage current is larger than the reverse leakage current for all devices. The breakdown voltages of all MOS devices all behave similarly. When a forward bias is applied on gate, many electrons supplied by n-GaN accumulate at the interface. When a reverse bias is applied, the n-GaN cannot supply a sufficient number of holes to accumulate at the interface. The phenomenon mentioned above can be used to explain why the substantially larger forward leakage current and forward breakdown voltage are obtained compared to the reverse parameters. The interface state density of all MOS diodes can be extracted by using photoassisted capacitance-voltage measurement. The parameters of all GaN MOS diodes are shown in Table 1. The carrier transport mechanism in insulating layer is analyzed using Frenkel-Poole model (Sze, 2002). The Frenkel-Poole emission current density can be expressed as:

$$J(E, T)=B\text{Eexp}\{-q\left[\Phi_B-(qE/\pi\epsilon_i\epsilon_0)\right]/kT\} \tag{10}$$

where B is the proportional constant, Φ_B is the barrier height, ε_i is the dielectric constant of Ga₂O₃, and k is the Boltzmann constant. To estimate the barrier height of the MOS diodes, equation (5) can be rewritten as follows:

$$\ln (J/E)=\ln B-q\left[\Phi_B-(qE/\pi\epsilon_i\epsilon_0)^{0.5}\right]/kT \tag{11}$$

The values of Φ_B were estimated from the relationship between ln(J/E) and 1/T of the MOS devices operated at -10V and 25°C, 50°C, 75°C, and 100°C, respectively, and are shown in Table 1. It can be seen that the barrier height of oxide films enhances with an increase in annealing temperature of the as-grown Ga₂O₃ oxide layers. Those results indicate that the gate leakage current also decreases with the increase of the annealing temperature.

Fig. 51. The cross-sectional schematic configuration of the GaN MOS diode with stack gate insulator.

Fig. 52. The current-voltage characteristics of the GaN MOS diodes with stack gate insulators.

Fig. 53. The current-voltage characteristics of the GaN MOS diodes with stack gate insulators with an magnified current scale.

	Device 1	Device 2	Device 3	Device 4	Device 5	Device 6
Insulating layer thickness (nm)	Ga ₂ O ₃ 80	SiO ₂ /Ga ₂ O ₃ 20/80	SiO ₂ /Ga ₂ O ₃ 20/42	SiO ₂ /Ga ₂ O ₃ 20/32.6	SiO ₂ /Ga ₂ O ₃ 20/25.5	SiO ₂ /Ga ₂ C ₃ 20/20.1
Forward breakdown voltage (V)	22.0	35.6	16.2	14.7	12.0	11.7
Forward breakdown field (MV/cm)	2.75	3.56	2.61	2.79	2.64	2.92
Reverse breakdown voltage (V)	47.0	59.0	47.5	43.0	40.5	46.0
Reverse breakdown field (MV/cm)	5.88	5.90	7.66	8.17	8.90	11.50
Barrier height (qφ _B , eV)	0.60	0.63	0.86	0.98	1.09	1.21
Interface state density (10 ¹¹ cm ⁻² eV ⁻¹)	2.53	2.50	2.42	2.34	2.21	2.00

Table 1. The parameters of the GaN MOS diodes with stack gate insulators.

The schematic configuration of Al_{0.15}Ga_{0.85}N MOS diode with 45-nm-thick annealed oxide film is shown in Fig. 54. The oxide film is annealed at 700°C in O₂ ambient for 2h. The inner radius and outer radius of the structure are 150μm, 400μm, respectively. Fig. 55 shows the current-voltage characteristics of AlGaN MOS diode. The gate leakage current is only 45nA and 69pA at 5V and -15V, respectively. The forward breakdown voltage and reverse breakdown voltage are 2.2MV/cm and 6.6MV/cm, respectively. Those results suggest the excellent insulation of the oxidized AlGaN films is indeed realized after annealing treatment. Furthermore, it can be seen that the forward leakage current is larger than the reverse leakage current. When applying forward bias to the gate electrode, many electrons would accumulate at the oxide/semiconductor interface. On the other hand, when the reverse bias is applied, the AlGaN semiconductor could not supply an enough number of holes to accumulate at the interface, since inducing minor carriers by the applied bias alone in AlGaN semiconductors is very difficult. The interface state density of annealed oxidized AlGaN/AlGaN interface estimated using the photoassisted capacitance-voltage measurement and the C-V characteristics of AlGaN MOS diodes are shown in Fig. 56. The average interface state density is 5.1×10¹¹cm⁻²eV⁻¹.

Fig. 54. The schematic configuration of Al_{0.15}Ga_{0.85}N MOS diodes with 45-nm-thick annealed oxide films grown using PEC oxidation method.

Fig. 55. The current-voltage of Al_{0.15}Ga_{0.85}N MOS diodes.

Fig. 56. The photoassisted capacitance-voltage characteristics of $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$ MOS diodes.

The performance of AlGaN/GaN MOS-HEMTs with gate oxide films grown using PEC oxidation method are demonstrated by Huang and Yeh, et al. (Huang et al., 2008) for the first time. The schematic configuration of the MOS-HEMTs is shown in Fig. 57. The HEMT structure is consisted of a 100nm $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$ layer, a 0.3 μm undoped GaN channel, a 1.5 μm insulating carbon-doped GaN, and a 20nm AlN nucleation layer, are all grown on a sapphire substrate using molecular-beam epitaxy system (MBE). This HEMT sample shows a sheet resistance of 726 $\Omega/\text{sq.}$, a sheet electron density of $6.93\times 10^{12}\text{cm}^{-2}$, and Hall mobility of 1240 cm^2/Vs . The gate width, gate length, and the thickness of annealed insulators are 300 μm , 3 μm , and 45nm, respectively. Fig. 58 shows the output characteristics of AlGaN/GaN MOS-HEMTs. The I_{DSS} at $V_{\text{GS}}=0\text{V}$ and the threshold voltage are 200mA/mm and -5V, respectively. The transfer characteristics of MOS-HEMTs operated at $V_{\text{DS}}=10\text{V}$ are shown in Fig. 59. The peak g_{m} value of 50mS/mm is obtained at $V_{\text{GS}}=-2.09\text{V}$. The gate leakage currents at forward gate bias of $V_{\text{GS}}=10\text{V}$ and reverse gate bias of $V_{\text{GS}}=-10\text{V}$ are 50pA and 2pA, respectively. It clearly indicates that the forward gate leakage current is larger than the reverse gate leakage current.

Fig. 57. The cross sectional schematic configuration of $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}/\text{GaN}$ MOS-HEMTs.

Fig. 58. The output characteristics of $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}/\text{GaN}$ MOS-HEMTs.

Fig. 59. The transfer characteristics of $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}/\text{GaN}$ MOS-HEMTs operated at $V_{DS}=10\text{V}$.

To realize the high-frequency performance of AlGaIn/GaN MOS-HEMTs with gate oxide films grown using PEC oxidation method, the transistors with $1\text{-}\mu\text{m}$ -long and $50\text{-}\mu\text{m}$ -wide two-finger gate are also reported (Huang et al., 2008). The schematic configuration of fabricated MOS-HEMTs is shown in Fig. 60. The oxide thickness is 40nm . Fig. 61 shows the dc electrical performances of MOS-HEMTs. The I_{DSS} at $V_{GS}=0\text{V}$ and threshold voltage are 580mA/mm and -9V , respectively. The maximum extrinsic transconductance ($g_{m(\max)}$) and gate voltage swing (GVS) are 76.72mS/mm and 2.6V , respectively. The gate leakage current is only 102nA and 960nA when V_{GS} are respectively set at -60V and 20V . The forward breakdown voltage and reverse breakdown voltage are 25V and larger than -100V , respectively. Figure 62 shows the short-circuit current gain ($|h_{21}|$) and the maximum available power gain ($G_{\max}$) as a function of frequency derived from S-parameters measured at $V_{DS}=10\text{V}$. The f_T and $f_{\max}$ value of AlGaIn/GaN MOS-HEMTs are 5.6GHz and 10.6GHz , respectively.

Fig. 60. The cross sectional schematic configuration of Al_{0.15}Ga_{0.85}N/GaN MOS-HEMTs.

Fig. 61. The dc performances of Al_{0.15}Ga_{0.85}N/GaN MOS-HEMTs.

Fig. 62. The short-circuit current gain (h_{21}) and maximum available power gain (G_{max}) of Al_{0.15}Ga_{0.85}N/GaN MOS-HEMTs.

When the transistors are applied as oscillators or mixers in communications and electronic systems, the presence of flicker noise or 1/f noise limits the phase noise characteristics, thereby causing the performance degradation of the associated systems. In general, the flicker noises are caused by contact resistance, gate leakage current, and bulk resistance. The contact resistance is only about 18Ω for AlGa_N/Ga_N MOS-HEMTs. The gate leakage current is five orders of magnitude smaller than the drain-source current of the MOS-HEMTs operated at V_{DS}=10V. Therefore, it can be deduced that the bulk noise is the dominant flicker noise source. Figure 63 shows the normalized noise power spectra of the MOS-HEMTs measured in saturation region (V_{DS}=10V) in the frequency range from 4Hz to 10kHz. It can be seen that the flicker noises are proportional to 1/f fitting line.

Fig. 63. The normalized noise power spectra of Al_{0.15}Ga_{0.85}N/GaN MOS-HEMTs measured at room temperature and V_{DS}=10V.

The mobility fluctuation model (Hooge et al., 1981; Hooge, 1994; Vandamme et al., 1994) is used to analyze the flicker noise performance in this work. The Hooge’ s coefficient (α_{ch}) can be calculated from the following equation:

$$\alpha_{ch}=S_I(f) \times f \times N/I^2=[S_I(f) \times f \times (L_g^2/q \times \mu \times R_{ch})]/I^2$$

(12)

where S_I(f)/I² is the normalized noise power density, f is the frequency, N is the total number of carriers, L_g is the gate length, μ is the carrier mobility, q is the elementary charge, and R_{ch} is the channel resistance. According to the noise spectrum shown in Fig. 63, the 1.25×10⁻³ value of MOS-HEMTs biased at V_{GS}=0V and V_{DS}=10V is obtained at 100Hz and it is comparable to other reported values (Chiou et al., 2006). In Fig. 63, it can also be found that the normalized noise power density increases with the decrease of gate bias. The total low frequency noise (S_{Rt}) between source and drain regions can be expressed as follows:

$$S_{Rt}=S_{Rch}+S_{Rs}$$

(13)

where S_{Rch} and S_{Rs} are the noises power densities originated from channel resistance and series resistance in un-gated region, respectively. The total resistance (R_t) of the transistors can be expressed as (Peransin et al., 1990):

$$R_t=R_s+R_{ch}=R_s+I_{gate} \mid V_{off} \mid (Wq\mu n_{ch}V_G)$$

(14)

where R_s is the series resistance of un-gated regions, R_{ch} is the resistance of channel, l_{gate} is the gate length ($1\mu\text{m}$), V_{off} is the pinch-off voltage (-9V), W is the width of the channel ($50\mu\text{m}$), q is the elementary charge, μ is the mobility of 2DEG ($1240\text{cm}^2/\text{Vs}$), n_{ch} is the concentration of 2DEG at $V_G = |V_{off}|$, and $V_G = V_{GS} - V_{off}$ is defined as the effective gate bias. The channel resistance is larger than the series resistance when gate bias is negative ($V_{GS} = 0\text{V}$). Therefore, the total flicker noise is dominated by the channel resistance. The normalized noise power density can be expressed as:

$$S_I(f)/I^2 = S_{Rt}/R_t^2 = (S_{Rch} + S_{Rs})/(R_{ch} + R_s)^2 \approx S_{Rch}/R_{ch}^2 \quad (15)$$

$$S_I(f)/I^2 = \alpha/fN \propto V_G^{-1} \quad (16)$$

Using the equations mentioned above, the reason for observing an increase in the normalized noise power density in response to the decrease of gate bias could then be clearly explained.

The direct-current (dc), radio-frequency (rf) and low frequency noise performances of AlGaIn/GaN MOS-HEMTs with gate insulators grown using the PEC oxidation method have been reported in recent years. An oxide/semiconductor interface with low interface state density and good insulation of oxide films can be obtained by oxidizing GaN and AlGaIn using the PEC oxidation method directly. Therefore, the PEC oxidation method is a promising technique for fabricating high caliber GaN-based MOS devices and GaN-based integrated circuits in the future.

5. Conclusions

The GaN-based semiconductors are potentially suitable materials for optoelectronic and electronic applications. Among various GaN-based electronic devices investigated, the MOS devices show potentially higher operating frequency, large output power gain, and better thermal stability, in comparison with the well developed Si-based MOS devices. Various deposition methods, which have been used to deposit oxides or insulators on GaN-based semiconductors to fabricate MOS devices, are summarized. The resultant devices demonstrate promising performances. In particular, the newly developed photoelectrochemical (PEC) oxidation method has aroused increasing interests due to its intrinsic advantage in producing high quality oxide/semiconductor interface over the other conventional deposition methods. It is expected that with the progress in dielectric deposition techniques, in combination with improvements in GaN-based materials and device configurations, the GaN-based MOS devices will certainly play an important role in high-frequency and high-power applications such as GaN-based integrated circuits (ICs) and opto-electronic integrated circuits (OEICs) in the future.

The processing techniques for Si-based materials and devices are well developed but unfortunately they are not suitable for fabricating LEDs and LDs. On the other hand, the epitaxial techniques for GaN-based semiconductors are still under development and certainly there are still ample rooms for improvements. Someday, the obstacles presently encountered would be overcome and the electrical properties of GaN-based semiconductors are expected to improve tremendously. There is a great expectation in the future to efficiently combine electronic devices with the optoelectronic devices in order to produce the so-called the optoelectronic integrated circuits (OEICs). Therefore, the most important

challenges facing the researchers nowadays are to come up with innovative designs of high performance GaN-based electronic devices before these devices could be anticipated to combine with other GaN-based photonic components to eventually produce the ultimate optoelectronic integrated circuits (OEICs) of high caliber in the future.

6. References

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