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Computational Study of the Effects of Channel Materials & Channel Orientations and Dimensional Effects on the Performance of Nanowire FETs

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1. Introduction

Silicon has been extensively studied for decades due to its successful applications in semiconducting devices such as metal-oxide-semiconductor field-effect-transistors (MOSFETs). With the demand for high performance devices and packing density, scaling of Si based MOSFETs was drastically driven into nano-scale regime. However, quantum tunneling starts play an important role in degrading the device performance of a conventional Si MOSFET, such as drain-induced barrier-lowering (DIBL) in nano-scale regime. Furthermore, silicon based devices will face its own physical limitation in near future (ITRS, 2007) due to this. Therefore, in order to overcome the challenges of scaling limitation, search for other potential channel materials, such as high carrier mobility material and structure modification have been the heart of research. Among the various proposed materials and device structures, gate-all-around (GGA) Si nanowire (NW) field-effect-transistors (FETs) stand out because their perfect surrounding gates enhance the ability of gate control to suppress the problem of DIBL and fully compatible with Si based technology integration. With the successful fabrication of Si nanowires in the different laboratories (Singh, N. *et. al.*, 2006), nanowires (NWs) have been extensively studied as they are promising for building blocks as nanowire MOSFETs (Cui, Y. *et. al.*, 2003; Pecchia, A. *et. al.*, 2007; Kumar, M. Jagadesh *et. al.*, 2008; Wei, Lu & Lieber, C.M., 2006; Wei, Lu. *et. al.*, 2008), nanophotonic systems (Greytak, A.B. *et. al.*, 2005; Agarwal, R. & Lieber, C.M, (2006); Tian, B. *et. al.*, 2007; McAlpine, M.C. *et. al.*, 2004) and as biochemical sensors (Patolsky, F. & Lieber, C. M., 2005; Hahm, J. & Lieber, C. M., 2004; Cui, Y. *et. al.*, 2001; Gengchiao, L. *et. al.*, 2007). Recent advanced development reveals that physical properties of nanowires could be modified depending on the NW growth direction and diameter. This suggests that material structure such as channel orientations play an important role in device performance optimization. Coupled with the fact that besides silicon, other semiconductor materials such as germanium (Ge) demonstrates promising results (Wang, J. *et. al.*, 2005; Rahman, A. *et. al.*, 2005), a new chapter of study on alternate high mobility channels in nano world has been opened.

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Previous theoretical study on this topic using the effective mass model has been carried out (Wang J. *et. al.*, 2004) with the lack of detailed information portraying the electronic structures in the nano-scale regime. Recently, tight-binding (TB) method has been used (Neophytou, N. *et. al.*, 2008; Rahman, A. *et. al.*, 2003) as an alternative procedures to evaluate device performance. However, the former focuses their analysis and simulations on cylindrical cross-section nanowires (Wang, J., *et. al.*, 2004) and the latter discussed on ultra-thin body dual gate (UTB DG) MOSFET (Rahman, A. *et. al.*, 2003). Although TB and non-equilibrium Green's Functions (NEGF) has been developed and implemented to study nanowire MOSFETs (Luisier, M., *et. al.*, 2008) as it provides better transport results compared to top-of-barrier approach, it is time-consuming especially in simulating large nanowire size and long channel. As the objective of this work is to investigate the effects of nanowire orientations to the ultimate performance of nanowire, it is suffice to apply top-of-barrier approach in our work to do the comparison. Therefore, in this work, we explore and compare the ultimate performance of a set of cylindrical nanowire devices with different semiconductor materials (Si and Ge) and channel orientations using TB model and top-of-barrier model (Neophytou, N. *et. al.*, 2008) approaches. TB approach is employed to investigate the electronic properties of NWs in terms of E-k dispersion in order to accurately capture the orientation as well as quantum effects in a nano-scale system. Based on the calculated E-k dispersion, we engaged a semi-classical top-of-barrier MOSFET model to evaluate the ballistic I-V characteristics of NW FETs by self-consistently solving Poisson equation in order to evaluate the ultimate performance of these semiconductor NW FETs with various channel orientations. The schematic of the device structure is shown in Fig. 1. The simulation is conducted in two parts: a) simulate I-V characteristics of circular nanowire (CW) with diameter of 3nm for Si and Ge with different orientations to study the effects of materials and orientations on the device performance and b) extend this simulations to explore performance of CW with different diameters. In this work, we explore four different diameters: 3nm, 5nm, 8nm and 10nm.

Fig. 1. A schematic of the simulated cylindrical nanowire FETs. The diameter of the circular cross-section (D) varies from 3nm, 5nm, 8nm and 10nm. The oxide thicknesses (t_{ox}) for this simulation are set at 1.6nm and 0.5nm for comparison.

2. Methodology

To investigate the ultimate performance of NW MOSFETs based on structural effects, we follow a two-step approach. Firstly, we assume a NW with certain size and orientation, and then, a $sp^3d^5s^*$ tight-binding model is implemented to investigate the electronic properties of NWs in terms of E-k dispersion relations. Next, we use the simulated dispersion relations obtained from TB model to calculate the ballistic current-voltage (I-V) characteristics of both p-channel and n-channel NW MOSFETs using a semi-classical “top-of-the-barrier” MOSFET

model. The results shown in (Neophytou, N. *et. al.*, 2008) with and without including self-consistency of bandstructure do not differ significantly to render the results invalid. Therefore, in this work, we do not calculate self-consistency of bandstructure.

A. Electronic Bandstructure Calculations:

To obtain the bandstructure of the Si NWs of different orientations, we assume an unrelaxed nanowire atomic geometry and construct the Hamiltonian of the NW unit cell using the orthogonal-basis $sp^3d^5s^*$ tight-binding method developed for bulk electronic structure. (Boykin, T.B. *et. al.*, 2004) In this approach, we model each atom using 10 orbitals per atom in total. The different energy parameters in this TB model were obtained by fitting a genetic algorithm to reproduce the bandgap and the electron/hole effective masses in different valleys. The simulated NW is assumed to be infinitely long, and the nanowire surface is passivated by hydrogen atoms, which in this case is treated numerically using a hydrogen termination model of the sp^3 hybridized interface atoms. This technique is reported to be successfully removing all the interface states from the bandgap. (Lee, S. *et. al.*, 2004) This model has shown good agreement with the measured bandgap vs. diameter of silicon nanowires despite the exclusion of relaxation or strain effects. Once the transport direction is specified, the size t_{Si} of the NW and unit cell can be defined, cf. Fig. 1. The Hamiltonian of atoms within the unit cell and atoms within neighboring unit cells are obtained as H_l , where l is the unit cell index with $l=0$ for the center unit cell and $l \neq 0$ for the l -th nearest-neighboring cell. In this model, we only consider the nearest neighbors i.e., $l=1$ and -1 . Then, the Hamiltonian in 1D k -space is calculated by taking the Fourier transform:

$$H_{k_m} = \sum_l H_l \exp[-j \cdot k_m (z_l - z_0)] \quad (1)$$

where $k_m = m\pi/L$ is the wavevector within the 1st Brillouin zone, m is the real number between 0 and 1, and L is the periodicity of the 1D lattice, $z_l = lL$, referring to the unit cell position. Due to the orthogonality of the TB basis sets, a simple eigenvalue problem, $H_{k_m} \Psi = E_{k_m} \Psi$, can be solved for each k_m within the first Brillouin zone. The electronic structures of the nanowires such as bandgap, bandstructure, etc., can be provided and used for the transport calculations. The conduction and valance bands for Si and Ge are shown in Fig. 2(a) to 2(d). From Fig. 2, it can be seen that valley splitting occurs and the degeneracy is lifted, giving rise to two subbands. Figs. 3a and 3b show the valley splitting as a function of nanowire diameters for n-type Si and Ge and p-type Si and Ge for [110] orientation, respectively. Fig. 3a shows that valley splitting is more evident when the diameter falls beyond 5nm. In general, valley splitting for Ge is always larger than Si, as shown in Fig. 3a due to Ge having lighter mass. However, a great distinction in valley splitting can be observed when the NW diameter is smaller than 5nm for Si and 8nm for Ge, respectively.

B. Transport Calculation:

Next, we use a semi-classical top-of-the-barrier MOSFET model (Rahman, A. *et. al.*, 2003) to simulate the ballistic I-V characteristics. In this model, a simplified 3-dimensional self-consistent electrostatic model with ballistic treatment of carrier transport is used. In addition, quantum capacitance effects are included into this approach. Three-dimensional electrostatics is described by a simple capacitance model (Rahman, A. *et. al.*, 2003). The capacitors represent the electrostatic coupling of the gate (C_G), drain (C_D), and source terminals (C_S) to the top of the potential barrier at the source end of the channel. These

Fig. 2. Conduction and valence band bandstructure for (a) 3nm Si with [110] orientation and (b) 3nm Ge with [110] orientation.

Fig. 3. (a) and (b) show the valley splitting as a function of nanowire diameters for n-type and p-type respectively. It can be observed that valley splitting is a strong function of quantum confinement. In terms of semiconducting material, valley splitting is more evident in Ge compare to Si. This is due to Ge having lighter mass compared to Si. The solid line, dashed line, and dotted line represent NW's orientation along [100], [110], and [111], respectively.

capacitors control the subthreshold swing, S , of the transistors and the drain-induced barrier lowering (DIBL) according to the following equations:

$$\frac{C_G}{C_\Sigma} = \frac{2.3k_B T / q}{S} \quad (2a)$$

$$\frac{C_D}{C_\Sigma} = \frac{2.3k_B T / q}{S} \times DIBL \quad (2b)$$

$$C_\Sigma = C_G + C_D + C_S \quad (2c)$$

Then, the Poisson's equation is solved using a simplified capacitance model. The Poisson's potential (U_P) is equal to $U_0 \cdot (N - N_0)$, where $U_0 = q/C_\Sigma$ is the single electron charging energy, N_0 and N are the number of mobile carriers at the top of the barrier at equilibrium and under applied bias, respectively, while C_Σ is the total capacitance. The carrier density N , can be directly computed from E - k relations determined earlier by applying the below equation,

$$N = \int_{-\infty}^{\infty} \frac{dk}{\pi} [f(E - E_{fs} + U_{scf}) + f(E - E_{fs} + qV_D + U_{scf})] \quad (3)$$

where $f(E)$ is the Fermi function and E_{fs} is the chemical potential in the source region. Iteration between N and U_{scf} is repeated until the self-consistency converges. The NW MOSFET current is then evaluated using the semi-classical transport equation in the ballistic limit, which is given by:

$$I = \frac{2q}{h} \int_{U_{scf}}^{\infty} dE [f(E - E_{fs}) - f(E - E_{fs} + qV_D)] \quad (4)$$

3. Simulation results and discussions

Firstly, using top-of-barrier model, the I-V characteristics of Si and Ge for different orientations of CW NW transistors with the effective gate oxide thickness (EOT) of 1.6nm and 0.5nm are investigated. The off-state currents of all cases are set to be $0.2 \mu A / \mu m \cdot (2D)$ in our simulation. Solid lines represent [100] orientation while dash lines represent [110] orientation and dotted lines represent [111] orientation. Red lines represent p-type and blue lines represent n-type devices. Fig. 4(a) and 4(b), respectively, show the I_{ds} - V_{ds} curves for 3nm Si and Ge at $V_{gs}=0.6V$ for EOT of 1.6nm while Fig. 4(c) and 4(d), respectively, show the I_{on}/I_{off} ratio as a function of nanowire diameter for Si and Ge with EOT of 1.6nm. For N-type NW FETs, as shown in Fig. 4(a) and (b), Si and Ge of [110] orientation give the highest on-currents, which is about 45% and 146%, respectively, compared to the current along [100] orientation. Comparing best orientation with the highest ON-state currents for different materials, Ge [110] outperforms Si [110] by 1.18 times due to Ge [110] having lighter effective mass compared to Si [110]. Similarly for p-type NW FETs, Si of [110] orientation and Ge of [111] orientation give the highest ON-state currents, with Ge [111] outperforms Si [110] by 1.78 times. Moreover, for Si NW FETs, n-type device has similar performance as p-

type device. This is due to lifting of degeneracy of the dispersion as an effect of quantum confinement. This resulted in a decrease in effective mass (Neophytou, N. *et. al.*, 2008). From Fig. 4(c) and 4(d), n-type Si and Ge NW FETs with [110] orientation has the highest Ion/Ioff ratio while for p-type NW FETs, Si and Ge with [111] orientation has highest Ion/Ioff ratio. Furthermore, it is also observed that Ion/Ioff decreases as nanowire diameter increases because small nanowire has better gate control due to larger capacitance.

Fig. 4. (a) and (b) shows the I-V characteristics for 3nm n-type and p-type Si and Ge , respectively while (c) and (d) respectively show the Ion/Ioff ratio for n-type and p-type devices, respectively. In general for n-type devices, Si and Ge with [110] orientation give highest on-current while p-type devices, [110] Si and [111] Ge give highest on-current. This is due to these orientations having lightest effective mass.

Next, the current density of n-type and p-type Si and Ge for different orientations with EOT of 1.6nm and 0.5nm were investigated, as shown in Fig. 5. As expected, the current density for EOT of 0.5nm is higher, about doubled comparing to Si and Ge with EOT of 1.6nm for all orientations due to better gate control as a result of larger gate capacitance. In terms of semiconducting materials, Ge always outperforms Si regardless of nanowire diameters for p-type NW FETs (Fig. 5b and Fig. 5d). However, for n-type NW FETs (Fig. 5a and Fig. 5c), the current density for Si does not differ much from Ge. This phenomenon could be explained by the effective mass of Si and Ge. From calculation of hole effective mass, it could be deduced that the effective mass of Ge is far apart compared to Si while for the electron effective mass, the differences of Si and Ge is not significantly far apart. Furthermore, two important points could be obtained for both Si and Ge electronic

bandstructures: a) It is shown, from calculation, that [110] orientation has the lightest electron effective mass compared with the other two orientations and b) Ge has lighter mass compared to Si in terms of semiconducting material, regardless of NW diameter. As a result, Ge with [110] orientation outperforms Si with [110] orientation, giving rise to better performance, in terms of the higher ON-state current.

Fig. 5. (a) and (b) shows the current density as a function of nanowire size for n-type and p-type Si and Ge with EOT=1.6nm while (c) and (d) shows the current density as a function of nanowire size for n-type and p-type Si and Ge with EOT=0.5nm. In general, the current density with EOT of 0.5nm is twice larger than that of 1.6nm due to better gate control.

In addition, we explore the capacitance effect on the device as the device current tightly depends on the capacitance, gate capacitance in particular. The C_g/C_{ox} ratio as a function of nanowire diameter for n-type and p-type Si and Ge NW GAA FETs with oxide thickness of 1.6nm and 0.5nm are shown in Fig. 6(a), (b), (c), and (d), respectively. It can be observed that the capacitance value degraded from the gate oxide capacitance for both Si and Ge regardless of oxide thickness. Detailed calculation with capacitance value given by

$$C_g = \frac{C_{ox}C_s}{C_{ox} + C_s} \text{ shows that [110] orientation for Si and Ge encounter greatest degradation}$$

from oxide capacitance by 31.6% while [100] orientation encounters degradation of 15.4% and [111] Si and [111] Ge both encounter degradation of 7.14% and 25%, respectively. All these translate to an effective increase in gate oxide thickness, which in general reduces the gate control to the device. However, in all cases, we found $C_g < C_{ox}$ and as gate oxide

thickness, t_{ox} decreases, the difference increases. It suggests that C_{ox} is not much larger than C_s and dominating C_g , under the approximation of a conventional Si planar MOSFET.

As shown in Fig. 6, in general, we could see that as the diameter of cylindrical NW is large,

given t_{ox} is thick, $C_g \approx C_{ox}$, where $C_g = \frac{dQ}{dV_g} \bigg|_{V_{ds}=0.05V}$. It indicates that $C_s \gg C_{ox}$ which is in

agreement with the classical approximation. However, as the diameter decreases, we found that in all cases, C_g/C_{ox} ratio is less than 1, indicating that the approximation $C_s \gg C_{ox}$ does not hold. For example, using $C_{ox} \approx 0.6448 nF/m$ and C_g obtained from simple calculation for 8nm cylindrical NW with $t_{ox}=1.6nm$, C_g/C_{ox} for n-type Si and Ge with [110] orientations is 0.8375 and 0.7444, respectively, and C_g/C_{ox} for p-type [110] Si and [111] Ge is 0.8685 and 0.8995, respectively. Similarly, for 3nm cylindrical NW with $t_{ox}=1.6nm$, C_g/C_{ox} for n-type Si and Ge with [110] orientations is 0.6993 and 0.7467, respectively, and for p-type [110] Si and [111] Ge, C_g/C_{ox} for both cases is about 0.76. For comparison, we did a calculation for 3nm cylindrical NW with t_{ox} of 0.5nm and the C_g/C_{ox} ratio falls to below 0.7 for n-type [110] Si and Ge as well as for p-type [110] Si. This is due to the larger gate capacitance caused by the thinner gate oxide.

Fig. 6. C_g/C_{ox} as a function of nanowire diameter for n-type and p-type Si and Ge with oxide thickness of 1.6nm (6a and 6b) and oxide thickness of 0.5nm (6c and 6d). The capacitance value is degraded from the gate oxide capacitance for both Si and Ge regardless of oxide thickness.

On the other extreme region, when the oxide thickness is reduced further due to shrinking of devices, $C_s \ll C_{ox}$, and $C_g \approx C_s$. At this point, the current does not depend on the effective mass of the material, and channel orientations. As a result, all the I-V curves of all cases with different materials and different orientations will overlap (Liang, G.C., *et. al.*, 2007).

To further explore device performance from a different perspective, the transconductance

$\left(g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \right)_{V_{ds}=0.05V}$, of FETs is investigated. For an ideal nanowire FET at low bias, the transconductance is given by $g_m = \frac{W\mu_{eff}C_g}{L}v_{ds}$, where C_g is the gate capacitance per unit

length. In this simulation, we have chosen gate length, L to be 16nm. This value is obtained from IRTS 2007 PIDS table, to be consistent with the production year in which off-current for dual gate is chosen. Fig. 7(a) and 7(b) show the transconductance of n-type Si and Ge and p-type Si and Ge NW FETs for EOT of 1.6nm at low drain to source bias of 0.05V for n-type and -0.05V for p-type, respectively, as a function of different diameters. Similarly, Fig. 7(c) and 7(d) show the transconductance of n-type Si and Ge and p-type Si and Ge NW FETs for

Fig. 7. (a) and (b) show the transconductance for Si and Ge with EOT of 1.6nm while (c) and (d) show the transconductance for Si and Ge with EOT of 0.5nm. In general, for n-type devices, [110] orientation has highest transconductance regardless of channel material and diameter size while for p-type devices, [110] Si and [111] Ge give highest transconductance.

EOT of 0.5nm at drain to source bias of 0.05V for n-type and -0.05V for p-type, respectively, as a function of NW's diameter. In general, the transconductance decreases as the diameter decrease due to lower ON-currents of the smaller diameter NWs. As the difference in gate voltage is a constant of 0.05V, the transconductance, g_m is proportional to on-current.

For n-type devices, Si and Ge of [110] orientation, in general, have the highest transconductance compared to the other two orientations regardless of nanowire area, as shown in Fig. 7(a). The transconductance of Ge [110] is about 1.15 times the value of Si [110] at 3nm and slowly widens to 1.5 times at 10nm. For p-type devices, in general, Si and Ge with [111] orientation have larger transconductance. Fig. 7(c) and 7(d) show the transconductance for EOT of 0.5nm for n-type Si and Ge and p-type Si and Ge. As expected, the transconductance for EOT of 0.5nm in general is more than twice the value with that of EOT of 1.6nm. This is in agreement with the trend of on-current simulation results for drain voltage of $\pm 0.05V$. For amplifiers, we require the gain to be large so as to amplify the output by a few magnitudes. Transconductance is a measurement of gain of amplifier. As such, if NW FETs were to be used as amplifiers, large transconductance is required. From the above observation, Ge is the best candidate for both n-type and p-type NW FETs.

4. Conclusion

In this work, we present the device performance of Si and Ge and channel orientations in NW FETs and extend the discussion for different NW diameters. We show that in terms of channel orientation, for n-type devices, Si [110] and Ge [110] give the highest on-current compared to other orientations while in terms of channel material, Ge outperforms Si by between 1.17 to 1.42 times due to the lighter effective mass. Moreover, it is also observed that valley splitting is a strong function of quantum confinement, and it is more significant for NW diameter smaller than 5nm. We also explore the effect of different oxide thickness on the performance of devices as the oxide thickness determines the device capacitance. In investigating the effects of gate capacitance on devices of different NW sizes, we conclude that gate capacitance degrades as the device shrinks into sub-nanometer regime. Therefore, conventional approximation to calculate transport property does not apply. As we examine the gate oxide capacitance further, we found that it has not reached the other extreme where $C_s \ll C_{ox}$ as at this extreme, the on-current for same material will overlap as the on-current only depends on effective mass. This phenomenon is not observed in the I_{ds} - V_{ds} curves even at EOT of 0.5nm. For transconductance, n-type Si and Ge of [110] orientation gives best performance while in terms of semiconducting material, both Si and Ge does not differ much. For p-type devices, Ge NW FETs show the better transconductance than Si NW FETs.

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The evolution of solid-state circuit technology has a long history within a relatively short period of time. This technology has lead to the modern information society that connects us and tools, a large market, and many types of products and applications. The solid-state circuit technology continuously evolves via breakthroughs and improvements every year. This book is devoted to review and present novel approaches for some of the main issues involved in this exciting and vigorous technology. The book is composed of 22 chapters, written by authors coming from 30 different institutions located in 12 different countries throughout the Americas, Asia and Europe. Thus, reflecting the wide international contribution to the book. The broad range of subjects presented in the book offers a general overview of the main issues in modern solid-state circuit technology. Furthermore, the book offers an in depth analysis on specific subjects for specialists. We believe the book is of great scientific and educational value for many readers. I am profoundly indebted to the support provided by all of those involved in the work. First and foremost I would like to acknowledge and thank the authors who worked hard and generously agreed to share their results and knowledge. Second I would like to express my gratitude to the Intech team that invited me to edit the book and give me their full support and a fruitful experience while working together to combine this book.

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