Chapter 1

Introductory Chapter: Green Electronics Starting from Nanotechnologies and Organic Semiconductors

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1. Introduction

Worldwide communities, governmental agencies or international research programs like Horizon2020 or Green Program2030, made huge concerted efforts to launch new visions in economy and society, [1]: green building, green cities, promoting the green transport development [2], eco-labels for logistics, green economy—bioeconomy, new green energy resources, network on bio-products, green and cost efficient aircraft design and not in the last time—smart, green and integrated electronics, [3]. The main pillar for a future green electronic industry is foreseen by the sustainable electronics that imply a feedback technological flow, to 99.99% reuse of the output products transformed in wastes, back to the input, as raw material. In this scope, new insights must be assimilated for a green factory vision: lifecycle of electronic technologies, recycling electronics, green energy convertors, electronic wastes reconversion new technologies, materials reconversion, mobile phones eco-rating and the list rests opened.

On the other hand, the traditional electronics industries can redistribute their objectives to comply the green electronics targets: low power consumption, low voltage-low size, low quantities of raw materials and resources—suitable to nanotechnologies or nanoelectronics, biomaterials in electronics, green organic semiconductors [4], long life products, electronics applied in ecology, solar cells development, green energy generators, green energy accumulators, nanoscale integrated electronics, hysteretic materials with memory property for smart electronics [5], integrated sensors and biosensors [6], environmental applications, sensors network, bio-medical-eco-electronics [7]. For instance, a recent ecological solution for integrated electronic biosensors follows a simultaneously 22 blood tests, concentrating 22 separate devices in one, using low quantities of blood samples, due to the revolutionary technology of dry biochemistry with minimal wastes, [8]. Also, the medical electronics have to take care in the next future to avoid not only the environment pollution or agglomeration with discarded equipments, but mainly to fulfill a green behavior face to the exposed human body.

Especially the Imagistics equipments that are extremely green with external environment, without wastes, without infected or contaminated rubbish, hardly interact with the human body, exposing at increased risk after multiple imagistic tests [9].

The general purpose products of low energy consumption as refrigerators, washing machines, laptops, etc. of A, A+, A+++ energetic class have an extraordinary success on market, offering advantage in the user pocket, but also consuming small resources from earth. Therefore, the green electronics must accompany the household goods industry, to produce extremely low power consumption components. Obviously, nanodevices that consume few femto-Watts are of primary interest, [10–12].

In the next sections, the integration technologies evolution and the electronic devices performances are selectively presented to meet these general green electronic demands. Some applications of nanomaterials cross over the electronic frontiers and provide multidisciplinary applications, briefly presented. Finally, some particular directions for the next future, in the field of the green electronics, are presented.

2. The integration technologies evolution

The nanotechnologies applied in integrated circuits give new challenge in nanometric scale structures, launching new applications or new components [13]. The traditional CMOS is more than nanoelectronics, passing rapidly from the 22 nm technology in 2012 to 10 nm technology in 2017 and toward 5 nm in 2020. Therefore, some authors claim that the future solutions require a diversification among nanocomponents, so that other devices than CMOS can restore or can be co-integrated together with CMOS circuitry to allow new functions, [14]. An extremely large palette of diversified devices is accomplished by the Silicon On Insulator (SOI) technologies [15]: from SOI-MOSFETs to radiation hardened circuits [16], up to micromachined NMEMS and sensors [17].

The classical High Temperature Annealing Separation by IMplanted OXygen (HTA SIMOX) technology still offers clean SOI wafers with 200 nm Si-film on 400 nm buried oxide (BOX), and fixed interface charges of $Q_{ox} = 10^{10} \div 10^{12}$ e/cm^2, [15]. These charges are dispersed inside a thin oxide slice. Any SOI device possesses two interfaces: Si-film with BOX, and BOX with Substrate and thirdly the superior interface near gate oxide with Si-film, [18]. The classical model considers the electric charge included in first two interfaces, [15]. These fixed charges are spatially expanded inside a volume in oxide. In ultrathin SOI structures, consequently this charges can be modeled by a surface charge density, [18].

There are some distinct methods of the electrical characterization of the SOI products. If the studied SOI transistor has an uniform film, thicker than 200 nm, the classical method can be applied. In this case, the effect of the interface charges is modeled by the classical physics by V_{FB-C}, [19]:

$$V_{FB-C} = -\frac{Q_{i1}}{\varepsilon_{ox}} \cdot x_{ox} - \frac{Q_{ox}}{2\,\varepsilon_{Si}\,qN_A} \tag{1}$$

where N_A is the same doping concentration in film and substrate, Q_{i1} is the electric charge densities at upper interface, Q_{ox} is the fixed charges density, x_{ox} is the thickness of the buried oxide, ε_{Si}, ε_{ox} are the dielectric permittivity respectively for silicon and for oxide, $V_{FB\text{-}C}$ is the classical model of the flat-band voltage. For a thick SOI film, the total charge density in BOX is $Q_{ox} = Q_{i1} + Q_{i2}$, where Q_{i1} and Q_{i2} are the upper, respectively bottom interface charge density.

If the SOI structure has Si-film thickness less than 10 nm, the sheet interface charge belongs to a space and can be treated by the distribution theory, [20]. Assuming the Dirac δ-distribution as a limit of the regulates distribution string, I_x, [21], where x_k is the spatial coordinate for Q_{ik}, k = 1 or 2 and $\Delta x_k \to 0$ stands for the spatial dispersion coefficients for Q_{i1}, Q_{i2}, the final flat-band model with distributions, V_{FB-D}, can be computed by:

$$V_{FB-D} = -\frac{Q_{i1}}{\varepsilon_{ox}} \cdot \left(x_{ox} - \frac{\Delta x_1}{2}\right) - \frac{Q_{i2}}{2\,\varepsilon_{ox}} \cdot \Delta x_2 - \frac{Q_{ox}^2}{2\,\varepsilon_{Si} \cdot qN_A} \tag{2}$$

For this model, if the spreading coefficients reset to zero ($\Delta x_{1,2} = 0$), the distribution (Eq. (2)) becomes the conventional (Eq. (1)).

The accurate model with distribution (Eq. (2)) shows that the effect of a fixed charges about 10^{12} e/cm^2, at the back interface can be neglected in a classical SOI-MOSFET with more than 200 nm Si/400 nm BOX sizes, but the same value is vital to characterize the SOI ultrathin technology of 10 nm Si/10 nm BOX.

3. Toward green electronic devices

Green electronic devices represent a new paradigm of recycling electronic nanodevices. Some revolutionary features are touched if bio-nanomaterials are used for integrated structures or combine organic semiconductors on organic insulators from non-toxic precursors for a green technological flow. Topic includes low voltage circuits and low size devices, recycling electronic bio-nanotechnologies, electronic re-conversion, solar cells as green energy provider and supra-capacitors as green accumulators and new solution of energy generation, coupled to almost zero electronic power consumption. Some devices reply to this demand, when we speak about Few—Electron Transistors or at limit the Single Electron Transistor that consumes current sub one electron per microsecond, possessing capacities sub 1atto-Farad, [22].

Some recent nanotechnologies could serve the green electronics purposes: Carbon Nano-Tube Field Effect Transistors (CNT-FET), [23], Nanowire-FETs, [24], Tunnel-FETs, Nanocore-shell technology for thin film transistors operated at 300 K temperature in white rooms, accompanied by low wastes by nanotechnologies, [25].

Also, the ULSI integrated circuits work at low voltages, providing low power consumption in electronics. Nanodevices with thin films or with one atomic layer exhibit confinement effects that decrease the conduction current. Currently the leading technology nodes are FinFET, [26] transistors that exploit raised inversion channels, multiplying the MOSFET capabilities.

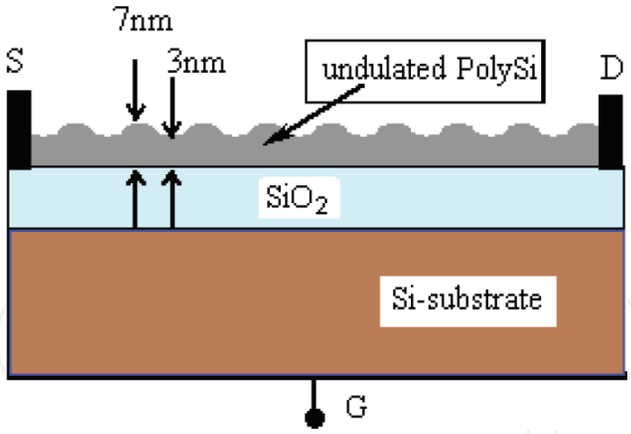

Figure 1. A manufactured SOI nanotransistor with maximum 7 nm.

Sometimes the SOI device studies go to other aims: devices suitable for high temperature work regime, micro-nanosensors, [27], low power consumption, atypical SOI-MOSFET transistors, [28]. Other materials than Silicon on insulator were also intensively approached in the last period, (e.g. Germanium on oxides thin layers). The germanium growth is starting from the silicon seed and continues by wetting the SiO2 film, producing mono-crystalline layers [29].

The Nothing On Insulator (NOI) transistor is another candidate to green electronic devices. Its technology can be rather based on room temperature processes. A sub-10 nm undulated polysilicon structure on insulator, [30] can be manufactured by the Secco etching that etches especially the boundaries of the polysilicon nanoclusters, providing nanoundulated films with top of 7 nm and valley of 3 nm thickness, **Figure 1**.

This undulation technology can be adapted for the NOI manufacturing, increasing the etching time, up to the Si valleys reaches the oxide. The NOI nanotransistor is a link device among vacuum transistors, SOI-MOSFETs, and Few Electron Transistors (FET), borrowing some characteristics from all of these, but being distinct.

In a mirror relation there is placed another representative of the SOI limit devices: the Silicon On Nothing transistor made by special etching techniques of the Si-membrane, [31].

4. Nanodevices based on SOI configuration of low consumption

The SOI structures stand for an alternative manufacturing technique for many nanodevices. An uniatomic semiconductor layer is able to be deposited onto an insulator support, since to be mechanical handled and to avoid the electrical leakage current thru substrate, [32].

When the film thickness is decreased sub-20 nm, a distinct nanostructure with a cavity was proposed. The upper source or drain zones that contain two higher undulations of the Si-n^+ layer are placed onto the oxide substrate. The middle Si-p region is thinned down to 1 nm and then to 0.3 nm. The carriers transport is constrained to one by one carrier for 0.3 nm structure. Essentially, the device could be conceived as a Single Electron Transistor type, at the theoretical

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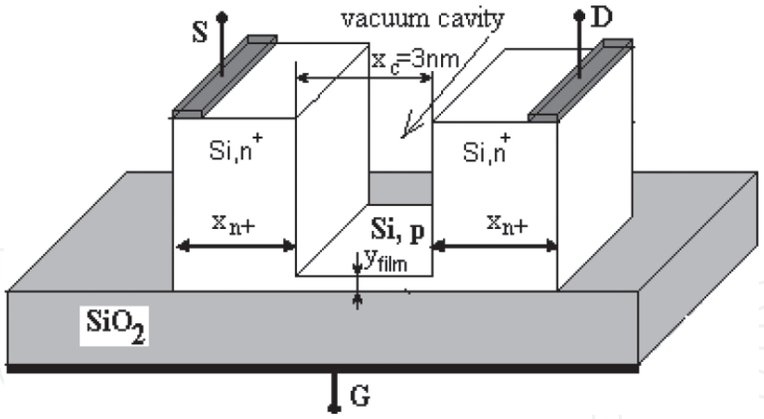

Figure 2. The conceptual architecture of the a-NOI nanotransistor sub-10 nm with a cavity.

limit. This cavity nanodevice is presented in **Figure 2** and can associate a green implementation technology, by undulated polysilicon film. In this case, just two high rectangular undulations of Silicon are preserved on the oxide layer. Therefore it was also called almost-NOI device, [33]. The substrate electrode acts as a back-gate terminal. Due to a vacuum distance under 4 nm ($x_c < 4$ nm), the tunneling probability between the islands - n^+ – source / n^+ – drain significantly increases, [34, 35].

Other recent research studies, in the field of the electron device with low power consumption, indicated an elevated interest for the pin devices as tunneling transistor or Tunnel-pin-FETs with extremely low sub-threshold slope, less than 60 mV/dec—the MOSFET physical limit, [36]. They are also based on the tunneling conduction mechanism, as a direct band to band tunneling, [37]. Other authors claimed in 2014 "Introducing the vacuum transistor: a device made of Nothing", "Transistorizing the Vacuum Tube", "A vacuum-channel transistor closely resembles an ordinary MOSFET", [38]. This NASA research group fabricated and measured a vacuum nanotransistor, [39]. However, this experimental device gets weaker performances (SS = 4 V/dec, V_{DS} = 20 V) versus the simulated NOI characteristics, [40, 41] (SS = 650 mV/dec, V_{DS} = 10 V). Obviously, the NOI nanotransistor has a similar work principle as these nanotransistors with vacuum that incited the international interest, [38].

5. Nanomaterial, smart biomaterials and organic electronics

One direction in the organic thin film transistor (OTFT) optimization consists in alternative OTFT technologies by new organic nanocomposites, selecting green routes.

A starting semiconductor of OTFT structure, suitable for optimization, is the pentacene. It posses the additional advantage to be already fully depicted inside the Atlas library. The simulated static characteristics prove the transistor effect, ensuring the drain current saturation, [42].

A special phenomenon observed by simulations is the volume conduction channel onset—a transport way that avoids interfaces vicinities, [43], **Figure 3a**. In an opposite manner, applying a low drain voltage, a weak conduction way occurs thru the channel, **Figure 3b**.

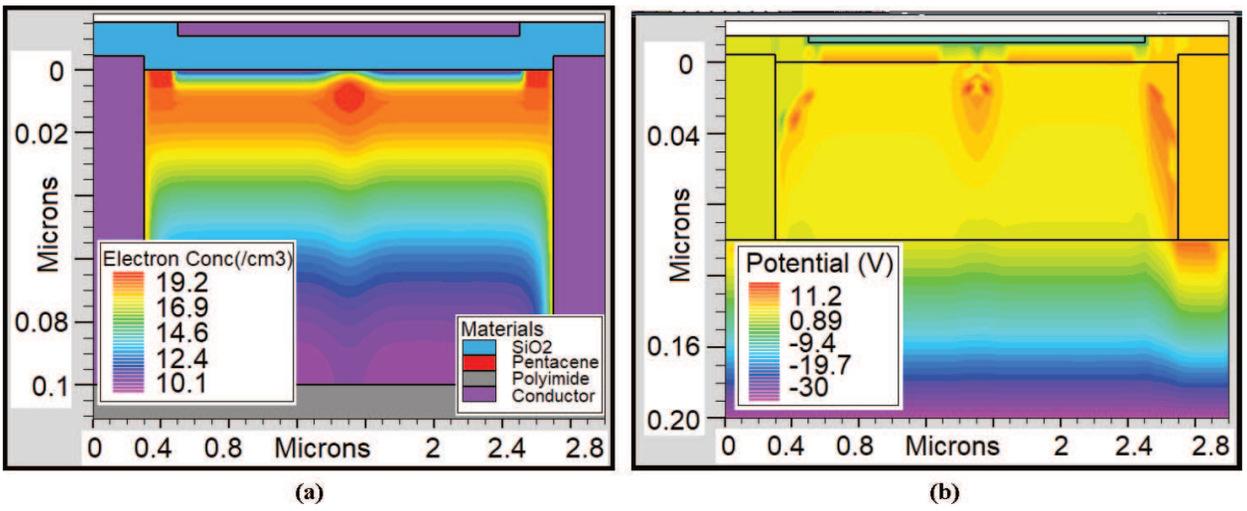

Figure 3. (a) The simulation results of a OTFT biased at $V_S = 0$ V, $V_D = 40$ V, $V_{TG} = -10$ V and $V_{BG} \leq 0$V, emphasizing the conduction by a volume electron conduction channel; (b) the potential distribution in OTFT biased at $V_S = 0$ V, $V_D = 4$ V, $V_{TG} = -10$ V and $V_{BG} = -30$ V emphasizing a weak conduction regime.

The optimization process is starting from simulation firstly and is passing to producing secondly some Organic-TFT transistors, fabricated at room temperatures, avoiding expensive white rooms. Also, their applications are useful in green industries, with the huge advantage of low cost, a high economical impact and green eco-technologies of fabrication. Traditional organic semiconductors based on polynuclear aromatic hydrocarbons like pentacene [44] are susceptible to processing problems related to the high toxicity/carcinogenic of the precursors [45]. Therefore, there are strongly envisaged OTFTs with green polymers grafted on the Nano-Core-Shells (NCS) structured materials or alternative nanocomposites, appealing to green chemistry synthesis routes.

For the experimental synthesis of semiconductors are considered those green polymers without carcinogenic precursors, suitable for multi-shell assembling on ferrite nanocore. A surface polymerization of polymer attaches a multi-shell structures of type Fe3O4 /Cu/Ag/Au-shell of stabilization-shell conductor polymer. The polymer grafting of the np's surface can be demonstrated by FT-IR and RAMAN tests.

On the other hand, the nanomaterials that are suitable to assemble smart bio-film, can be adapted to assemble organic semiconductors, too. In this sense, the Gold nanoparticles are very promising due to their applications, as catalysts, biosensing, photodynamic therapy, drugs delivery, and also in electronics [46]. The optoelectronics applicability occurs due to their quantum size effect, under the interaction between light and electrons onto the surface of the gold nanoparticles, [47]. Gold nanoparticles—AuNP - dendrimer structures match the therapeutic properties of AuNP with the dendrimers reactivity offering special properties for the cellular membrane transport.

6. Conclusions

The chapter presented a general vision on the nowadays green electronics products and technologies. The topic includes but not limited to low voltage circuits and low size devices,

recycling electronic, bio-nanotechnologies, electronic reconversion, solar cells, supra-capacitors, new solution of energy generation, coupled to almost zero electronic power consumption. Fortunately, the microelectronic technology evolves to nanotechnology that means lower sizes and by default the energy consumption decreases.

Among representatives, few promising candidates were touched: the SOI, NOI and SON transistors, the tunnel-FETs and vacuum nanotransistors. The targeted nanostructured materials for Organic Thin Film Transistors are green polymers attached to nanocomposite. From the green industry point of view, these OTFTs are associated with a room temperature technology, in absence of any expensive clean room.

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Conflict of interest

There is no conflict of interest.

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