We are IntechOpen, the world's leading publisher of Open Access books Built by scientists, for scientists

6,300

Open access books available

172,000

International authors and editors

190M

Downloads

Our authors are among the

154

Countries delivered to

TOP 1%

most cited scientists

12.2%

Contributors from top 500 universities

WEB OF SCIENCE™

Selection of our books indexed in the Book Citation Index
in Web of Science™ Core Collection (BKCI)

Interested in publishing with us?
Contact book.department@intechopen.com

Numbers displayed above are based on latest data collected.
For more information visit www.intechopen.com

Introductory Chapter: Green Electronics Starting from Nanotechnologies and Organic Semiconductors

Cristian Ravariu and Dan Eduard Mihaiescu

Additional information is available at the end of the chapter

<http://dx.doi.org/10.5772/intechopen.73312>

1. Introduction

Worldwide communities, governmental agencies or international research programs like Horizon2020 or Green Program2030, made huge concerted efforts to launch new visions in economy and society, [1]: green building, green cities, promoting the green transport development [2], eco-labels for logistics, green economy—bioeconomy, new green energy resources, network on bio-products, green and cost efficient aircraft design and not in the last time—smart, green and integrated electronics, [3]. The main pillar for a future green electronic industry is foreseen by the sustainable electronics that imply a feedback technological flow, to 99.99% reuse of the output products transformed in wastes, back to the input, as raw material. In this scope, new insights must be assimilated for a green factory vision: lifecycle of electronic technologies, recycling electronics, green energy convertors, electronic wastes reconversion new technologies, materials reconversion, mobile phones eco-rating and the list rests opened.

On the other hand, the traditional electronics industries can redistribute their objectives to comply the green electronics targets: low power consumption, low voltage-low size, low quantities of raw materials and resources—suitable to nanotechnologies or nanoelectronics, biomaterials in electronics, green organic semiconductors [4], long life products, electronics applied in ecology, solar cells development, green energy generators, green energy accumulators, nanoscale integrated electronics, hysteretic materials with memory property for smart electronics [5], integrated sensors and biosensors [6], environmental applications, sensors network, bio-medical-eco-electronics [7]. For instance, a recent ecological solution for integrated electronic biosensors follows a simultaneously 22 blood tests, concentrating 22 separate devices in one, using low quantities of blood samples, due to the revolutionary technology of dry biochemistry with minimal wastes, [8]. Also, the medical electronics have to take care in the next future to avoid not only the environment pollution or agglomeration with discarded equipments, but mainly to fulfill a green behavior face to the exposed human body.

Especially the Imagistics equipments that are extremely green with external environment, without wastes, without infected or contaminated rubbish, hardly interact with the human body, exposing at increased risk after multiple imagistic tests [9].

The general purpose products of low energy consumption as refrigerators, washing machines, laptops, etc. of A, A+, A+++ energetic class have an extraordinary success on market, offering advantage in the user pocket, but also consuming small resources from earth. Therefore, the green electronics must accompany the household goods industry, to produce extremely low power consumption components. Obviously, nanodevices that consume few femto-Watts are of primary interest, [10–12].

In the next sections, the integration technologies evolution and the electronic devices performances are selectively presented to meet these general green electronic demands. Some applications of nanomaterials cross over the electronic frontiers and provide multidisciplinary applications, briefly presented. Finally, some particular directions for the next future, in the field of the green electronics, are presented.

2. The integration technologies evolution

The nanotechnologies applied in integrated circuits give new challenge in nanometric scale structures, launching new applications or new components [13]. The traditional CMOS is more than nanoelectronics, passing rapidly from the 22 nm technology in 2012 to 10 nm technology in 2017 and toward 5 nm in 2020. Therefore, some authors claim that the future solutions require a diversification among nanocomponents, so that other devices than CMOS can restore or can be co-integrated together with CMOS circuitry to allow new functions, [14]. An extremely large palette of diversified devices is accomplished by the Silicon On Insulator (SOI) technologies [15]: from SOI-MOSFETs to radiation hardened circuits [16], up to micro-machined NMEMS and sensors [17].

The classical High Temperature Annealing Separation by IMplanted OXygen (HTA SIMOX) technology still offers clean SOI wafers with 200 nm Si-film on 400 nm buried oxide (BOX), and fixed interface charges of $Q_{ox} = 10^{10} \div 10^{12} \text{ e/cm}^2$, [15]. These charges are dispersed inside a thin oxide slice. Any SOI device possesses two interfaces: Si-film with BOX, and BOX with Substrate and thirdly the superior interface near gate oxide with Si-film, [18]. The classical model considers the electric charge included in first two interfaces, [15]. These fixed charges are spatially expanded inside a volume in oxide. In ultrathin SOI structures, consequently this charges can be modeled by a surface charge density, [18].

There are some distinct methods of the electrical characterization of the SOI products. If the studied SOI transistor has an uniform film, thicker than 200 nm, the classical method can be applied. In this case, the effect of the interface charges is modeled by the classical physics by $V_{FB-C'}$ [19]:

$$V_{FB-C'} = -\frac{Q_{it}}{\epsilon_{ox}} \cdot x_{ox} - \frac{Q_{ox}}{2 \epsilon_{Si} q N_A} \quad (1)$$

where N_A is the same doping concentration in film and substrate, Q_{i1} is the electric charge densities at upper interface, Q_{ox} is the fixed charges density, x_{ox} is the thickness of the buried oxide, ϵ_{Si} , ϵ_{ox} are the dielectric permittivity respectively for silicon and for oxide, V_{FB-C} is the classical model of the flat-band voltage. For a thick SOI film, the total charge density in BOX is $Q_{ox} = Q_{i1} + Q_{i2}$, where Q_{i1} and Q_{i2} are the upper, respectively bottom interface charge density.

If the SOI structure has Si-film thickness less than 10 nm, the sheet interface charge belongs to a space and can be treated by the distribution theory, [20]. Assuming the Dirac δ -distribution as a limit of the regulates distribution string, I_x , [21], where x_k is the spatial coordinate for Q_{ik} , $k = 1$ or 2 and $\Delta x_k \rightarrow 0$ stands for the spatial dispersion coefficients for Q_{i1} , Q_{i2} , the final flat-band model with distributions, V_{FB-D} , can be computed by:

$$V_{FB-D} = -\frac{Q_{i1}}{\epsilon_{ox}} \cdot \left(x_{ox} - \frac{\Delta x_1}{2} \right) - \frac{Q_{i2}}{2 \epsilon_{ox}} \cdot \Delta x_2 - \frac{Q_{ox}^2}{2 \epsilon_{Si} \cdot q N_A} \quad (2)$$

For this model, if the spreading coefficients reset to zero ($\Delta x_{1,2} = 0$), the distribution (Eq. (2)) becomes the conventional (Eq. (1)).

The accurate model with distribution (Eq. (2)) shows that the effect of a fixed charges about 10^{12} e/cm², at the back interface can be neglected in a classical SOI-MOSFET with more than 200 nm Si/400 nm BOX sizes, but the same value is vital to characterize the SOI ultrathin technology of 10 nm Si/10 nm BOX.

3. Toward green electronic devices

Green electronic devices represent a new paradigm of recycling electronic nanodevices. Some revolutionary features are touched if bio-nanomaterials are used for integrated structures or combine organic semiconductors on organic insulators from non-toxic precursors for a green technological flow. Topic includes low voltage circuits and low size devices, recycling electronic bio-nanotechnologies, electronic re-conversion, solar cells as green energy provider and supra-capacitors as green accumulators and new solution of energy generation, coupled to almost zero electronic power consumption. Some devices reply to this demand, when we speak about Few—Electron Transistors or at limit the Single Electron Transistor that consumes current sub one electron per microsecond, possessing capacities sub 1atto-Farad, [22].

Some recent nanotechnologies could serve the green electronics purposes: Carbon Nano-Tube Field Effect Transistors (CNT-FET), [23], Nanowire-FETs, [24], Tunnel-FETs, Nanocore-shell technology for thin film transistors operated at 300 K temperature in white rooms, accompanied by low wastes by nanotechnologies, [25].

Also, the ULSI integrated circuits work at low voltages, providing low power consumption in electronics. Nanodevices with thin films or with one atomic layer exhibit confinement effects that decrease the conduction current. Currently the leading technology nodes are FinFET, [26] transistors that exploit raised inversion channels, multiplying the MOSFET capabilities.

Figure 1. A manufactured SOI nanotransistor with maximum 7 nm.

Sometimes the SOI device studies go to other aims: devices suitable for high temperature work regime, micro-nanosensors, [27], low power consumption, atypical SOI-MOSFET transistors, [28]. Other materials than Silicon on insulator were also intensively approached in the last period, (e.g. Germanium on oxides thin layers). The germanium growth is starting from the silicon seed and continues by wetting the SiO₂ film, producing mono-crystalline layers [29].

The Nothing On Insulator (NOI) transistor is another candidate to green electronic devices. Its technology can be rather based on room temperature processes. A sub-10 nm undulated polysilicon structure on insulator, [30] can be manufactured by the Secco etching that etches especially the boundaries of the polysilicon nanoclusters, providing nanoundulated films with top of 7 nm and valley of 3 nm thickness, **Figure 1**.

This undulation technology can be adapted for the NOI manufacturing, increasing the etching time, up to the Si valleys reaches the oxide. The NOI nanotransistor is a link device among vacuum transistors, SOI-MOSFETs, and Few Electron Transistors (FET), borrowing some characteristics from all of these, but being distinct.

In a mirror relation there is placed another representative of the SOI limit devices: the Silicon On Nothing transistor made by special etching techniques of the Si-membrane, [31].

4. Nanodevices based on SOI configuration of low consumption

The SOI structures stand for an alternative manufacturing technique for many nanodevices. An uniaxial semiconductor layer is able to be deposited onto an insulator support, since it can be mechanically handled and to avoid the electrical leakage current through the substrate, [32].

When the film thickness is decreased sub-20 nm, a distinct nanostructure with a cavity was proposed. The upper source or drain zones that contain two higher undulations of the Si-n⁺ layer are placed onto the oxide substrate. The middle Si-p region is thinned down to 1 nm and then to 0.3 nm. The carrier transport is constrained to one by one carrier for 0.3 nm structure. Essentially, the device could be conceived as a Single Electron Transistor type, at the theoretical

Figure 2. The conceptual architecture of the a-NOI nanotransistor sub-10 nm with a cavity.

limit. This cavity nanodevice is presented in **Figure 2** and can associate a green implementation technology, by undulated polysilicon film. In this case, just two high rectangular undulations of Silicon are preserved on the oxide layer. Therefore it was also called almost-NOI device, [33]. The substrate electrode acts as a back-gate terminal. Due to a vacuum distance under 4 nm ($x_c < 4$ nm), the tunneling probability between the islands - n^+ – source / n^+ – drain significantly increases, [34, 35].

Other recent research studies, in the field of the electron device with low power consumption, indicated an elevated interest for the pin devices as tunneling transistor or Tunnel-pin-FETs with extremely low sub-threshold slope, less than 60 mV/dec—the MOSFET physical limit, [36]. They are also based on the tunneling conduction mechanism, as a direct band to band tunneling, [37]. Other authors claimed in 2014 “Introducing the vacuum transistor: a device made of Nothing”, “Transistorizing the Vacuum Tube”, “A vacuum-channel transistor closely resembles an ordinary MOSFET”, [38]. This NASA research group fabricated and measured a vacuum nanotransistor, [39]. However, this experimental device gets weaker performances ($SS = 4$ V/dec, $V_{DS} = 20$ V) versus the simulated NOI characteristics, [40, 41] ($SS = 650$ mV/dec, $V_{DS} = 10$ V). Obviously, the NOI nanotransistor has a similar work principle as these nanotransistors with vacuum that incited the international interest, [38].

5. Nanomaterial, smart biomaterials and organic electronics

One direction in the organic thin film transistor (OTFT) optimization consists in alternative OTFT technologies by new organic nanocomposites, selecting green routes.

A starting semiconductor of OTFT structure, suitable for optimization, is the pentacene. It poses the additional advantage to be already fully depicted inside the Atlas library. The simulated static characteristics prove the transistor effect, ensuring the drain current saturation, [42].

A special phenomenon observed by simulations is the volume conduction channel onset—a transport way that avoids interfaces vicinities, [43], **Figure 3a**. In an opposite manner, applying a low drain voltage, a weak conduction way occurs thru the channel, **Figure 3b**.

Figure 3. (a) The simulation results of a OTFT biased at $V_s = 0$ V, $V_D = 40$ V, $V_{TG} = -10$ V and $V_{BG} \leq 0$ V, emphasizing the conduction by a volume electron conduction channel; (b) the potential distribution in OTFT biased at $V_s = 0$ V, $V_D = 4$ V, $V_{TG} = -10$ V and $V_{BG} = -30$ V emphasizing a weak conduction regime.

The optimization process is starting from simulation firstly and is passing to producing secondly some Organic-TFT transistors, fabricated at room temperatures, avoiding expensive white rooms. Also, their applications are useful in green industries, with the huge advantage of low cost, a high economical impact and green eco-technologies of fabrication. Traditional organic semiconductors based on polynuclear aromatic hydrocarbons like pentacene [44] are susceptible to processing problems related to the high toxicity/carcinogenic of the precursors [45]. Therefore, there are strongly envisaged OTFTs with green polymers grafted on the Nano-Core-Shells (NCS) structured materials or alternative nanocomposites, appealing to green chemistry synthesis routes.

For the experimental synthesis of semiconductors are considered those green polymers without carcinogenic precursors, suitable for multi-shell assembling on ferrite nanocore. A surface polymerization of polymer attaches a multi-shell structures of type Fe₃O₄ /Cu/Ag/Au-shell of stabilization-shell conductor polymer. The polymer grafting of the np's surface can be demonstrated by FT-IR and RAMAN tests.

On the other hand, the nanomaterials that are suitable to assemble smart bio-film, can be adapted to assemble organic semiconductors, too. In this sense, the Gold nanoparticles are very promising due to their applications, as catalysts, biosensing, photodynamic therapy, drugs delivery, and also in electronics [46]. The optoelectronics applicability occurs due to their quantum size effect, under the interaction between light and electrons onto the surface of the gold nanoparticles, [47]. Gold nanoparticles—AuNP - dendrimer structures match the therapeutic properties of AuNP with the dendrimers reactivity offering special properties for the cellular membrane transport.

6. Conclusions

The chapter presented a general vision on the nowadays green electronics products and technologies. The topic includes but not limited to low voltage circuits and low size devices,

recycling electronic, bio-nanotechnologies, electronic reconversion, solar cells, supra-capacitors, new solution of energy generation, coupled to almost zero electronic power consumption. Fortunately, the microelectronic technology evolves to nanotechnology that means lower sizes and by default the energy consumption decreases.

Among representatives, few promising candidates were touched: the SOI, NOI and SON transistors, the tunnel-FETs and vacuum nanotransistors. The targeted nanostructured materials for Organic Thin Film Transistors are green polymers attached to nanocomposite. From the green industry point of view, these OTFTs are associated with a room temperature technology, in absence of any expensive clean room.

Acknowledgements

This work was developed by a grant of Ministry of Research and Innovation, CNCS - UEFISCDI, project number PN-III-P4-ID-PCE-2016-0480, within PNCDI III, project number 4/2017, acronym TFTNANOEL.

Conflict of interest

There is no conflict of interest.

Author details

Cristian Ravariu^{1*} and Dan Eduard Mihaiescu²

*Address all correspondence to: cristian.ravariu@upb.ro

1 Faculty of Electronics Telecommunications and Information Technology, Department of Electronic Device, Circuits and Architectures, Group of Biodevices and Nanoelectronics of Cells, "Politehnica" University of Bucharest, Bucharest, Romania

2 Faculty of Applied Chemistry and Material Science, Department of Organic Chemistry, "Costin Nenițescu", Politehnica University of Bucharest, Bucharest, Romania

References

- [1] European Commission Strategies [Internet]. 2017. Available from: http://ec.europa.eu/geninfo/query/action?query_source=RESEARCHPP&swlang=en&QueryText=green [Accessed: 2017-10-25]
- [2] Kitthamkesorn S, Chen A. Alternate weibit-based model for assessing green transport systems with combined mode and route travel choices. *Transportation Research Part B: Methodological* – Elsevier. 2017;**103**(9):291-310. DOI: 10.1016/j.trb.2017.04.011

- [3] Zhu H, Luo W, Ciesielski P, Fang Z, Zhu JY, Henriksson G, Himmel ME, Hu L. Wood-derived materials for green electronics, biological devices and energy applications. *Chemical Reviews - American Chemical Society*. 2016;**116**(16):9305-9374. DOI: 10.1021/acs.chemrev.6b00225
- [4] Faurie A, Grolleau J, Gohier F, Allain M, Legoupy S, Frère P. Toward sustainable organic semiconductors from a broad palette of green reactions. *European Journal of Organic Chemistry*. 2017;**2017**(19):2707-2714. DOI: 10.1002/ejoc.201700317
- [5] Ionescu AM, Lattanzio L, Salvatore GA, Michielis LD, Boucart K, Bouvet D. The hysteretic ferroelectric tunnel FET. *IEEE Transactions on Electron Devices*. 2010;**57**(12):3518-3524. DOI: 10.1109/TED.2010.2079531
- [6] Ravariu C, Manea E, Babarada F. Masks and metallic electrodes compounds for silicon biosensor integration. *Journal of Alloys and Compounds, Elsevier*. 2017;**697**:72-79. DOI: 10.1016/j.jallcom.2016.12.099
- [7] Bondarciuc A, Ravariu C, Bondarciuc V, Alecu G. Non-polluting medical technology for environment and patient used in inflammatory diseases monitoring. *Environmental Engineering and Management Journal*. 2015;**14**(4):763-768. DOI: 10.1015/eemj.2015.12.012
- [8] SPOTCHEM EZ SP-4430 [Internet]. 2017. Available from: <http://www.tehnoindustrial.ro/toate-produsele/automated-analyzer-for-clinical-chemistry-spotchem-ez-sp-4430.html> [Accessed: 2017-10-24]
- [9] Dobrescu L, Radulescu GC. Radiation dose risk and diagnostic benefit in imaging investigations. *American Journal of Bioscience and Bioengineering*. 2015;**3**(3-1):22-26. DOI: 10.11648/j.bio.s.2015030301.11
- [10] Ravariu C. Gate swing improving for the nothing on insulator transistor in weak tunneling. *IEEE Transactions on Nanotechnology*. 2017:1-8, Early access paper. DOI: 10.1109/TNANO.2017.2764802
- [11] Poljak M, Suligoj T. Quantum transport analysis of conductance variability in graphene nanoribbons with edge defects. *IEEE Transactions on Electron Devices*. 2016;**63**(2):537-543. DOI: 10.1109/TED.2015.2505003
- [12] Ravariu C, Babarada F. Resizing and reshaping of the nothing on insulator NOI transistor. *Advanced Nano-Bio-Materials and Devices*. 2017;**1**(1):18-23
- [13] Ray SK. Core-shell Ge nanowires and heterojunctions for memory and photodetector devices. In: *Proceedings of the IEEE International Conference on Computers and Devices for Communication (CODEC'09)*; 14-16 December 2009; Kolkata. India; 2009. pp. 1-2
- [14] Deleonibus S. CMOS nanoelectronics at the time of diversifications. In: *Proceedings of the International Symposium on VLSI Technology Systems and Applications (VLSI-TSA'11)*; 25-27 April 2011; Hsinchu. Japan; 2011. pp. 1-2
- [15] Cristoloveanu S, Li SS. *Electrical Characterization of Silicon-on-Insulator Materials and Devices*. 1st ed. New York: Kluwer Academic Publishers: Springer; 1995. p. 373. ISBN 978-1-4615-2245-4

- [16] Placinta VM, Cojocariu LN, Ravariu C. Test bench design for radiation tolerance of two ASICs. *Romanian Reports in Physics*. 2017;**69**(903):1-12
- [17] Ravariu C, Alecu LG, Bondarciuc A, Babarada F. Advanced SOI semiconductor structures for micro-dose biological samples handling. *Journal of Optoelectronics and Advanced Materials – Rapid Communications*. 2010;**4**(9):1375-1378
- [18] Ravariu C, Babarada F. Modeling and simulation of special shaped SOI materials for the nanodevices implementation. *Journal of Nanomaterials - Hindawi*. 2011;**792759**:1-11. DOI: 10.1155/2011/792759
- [19] Ravariu C, Babarada F, Rusu A. More accurate models of the interfaces oxide ultra-thin SOI films. *AIP Conference Proceedings from American Institute of Physics*. 2007;**893**:3-4. DOI: 10.1063/1.2729741
- [20] Ravariu C, Rusu A, Ravariu F. Interface electric charge modeling and characterization with δ distribution generator strings in thin SOI films. *Microelectronics*. 2006;**37**(3):943-947. DOI: 10.1016/j.mejo.2006.01.018
- [21] Quijano N, Passino KM. The ideal free distribution: Theory and engineering application. *Systems, Man, and Cybernetics Part B: IEEE Transactions on Cybernetics*. 2007;**37**(1):154-165. DOI: 10.1109/TSMCB.2006.880134
- [22] Kumar A, Dubey D. Single electron transistor: Applications and limitations. *Advance in Electronic and Electric Engineering*. 2013;**3**(1):57-62
- [23] Morishita K, Fujita K, Kakei R, Furuki H, Okada T. Carbon nanotube sheets used in field-emission lamps with vacuum-sealed diode structures. *Fullerenes, Nanotubes, and Carbon Nanostructures*. 2016;**24**(5):293-297. DOI: 10.1080/1536383X.2016.1154048
- [24] Kang TK, Yang YY, Chien FT. Poly Si nanowire thin film transistors with vacuum gap design. *IEEE Transactions on Electron Devices*. 2014;**61**(6):2113-2118. DOI: 10.1109/TED.2014.2318706
- [25] Barraud S, Hartmann JM, Maffini-Alvaro V, Tosti L, Delaye V, Lafond D. Top-down fabrication of epitaxial SiGe/Si multi-(Core/Shell) p-FET nanowire transistors. *IEEE Transactions On Electron Devices*. 2014;**61**(4):953-960. DOI: 10.1109/TED.2014.2306232
- [26] Huang YC, Chiang MH, Wang SJ, Fossum JG. GAAFET versus pragmatic FinFET at the 5nm Si-based CMOS technology node. *IEEE Journal of the Electron Devices Society*. 2017;**5**(3):164-169. DOI: 10.1109/JEDS.2017.2689738
- [27] Ravariu C, Ravariu F, Rusu A, Dobrescu D, Dobrescu L. The modeling of a SOI mechanical sensor. In: *Proceedings of the IEEE International Conference (SISPAD'01)*. 11-13 September 2001, Athens, Greece; 2001. pp. 328-331
- [28] Numata T, Takagi S. Device design for subthreshold slope and threshold voltage control in sub-100-nm fully depleted SOI MOSFETs. *IEEE Transactions on Electron Devices*. 2004;**51**(12):2161-2167. DOI: 10.1109/TED.2004.839760
- [29] Cammilleri VD, Yam V, Fossard F, Renard C, Bouchier D, Zheng Y, Fazzini PF, Houdellier F, Hÿtch M. Lateral growth of monocrystalline Ge on silicon oxide by ultrahigh vacuum

- chemical vapor deposition. *Materials Science in Semiconductor Processing* - Elsevier. 2008;**11**(5):214-216. DOI: 10.1016/j.mssp.2008.07.003
- [30] Badila D, Ecoffey S, Bouvet D, Ionescu AM. A study of fabrication technique for sub 10-nm thin undulated polysilicon films. In: *Proceedings of the IEEE International Conference Annual of Semiconductors (CAS'03)*. 9-12 Oct. 2003, Sinaia, Romania; 2003. pp. 95-98
- [31] Durand C, Casset F, Renaux P, Abele N, Legrand B, Renaud D, Ollier E, Ancey P, Ionescu AM, Buchaillot L. In-plane silicon-on-nothing nanometer-scale resonant suspended gate MOSFET for in-IC integration perspectives. *Electron Device Letters IEEE*. 2008;**29**(5):494-496. DOI: 10.1109/LED.2008.919781
- [32] Johnson RW, Hultqvist A, Bent SF. A brief review of atomic layer deposition: From fundamentals to applications. *Materials Today*. 2014;**17**(5):236-246. DOI: 10.1016/j.mattod.2014.04.026
- [33] Ravariu C. Field Effect Transistors with a Cavity on Insulator, NOI and a-NOI. Romanian Patent Number: RO126811-A0, OSIM, Romania, Aug; 2013
- [34] Forbes RG. Description of field emission current/voltage characteristics in terms of scaled barrier field values (f-values). *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*. 2008;**26**(209):187-195. DOI: 10.1116/1.2834563
- [35] Ravariu C, Rusu A, Profirescu M, Ravariu F. A Nano-Transistor with a Cavity. In: *Proceedings of the International Conference Nanotech-Microsystems (MSM'05)*. 1-3 April 2005, Anaheim, SUA, vol. 1, cap. 4; 2005. pp. 111-114
- [36] Liu L, Mohata D, Datta S. Scaling length theory of double-gate Interband tunnel field-effect transistors. *IEEE Transactions on Electron Devices*. 2012;**59**(4):902-909. DOI: 10.1109/TED.2012.2183875
- [37] Koswatta SO, Lundstrom MS, Nikonov DE. Performance comparison between p-i-n tunneling transistors and conventional MOSFETs. *IEEE Transactions on Electron Devices*. 2009;**56**(3):456-465. DOI: 10.1109/TED.2008.2011934
- [38] Han J, Meyyappan M. Introducing the vacuum transistor: A device made of nothing. *IEEE Spectrum*. 2014;**51**:25-29
- [39] Han J, Oh J, Meyyappan M. Vacuum nanoelectronics: Back to the future?-gate insulated nanoscale vacuum channel transistor. *Applied Physics Letters*. 2012;**100**(213505):1-4. DOI: 10.1063/1.4717751
- [40] Ravariu C. Compact NOI Nano-device simulation. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*. 2014;**22**(8):1841-1844. DOI: 10.1109/TVLSI.2013.2278474
- [41] Ravariu C. Semiconductor materials optimization for a TFET device with nothing region on insulator. *IEEE Transactions on Semiconductor Manufacturing*. 2013;**26**(3):406-413. DOI: 10.1109/TSM.2013.2258411
- [42] Ravariu C, Dragomirescu D. Different work regimes of an organic thin film transistor OTFT and possible applications in bioelectronics. *American Journal of Bioscience and Bioengineering*. 2015;**3**(3-1):7-13. DOI: 10.11648/j.bio.s.2015030301.12

- [43] Ravariu C, Dragomirescu D, Babarada F, Prelipceanu D, Patrichi B, Gorciu C, Manuc D, Salageanu A. Organic Field Effect Transistor OFET Optimization Considering Volume Channel Conduction Mechanism. In Proceedings of the IEEE International Conference Annual Conference of Semiconductors, (CAS'15), 12-14 October 2015, Sinaia, Romania; 2015. pp. 113-117
- [44] Yang D. Pentacene-based photodetector in visible region with vertical field-effect transistor configuration. IEEE Photonics Technology Letters. 2015;**27**(3):233-236. DOI: 10.1109/LPT.2014.2365498
- [45] Luch A, Baird WM. Carcinogenic Polycyclic Aromatic Hydrocarbons. Comprehensive Toxicology. 2nd ed. Amsterdam: Elsevier; 2010. p. 123
- [46] Daniel MC, Astruc D. Gold nanoparticles: Assembly, supramolecular chemistry, quantum-size-related properties, and applications toward biology, catalysis, and nanotechnology. Chemical Reviews. 2004;**104**(1):293-346. DOI: 10.1021/cr030698+
- [47] Bolocan A, Mihaiescu DE, Meșterca AR, Spirescu VA, Tote EM, Mogoantă L, Mogoșanu GD, Grumezescu AM. In vitro and in vivo applications of 3D dendritic gold nanostructures. Romanian Journal of Morphology and Embryology. 2015;**56**(3):915-924. PMID 26662123

IntechOpen