Chapter 5

Dual-Inverter Circuit Topologies for Supplying Open-Ended Loads

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Additional information is available at the end of the chapter

http://dx.doi.org/10.5772/intechopen.68450

Abstract

Power electronic converters are nowadays the most suitable solution to provide a variable voltage/current in industry. The most commonly used power converter is the three-phase two-level voltage source inverter which transforms a direct-current input voltage into alternating-current output voltage with adjustable magnitude and frequency. Power inverters are used to supply three-phase loads which are typically connected in wye or delta configurations. However, in previous years, a type of connection consisting on leaving both terminal ends of the load opened has been studied as an alternative to standard wye or delta connection. To supply loads with this type of connection, two power inverters (one at each terminal end of the load) are required in a circuit topology called dual-inverter. In this chapter, a general study of the dual-inverter topology is presented. The advantages and issues of such converter are studied and different modulation strategies are shown and discussed. Moreover, multilevel dual-inverter converters are presented as an extension to the basic two-level idea. For evaluation purposes, simulations results are presented.

Keywords: voltage source inverter, dual-inverter, open-end winding, pulse width modulation

1. Introduction

In industrial applications, typical loads generally require to be supplied with alternating voltage of variable magnitude and frequency. To produce such voltages, power electronic converters are nowadays the standard and more suitable solution. The most commonly used power converter

is the three-phase two-level voltage source inverter (VSI) which transforms a DC input voltage into AC output voltage with adjustable magnitude and frequency (**Figure 1**) [1, 2]. Three-phase VSIs typically supply loads connected in delta (called closed connection) or in wye (called semi-closed connection) (**Figure 2**), depending on the load requirements of voltage and current.

Regarding the VSI, to produce an AC output voltage, a modulation scheme should be used. The carrier-based pulse width modulation (PWM) strategy is a standard modulation technique for power inverters [2] where a triangular (carrier) signal v_{tri} is compared with a sinusoidal (reference) signal v_{ref}, as shown in **Figure 3**. The following control logic is used to generate the VSI-IGBTs gate pulses:

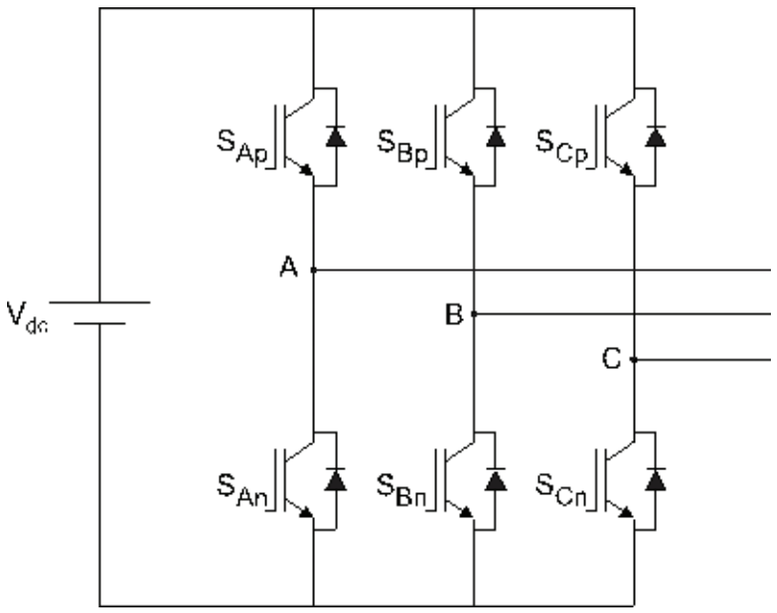

Figure 1. Two-level voltage source inverter.

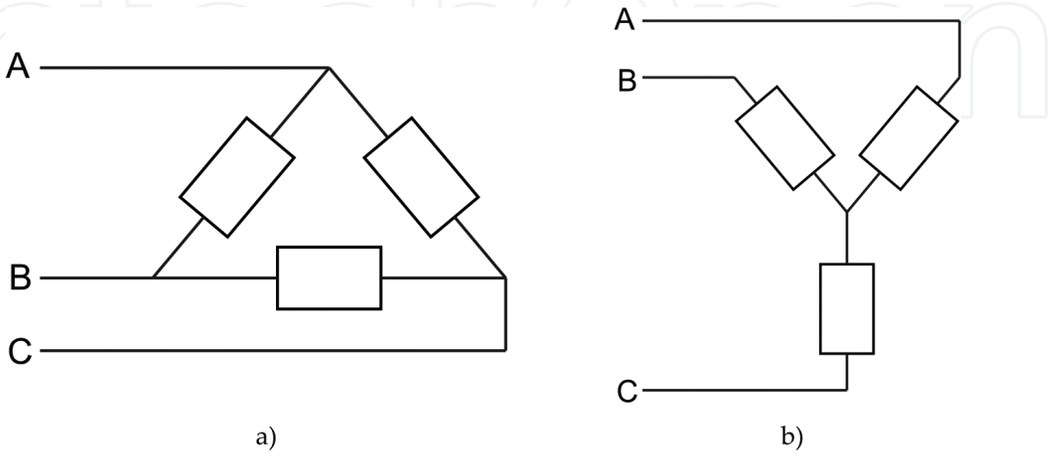

Figure 2. (a) Delta connection and (b) wye connection.

$$v_{ref} \geq v_{tri} \Rightarrow S_{xp} = 1$$
$$v_{ref} < v_{tri} \Rightarrow S_{xp} = 0$$

where S_{xp} with $x = A, B, C$ is an upper switch of the inverter.

To modulate the three legs of the inverter, three sinusoidal reference signals are required of equal magnitude and frequency but phase shift 120°.

The other standard PWM strategy for three-phase VSIs is the space vector modulation (SVM) where the possible switching states of the inverter are expressed as space vectors (**Table 1**) which when represented graphically form a hexagon divided in six sectors (**Figure 4**). The reference vector (v_{ref}) that represents the desired output voltage of the VSI should be synthetized using the available switching states in a sector [2].

To apply the switching states of the inverter, the following duty cycles are considered for the active vectors [1]:

$$d_\alpha = m \cdot \sin\left(\frac{\pi}{3} - \theta_{ref,o}\right), \; d_\beta = m \cdot \sin\left(\theta_{ref,o}\right) \tag{1}$$

where $\theta_{ref,o}$ is the angle of the output reference voltage vector and m is a modulation index.

The duty cycle of the zero vectors is given by

$$d_0 = 1 - d_\alpha - d_\beta \tag{2}$$

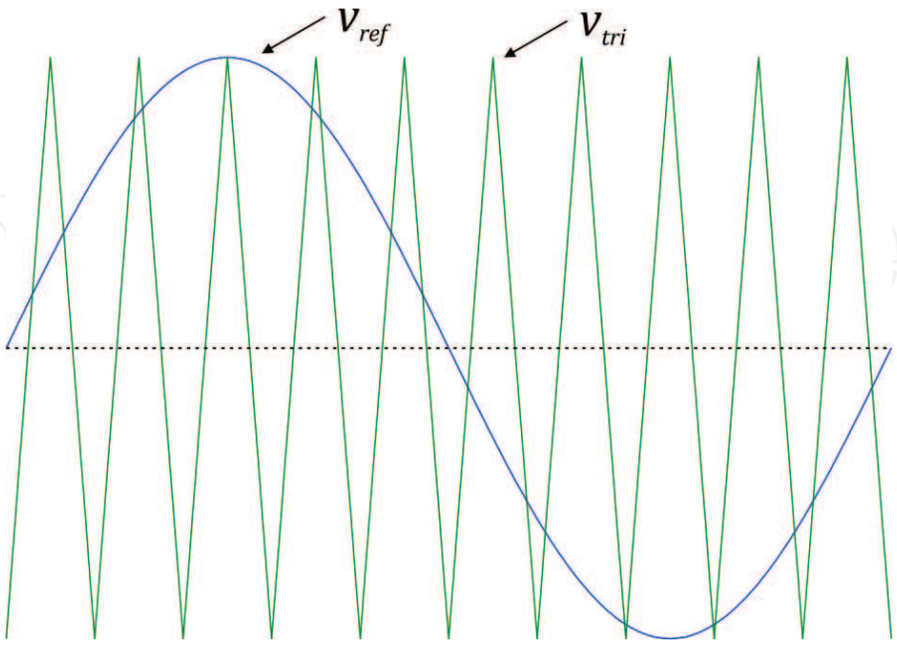

Figure 3. Signals used in a carrier-based modulation strategy (one leg of the inverter).

States of inverter $[S_A S_B S_C]$			
$V_1 = [100]$	$V_2 = [110]$	$V_3 = [010]$	$V_4 = [011]$
$V_5 = [001]$	$V_6 = [101]$	$V_7 = [111]$	$V_8 = [000]$

Table 1. Switching vectors of a VSI.

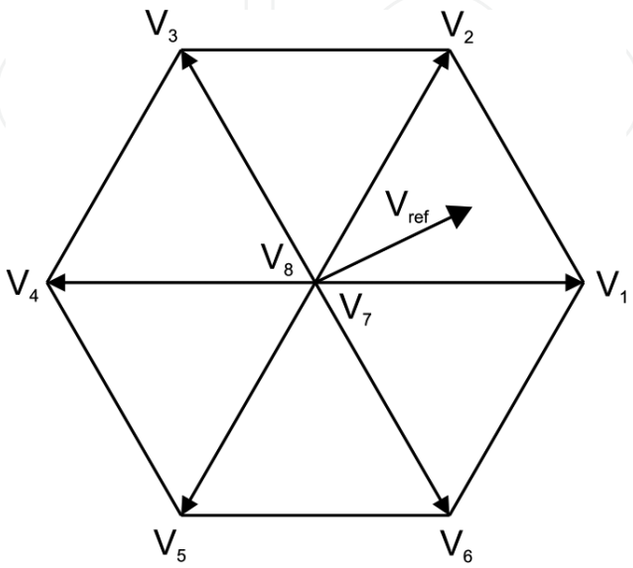

Figure 4. Graphic representation of the switching vectors.

A representation of the switching sequence in a switching period for each leg of the VSI is shown in **Figure 5**. As can be noted, the switching sequence aims to change the state of one switch at a time, then reducing the switching losses of the inverter.

Independent of the modulation strategy used, the standard two-level VSI supplying delta- or wye-connected loads has been widely studied for years and is a well-known and reliable engineering solution in the industry. However, in previous years, a type of connection consisting on leaving both terminal ends of the load opened has been studied as an alternative to standard wye or delta connection (**Figure 6**). To supply loads with this type of connection, two VSIs are required in a circuit topology called dual-inverter [1]. The dual-inverter circuit can be supplied by isolated DC sources (**Figure 7**) [3, 4] or by a single DC source (**Figure 8**) [5, 6]. It can be noted that when supplying the dual-inverter with a single DC source is equivalent to supplying each phase load with a single-phase VSI (H-bridge), hence the modulation scheme could be unipolar or bipolar [2].

Open-ended load connection offers certain advantages compared to wye or delta connections, such as [7, 8]:

- Equal power input from both sides of the load; thus, each VSI is rated at half the load power rating.
- Each load phase current can be controlled independently.

- Possibility to have twice the effective switching frequency (depending on the modulation strategy).
- Possibility of reducing the common-mode voltage (CMV).
- Extensible to more phases, therefore multiphase loads can be considered if current reduction is required.

However, an open-ended load can have some drawbacks, such as:

- Possibility of zero sequence current flowing in the machine because of the occurrence of zero sequence voltage (ZSV).
- More complex power converter requirements, i.e. more power devices, circuit gate drives, etc.
- Complexity could affect the reliability.
- Greater weight and volume of the power converter.

When using two isolated DC sources to supply a dual-inverter (**Figure 7**), the main feature is that the circulation of zero sequence current is avoided due to the circuit configuration; therefore, the focus should be in reducing the common-mode voltage. Nevertheless, this topology requires two isolated DC sources which means two isolation transformers, increasing the cost and volume of the converter.

Several articles have been published with the use of this circuit configuration. For instance, Ref. [3] proposes a voltage harmonic suppression scheme for the dual-inverter, whereby selecting a

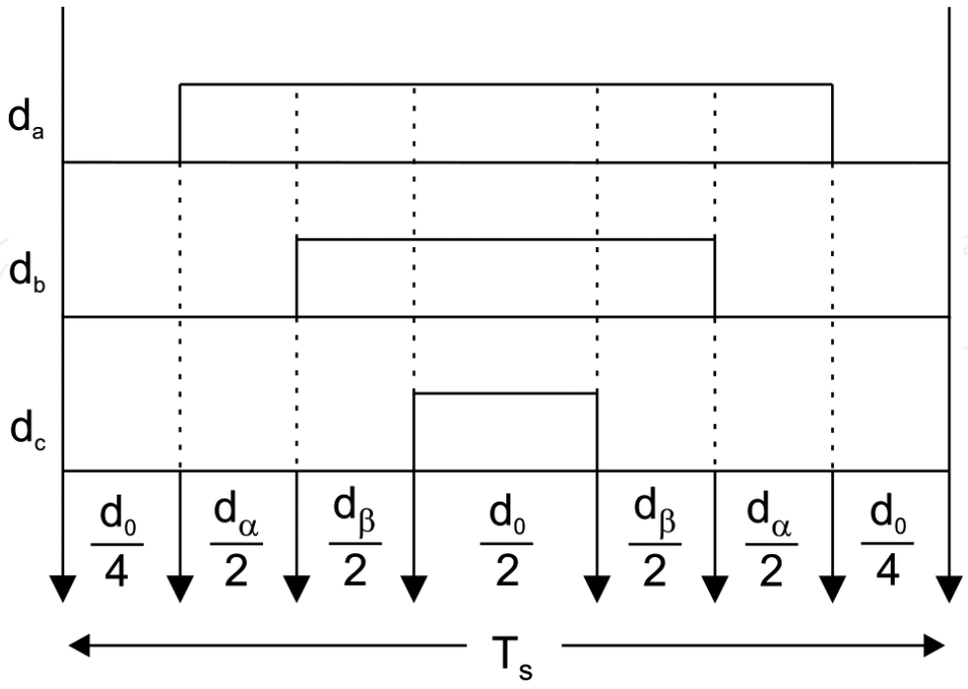

Figure 5. Switching sequence in one period.

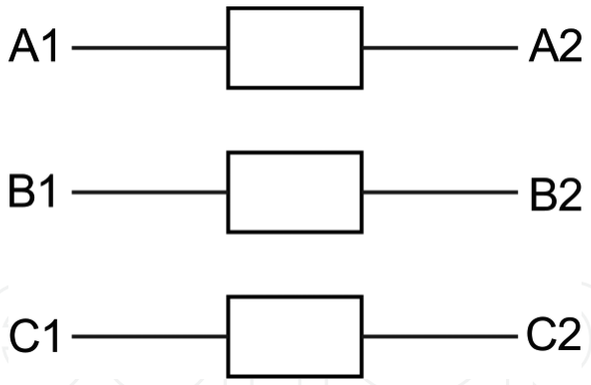

Figure 6. Open-ended load.

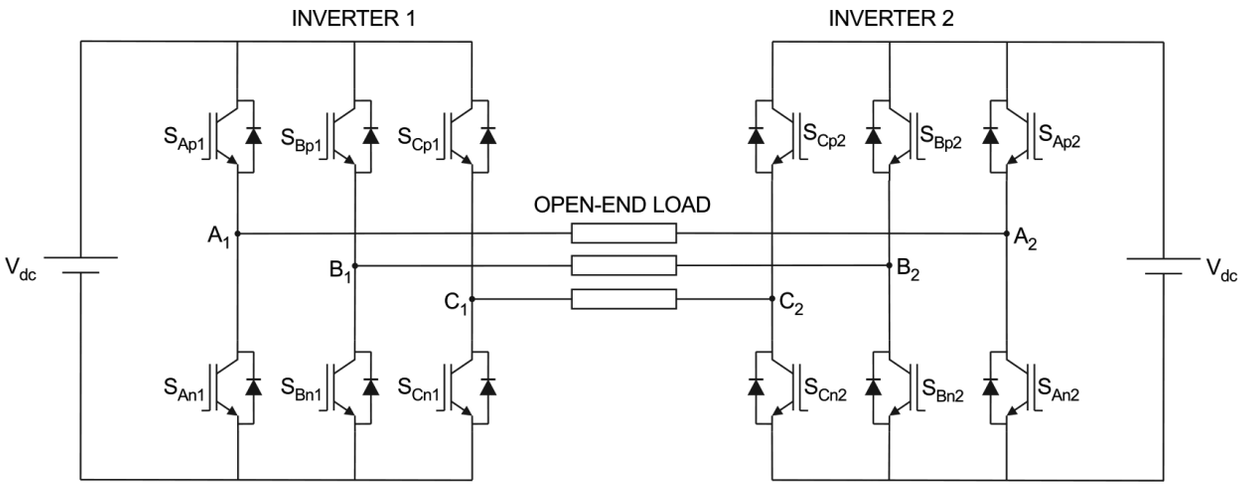

Figure 7. Two two-level VSIs fed by isolated DC sources for an open-ended load.

specific magnitude ratio of the DC sources, certain harmonic components of the output phase voltage can be eliminated. In Ref. [9], a method to extend the operating speed range of an open-end winding electrical machine is proposed based on the voltage range enhancement.

In Ref. [10], a modulation strategy for reducing the voltage total harmonic distortion (THD) in a dual-inverter is presented consisting on adjusting the pulses times of one of the inverters with respect to the other. In Ref. [11], a unified SVM strategy is proposed for a dual two-level inverter system in accordance with the voltage-second integral principle and the ratio of the two DC sources can be arbitrary positive values.

To reduce the switching losses of a dual-inverter, a space vector modulation (SVM) strategy is presented in Ref. [12]. The strategy does not require sector identification and allows a reduction of 50% in the switching losses, in comparison to other dual-inverter PWM techniques where one inverter is clamped at a determined switching state, while the other inverter commutates. In Ref. [13], a comparative study between three different modulation strategies for open-ended windings AC machine drives is carried out. Simulation results are presented and the current ripple under each PWM method is analysed.

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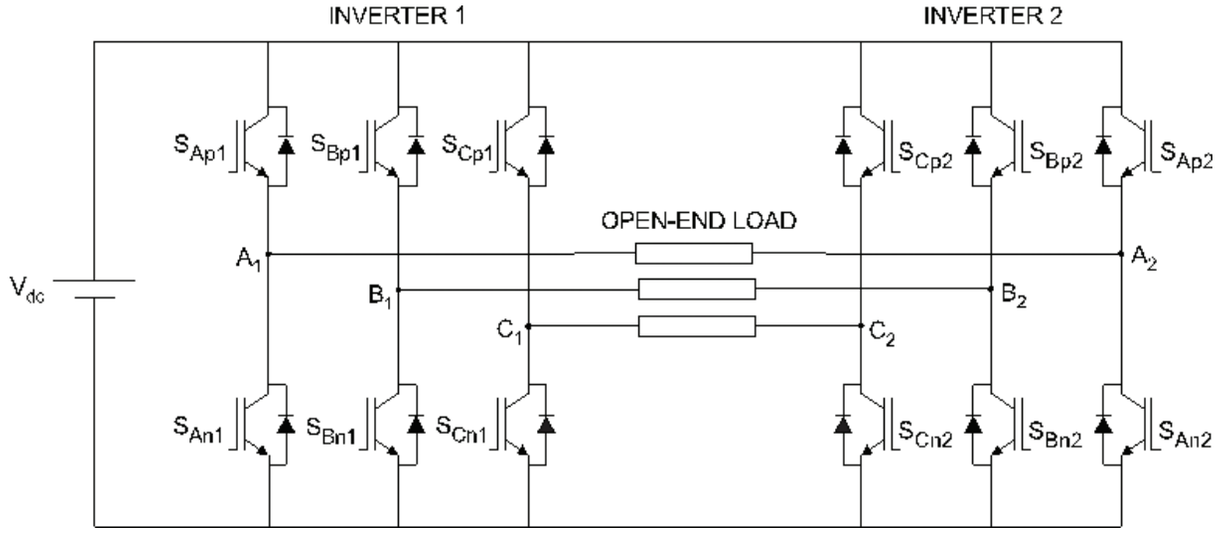

Figure 8. Two two-level VSIs fed by a single DC source for an open-end load.

The extension of the three-phase open-ended windings AC machine drive to multiphase machines is presented in Refs. [14–17] where different modulation strategies are presented and discussed. This extension is not straightforward because the number of possible switching states increases exponentially with the number of phases.

On the other hand, the dual-inverter supplied by a single DC source is a cheaper and of lower volume alternative, but circulation of zero sequence current could occur if zero sequence voltage is produced. Therefore, the attention should be put on reducing the common-mode voltage as well as the zero sequence voltage.

To eliminate the occurrence of zero sequence currents in the load, PWM strategies intended to eliminate the zero sequence voltage are proposed in Refs. [5, 6]. In Ref. [18], a SVM strategy is proposed to dynamically compensate the zero sequence current by applying the null vectors with asymmetrical duty cycles in each switching period and, in Ref. [19], the effect of the null-vector placement in the modulation for the dual-inverter system is thoroughly analysed. On the other hand, a closed-loop compensation scheme to suppress the zero sequence currents in the machine is developed in Ref. [20].

In Ref. [21], a vector control scheme for an open-end winding permanent magnet synchronous motor (PMSM) is presented considering a regulation mechanism for the zero sequence voltage, whereas in Ref. [22], a closed-loop control strategy intended to reduce the torque ripple in a PMSM with non-sinusoidal back electromotive force (EMF) is proposed.

To obtain a common-mode voltage reduction, a SVM switching strategy is presented in Ref. [23]. This modulation strategy considers only voltage space vectors that do not produce common-mode voltage then reducing the problems associated to it such as the bearing currents.

A dual-inverter configuration fed by an active rectifier without DC-link energy storage element (so-called direct-link converter) is presented in Refs. [24, 25]; in Ref. [24], three

modulation strategies are presented for the drive: a carrier-based PWM and two SVM strategies. In Ref. [25], common-mode voltage suppression is proposed and an active filter is added to the topology to inject compensating harmonic currents into the supply and allow controllable input power factor.

Finally, multiphase open-ended windings induction motor drives are presented in Refs. [26–29], where the proposed PWM techniques are intended to reduce the common-mode voltage at the machine terminals; simulation and experimental results are also shown.

In this chapter, a general study of the dual-inverter topology is presented. The issues of zero sequence and common-mode voltages are thoroughly studied and different modulation strategies for the converter are shown and discussed; for evaluation purposes, simulations results are presented. Although the chapter is mainly focused on a two-level dual-inverter system supplied with isolated and non-isolated DC source, multilevel dual-inverter topologies are also discussed briefly.

2. The dual two-level inverter

In this section, a mathematical model of a two-level dual-inverter system will be developed. The model allows understanding the generation of the phase output voltage produced by the dual-inverter by means of the output voltage produced by the individual VSIs. The basic circuit configuration for supplying an open-ended load consists on connecting a standard two-level VSI at each side of the load (**Figures 7** and **8**). The output pole voltage of Inverter 1 ($\boldsymbol{v_{o1}}$) and Inverter 2 ($\boldsymbol{v_{o2}}$) with respect to the negative DC-link rail, is defined by

$$\boldsymbol{v_{o1}} = \boldsymbol{S_{i1}} \cdot v_{DC},\ \boldsymbol{v_{o2}} = \boldsymbol{S_{i2}} \cdot v_{DC} \tag{3}$$

where the switching matrices of Inverter 1 ($\boldsymbol{S_{i1}}$) and Inverter 2 ($\boldsymbol{S_{i2}}$) are as follows:

$$\boldsymbol{S_{i1}} = \begin{bmatrix} S_{A1} \\ S_{B1} \\ S_{C1} \end{bmatrix} = \begin{bmatrix} S_{Ap1} - S_{An1} \\ S_{Bp1} - S_{Bn1} \\ S_{Cp1} - S_{Cn1} \end{bmatrix},\ \boldsymbol{S_{i2}} = \begin{bmatrix} S_{A2} \\ S_{B2} \\ S_{C2} \end{bmatrix} = \begin{bmatrix} S_{Ap2} - S_{An2} \\ S_{Bp2} - S_{Bn2} \\ S_{Cp2} - S_{Cn2} \end{bmatrix}. \tag{4}$$

and $S_{xpx} = \overline{S}_{xnx} \in \{0, 1\}$ with $x = a, b, c, k = 1,\ 2$. The output phase voltages correspond to the pole voltage difference of both inverters:

$$\boldsymbol{v_{ph,o}} = \begin{bmatrix} v_{ph,oa} & v_{ph,ob} & v_{ph,oc} \end{bmatrix}^T = \boldsymbol{v_{o1}} - \boldsymbol{v_{o2}} = (\boldsymbol{S_{i1}} - \boldsymbol{S_{i2}}) v_{DC} \tag{5}$$

The three voltages produced by both output VSIs are depicted in **Figure 9**. These voltages are measured with respect to a midpoint of the DC link. Then it is possible to calculate the sum of the voltage vectors:

$$\underline{v}_{sum} = \underline{v}_{A1} + \underline{v}_{B1} + \underline{v}_{C1} + \underline{v}_{A2} + \underline{v}_{B2} + \underline{v}_{C2} \tag{6}$$

$$\underline{v}_{sum} = v_{A1}e^{j0} + v_{B1}e^{-j\frac{2\pi}{3}} + v_{C1}e^{j\frac{2\pi}{3}} + v_{A2}e^{j\pi} + v_{B2}e^{j\frac{\pi}{3}} + v_{C2}e^{-j\frac{\pi}{3}} \tag{7}$$

Using the Euler's formula, $e^{j\alpha} = \cos\alpha + j\sin\alpha$, it is obtained as follows:

$$\underline{v}_{sum} = \left[v_{A1} - v_{A2} - \frac{1}{2}(v_{B1} - v_{B2}) - \frac{1}{2}(v_{C1} - v_{C2})\right] + j\frac{\sqrt{3}}{2}[-v_{B1} + v_{B2} + v_{C1} - v_{C2}] \tag{8}$$

that can be rewritten as follows:

$$\underline{v}_{sum} = \left(v_{A1A2} - \frac{1}{2}v_{B1B2} - \frac{1}{2}v_{C1C2}\right) + j\frac{\sqrt{3}}{2}(v_{C1C2} - v_{B1B2}) \tag{9}$$

Finally, the output voltage space vector can be defined as:

$$\underline{v}_o = \frac{2}{3}\underline{v}_{sum} = \frac{2}{3}\left(v_{A1A2} + v_{B1B2}e^{-j\frac{2\pi}{3}} + v_{C1C2}e^{j\frac{2\pi}{3}}\right) = v_o e^{j\theta} \tag{10}$$

where v_o is the magnitude and θ the angle of the space vector. The coefficient 2/3 is a scaling factor that has been added to keep constant magnitude of the vectors during the transformation [1].

In general, each inverter can produce eight independent voltage space vectors. Thus, there are a total of 64 vector combinations for the dual-inverter system, resulting in a space vector locus similar to a three-level neutral point clamped (NPC) inverter [4]. The space vectors for both inverters are shown in **Table 2**. A representation of the individual inverters space vectors is shown in **Figure 10**.

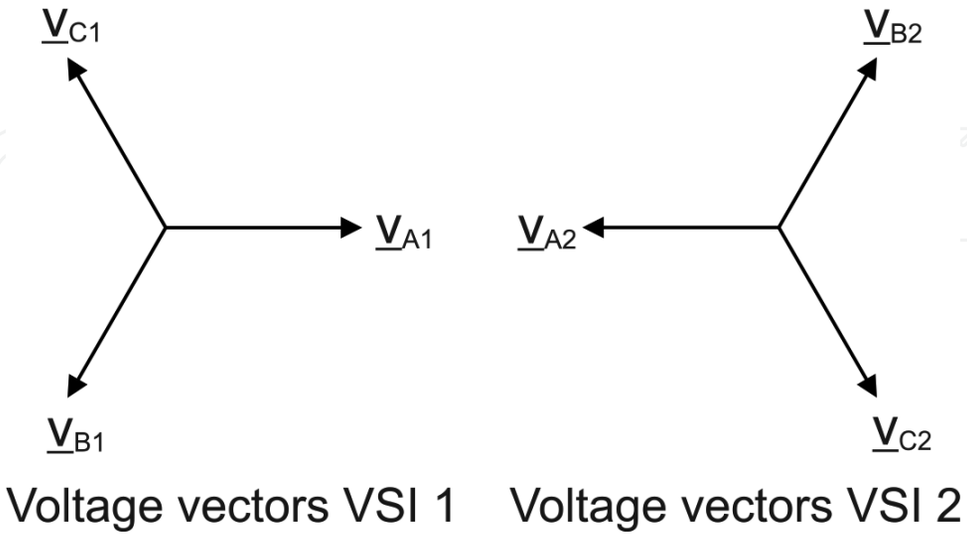

Figure 9. Voltages vectors of the individual inverters.

States of inverter 1 $[S_{A1}S_{B1}S_{C1}]$			
$V_1^1 = [100]$	$V_2^1 = [110]$	$V_3^1 = [010]$	$V_4^1 = [011]$
$V_5^1 = [001]$	$V_6^1 = [101]$	$V_7^1 = [111]$	$V_8^1 = [000]$
States of inverter 2 $[S_{A2}S_{B2}S_{C2}]$			
$V_1^2 = [100]$	$V_2^2 = [110]$	$V_3^2 = [010]$	$V_4^2 = [011]$
$V_5^2 = [001]$	$V_6^2 = [101]$	$V_7^2 = [111]$	$V_8^2 = [000]$

Table 2. Switching states of the individual inverters.

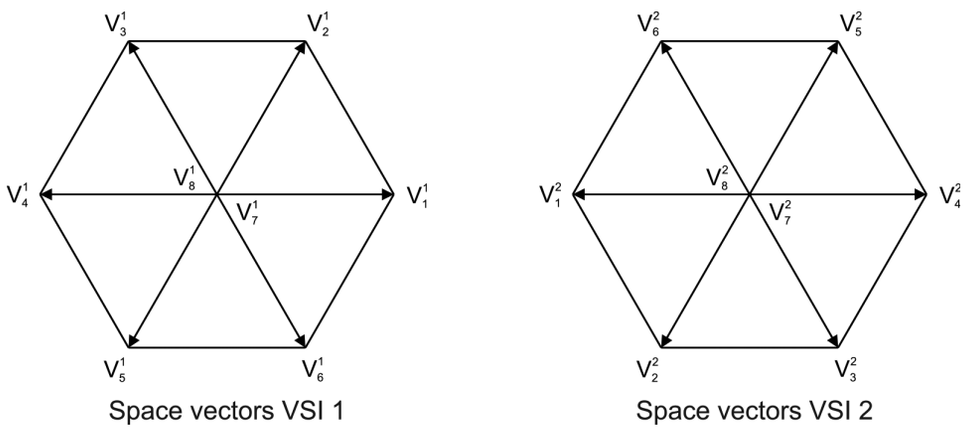

Figure 10. Space vectors representation of the individual inverters.

Let $V_{ij} = \left[V_i^1 V_j^2\right]$ with $i,\ j = 1 \ldots 8$, be the phase voltage vector combination of the dual-inverter system; hence, a diagram of the vector locations is shown in **Figure 11** [4], where the availability of redundant switching states for some voltage space vectors of the dual-inverter can be appreciated. This diagram is obtained by carrying out the vector sum of all the possible space vector combinations of inverters 1 and 2 (**Figure 10**).

The magnitude of the active space voltage vectors can be calculated considering that each phase load can be supplied with a voltage of $-V_{DC}$, 0 or $+V_{DC}$. For instance, the vector V_{14} applies $+V_{DC}$ to the phase-*a* load and $-V_{DC}$ to phase-*b* and phase-*c* loads. This results in:

$$\underline{V}_{14} = V_{DC} - V_{DC}e^{-j\frac{2\pi}{3}} - V_{DC}e^{j\frac{2\pi}{3}} = 2V_{DC} < 0^{\circ}[V] \tag{11}$$

The same procedure can be used to calculate the magnitude of each active space voltage vector of the dual-inverter system. This is summarized in **Table 3**.

As can be noted from **Table 3** and **Figure 11**, the six largest vectors have a magnitude of twice the DC-link voltage and have no redundancy. On the other hand, the higher redundancy is present for the lowest vectors each having six switching states available to produce the same output voltage.

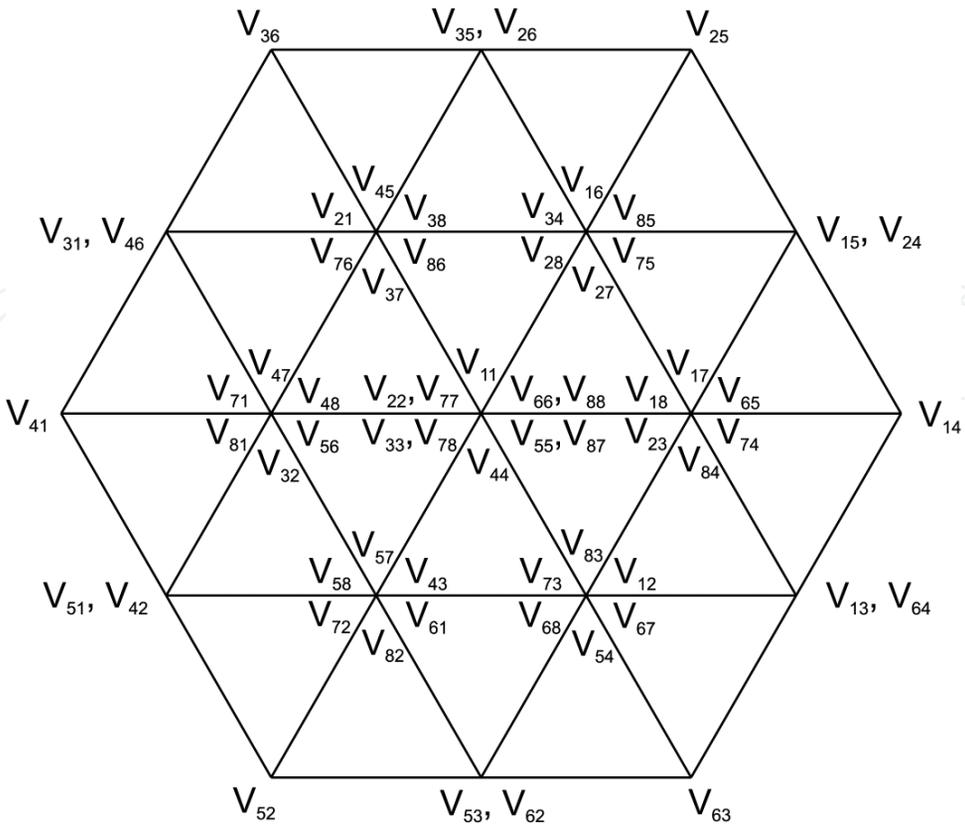

Figure 11. Space vector locations of the dual-inverter scheme.

	Space Vectors	Magnitude
Largest	$V_{14}, V_{25}, V_{36}, V_{41}, V_{52}, V_{63}$	$2V_{DC}$
Medium	$V_{15}, V_{24}, V_{35}, V_{26}, V_{31}, V_{46}, V_{51}, V_{42}, V_{53}, V_{62}, V_{13}, V_{64}$	$\sqrt{3}V_{DC}$
Lowest	$V_{65}, V_{17}, V_{18}, V_{23}, V_{84}, V_{74}, V_{85}, V_{16}, V_{34}, V_{28}, V_{27}, V_{75}$	V_{DC}
	$V_{38}, V_{45}, V_{21}, V_{76}, V_{37}, V_{86}, V_{48}, V_{47}, V_{71}, V_{81}, V_{32}, V_{56}$	
	$V_{43}, V_{57}, V_{58}, V_{72}, V_{82}, V_{61}, V_{12}, V_{83}, V_{73}, V_{68}, V_{54}, V_{67}$	

Table 3. Magnitude of the dual-inverter active space vectors.

3. Common-mode and zero sequence voltages in dual-inverters

As aforementioned, one of the main features of a dual-inverter circuit is that it allows reducing the common-mode voltage in the load then reducing the problems associated to it. On the other hand, it has been also stated that when supplying the dual-inverter with a single DC source, zero sequence current can flow in the load because of the generation of zero sequence voltage. In this section, a detailed explanation about the common-mode voltage and zero sequence voltage issues is given and solutions to reduce them are indicated.

3.1. Common-mode voltage

A typical three-phase sinusoidal power supply is balanced and symmetrical under normal conditions; that is, the sum of the three instantaneous voltages is zero. Thus, when supplying a balanced three-phase load, the voltage between an equivalent neutral point of the load and the neutral point of the voltage source is zero. Usually, the neutral point of the power source is grounded.

On the other hand, a three-phase PWM inverter is a source of asymmetrical voltages that switches a DC bus voltage (V_{DC}) into the three-phase terminals of the load, with a switching pattern that generates the proper fundamental frequency output voltage [2]. Since the output pole voltage of a two-level inverter, with respect to the negative rail of the DC bus, can be either $+V_{DC}$ or zero, it is not possible to have the three terminal voltages added to zero at any instant of time. The average voltage applied to the motor (over a cycle) is kept zero, but the instantaneous sum of the voltages at the load terminals is non-zero. Then, a voltage will appear between an equivalent neutral point of the load and the electrical ground of the system. This voltage is called common-mode voltage [30].

In an open-end load, such as depicted in **Figure 8**, the common-mode voltage is given by [23]:

$$v_{cm} = \frac{1}{6}(v_{A1G} + v_{B1G} + v_{C1G} + v_{A2G} + v_{B2G} + v_{C2G}) \tag{12}$$

where v_{AiG}, v_{BiG}, v_{CiG}, with $i = 1,\ 2$, are the pole voltages of each inverter with respect to the grounded neutral point of the power source (assuming in **Figure 8** that the DC voltage is provided by the rectification of a grounded AC system).

Because of the typically high switching frequency of a PWM inverter in the kHz range, the common-mode voltage has a high rate of change with respect to time (high dV/dt) and will generate common-mode currents due to capacitive couplings ($I_{cm} = C\,dV/dt$). Moreover, higher inverter switching frequencies will originate higher common-mode currents.

In AC motor drives, the capacitive couplings between different parts of a machine originate many potential paths for these common-mode currents to flow. The most common paths are [31] stator to rotor, stator winding to frame, rotor to shaft and shaft to frame. Therefore, the circulation of common-mode currents via the motor bearings back to the grounded stator case is possible. The so-called bearing currents have been found to be a major cause of premature bearing failure in PWM inverter motor drives [31]. Thus, a common-mode voltage reduction has been a topic of interest for many years.

3.1.1. Common-mode voltage in open-ended loads

One of the main advantages of an open-ended load connection is that it allows the possibility of reducing the common-mode voltage, then reducing the problems associated to it.

In the power converter topology shown in **Figure 8**, the pole voltages v_{AiG}, v_{BiG}, v_{CiG}, with $i = 1,\ 2$, can be expressed as follows:

$$\begin{aligned} v_{AiG} &= S_{Api}v_{pG} + S_{Ani}v_{nG} \\ v_{BiG} &= S_{Bpi}v_{pG} + S_{Bni}v_{nG} \\ v_{CiG} &= S_{Cpi}v_{pG} + S_{Cni}v_{nG} \end{aligned} \tag{13}$$

where v_{pG} and v_{nG} are the positive and negative rail voltages of the DC link with respect to the grounded neutral point of the power source, respectively. $S_{xpi}, S_{xni} \in \{0, 1\}$ with $x = A, B, C$, and $i = 1, 2$ are the switching functions of the inverter devices (0: switch closed, 1: switch opened) and $S_{xni} = 1 - S_{xpi}$ (due to the complementary operation of the upper and lower switches of each inverter leg). Hence, the common-mode voltage of Eq. (12) can be rewritten as follows:

$$\begin{aligned} v_{cm} = \frac{1}{6}\big[&\big(S_{Ap1} + S_{Bp1} + S_{Cp1} + S_{Ap2} + S_{Bp2} + S_{Cp2}\big)v_{pG} \\ &+ (S_{An1} + S_{Bn1} + S_{Cn1} + S_{An2} + S_{Bn2} + S_{Cn2})v_{nG}\big] \end{aligned} \tag{14}$$

Let $N_{sw} = S_{Ap1} + S_{Bp1} + S_{Cp1} + S_{Ap2} + S_{Bp2} + S_{Cp2}$, and considering that $v_{nG} = -v_{pG}$, thus

$$v_{cm} = \frac{1}{6}\big[N_{sw}v_{pG} + (6 - N_{sw})\big(-v_{pG}\big)\big] = \frac{1}{6}v_{pG}[2N_{sw} - 6] \tag{15}$$

where N_{sw} is the number of upper inverter switches closed.

The squared RMS value of the common-mode voltage is as follows:

$$v_{cm_{RMS}}^2 = \frac{1}{36T}\int_0^T [2N_{\mathrm{sw}} - 6]^2 dt \tag{16}$$

where T is the period of v_{pG}. Further expansion yields:

$$36v_{cm_{RMS}}^2 = \big(4N_{sw}^2 - 24N_{sw} + 36\big)\frac{1}{T}\int_0^T dt = 4N_{sw}^2 - 24N_{sw} + 36 \tag{17}$$

Differentiating Eq. (17) with respect to N_{sw} and equating to zero, it can be found that $v_{cm_{RMS}}^2$ (and implicitly $v_{cm_{RMS}}$) achieves a minimum value at $N_{sw} = 3$, which means that in order to reduce the RMS common-mode voltage at the machine terminals, only three upper inverter switches should be closed at each switching period.

This can be further investigated by considering a virtual midpoint of the DC link as a reference point. Then, Eq. (12) can be rewritten as follows:

$$v_{cm} = \frac{1}{6}(v_{A10} + v_{B10} + v_{C10} + v_{A20} + v_{B20} + v_{C20}) + v_{0G} = v_{cm0} + v_{0G} \tag{18}$$

where v_{cm0} is the common-mode voltage produced by the dual-inverter circuit with respect to a midpoint of the DC link and v_{0G} is the voltage between a midpoint of the DC source and the ground of the system.

The common-mode voltage produced by the 64 switching states combinations of the dual-inverter topology (v_{cm0}) can be calculated with Eq. (18) and is shown in **Table 4**.

Therefore, reducing the common-mode voltage in an open-end load is feasible if voltage vectors contained in the fourth row in **Table 4** are used.

However, it can be noted from **Table 3** and **Table 5** that the space vector combinations of the dual-inverter topology which eliminate the zero sequence voltage are not the same vectors which reduce the common-mode voltage.

V_{cm0}	Voltage vector combinations
$-V_{DC}/4$	V_{88}
$-V_{DC}/6$	$V_{85}, V_{83}, V_{81}, V_{58}, V_{38}, V_{18}$
$-V_{DC}/12$	$V_{84}, V_{86}, V_{82}, V_{55}, V_{35}, V_{33}, V_{51}, V_{31}$
	$V_{15}, V_{13}, V_{11}, V_{48}, V_{68}, V_{28}, V_{53}$
0	$V_{14}, V_{25}, V_{36}, V_{52}, V_{87}, V_{54}, V_{34}, V_{56}, V_{32}, V_{16}$
	$V_{12}, V_{45}, V_{43}, V_{41}, V_{65}, V_{63}, V_{23}, V_{21}, V_{78}, V_{61}$
$+V_{DC}/12$	$V_{17}, V_{57}, V_{37}, V_{44}, V_{46}, V_{64}, V_{24}, V_{42}$
	$V_{62}, V_{26}, V_{22}, V_{75}, V_{73}, V_{66}, V_{71}$
$+V_{DC}/6$	$V_{47}, V_{74}, V_{76}, V_{67}, V_{72}, V_{27}$
$+V_{DC}/4$	V_{77}

Table 4. Active space vectors producing null common-mode voltage.

V_{zs}	Voltage vector combinations
$-V_{DC}/2$	V_{87}
$-V_{DC}/3$	$V_{84}, V_{86}, V_{82}, V_{57}, V_{37}, V_{17}$
$-V_{DC}/6$	$V_{85}, V_{83}, V_{54}, V_{34}, V_{81}, V_{56}, V_{52}, V_{36}$
	$V_{32}, V_{47}, V_{14}, V_{16}, V_{12}, V_{67}, V_{27}$
0	$V_{88}, V_{55}, V_{53}, V_{35}, V_{33}, V_{44}, V_{51}, V_{31}, V_{46}, V_{42}$
	$V_{15}, V_{13}, V_{64}, V_{24}, V_{11}, V_{66}, V_{62}, V_{26}, V_{22}, V_{77}$
$+V_{DC}/6$	$V_{58}, V_{38}, V_{45}, V_{43}, V_{18}, V_{65}, V_{25}, V_{63}$
	$V_{23}, V_{74}, V_{41}, V_{61}, V_{21}, V_{76}, V_{72}$
$+V_{DC}/3$	$V_{48}, V_{68}, V_{82}, V_{75}, V_{73}, V_{71}$
$+V_{DC}/2$	V_{78}

Table 5. Zero sequence voltage contributions from different space vector combinations.

3.2. Zero sequence voltage

It is well known that unbalanced three-phase voltages (or currents) can be transformed into three sets of voltage components [32]. These so-called symmetrical components are known as positive, negative and zero sequence components and can be schematically represented as shown in **Figure 12a**. Positive and negative sequence components correspond to three-phase balanced rotating phasors and zero sequence components are phasors with zero-phase shift angle. **Figure 12b** shows a decomposition of an unbalanced three-phase voltage into symmetrical voltage components.

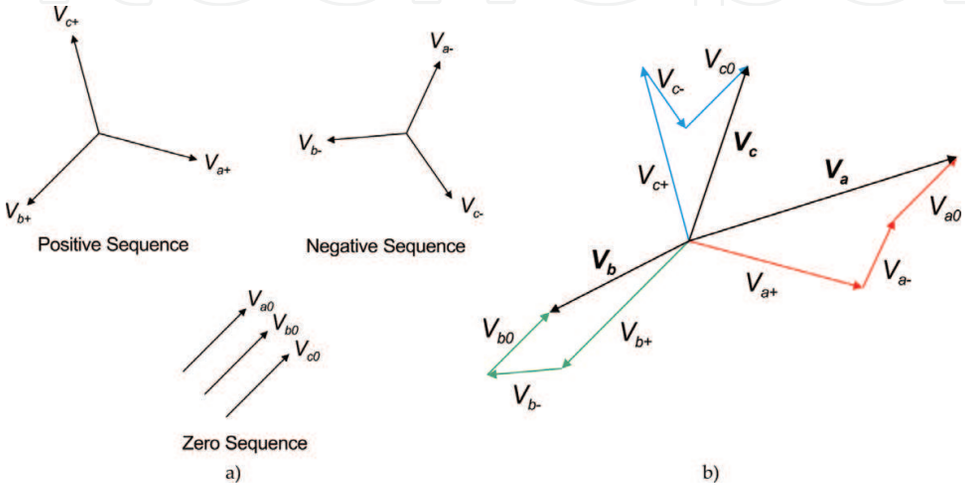

Figure 12. (a) Symmetrical components and (b) decomposition of unbalanced three-phase voltage into symmetrical components.

Unlike the positive and negative sequence currents, the main issue of the zero sequence currents is that they do not cancel but add up arithmetically at the neutral point of a four wire three-phase system, eventually overloading the neutral line or producing a higher neutral to ground voltage. Additionally, harmonic currents of any sequence circulating in an AC drive may give rise to increased RMS current, thus increasing the system losses, high current/voltage THD and machine over-heating and vibrations.

3.2.1. Zero sequence voltage in open-end loads

An open-end load supplied by a dual-inverter with a single DC source may suffer from zero sequence current caused by zero sequence voltage. This zero sequence voltage is produced because of the asymmetry of the instantaneous pulse width modulated phase voltages applied to the load phases (due to the voltage space vectors used). The zero sequence voltage is given by [18]:

$$v_{zs} = \frac{v_{A1A2} + v_{B1B2} + v_{C1C2}}{3} \tag{19}$$

or in terms of Eq. (5) as follows:

$$v_{zs} = \frac{1}{3}\sum_{k=a,\ b,\ c} v_{ph,ok} = \frac{v_{DC}}{3}\sum_{k=A,\ B,\ C}(S_{k1} - S_{k2}) \tag{20}$$

Thus, in order to make $v_{zs} = 0$, the following relationship must be satisfied:

$$\sum_{k=A,\ B,\ C} S_{k1} = \sum_{k=A,\ B,\ C} S_{k2} \tag{21}$$

Therefore, to eliminate the instantaneous zero sequence voltage in the load is necessary and sufficient to have the same number of upper (or lower) switches closed on both output inverters at every switching period.

By using Eq. (19), the zero sequence voltage contribution from the 64 space vector combinations of the dual-inverter topology can be calculated and is shown in **Table 5**. As can be noted, there are 20 space voltage vectors that do not produce zero sequence voltage, thus satisfying Eq. (21). Hence, in order to avoid the circulation of zero sequence current in the load, only these space voltage vector combinations could be used in the modulation strategy for the dual-inverter [24].

Moreover, from **Table 5** and **Figure 11**, it can be noted that there are two different but equivalent sets of active voltage vectors producing null zero sequence voltage (see **Table 6**), which could be used along with the zero voltage vectors: V_{11}, V_{22}, V_{33}, V_{44}, V_{55}, V_{66}, V_{77} and V_{88}.

Set 1	V_{15}	V_{35}	V_{31}	V_{51}	V_{53}	V_{13}
Set 2	V_{24}	V_{26}	V_{46}	V_{42}	V_{62}	V_{64}

Table 6. Active space vectors producing null zero sequence voltage.

Besides the use of space voltage vectors producing null v_{zs}, the occurrence of low order triplen harmonics in the load phase currents could be avoided performing a dynamic balance for the zero sequence current as proposed in Ref. [18]. This dynamic compensation method will be further discussed in Section 5.

4. Two two-level inverters fed by isolated DC sources

This circuit configuration is shown in **Figure 7**, where a standard two-level VSI is connected at each side of the load. The VSIs are supplied by isolated DC power sources. In general, the main characteristic of this topology is that circulation of zero sequence current in the load is avoided; however, it requires two isolation transformers to supply the DC sources increasing the cost and volume of system.

As the circuit configuration does not allow to have circulation of zero sequence current, the modulation strategy should aim to reduce only the common-mode voltage.

4.1. SVM strategy for common-mode voltage reduction

It has been shown that an open-end load offers the possibility of reducing the common-mode voltage by using certain voltage space vector combinations of the dual-inverter [23], as shown in **Table 4**. The locus of the vectors that theoretically eliminate the common-mode voltage of the system is shown in **Figure 13**.

As can be noted in the locus, the vectors that reduce the common-mode voltage are the largest and some of the lowest, then depending on the output voltage requirement, the modulation for the dual-inverter could use the vectors of **Figure 13a** or **b**. Moreover, for the lowest vectors, there is switching states redundancy, opposite to the situation for the largest ones where all the voltage vectors can be produced by a unique switching state combination of the inverters.

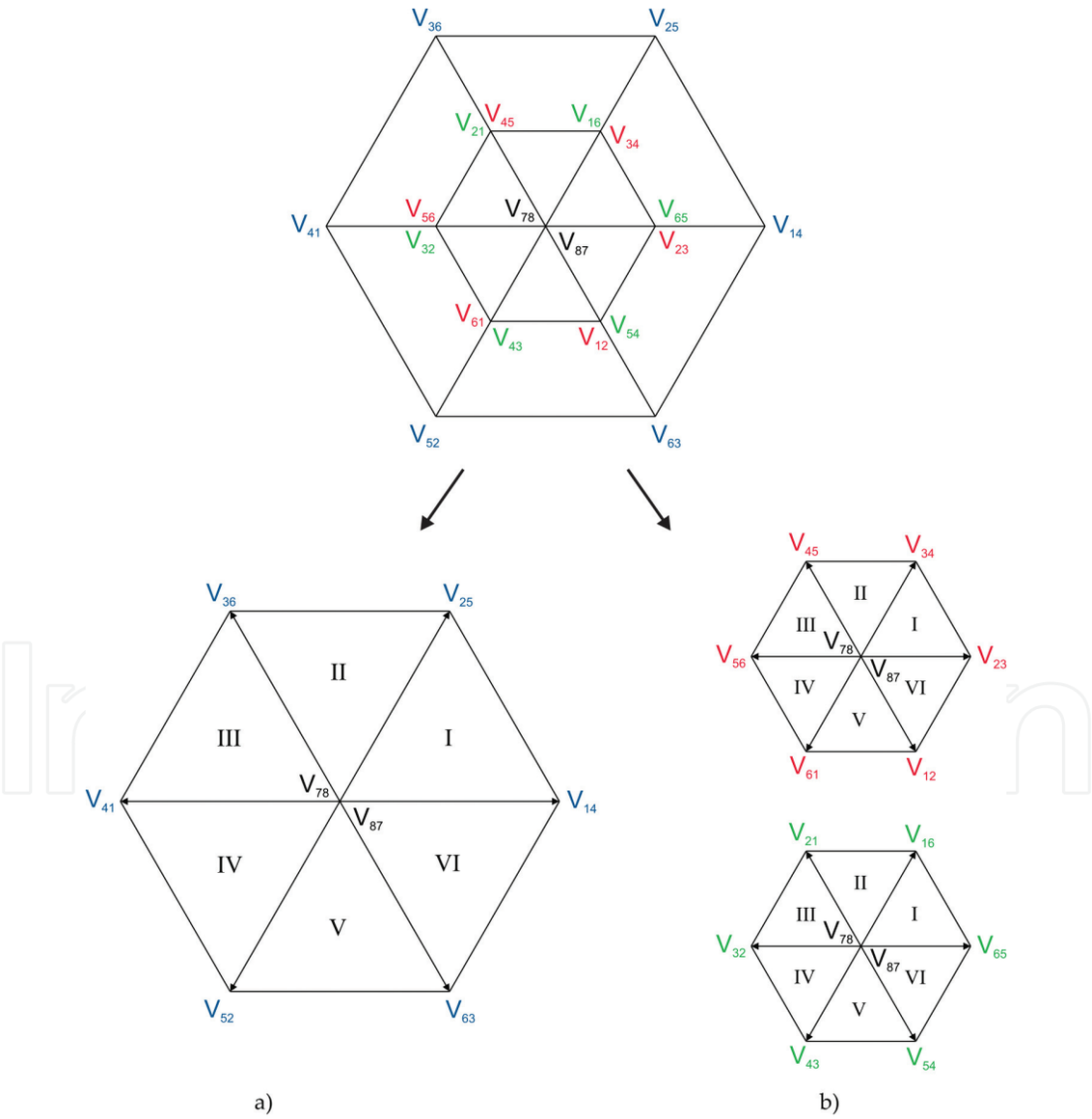

Figure 13. Locus of vectors for reduced common-mode voltage.

Symbol	Parameter	Value
R	Load resistance	4 Ω
L	Load inductance	6 mH
f_s	Switching frequency	10 kHz
f_o	Output voltage frequency	50 Hz
V_{DC}	DC voltage source	300 V

Table 7. Simulation parameters.

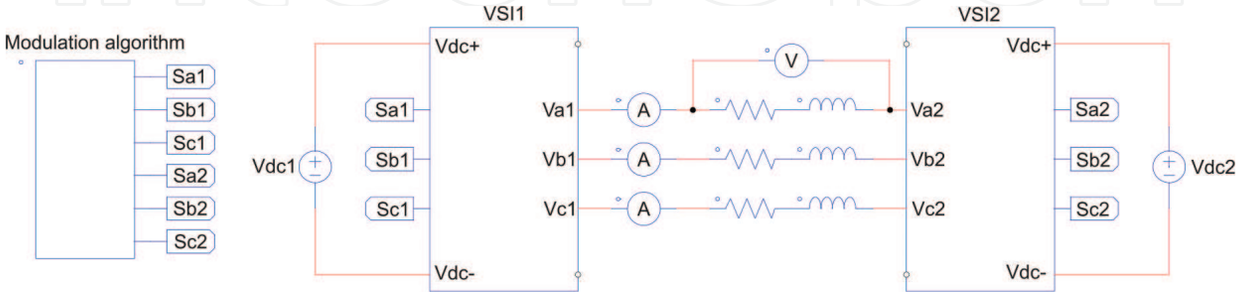

Figure 14. Circuit implemented in PSim.

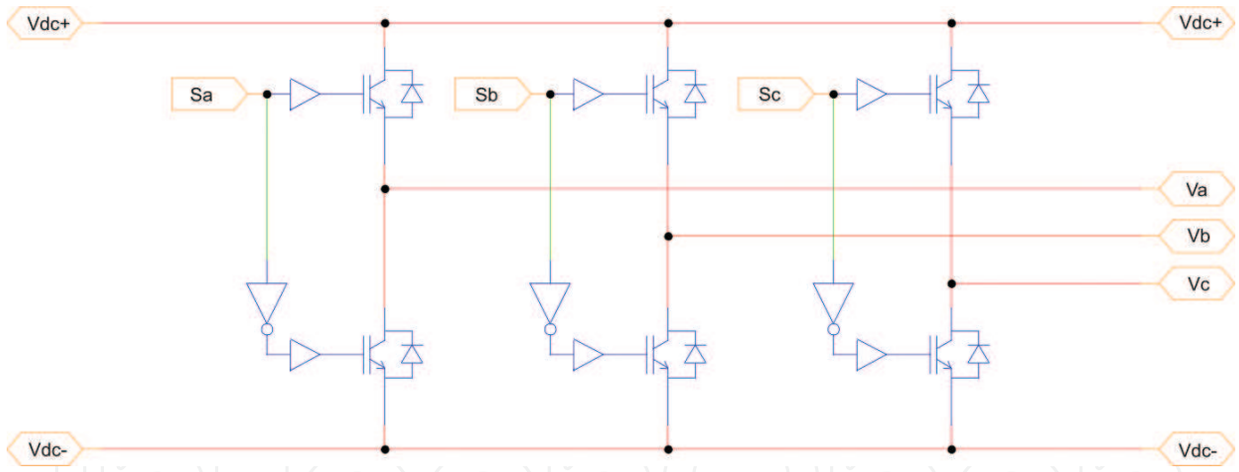

Figure 15. Individual inverter in PSim.

However, despite the aforementioned advantage of the lowest vectors, for the modulation strategy proposed, only the largest vectors will be used attending to maximize the output voltage and because the using of all the vectors available will complicate the modulation algorithm and the benefits in terms of current/voltage THD of applying the lowest space vectors are not significant. Once selected, the space vectors to be used, Eqs. (1) and (2), are valid for calculating the duty cycles and the switching sequence is the standard used in two-level VSIs (**Figure 5**).

4.1.1. Simulation results

The modulation strategy for common-mode voltage reduction has been simulated in PSim/Matlab simulation platform for the topology depicted in **Figure 7**, considering an R-L load and

the parameters of **Table 7**. The modulation index used is the maximum possible without overmodulation. The circuit implemented in PSim is shown in **Figure 14** where the modulation algorithm is programmed in 'C' language in a special block provided by PSim software. The sub-circuits VSI1 and VSI2 (**Figure 14**) contain the standard two-level inverter shown in **Figure 15**. These circuits are used to simulate the required system and the obtained results (data tables) are then exported and plotted in Matlab environment.

The results are shown in **Figures 16–18**. **Figure 16** shows the output phase voltage (top) and its frequency spectrum (bottom). It can be noted that three levels are obtained in the load phase voltage. The frequency spectrum contains a fundamental component of 50 Hz and some low harmonic content around the switching frequency.

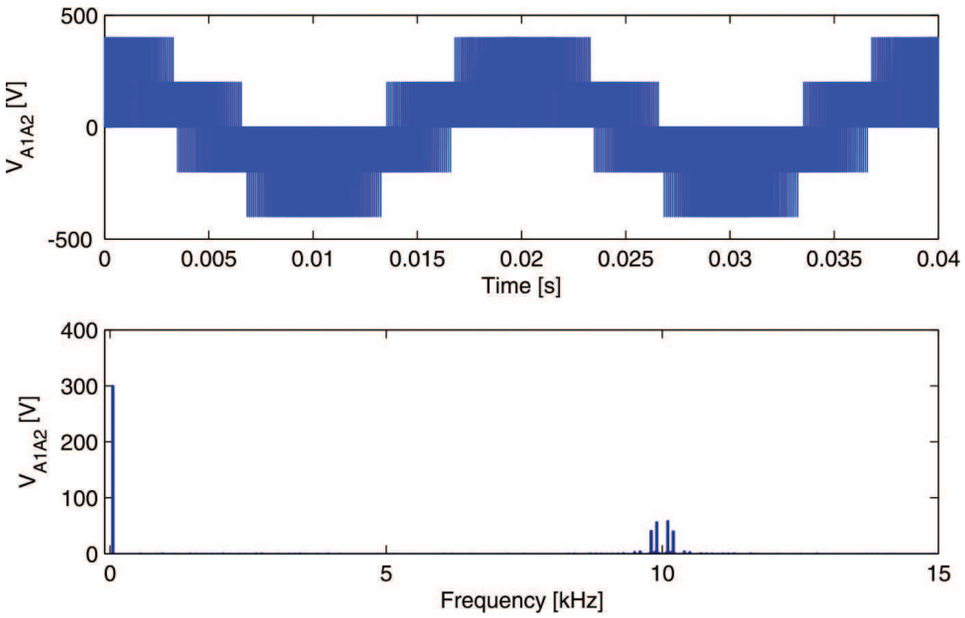

Figure 16. Output phase voltage (top) and its frequency spectrum (bottom) with SVM for reduced CMV and dual-inverter supplied with isolated DC sources.

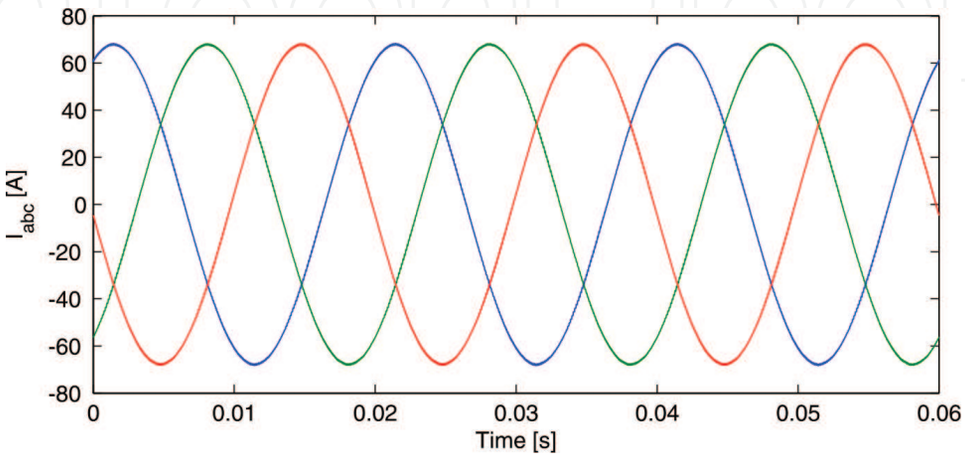

Figure 17. Output currents with SVM for reduced CMV and dual-inverter supplied with isolated DC sources.

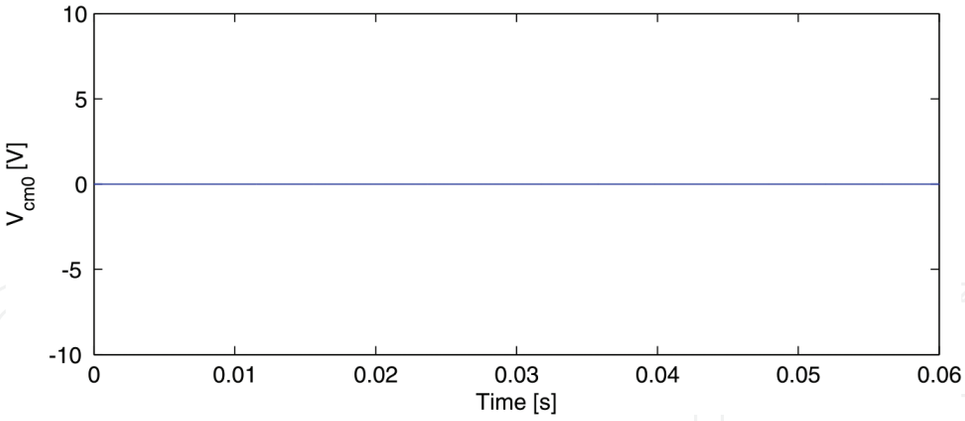

Figure 18. Common-mode voltage with SVM for reduced CMV and dual-inverter supplied with isolated DC sources.

The output currents are shown in **Figure 17** and the common-mode voltage is shown in **Figure 18**. It can be seen that the sinusoidal characteristic of the currents is due to the inductive nature of the load. Moreover, it can be noted that the CMV is eliminated due to the space vectors used in the modulation.

5. Two two-level inverters fed by a single DC source

The circuit configuration for a single DC source supplying a dual-inverter has been presented in **Figure 8**. The main disadvantage of this converter is that zero sequence current could circulate through the load due to the generation of output zero sequence voltage. Hence, a possible solution is to modulate the dual-inverter using only the space vectors that do not produce zero sequence voltage (**Table 5**). On the other hand, if the requirement is to reduce the CMV, the vectors of fourth row of **Table 4** can be used. However, it can be noted from **Table 4** and **Table 5** that the space vectors that reduce the CMV are not the same vectors that reduce the ZSV; therefore, to reduce both voltages at a time, a special modulation strategy is presented in this section.

5.1. SVM strategy for zero sequence voltage reduction

As mentioned above, the zero sequence voltage applied to the load can be eliminated by using certain voltage space vectors as shown in **Table 5**. Moreover, it has been mentioned that there are two equivalent sets of active vectors producing $v_{zs} = 0$ that can be used along with eight null vectors available in the dual-inverter. The locus of the vectors producing null v_{zs} is shown in **Figure 19**.

As can be seen in **Figure 19**, the hexagon is divided into six sectors and among the eight null vectors available, only six are finally used (three null vectors per set) [24]. Moreover, the null vectors should be mapped depending on the sector information [24] in order to reduce the commutations in a period. The mapping is shown in **Table 8**.

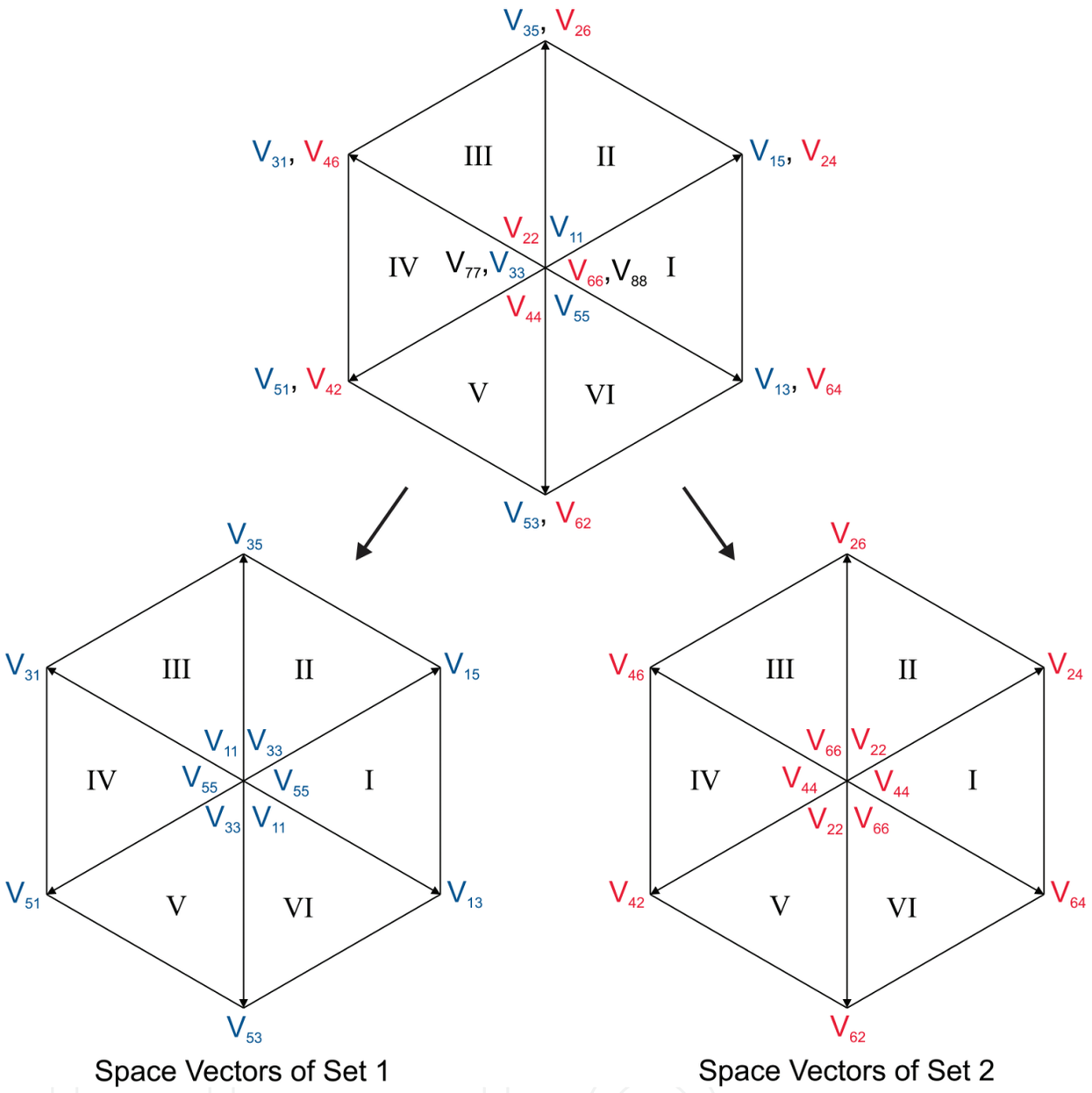

Figure 19. Locus of vectors producing null zero sequence voltage.

From **Tables 6** and **8**, it can be noted that in each sector, one of the inverters keeps clamped in a specific state and the other inverter commutates between three different switching states. This allows reducing the switching losses of the converter output stages.

The zero vectors V_{77} and V_{88} are not considered for this modulation scheme since none of the active vectors (**Table 6**) use the states $V_7 = [111]$ or $V_8 = [000]$ for the individual inverters. Hence, the application of V_{77} or V_{88} in the output stages will result in more commutations per period and thus in higher switching losses than the strategy proposed with the mapping of **Table 8**. However, these zero states are available if vectors redundancy is required.

Sector	I	II	III	IV	V	VI
Set 1 zero vectors	V_{55}	V_{33}	V_{11}	V_{55}	V_{33}	V_{11}
Set 2 zero vectors	V_{44}	V_{22}	V_{66}	V_{44}	V_{22}	V_{66}

Table 8. Mapping of zero vectors.

The space vector modulation presented allows reducing the output zero sequence voltage, then reducing the undesirable effects of the zero sequence currents. Moreover, there is voltage vectors redundancy thus allowing choosing between two equivalent sets of vectors producing the same phase voltage.

5.1.1. Simulation results

The modulation strategy for zero sequence voltage reduction has also been simulated in PSim considering the parameters of **Table 7** and the circuit shown in **Figure 14**, but considering a single DC source to supply both individual inverters. The modulation index used is the maximum possible without overmodulation. The results are shown in **Figures 20–22**. **Figure 20** shows the output phase voltage produced by the dual-inverter (top) and its frequency spectrum (bottom). The output PWM voltage obtained is unipolar and it has a fundamental voltage of 300 V, 50 Hz and harmonic content around the switching frequency (10 kHz). As can be seen, the frequency spectrum is similar to that of SVM for CMV reduction supplying the dual-inverter with a single DC source (**Figure 16**).

The output currents are shown in **Figure 21**. Due to the inductive nature of the load, the high frequency components of the voltage have a negligible effect on the current. **Figure 22** shows

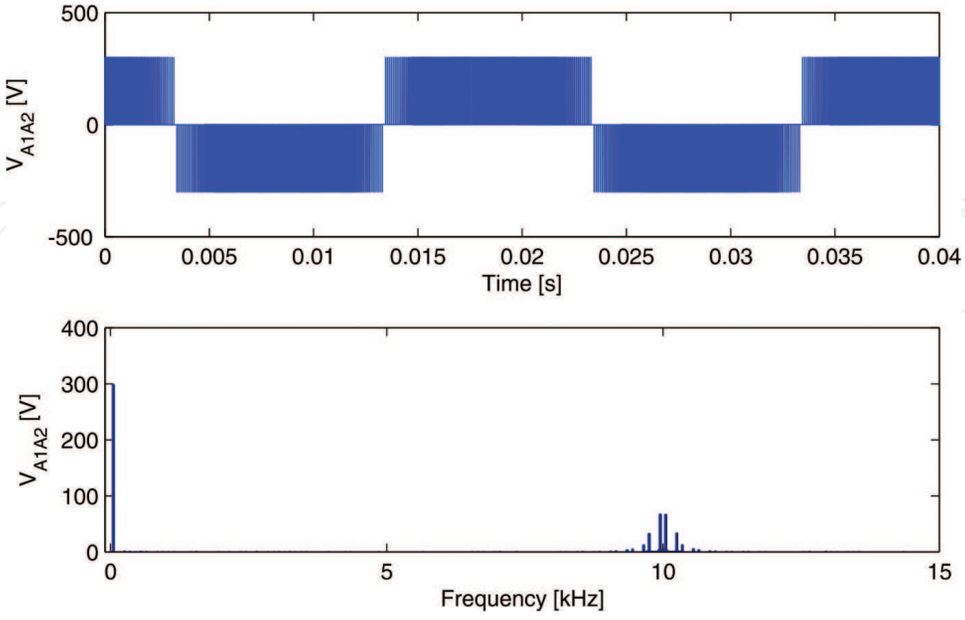

Figure 20. Output phase voltage (top) and its frequency spectrum (bottom) with SVM for reduced ZSV and dual-inverter supplied with single DC source.

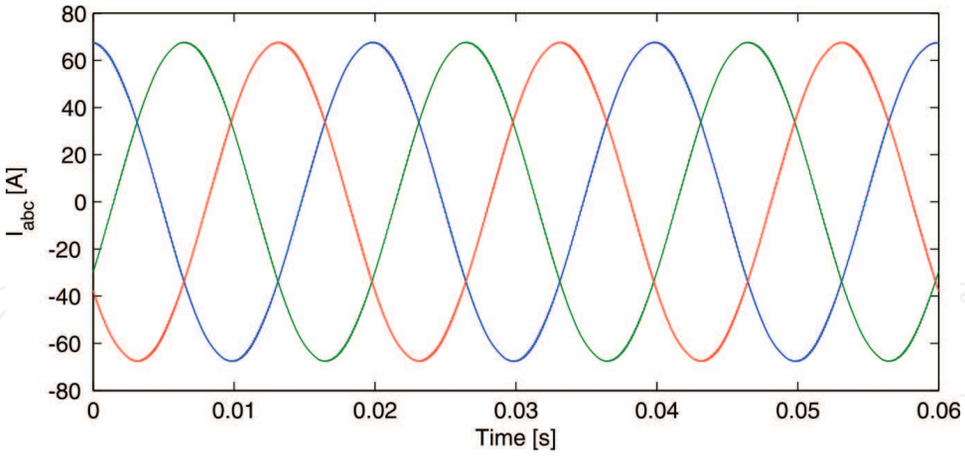

Figure 21. Output currents with SVM for reduced ZSV and dual-inverter supplied with single DC source.

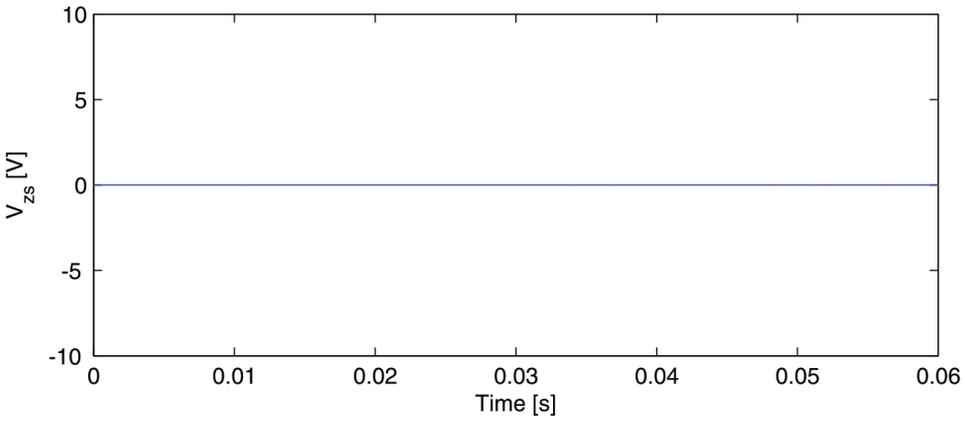

Figure 22. Zero sequence voltage with SVM for reduced ZSV and dual-inverter supplied with single DC source.

the zero sequence voltage that has been eliminated due to the space vectors used in the modulation of the dual-inverter.

5.2. SVM strategy for CMV reduction and ZSV compensation

It has been shown that an open-end load offers the possibility of reducing the common-mode voltage by using certain voltage space vector combinations of the dual-inverter [23], as shown in **Table 4**. Moreover, it has been mentioned that the vectors reducing the common-mode voltage will produce zero sequence voltage as can be noted in **Tables 4** and **5**. Therefore, compensation must be performed in order to avoid the circulation of zero sequence currents in the machine.

The compensation consists on eliminating the average zero sequence voltage within a sampling interval by forcing the zero sequence volt-seconds to zero [18]. This can be done by applying the null voltage vectors with unequal times [18], then modifying the standard switching pattern shown in **Figure 5** and commutating the inverters with the switching pattern of **Figure 23**.

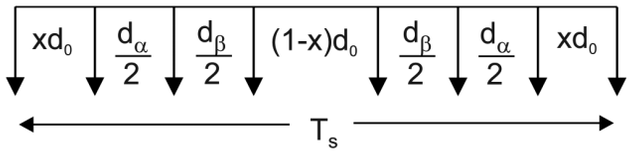

Figure 23. Modified switching sequence.

As it is known which space vector will be applied in every switching period, it can be known what the zero sequence voltage will be in every switching period as well. The value of x, which causes the cancellation of the zero sequence volt-seconds, is calculated at every sampling period to satisfy [18]:

$$2v_{zs1}xd_0 + v_{zs2}d_\alpha + v_{zs3}d_\beta + v_{zs4}(1-x)d_0 = 0 \tag{22}$$

where v_{zsk} with $k = 1,\ 2,\ 3,\ 4$, is the zero sequence voltage value (calculated with Eq. (10)) at intervals xd_0, d_α, d_β and $(1-x)d_0$, respectively.

The x coefficient must be calculated at every switching period to allow a correct reduction of the output zero sequence volt-seconds. The modulation strategy that is presented reduces the common-mode voltage produced by the output VSIs of the power converter and compensates the occurrence of zero sequence voltage.

5.2.1. Simulation results

The modulation for common-mode voltage reduction and zero sequence voltage compensation is simulated considering the parameters shown in **Table 7**. The modulation results in a bipolar PWM waveform can be seen in the output voltage of **Figure 24** (top). **Figure 24** (bottom) shows the frequency spectrum of the output voltage where the high frequency components (around

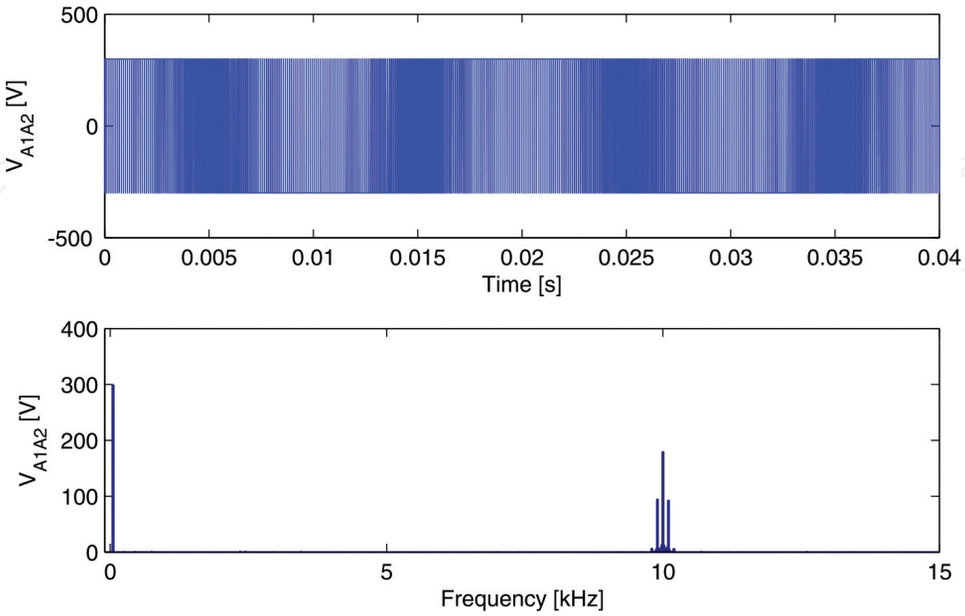

Figure 24. Output phase voltage (top) and its frequency spectrum (bottom) with SVM for CMV-ZSV reduction and dual-inverter supplied with single DC source.

10 kHz) are of higher magnitude than the modulation for zero sequence voltage reduction (**Figure 20**). This is due to the bipolarity of the PWM.

The output currents are shown in **Figure 25**, where it can be noted that zero sequence components are not present due to compensation method used. **Figure 26** shows the common-mode voltage that has been eliminated due to the space vectors used in the modulation.

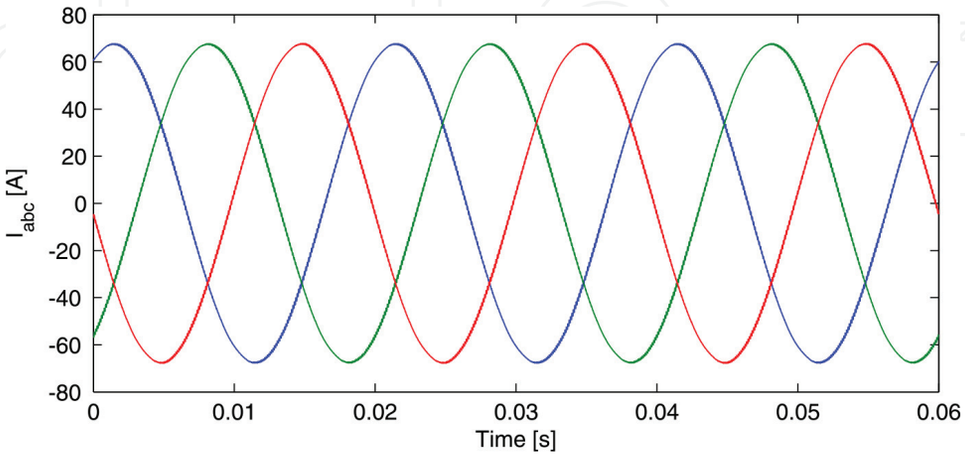

Figure 25. Output currents with SVM for CMV-ZSV reduction and dual-inverter supplied with single DC source.

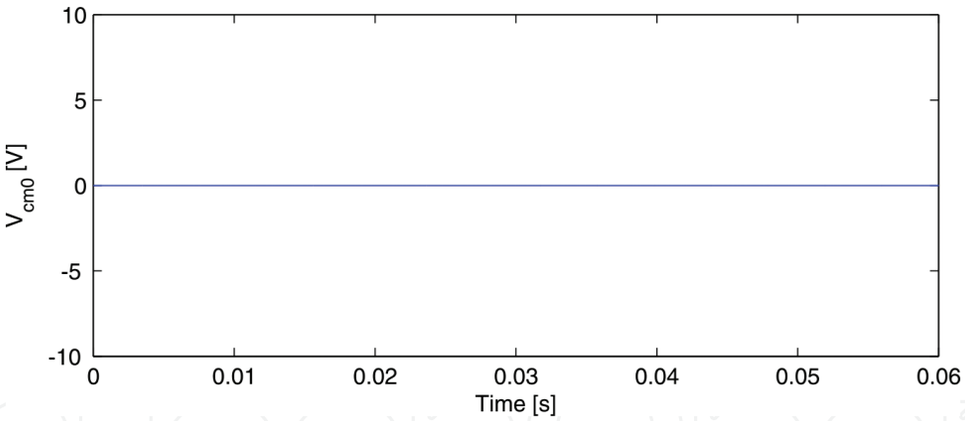

Figure 26. Common-mode voltage with SVM for CMV-ZSV reduction and dual-inverter supplied with single DC source.

6. Multilevel topologies

Several multilevel power converters have been developed for open-end loads, specifically open-end winding drive. For example, **Figure 27a** shows a three-level inverter [33] and **Figure 27b** shows a five-level inverter [34]. It can be noted that the five-level inverter presents the same topology of the three-level inverter but considering isolated DC supplies. The main advantage of the multilevel topologies is that the machine phase voltage presents lower voltage distortion increasing the performance of the drive but on the other hand, the complexity and cost of the system is also increased.

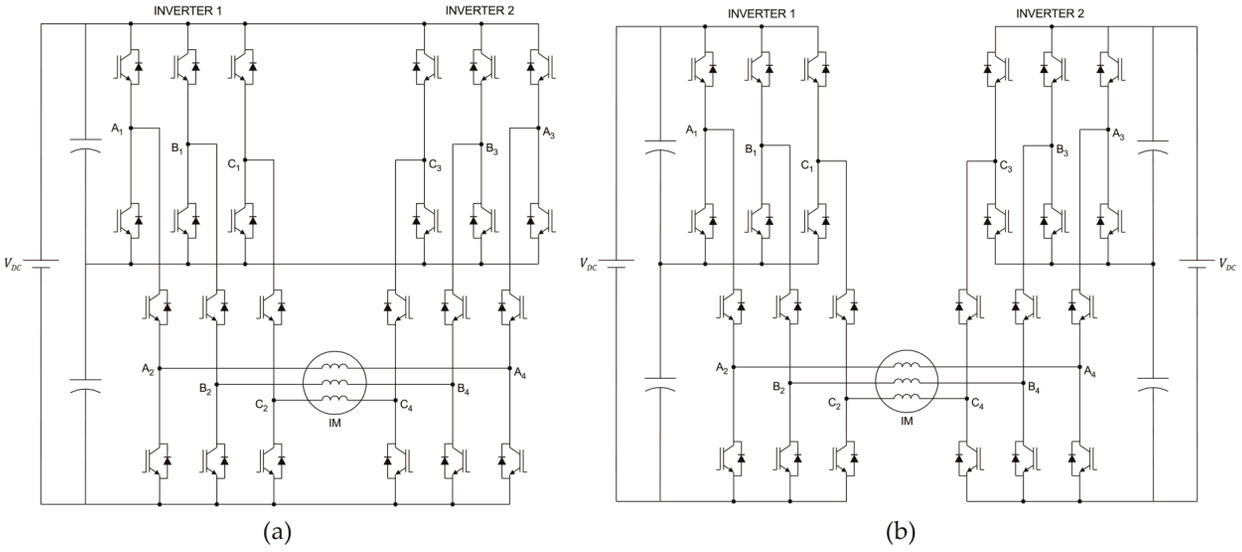

Figure 27. (a) Three-level inverter and (b) five-level inverter for open-end winding AC machine drives.

6.1. Carrier-based modulation strategy

In a standard two-level inverter, a sinusoidal (carrier-based) pulse width modulation (SPWM) strategy requires the comparison of a triangular wave (carrier) with a sinusoidal reference signal (**Figure 3**). However, in multilevel inverters, more than one carrier signals are needed to perform a SPWM strategy [35]. Considering the five-level inverter of **Figure 27b**, four triangular carriers are required to be compared with three sinusoidal reference signals (one reference signal for each phase). The carriers and a reference signal for one phase are shown in **Figure 28**. The reference

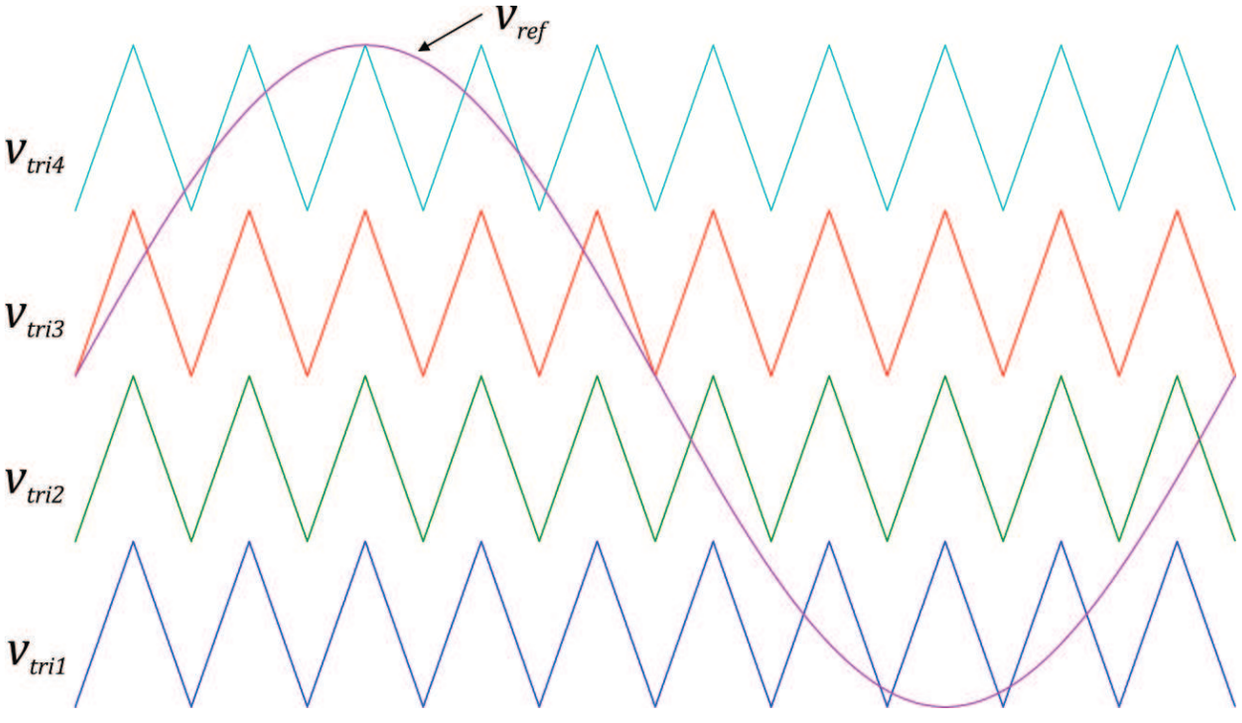

Figure 28. Signals used in a five-level carrier-based modulation strategy (one phase of the inverter).

signals of the other two phases are phase-shifted ±120° and the control logic for triggering the power devices of the converter is similar to that shown in Section 1.

6.1.1. Simulation results

A SPWM strategy for a five-level dual-inverter is simulated in PSim platform. The circuit implemented in PSim is basically the same as **Figure 14**, but the sub-circuits inside VSI1 and VSI2 are those corresponding to the five-level inverter shown in **Figure 27b**. The simulation considers the parameters of **Table 7**.

Figure 29 shows the output phase voltage (top) and its frequency spectrum (bottom). The benefit of five-level operation in terms of voltage quality can be noted in the almost negligible harmonic content of the waveform. The output currents are shown in **Figure 30** which presents a sinusoidal waveform due to the inductive nature of the load.

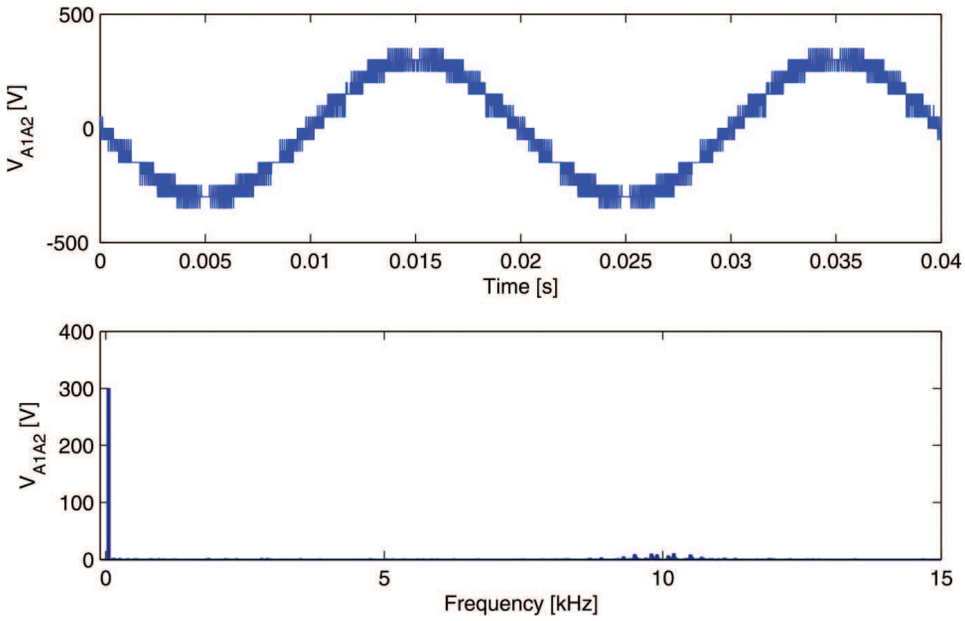

Figure 29. Output phase voltage (top) and its frequency spectrum (bottom) with SPWM for five-level inverter.

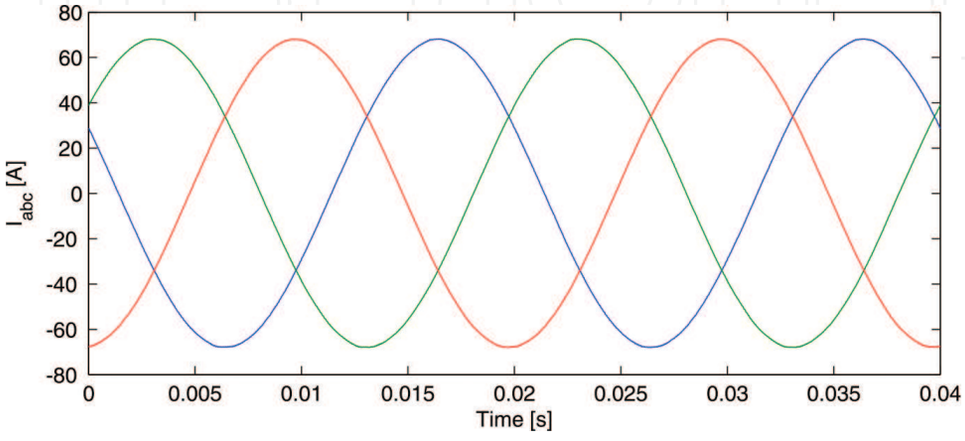

Figure 30. Output currents with SPWM for five-level inverter.

7. Conclusion

The dual-inverter circuit to supply open-ended loads has been presented. The possibility of supplying the VSI either from different or the same DC voltage sources have been emphasized, stating the main advantages and disadvantages of both alternatives. The main features of the topology have been studied and different modulation strategies have been developed attending the reduction of common-mode voltage when the topology uses different DC power sources and the reduction of common-mode voltage and/or zero sequence voltage when the topology uses a single DC power supply for both VSIs. Simulation results showing the performance of the modulation strategies proposed have been presented where isolated and non-isolated DC power supplies have been considered. Moreover, multilevel dual-inverter circuits have been discussed as an alternative to produce higher quality voltages and a standard SPWM strategy has been commented and simulated. The results are encouraging and demonstrate the applicability of the topology for open-end terminal loads.

Acknowledgements

This work was funded by The Chilean Research Fondecyt Grant 1151325 and by CONICYT/FONDAP/15110019. The financial support given by University of Bío-Bío Research Project N°GI160510 EF is also acknowledged.

Nomenclature

AC	Alternating-current
CMV	Common-mode voltage
DC	Direct-current
EMF	Electromotive force
IGBT	Insulated gate bipolar transistor
NPC	Neutral point clamped
PMSM	Permanent magnet synchronous motor
PWM	Pulse width modulation
SPWM	Sinusoidal (carrier-based) pulse width modulation
SVM	Space vector modulation
THD	Total harmonic distortion
VSI	Voltage source inverter
ZSV	Zero sequence voltage

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