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Operational Amplifier Design in CMOS at Low-Voltage for Sensor Input Front-End Circuits in VLSI Devices

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Abstract

Today, digital circuit cores provide the main circuit implementation approach for integrated circuit (IC) functions in very-large-scale integration (VLSI) circuits and systems. Typical functions include sensor signal input, data storage, digital signal processing (DSP) operations, system control and communications. Despite the fact that a large portion of the circuitry may be developed and implemented using digital logic techniques, there is still a need for high performance analogue circuits such as amplifiers and filters that provide signal conditioning functionality prior to sampling into the digital domain using an analogue-to-digital converter (ADC) for analogue sensor signals. The demands on the design require a multitude of requirements to be taken into account. In this chapter, the design of the operational amplifier (op-amp) is discussed as an important circuit within the front-end circuitry of a mixed-signal IC. The discussion will focus on the design of the op-amp using different compensation schemes incorporating negative Miller compensation and designed to operate at lower power supply voltage levels. A design case study is included which utilises the g_m/I_D ratio design approach to determine the transistor sizes. The simulation approach is focussed on the open-loop frequency response performance of the op-amp.

Keywords: op-amp, design, stability, g_m/I_D , Miller compensation, negative Miller compensation

1. Introduction

In this chapter, the focus of the discussion is on the design of the op-amp, which will act as an integral part of the on-chip analogue signal conditioning circuitry for the front-end section of a

Figure 12. MOSFET characteristics: (a) g_m/I_D ratio versus normalised current ($I_D(W/L)$) and (b) transit frequency (f_T) versus g_m/I_D ratio.

5.2.1. Strong inversion

When v_{GS} is higher than the threshold voltage V_T , the inversion channel is strongly created, and the drift current is dominant. The classical quadratic i_D - v_{GS} MOSFET equation is based on this condition. The value for g_m in strong inversion is independent of MOSFET sizing and process parameters, and it depends only on the DC bias conditions, I_D and v_{eff} . Similarly, g_m/I_D depends only on v_{eff} and the transistor has a small g_m/I_D , a high gate-source voltage, a high drain current, a high f_T , low noise and small dimensions (width and length).

5.2.2. Moderate inversion

The transition between weak inversion and strong inversion is called moderate inversion. Moderate inversion is important for modern analogue CMOS circuit design where designs are created to operate the MOSFET in this condition. Moderate inversion presents a higher g_m/I_D ratio and a lower gate-source voltage in relation to strong inversion combined with smaller gate area and capacitance, and a higher bandwidth compared to weak inversion.

5.2.3. Weak inversion

In weak inversion, the drain current can be determined using an exponential expression. The transistor has a large g_m/I_D , a low gate-source voltage, a low drain current, a low f_T , high noise and large dimensions (width and length).

Each channel inversion condition has different performance characteristics and a circuit design would then be optimised to account for these characteristics. Given that a design can be created by either using the conventional design approach or the g_m/I_D ratio design approach, **Table 1** provides a summary comparison between the approaches.

g_m/I_D design approach	Conventional design approach using V_T , KP and λ
Is valid in all channel operating conditions (weak, moderate and strong) of the MOSFET.	Is valid only in strong inversion of the MOSFET.
Not necessary to create the condition $V_{GS} > V_T$.	Valid only if $V_{GS} > V_T$.
There are different curves for g_m/I_D depending on the inversion region.	Uses the I_D versus V_{GS} and I_D versus V_{DS} curves.
Used for circuits operating on lower power supply voltage levels.	Used for circuits operating on higher power supply voltage levels.
A simplified technique suitable for new evolving fabrication process technologies.	Not suitable for new evolving fabrication process technologies.
A fast design technique as the equations that model the electrical behaviour of circuits can be signified by g_m/I_D .	Not appropriate as a fast design technique. It does not have compact electrical models capable of simple current and voltage relationships.
In this design approach, V_{GS} should be kept as small as possible and transistor gate-source capacitance should be small as possible.	If $(V_{GS} - V_T)$ is small, a large geometry device is required and thus large transistor gate-source capacitance.
The g_m/I_D ratio is used directly as a central design variable to determine circuit performance.	The g_m/I_D ratio is not directly used to determine the performance of the circuit.
Links the variables such as g_m , f_T , I_D and V_{eff} to specifications such as bandwidth and power.	Parameters such as μC_{ox} , V_T and $v_{DS(sat)}$ are considered as poorly defined parameters.
Uses charts and simple equations.	Depends on complex equations and sometimes based on assumptions such as ignoring the effect of channel length modulation (λ).
The g_m/I_D ratio associates small-signal and a large-signal ($g_m \rightarrow I_D$) parameters.	Small- and a large-signal models are not associated.

Table 1. Differences between the g_m/I_D ratio design approach and the conventional design approach.

6. Case study op-amp design

6.1. Introduction

The op-amp is an important differential amplifier circuit that has formed the basis of many analogue and mixed-signal IC designs. In this design case study, a two-stage op-amp has been designed and internally compensated by using negative Miller capacitance in the first stage and Miller capacitance in the second stage as shown in **Figure 5**. The idea behind this approach was to develop circuit stability using Miller compensation and increase the bandwidth using negative Miller compensation. The op-amp was designed using the g_m/I_D ratio design approach in order to consider low-voltage operation and is based on the architecture shown in **Figure 5**, with the circuit as shown in **Figure 6**. When operated on a 3.3 V power supply voltage, the MOSFETs operate in moderate inversion to optimise DC gain, unity gain frequency, PM and GM. The op-amp operation was simulated using Cadence Spectre simulator, the MOSFET models were based on a 0.35 μm CMOS fabrication process, and the AC performance both without and with an output load capacitance was assessed in simulation. A differential input voltage was applied to the op-amp in open loop and a single-ended output voltage monitored.

6.2. Op-amp simulation and results

The op-amp simulation study was performed with two conditions: first, no output load capacitance and second, with a variable output load capacitance. An AC analysis was performed on the op-amp design using typical transistor models with the transistors biased for a 3.3 V single-rail power supply voltage operation.

6.2.1. Study 1: without output load capacitance

In this study, the simulation approach and results obtained concentrated on the frequency response by using the op-amp with different internal compensation techniques and no output load capacitance. First, no internal compensation was incorporated and then compensation using Miller, negative Miller and a combination of Miller and negative Miller arrangements were considered. **Table 2** shows the results of the simulation study that are shown in Bode plot format in **Figure 13**.

For the op-amp with no compensation and negative Miller compensation only, the GM was a positive number (based on the simulator output value), and hence, the op-amp would be unstable in closed loop. In addition, with these two scenarios, the PM was negative (simulator output value) and this also indicated that the op-amp would be unstable in closed-loop. The results show that the gain magnitude and phase shift are controllable with the different

C_{NM} and $C_M = 0.31$ pF	No compensation	Negative Miller only	Miller only	Miller and negative Miller
DC gain (dB)	82.5	82.5	82.5	82.5
Phase margin (degrees)	-65.19	-52.56	57.47	63.03
Unity gain frequency (MHz)	1073	1177	177.33	205.54
Gain margin (dB)	14.27	11.08	-10.61	-9.93

Table 2. Open-loop op-amp performance with different compensation techniques.

Figure 13. Bode plot of the open-loop op-amp performance with different compensation techniques: (a) gain and (b) phase (Spectre simulation on the transistor circuit model).

compensation techniques and that the choice of compensation technique would determine whether the op-amp is stable or not in closed loop.

6.2.2. Study 2: with output load capacitance

In this study, the simulation approach and results obtained concentrated on the frequency response by using the op-amp with different internal compensation techniques and an output load capacitance with values of 0.1, 0.5 and 1.0 pF. **Table 3** shows the results of the simulation study that are shown in Bode plot format in **Figure 14**.

6.3. Transfer function analysis

An additional form of analysis undertaken with this design was to consider the transfer function for the op-amp input-output relationship. The transfer function is a useful form for evaluating the op-amp frequency response. For a typical op-amp, then the transfer function would contain a large number of poles and zeros. This form would be too complex for initial design development, and so it is common to approximate the transfer function to a simple form that contains typically only two or three poles. These can be estimated from the small-signal equivalent circuit. In addition, once the op-amp design has been created, it is possible to extract the poles and zeros using the circuit simulator and to minimise the initial transfer function of the circuit model having large number of poles and zeros into a simpler transfer

Characteristic	No output load capacitance	0.1 pF	0.5 pF	1.0 pF
DC gain (dB)	82.5	82.5	82.5	82.5
Phase margin (degree)	63.03	61.39	55.99	50.96
Unity gain frequency (MHz)	205.54	203.83	195.54	183.38
Gain margin (dB)	−9.93	−9.80	−9.44	−9.23

Table 3. Open-loop op-amp performance with different output load capacitance values (with combined Miller and negative Miller compensation).

Figure 14. Frequency response of the open-loop op-amp design with different load capacitances: (a) gain and (b) phase (Spectre simulation on the transistor circuit model).

function having a reduced number of poles and zeros. The process for investigating the circuit operation and simplifying the transfer function considered was to:

1. Extract the poles and zeros from the circuit model using Cadence Spectre simulator.
2. Transfer the pole and zero values to MATLAB and create the transfer function.
3. Use MATLAB to reduce the number of poles and zeros in the transfer function and simulate the transfer function behaviour to ensure that the reduced transfer function Bode plot and key characteristics are comparable to the original transfer function.
4. Translate the new transfer function to high-level Verilog-A model and compare the Verilog-A model to the original analogue circuit simulation results and the MATLAB simulation study results.

From the analysis of the open-loop op-amp pole and zero locations as extracted from the circuit, the initial transfer function consisted of 23 poles and 23 zeros. Although it would be expected that the number of poles should be greater than the number of zeros in the transfer function for a strictly proper system, the original 23 pole and zero transfer function extracted is used in the following discussion, and hence, the results are used with a certain level of caution. These were the raw results obtained from the pole-zero analysis in Spectre. It should be noted that the transfer function has the same number of poles and zeros and hence would be referred to as a biproper system. When the transfer function is biproper, it is not reflective of a realisable system at high frequencies as it would have a finite gain at the higher signal frequencies. A strictly proper system where the gain reduces to zero at higher frequencies, as would be expected in a real op-amp, the number of poles must be greater than the number of zeros. This effect can be seen when simulating the transfer function for this design at the higher signal frequencies that would not actually be encountered. To simplify this transfer function from original number of poles and zeros, MATLAB was used to reduce the transfer function to one with just three poles and zeros. **Table 4** shows the resulting performance of the different simulation models, noting that the response of the three models would be valid only up to a certain frequency as the

Number of poles/zeros	Performance	Spectre	MATLAB	Verilog-A
23/23 (MATLAB and Verilog-A transfer function models only)	Gain margin (dB)	9.938	9.95	9.938
	Unity gain frequency (MHz)	205.5	198	205.5
	Phase margin (degrees)	63	63	63
	DC gain (dB)	82.47	82.5	82.47
3/3 (MATLAB and Verilog-A transfer function models only)	Gain margin (dB)	–	10.7	10.64
	Unity gain frequency (MHz)	–	192	200.8
	Phase margin (degrees)	–	54.4	54.61
	DC gain (dB)	–	83.9	83.88

Table 4. Simulated op-amp performance comparison (Spectre (transistor level model), MATLAB (transfer function) and Verilog-A (transfer function)).

transfer functions model a biproper system with a finite high frequency gain rather than a realistic strictly proper transfer function.

7. Op-amp design and operation at lower power supply voltages

Designing and operating analogue circuits at low power supply voltages are challenging tasks. In the past, the circuits typically encountered were designed to operate at higher voltage levels, and so circuit performance limitations due to a limited voltage range was not an issue for many designs. Today, the operation of electronic circuits with low-voltage power supplies is now a requirement for use in electronic systems where size, weight, and power consumption are especially important. For example, in battery-operated portable equipment, a reduction in the battery requirements such as size, weight and energy capacity can provide cost reduction benefits in equipment production, purchase and use as well as making the equipment more portable. The move towards low-voltage operation can be considered from three different perspectives:

1. The increasing use of battery-operated portable systems requires low-power dissipation in order to prolong circuit operation time with a battery energy source.
2. Reduced feature sizes in modern VLSI fabrication processes results in larger electric fields that, unless the power supply voltages are reduced, result in reliability problems.
3. Reduced feature sizes in modern VLSI fabrication processes results in a higher density of the electronics that increases the power dissipation per unit area. The low-voltage operation can be used to reduce the power dissipation per unit area.

As device geometries in CMOS are reduced, the benefits include reduced size, higher operating speeds and reduced power consumption (due to the ability to operate the designs on lower power supply voltage levels), which are mostly exploited in the digital parts of a design. However, this move comes at a cost of introducing device characteristics not seen with larger device geometries. Reducing the power supply voltage has been exploited effectively in digital circuits, but analogue circuits exploiting reduced geometry and voltage operation need to account for a range of circuit performance limiting issues not a concern in digital. In analogue circuits, reducing device geometries and power supply voltage levels have an enormous impact on the analogue circuit capability. For example, as the device geometries become smaller and circuit densities increase, currents in the circuit may need to be reduced in order to prevent excessive temperature increments due to the power consumption per unit area. In addition, reliability problems would exist at higher voltage levels (voltage levels which were commonly used in the past, such as 5 V, but now would be too high for reliable circuit operation) due to excessively high electric fields that would exist. Process variations as CMOS technology move to the lower (deep) sub-micron levels and their effects on low geometry devices, such as transistor width and length dimensions, means that analogue circuit performance can vary widely between devices of the same type and this is accompanied in reduced device geometries by an increase in transistor leakage currents. Whilst the geometries reduce, the transistor threshold voltage (V_T) is, however, remaining relatively constant, and as the power supply voltage is reduced, this causes as

reduction in the available voltage range for circuit operation (a reduction in the $(V_{DD} - V_T)$ value). Analogue circuits would typically require the creation of bias currents for circuits such as current mirrors which are created using transistors. The need to account for the transistor to be operating in either the weak, moderate or strong inversion regions of operation and the resulting transistor performance differences due to the region of operation would need to be accounted for. The use of fully differential structures is considered given their superior performance with circuit parameters such as *CMRR* and *PSRR* (power-supply rejection-ratio), lower signal distortion and wider signal swing range. Finally, the need to maximise dynamic signal range which often requires a rail-to-rail output voltage range and for op-amps operated in unity-gain configuration, the input stage should also have a rail-to-rail common mode input voltage range [9].

8. Conclusions

The op-amp is an integral part of the on-chip analogue signal conditioning circuitry for the front-end section of mixed-signal ICs. In this chapter, the design of the two-stage op-amp was considered, which was designed using a 0.35 μm CMOS fabrication process and working on a single rail 3.3 V power supply. Considerations were given to low-voltage design (operating at and below 3.3 V) by using the g_m/I_D ratio design approach and the use of both Miller and negative Miller compensation as an internal compensation scheme for op-amp stability and signal bandwidth reasons. The discussion was accompanied by an op-amp case study design and simulation study results that focused on AC performance.

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