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Library-Based Gate-Level Current Waveform Modeling for Dynamic Supply Noise Analysis

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1. Introduction

As the VLSI technology goes into the nanometer era, the device sizes and supply voltages are continually decreased. The smaller supply voltage reduces the power dissipation but also decreases the noise margin of devices. Therefore, the power integrity problem has become one of the critical issues that limit the design performance (Blakiewicz & Chrzaniwska-Jeske, 2007; kawa, 2008 & Michael et al., 2008). Most of the power supply noises (PSNs) come from two primary sources. One is the IR-drop and the other is the simultaneous switching noise (SSN). Figure 1(a) illustrates a typical RLC model for power supply networks, which is the combination of on-chip power grids and off-chip power pins. The IR-drop is a power supply noise when the supply current goes through those non-zero resistors and results in a I·R voltage drop. The simultaneous switching noise (SSN) is the supply noise which happens when large instantaneous current goes through those non-zero inductors on power networks and generates a L·(di/dt) voltage drop. When the supply voltage is reduced , the noise margin of devices also decreases as shown in Fig.1(b). It may induce worse performance because the driving capability of devices becomes week due to smaller supply voltage. If serious power supply noise occurs, the logic level may be changed, which causes function error in the circuit. The worst situation is the electron-migration (EM) effects. Supply wires are shorten or broken because a large current travels through the small supply wires. Therefore, the power supply noise analysis is reguired at design stages to evaluate the effects caused by power supply noise.

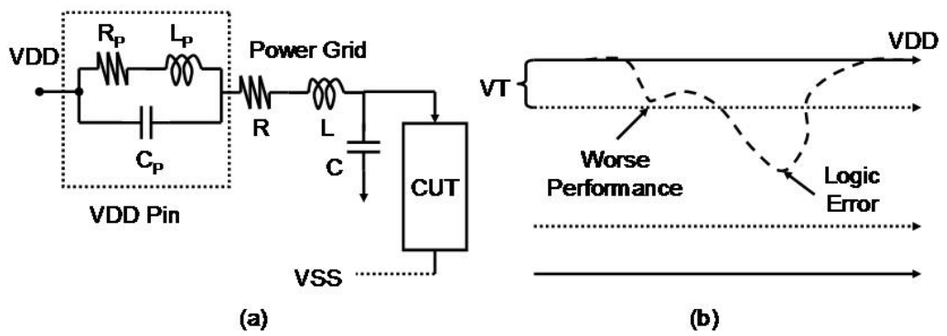
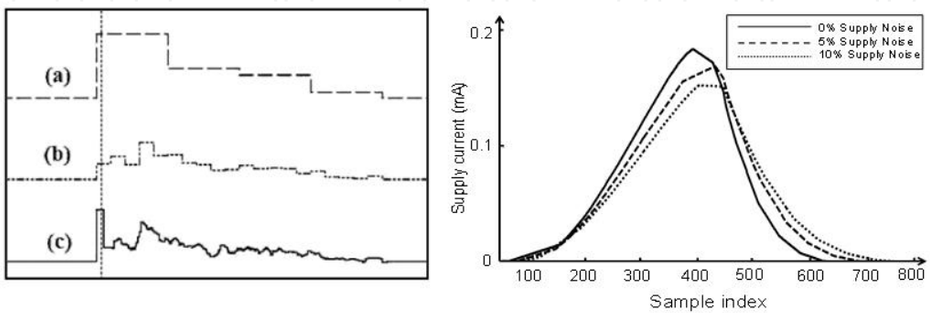


Fig. 1. (a)RLC model for power supply (b) Supply Voltage over Time at Silicon Device.

While esimating the power supply noise, both the magnitude and slope of supply currents are required. Traditionally, accurate supply current waveforms can only be obtained from the transistor-level simulation. Therefore, in the present design flow, the power supply noise (PSN) check is mostly performed at very late design stage. Although the analysis results are accurate at transistor level, this approach may be impractical for large designs because simulating the entire design at transistor level requires great computation resources. If any problem is found, the designers often tune the width of the supply lines or add another current path to fit the specification. However, if the supply current waveforms are obtained at early stage, more efficient low-power technologies, like multiple supply voltages and power-gating, can be used to reduce the supply power and noise (Chen et al., 2005; Juan et al., 2010; Kawa, 2008; Michael et al., 2008; Popovich et al., 2008; Xu et at., 2011 & Zhao et al. 2002). The primary reason of lacking tools for checking the power integrity problems at gate level or higher levels is the limited design information, that current cannot provide waveforms directly. In this research, we propose the gate-level IR-drop analysis method with limited design information to build the missing link of the traditional design flow.

The most popular format to store the gate-level information is the liberty format (LIB) (Synopsys, 2003). The LIB file of a cell library keeps the information of all cells and is widely used in the synthesis and timing analysis at gate level and RT level. However, due to the format limitation, only timing information and average energy consumption are kept in LIB files. They cannot provide instantaneous supply current information directly. One straightforward approach is to approximate the instantaneous supply current using the average power divided by the user-given time interval as illustrated in Fig. 2(a). However, even if the average power is the same, the waveforms can be quite different with different time intervals. It may not be accurate enough to estimate real instantaneous supply current.

Several advanced library formats have been proposed for recording voltage waveforms (ECSM) (Candence, 2006) or current waveforms (CCSM) (Synopsys, 2008) to provide the more accurate timing and power information. These formats need large storage space to record these piece-wise-linear waveforms. Therefore, those new formats are only used in very advanced process, like 65 nm technology. Typically, the libraries with new formats are used to support the static timing analysis to obtain more accurate estimation. It may also support the gate-level power estimation to obtain more accurate peak power. However, because the peak power is often evaluated in the cycle-accurate basis at gate level, it will suffer the same time-interval issue.



(a) (b)

Fig. 2. (a) The power waveforms with different time intervals (b) The current waveforms with different supply noises

In the literature, the authors in (Boliolo et al., 1997) propose an approach to estimate power supply noise at gate level. In their approach, the capacitance of each internal node in a cell, the energy consumption of each transition, and several regression equations representing the timing behavior, are required to estimate the supply current waveforms. Given an input pattern to a cell, its supply current will be approximated as a simple triangle, whose area is the total energy. The base and the height of this triangle are obtained from the regression equations. Then, combining all triangles of every changed cell in time obtains the overall supply current waveform. This approach is a practical solution that can be combined with logic simulation tools. The results shown in the paper are also accurate. However, the required timing behaviors of supply current waveforms are not available in standard library files. Extra characterization efforts for different cell libraries are still required before using this approach, which is a very time-consuming process.

In anthor work (Shimazaki et al., 2000), the authors propose an EMI-noise analysis approach based on a rough supply current waveform. Although their approach also uses standard library infotmation, their current waveform estimaiton approach is too simple to provide accurate supply current waveforms. Most importantly, their approach can be used in combination caircuits only, which is not feasibal for modern complex designs. Therefore, an accurate gate-level supply current model using standard library information, even for sequential circuits, is propsed to avoid addtional charcterization process (Lee et al., 2008).

The proposed current model has provided the solutions to estimate the ideal supply current waveforms without noise effects. However, the estimated waveforms cannot be directly used to analyze IR-drop effects because the supply currents will have significant difference with non-zero resistance on the supply lines. Figure 2(b) shows an example obtained from the c432 circuit suffering from different supply noises. In typical cases, the current with supply noise is less than the ideal current. If the ideal supply current waveforms are used to calculate the IR-drop, the results are often overestimated. The direct solution to consider the effects of IR-drop is to extend the libraries with different supply resistors. However, this approach will greatly increase the storage space and characterization efforts for library information, which may be not a good solution. Therefore, a library adjustment method is also proposed to consider the IR-drop effect on supply current modeling with standard library information (Lee et al., 2010).

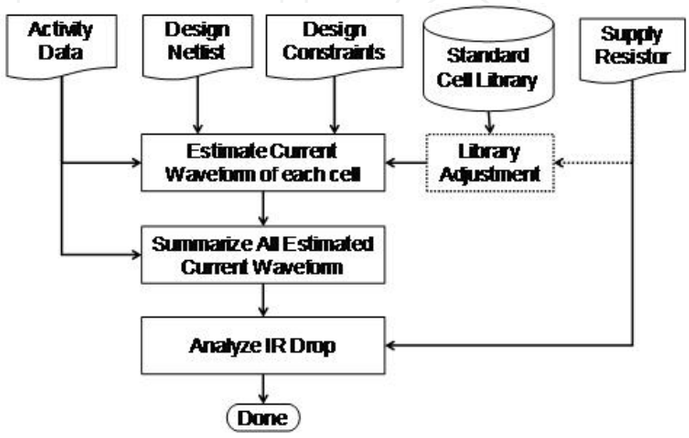


Fig. 3. The proposed gate-level IR-drop analysis flow

The proposed gate-level IR-drop analysis flow is illustrated in Fig.3. According to the cell switching from gate-level activity files, the corresponding supply current waveform of each cell can be constructed by using standard library information. The supply current waveforms obtained from the original standard libraries are then modified to consider IR-drop effects. Second, the estimated supply current waveforms of all switching cells are summarized in time to obtain the supply current waveforms of the whole circuit. Finally, the IR-drop voltage caused from the supply resistor can be derived from the current waveform.

The rest of this article is organized as follow. In Section 2, the most popular library format, the liberty format, is presented. A gate-level supply current waveform estimation method using standard library information is proposed in Section 3. A correction method of the library information is also proposed to modify the IR-drop effect in Section 4. The experimental results of this work are demonstrated in Section 5 and a simple conclusion is presented in Section 6.

2. Standard library: Liberty format (LIB)

Liberty format (LIB) (Synosys, 2003) is the most popular library format at gate level to store the timing information and the average energy consumption of each cell in the standard library. Those data are stored using some look-up tables. The definitions of some commonly used variables are listed as follows. They will be used later to derive the proposed current waveform model.

Transition Time: This is defined as the duration time of a signal from 10% to 90% VDD in the rising case and from 90% to 10% VDD in the falling case. TR(X) is defined as the transition time of the node X in the rising case. TF(X) is defined as the transition time of the node X in the falling case.

Propagation Time: This is defined as the duration time from the input signal crossing 50% VDD to the output signal crossing 50% VDD. TDR(X→Y) is defined as the propagation delay from the related pin X to the output Y when the output Y is rising. D represents the propagation delay and R represents the rising case. TDF(X→Y) is defined as the propagation delay from the related pin X to the output Y when the output Y is falling. F represents the falling case.

Setup Time: This is a timing constraint of the sequential cell, which is defined as the minimum time that the data input D must remain stable before the active edge of the clock CK to ensure correct functioning of the cell. In other words, it is the duration from D crossing 50% VDD to CK crossing 50% VDD if the output value can be evaluated successfully. TSR(D) is defined as the setup time when the data input D is rising. S represents the setup time and R represents the rising case. TSF(D) is the setup time when the data input D is falling. F represents the falling case.

Load: This is the total capacitance at a node. Load(Y) is defined as the capacitance at the node Y.

Internal Power: This is the internal energy consumption of a cell without the energy consumed on its output loading. E_{INT} is defined as the internal energy consumption of the cell.

Changing Time: T(X) is defined as the time that the signal X is crossing 50% VDD, which is the signal transition point in logic simulators recorded in VCD (Value Changed Dump) files.

Voltage Definitions: VDD is defined as the supply voltage. VT is defined as the threshold voltage of the transistor.

3. Current waveform estimation using library information

In order to avoid extra characterization efforts while migrating to new cell libraries, a supply current model is proposed based on standard library information. The key idea is using a triangular waveform to approximate the real supply current waveform generated by a cell switching as shown in Fig. 4. Then, the parameters of the triangle are calculated by standard library information only. Finally, the overall supply current waveform can be obtained by combining all triangles of every changed cells in time. Before presenting the proposed approach, some variables must be defined first. For each triangle shown in Fig. 4, four variables, T_{START}, T_{END}, T_{PEAK} and I_{PEAK}, are defined to represent the triangular waveform. T_{START} and T_{END} are the start/end time of the supply current waveform. These two variables define the duration of the waveform. T_{PEAK} and I_{PEAK} are the location and current value when the maximum supply current occurs.

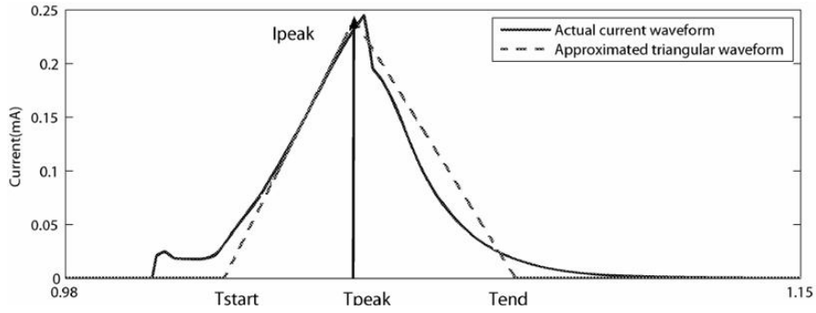


Fig. 4. The definition of the triangular current waveform

Although there are a lot of cells in a cell library, most of them can be classified into three categories in our approach. In the following sections, the formulas to construct the current waveform model in each category will be presented. During the formula construction, this work assumes that only the LIB file is available. Therefore, the transistor-level netlist and detailed device sizes are avoided. If some general structures are required to build the formulas, only the information provided in the library data sheet will be used. While applying the proposed methodology to different libraries, users can make necessary adjustment easily from that public information.

3.1 Simple logic cells

If the CMOS implementation of a cell is a single layer structure, it is called a simple logic cell in this work, such as **INVERTER**, **NAND**, **NOR** as shown in Fig. 5. Those cells can be modeled as an equivalent inverter with two parts, the equivalent PMOS and NMOS. Therefore, in the following discussion, an inverter is used as an example to discuss its supply current model in the charging period (the output signal is rising) and the discharging period (the output signal is falling).

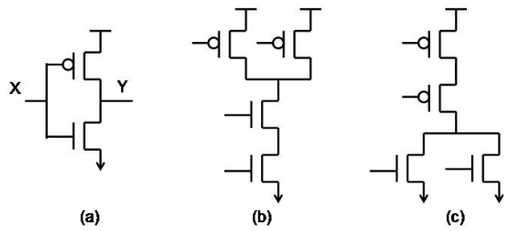


Fig. 5. The structures of simple logic cells (a) INVERTER (b) NAND (c) NOR

3.1.1 Charging period

In the charging period, the relationship between the input signal X, the output signal Y and the timing parameters of the triangular waveform can be illustrated in Fig. 6. T_{START} is defined as the time that the input voltage achieves (VDD-VT) because the equivalent PMOS turns on at this time. The corollary of T_{START} is shown as follows.

$$\frac{T_{START} - [T(X) - 0.625 \times TF(X)]}{VT} = \frac{1.25 \times TF(X)}{VDD}$$
$$\Rightarrow T_{START} = T(X) - 1.2 \times TF(X) \times \frac{0.5 \times VDD - VT}{VDD} \quad (1)$$

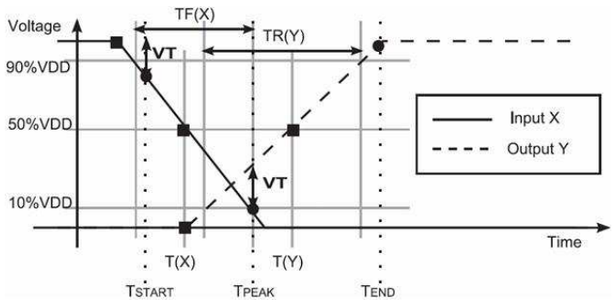


Fig. 6. The parameters of a simple cell in the charging period

In typical cases, the shape of the charging current for a simple logic cell is similar to a RC charging behavior. Therefore, the exponential RC charging function is used to approximate this behavior. Theoretically, T_{END} is defined as the time when the output loading is charged to VDD. However, due to the long tail of the RC charging curve, T_{END} is defined as the time that the output loading is charged to 95% VDD in this work to reduce the error while the waveform is simplified to a triangle. The corollary of T_{END} is shown as follows, where τ is the RC time constant.

$$V(t) = V_0 \times (1 - e^{(\frac{-t}{\tau})}) \Rightarrow t = \ln(\frac{V_0 - V(t)}{V_0}) \times \tau$$

$$\begin{cases} t_{10\%VDD} = \ln(\frac{VDD - 0.1 \times VDD}{VDD}) \times \tau \\ t_{90\%VDD} = \ln(\frac{VDD - 0.9 \times VDD}{VDD}) \times \tau \end{cases} \Rightarrow TR(Y) = [\ln(0.9) - \ln(0.1)] \times \tau \Rightarrow \tau = \frac{TR(Y)}{\ln(9)}$$

$$\begin{cases} t_{0\%VDD} = \ln(\dfrac{VDD}{VDD}) \times \tau \\ t_{50\%VDD} = \ln(\dfrac{VDD - 0.5 \times VDD}{VDD}) \times \tau \end{cases}$$
$$\Rightarrow TD[V(Y = 0\%VDD) \rightarrow V(Y = 50\%VDD)] = \ln(0.5) \times \tau$$

$$\begin{aligned} & T_{END} \\ & = T(Y) - TD[V(Y = 0\%VDD) \rightarrow V(Y = 50\%VDD)] \\ & \quad + TD[V(Y = 0\%VDD) \rightarrow V(Y = 95\%VDD)] \\ & = T(Y) - \ln(0.5) \times \tau + \ln(1 - 0.95) \times \tau \end{aligned} \tag{2}$$

In this paper, two points (X1, Y1) and (X2, Y2) on a plane are used to define a line. Then, the slope (a) and intercept (b) can be calculated as follows.

$$X(t) = \{(X_1, Y_1), (X_2, Y_2)\} = a \times t + b$$
$$Slope(a) \Rightarrow a = \frac{Y_2 - Y_1}{X_2 - X_1}$$
$$Intercept(b) \Rightarrow b = Y_1 - a \times X_1$$

Under this definition, the time t that the equation Y(t) is larger than the equation X(t) with VT can be calculated as follows.

$$\begin{cases} X(t) = a_X \times t + b_X \\ Y(t) = a_Y \times t + b_Y \end{cases}$$
$$If \quad (Y(t) - X(t) = VT)$$
$$Then \quad t = \frac{VT - (b_X - b_Y)}{a_X - a_Y} = T(Y(t) - X(t) = VT)$$

In the charging period, T_{PEAK} is defined as the time that the operation mode of NMOS is in the saturation mode and the operation mode of PMOS is changing from the saturation mode to the linear mode, which is the point that allows most current to flow through PMOS. In other words, T_{PEAK} happens at the time when the voltage difference between the output Y and the input X is equal to VT (VSG=VT). Therefore, T_{PEAK} can be obtained when Y(t) − X(t) = VT. Because the definitions of TF(X) and TR(Y) are the signal duration from 10% to 90% VDD, using them to calculate the signal duration from 0% to 50% VDD should be multiplied by 0.625(=0.5/(90% − 10%)) instead of 0.5. Finally, the corollary of T_{PEAK} is shown as follows.

$$\begin{cases} X(t) = \{(T(X), 0.5 \times VDD), (T(X) - 0.625 \times TF(X), VDD)\} \\ Y(t) = \{(T(Y), 0.5 \times VDD), (T(Y) - 0.625 \times TR(Y), 0)\} \end{cases}$$
$$\Rightarrow T_{PEAK} = T(Y(t) - X(t)) = VT) \tag{3}$$

If the total consumed energy is used as the area of this triangle and the base of this triangle is (T_{END}-T_{START}), I_{PEAK} can be obtained from the formula of the triangle area. Please note that the energy stored in the LIB file is the internal energy consumption (E_{INT}) of the cell only.

The energy consumed on the output loading (E_{LOAD}) should be added to obtain the correct area of the triangle. The corollary of I_{PEAK} is shown as follows.

$$E_{INT} + E_{LOAD} = \frac{1}{2} \times (T_{END} - T_{START}) \times I_{PEAK} \tag{4}$$
$$\Rightarrow I_{PEAK} = 2 \times \frac{E_{INT} + E_{LOAD}}{T_{END} - T_{START}}$$

3.1.2 Discharging period

Because the supply current does not charge the output loading in the discharging period, most of the supply current can appear only when NMOS is turned on but PMOS is not completely turned off yet. Therefore, in this case, T_{START} is defined as the time that input voltage achieves VT because NMOS is turned on at this time. T_{END} is defined as the time that the input voltage achieves (VDD-VT) when PMOS is turned off. Using these definitions, the duration of the supply current waveform in the discharging period can be decided. Following the same assumption in Section 3.1.1, T_{PEAK} is still defined as the time that the operation mode of PMOS is changed from linear to saturation. Figure 7 shows their relationship to the input/output waveforms. Because there is no current charging the output loading, the E_{INT} obtained in the LIB file can be used as the triangle area in the discharging period to obtain the T_{PEAK} value. The corollary of T_{END} is shown as follows.

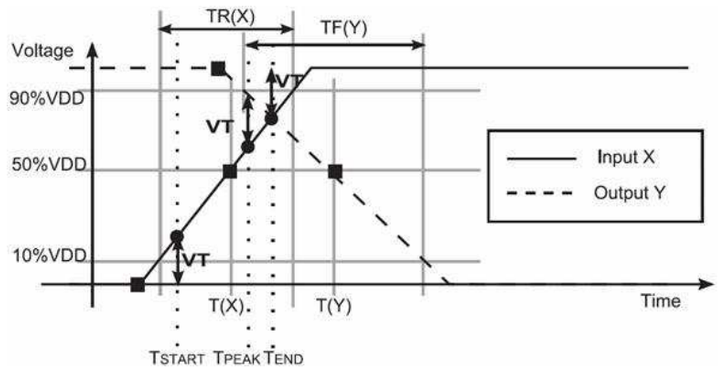


Fig. 7. The parameters of a simple cell in the discharging period

$$\frac{T_{START} - [T(X) - 0.625 \times TR(X)]}{VT} = \frac{1.25 \times TR(X)}{VDD} \tag{5}$$
$$\Rightarrow T_{START} = T(X) - 1.25 \times TR(X) \times \frac{0.5 \times VDD - VT}{VDD}$$

$$\frac{[T(X) + 0.625 \times TR(X)] - T_{END}}{VT} = \frac{1.25 \times TR(X)}{VDD} \tag{6}$$
$$\Rightarrow T_{END} = T(X) + 1.25 \times TR(X) \times \frac{0.5 \times VDD - VT}{VDD}$$

$$\begin{cases} X(t) = \{(T(X), 0.5 \times VDD), (T(X) - 0.625 \times TR(X), 0)\} \\ Y(t) = \{(T(Y), 0.5 \times VDD), (T(Y) - 0.625 \times TF(Y), VDD)\} \end{cases} \tag{7}$$
$$\Rightarrow T_{PEAK} = T(Y(t) - X(t)) = VT)$$

$$E_{INT} = \frac{1}{2} \times (T_{END} - T_{START}) \times I_{PEAK} \Rightarrow I_{PEAK} = 2 \times \frac{E_{INT}}{T_{END} - T_{START}} \quad (8)$$

3.2 Composite logic cells

As shown in Fig. 8, some cells are composed of two or more simple logic cells, such as **BUFFER**, **AND**, and **OR** cells. Those cells are called "composite logic cells" in this work. In the following descriptions, a **BUFFER** is used as an example to explain the proposed approach for those cells. Because the information of the internal signal I in Fig. 8(a) cannot be obtained in the LIB file, an assumption is made in this work that the input signal of the second stage in a composite cell will start rising/falling when the output voltage of its first stage achieves 50% VDD. With this assumption, the internal signal I can be rebuilt using existing library information as shown in Fig. 9. Since the timing information of the internal node can be estimated, the methods proposed in Sect. 3.1 can be used to handle the two simple cells respectively and the total current waveform of this composite cell can be estimated.

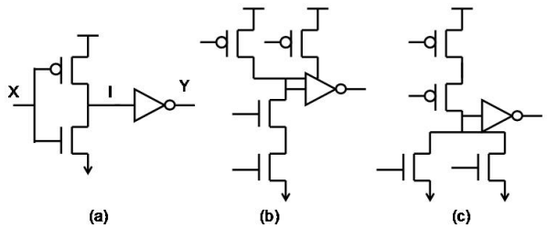


Fig. 8. The structure of the composite logic cell (a) BUFFER (b) AND (c) OR

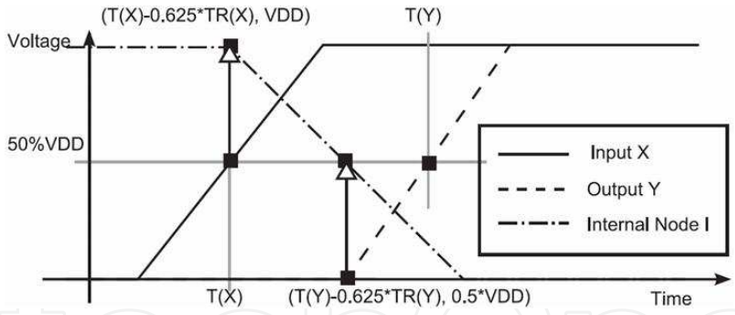


Fig. 9. The internal voltage waveform in a composite cell

3.2.1 Charging period

If the output of the composite cell is rising, the internal node I will be in the falling case as shown in Fig. 10. Therefore, the simple-cell methods in the discharging period are used to calculate T_{START_1stF}, T_{END_1stF} and T_{PEAK_1stF} of the first stage. Then, the simple-cell methods in the charging period are used to calculate T_{START_2ndR}, T_{END_2ndR} and T_{PEAK_2ndR} of the second stage. Because there is only one energy value in the library and no proper method to split it into two parts, an assumption is made that the transition of the two stages are very close such that the composition of the two triangles still approximates to a triangle. While combining the triangles of the two stages, the T_{START}, T_{PEAK} and T_{END} of the composed triangle are defined as the average values of the two triangles in this work for easier calculation. Then, I_{PEAK} can be obtained in the same way from those timing information and

the stored energy information. The detailed formulas to construct the current waveforms in this case are summarized as follows.

$$\begin{aligned} X(t) &= \{(T(X), 0.5\times VDD), (T(X) - 0.625\times TR(X), 0)\} \\ I(t) &= \{(T(X), VDD), (T(X) - 0.625\times TR(Y), 0.5\times VDD)\} \\ Y(t) &= \{(T(Y), 0.5\times VDD), (T(Y) - 0.625\times TR(Y), 0)\} \end{aligned} \tag{9}$$

$$\Rightarrow T_{START} = avg\{T_{START\_1stF}, T_{START\_2ndR}\} \tag{10}$$

$$\Rightarrow T_{PEAK} = avg\{T_{PEAK\_1stF}, T_{PEAK\_2ndR}\}$$

$$\Rightarrow T_{END} = avg\{T_{END\_1stF}, T_{END\_2ndR}\} \tag{11}$$

$$\Rightarrow I_{PEAK} = \frac{2\times(\frac{E_{INT}}{VDD} + Load(Y)\times VDD)}{T_{END} - T_{START}} \tag{12}$$

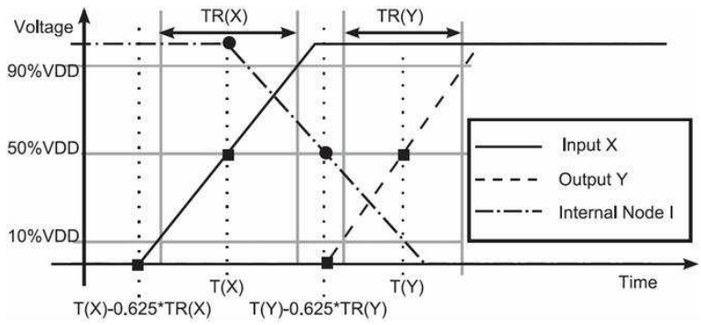


Fig. 10. The rebuilding voltage waveform of a composite logic cell in the charging period

3.2.2 Discharging period

If the output of a buffer is falling, the internal node I will be in the rising case. Therefore, the simple-cell formulas in the charging period are used to handle the first stage. The simple-cell formulas in the discharging period are used to handle the second stage. Then, using the similar approach for the case in charging period, T_{START}, T_{PEAK} and T_{END} can be obtained from the average values of the two triangles. The rebuilt voltage waveforms and timing parameters are shown in Fig. 11. Because the energy of the reversed supply current at the second stage can be eliminated by the energy of the first stage, the internal power in the discharging period can be used directly to estimate the I_{PEAK} of this cell. The detailed formulas to construct the current waveform in this case are listed as follows.

$$\begin{aligned} X(t) &= \{(T(X), 0.5\times VDD), (T(X) - 0.625\times TF(X), VDD)\} \\ I(t) &= \{(T(X), VDD), (T(X) - 0.625\times TF(Y), 0.5\times VDD)\} \\ Y(t) &= \{(T(Y), 0.5\times VDD), (T(Y) - 0.625\times TF(Y), VDD)\} \end{aligned} \tag{13}$$

$$\Rightarrow T_{START} = avg\{T_{START\_1stR}, T_{START\_2ndF}\}$$

$$\Rightarrow T_{PEAK} = avg\{T_{PEAK\_1stR}, T_{PEAK\_2ndF}\} \tag{14}$$

$$\Rightarrow T_{END} = avg\{T_{END\_1stR}, T_{END\_2ndF}\} \tag{15}$$

$$\Rightarrow I_{PEAK} = \frac{2 \times \frac{E_{INT}}{VDD}}{T_{END} - T_{START}} \tag{16}$$

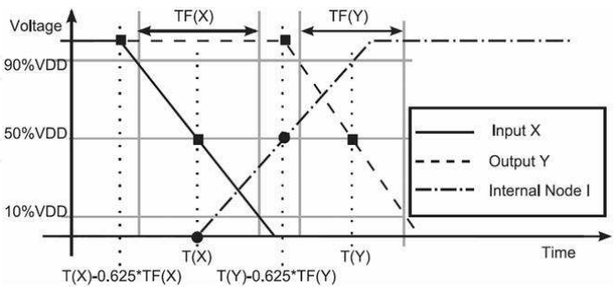


Fig. 11. The rebuilding voltage waveform of a composite logic cell in the discharging period

3.3 Sequential elements

In real applications, most circuits contain sequential cells. For a feasible solution, it is important to develop proper approaches to handle sequential cells. Like composite cells, sequential cells are often composed of several simple cells. In a standard library, the information of the internal nodes in a sequential cell is not stored, either. In order not to use extra information, some assumptions are made to rebuild the internal signals of a sequential cell. In the following descriptions, a positive-edge-triggered D-flip-flop (**DFF**) is used as an example to explain the proposed approach on sequential cells. Other flip-flops in the standard cell library, such as the flip-flops with set/reset, can be handled by using similar methods for their normal operations. The special set/reset behaviors can be characterized as a special case since they do not appear very often.

Figure 12 shows the typical architecture of a DFF. It can be divided into three blocks, which are clock generator, setup block and evaluation block. The total supply current waveform of the DFF is the summation of the waveforms from the three blocks. Since the operation modes of a DFF are more complex, its current waveform model is discussed in three cases.

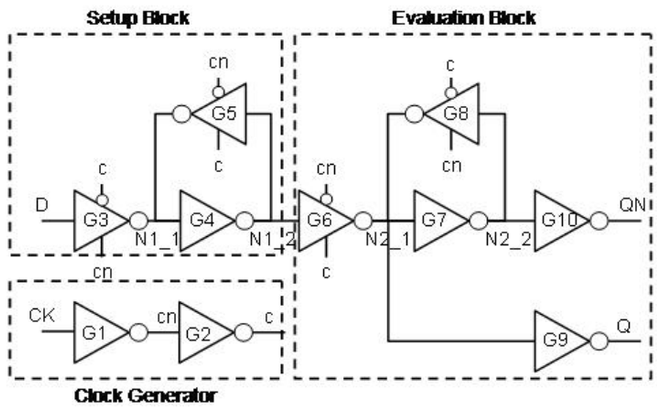


Fig. 12. The architecture of a typical DFF

3.3.1 Only clock pin is changed

In this case, the data pin D is stable and its value is the same as the output Q. In most cases, the internal signals, N1_1, N1_2, N2_1 and N2_2, are stable, too. Therefore, a supply current only occurs in the clock generator when only the clock pin is changing. The clock generator is often composed of two inverters to generate two inverse signals, c and cn, as shown in Fig. 13.

First, the case of CK rising (active edge) is discussed. Using the same idea for composite logic cells, the voltage waveforms of CK, cn and c will be rebuilt first. Then, the formulas of composite logic cells in the charging period can be used directly to decide T_{START}, T_{PEAK}, T_{END} and I_{PEAK}. However, there is still no timing information for the internal nodes of flip-flops in the LIB file. In order to solve this problem, two assumptions are made to rebuild the internal signals (cn and c) with approximate timing information.

The first assumption is that the maximum current of the tri-state inverter (G6) occurs when its output voltage (N2_1) reaches 50% VDD, as illustrated in Fig. 13. Then, following the T_{PEAK} definition of simple cells, the maximum current happens when the difference between the gate voltage of c and the drain voltage of N2_1 is equal to VT. The time that the voltage of c reaches [0.5×VDD+VT] can be implied with [T(CK) + TDR(CK→Q) − 0.625×TR(Q)].

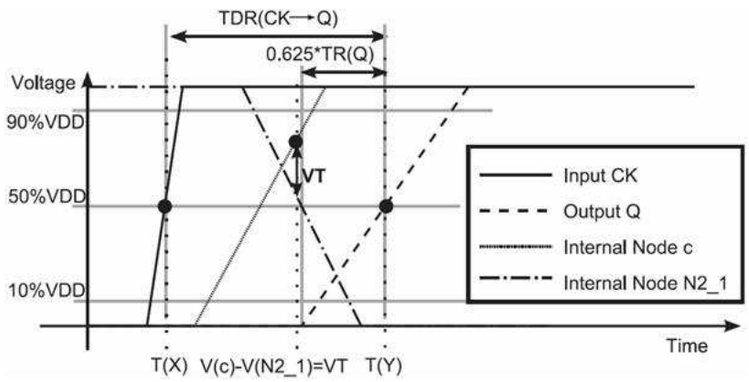


Fig. 13. The illustration of the first assumption to imply the timing information of internal node (c).

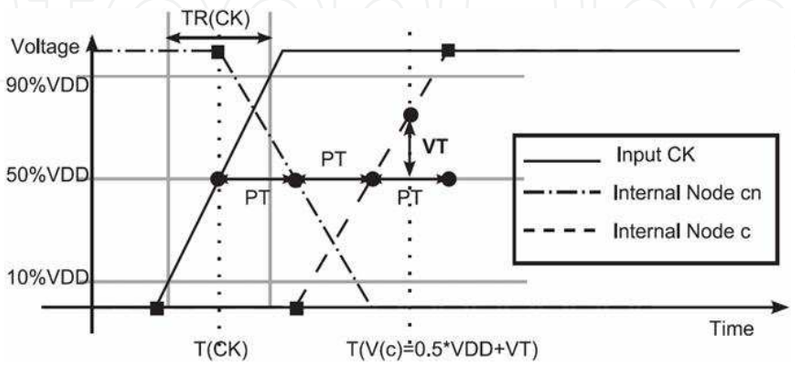


Fig. 14. The illustration of the second assumption to imply the timing information of internal nodes (cn) and (c).

The second assumption is that the rising and falling times of the nodes cn and c are very similar because most clock buffers are designed to have similar rising and falling time. From the first assumption, the time when V(c)=0.5 × VDD + VT can be obtained. Following the same assumption for composite cells, the input signal of the second stage will start rising/falling when the output voltage of the previous stage achieves 50% VDD. In order to simplify the explanation, a time interval (PT) is defined in Fig. 14. Since PT can be obtained with these two assumptions, the times that c and cn reach 0.5×VDD can be expressed with PT. Then, the internal voltage waveforms can be rebuilt as shown in Fig. 14. The detailed corollary is listed as follows.

$$
\begin{aligned}
&Assume \quad X = [T(V(c) = 0.5 \times VDD + VT] - [T(CK) + PT] \\
&T(V(c) = 0.5 \times VDD + VT) \\
&= T(CK) + TDR(CK \rightarrow Q) - 0.625 \times TR(Q) \\
&\frac{X}{0.5 \times VDD + VT} = \frac{2 \times PT}{VDD} \Rightarrow PT = \frac{VDD}{2 \times (VDD + VT)} \times [TDR(CK \rightarrow Q) - 0.625 \times TR(Q)]
\end{aligned}
$$

$$
\begin{aligned}
CK(t) &= \{(T(CK), 0.5 \times VDD), (T(CK) - 0.625 \times TR(CK), 0)\} \\
cn(t) &= \{(T(CK), VDD), (T(CK) + PT, 0.5 \times VDD)\} \\
c(t) &= \{(T(CK) + PT, 0), (T(CK) + 3 \times PT), VDD)\}
\end{aligned} \tag{17}
$$

$$
\Rightarrow T_{START} = avg\{T_{START\_1stF}, T_{START\_2ndR}\}
$$

$$
\Rightarrow T_{PEAK} = avg\{T_{PEAK\_1stF}, T_{PEAK\_2ndR}\} \tag{18}
$$

$$
\Rightarrow T_{END} = avg\{T_{END\_1stF}, T_{END\_2ndR}\} \tag{19}
$$

$$
\Rightarrow I_{PEAK} = \frac{2 \times \frac{E_{INT}}{VDD}}{T_{END} - T_{START}} \tag{20}
$$

As to the CK falling case, no outputs change and no timing information is stored in the library because it is not the active edge. Although the internal nodes might change in this case, there is no information to make any reasoning. Therefore, the same timing information in the CK rising case is used to be the T_{START}, T_{PEAK} and T_{END} when only CK is falling. The internal energy consumption when only CK is falling is available in the library. It can be used to calculate a different I_{PEAK} for CK falling case.

3.3.2 Only data pin is changed

In this case, the clock pin CK is stable and only the data pin D is changed. The supply current is generated by the setup block only. If CK is logic-1, the gate G3 is turned off such that the whole cell has no switching current. When CK is logic-0, the current waveform is determined by whether the data pin D is rising or falling. Because the timing information of the internal nodes N1_1 and N1_2 are not stored in the library, two assumptions are made in this case to rebuild the approximate voltage waveforms of N1_1 and N1_2.

The first assumption is that the data propagation time from the input D to the internal node N1_1 equals to the setup time of this DFF. Because the definition of setup time is the minimum time that input data must be stable before clock arriving, it can be viewed as the time that the data has been propagated to N1_1 to enter the first latch.

The second assumption is that the node N1_2 will become stable before the gate G6 is turned on to allow the data to enter the second latch successfully. Because N2_1 is discharging in the D rising case, N1_2 must reach VDD when the voltage of the node c achieves VT. TC(VT) is defined to express the duration time between V(CK)=0.5×VDD and V(c)=VT. Following these assumptions, the time that N1_1 reaches 50% VDD and the time that N1_2 reaches VDD can be obtained. Then, following the same assumption of composite cells, the time that N1_1 reaches 50% VDD is the time that N1_2 reaches 0. The voltage waveforms of N1_1 andN1_2 can be rebuilt as shown in Fig. 15.

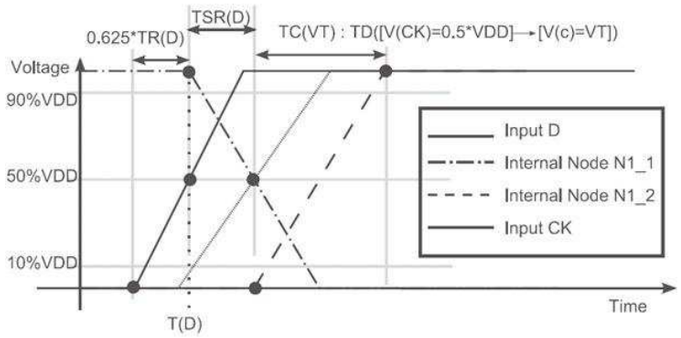


Fig. 15. The parameters of a DFF when only D is rising.

In the D falling case, TR(D) and TSR(D) are changed to TF(D) and TSF(D), respectively. E_{INT} is changed from the rising energy to the falling one. With the two internal waveforms of N1_1 and N1_2, the triangle parameters can be determined by the same approach for composite cells. Finally, the detailed corollary is shown as follows.

$$TC(VT):TD([V(CK)=0.5\times VDD]\rightarrow[V(c)=VT])$$

D Rising Case

$$D(t)=\{(T(D),0.5\times VDD),(T(D)-0.625\times TR(D),0)\}$$
$$N1\_1(t)=\{(T(D),VDD),(T(D)+TSR(D),0.5\times VDD)\}$$
$$N1\_2(t)=\{(T(D)+TSR(D),0),(T(D)+TSR(D)+TC(VT),VDD)\}$$

D Falling Case

$$D(t)=\{(T(D),0.5\times VDD),(T(D)-0.625\times TF(D),VDD)\}$$
$$N1\_1(t)=\{(T(D),0),(T(D)+TSF(D),0.5\times VDD)\}$$
$$N1\_2(t)=\{(T(D)+TSF(D),VDD),(T(D)+TSF(D)+TC(VT),0)\}$$

$$\Rightarrow T_{START}=avg\{T_{START\_1st},T_{START\_2nd}\} \quad (21)$$

$$\Rightarrow T_{PEAK}=avg\{T_{PEAK\_1st},T_{PEAK\_2nd}\} \quad (22)$$

$$\Rightarrow T_{END} = avg\{T_{END\_1st}, T_{END\_2nd}\} \tag{23}$$

$$\Rightarrow I_{PEAK} = \frac{2 \times \frac{E_{INT}}{VDD}}{T_{END} - T_{START}} \tag{24}$$

3.3.3 Output changed with clock active edge

In this case, the clock pin has an active edge, the data pin is stable, and the output Q is evaluated. Both the clock generator and the evaluation block generate supply currents. Therefore, the current waveform is composed of two triangular waveforms in this case. The first current waveform of the clock generator is discussed in Sect. 3.3.1. It is focus on how to estimate the second triangular waveform of the evaluation block in this section.

Figure 16 illustrates the rebuilt signals of the evaluation block when output Q is rising. First, using the rebuilt internal signal c in Sect. 3.1.1, the time that N2_1 starts to discharge can be obtained when the voltage of node c reaches VT. Second, T(Q) - 0.625 × TR(Q) implies the time that N2_1 reaches 0.5×VDD by the assumption of composite logic cells. Then, the internal waveform of N2_1 can be rebuilt. Third, T(QN) - 0.625 × TF(QN) implies the time that N2_2 reaches 0.5×VDD by the assumption of composite logic cells, which helps to rebuild the internal waveform of N2_2. After rebuilding the internal signals of the evaluation block, the similar approach for composite logic cells can be used to generate the composite triangular waveform of this DFF.

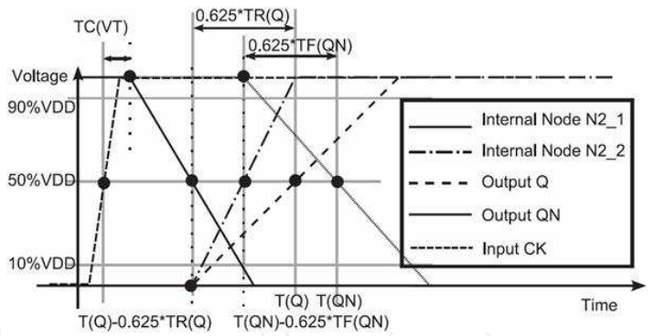


Fig. 16. The signals in a DFF when Q is rising with active clock edge.

When the output Q is falling, the time when c reaches VT is defined as the start time of N2_1 because the gate G6 starts to transition when c reaches VT. Then, changing TR(Q) and TF(QN) to TF(Q) and TR(QN) respectively, the same approach for the Q rising case can be used to rebuild the internal signals when the output Q is falling.

With the two internal waveforms of N2_1 and N2_2, T_{START} of the evaluation block is defined as the earliest start time of N2_1 and N2_2. T_{END} of the evaluation block is defined as the time that both Q and QN complete their transitions. T_{PEAK} can be calculated by the waveforms of internal nodes. The consumed internal energy of the evaluation block is the internal energy of total DFF minus the internal energy of the clock generator obtained in Sect. 3.3.1. After adding the energy of the output loading, the total triangle area of the evaluation block and the I_{PEAK} of this block can be obtained. Finally, combining the waveform of the evaluation block with the waveform of the clock generator calculated in

Sect. 3.3.1, the supply current waveform of the DFF in this case is obtained. The detailed formulas to construct the current waveform in this case are summarized as follows.

$$TC(VT):TD([V(CK)=0.5\times VDD]\rightarrow[V(c)=VT])$$

Q Rising Case

$$N2\_1(t)=\{(T(CK)+TC(VT),VDD),(T(Q)-0.625\times TR(Q),0.5\times VDD)\}$$
$$N2\_2(t)=\{(T(Q)-0.625\times TR(Q),0),(T(QN)-0.625\times TF(QN),0.5\times VDD)\}$$
$$Q(t)=\{(T(Q),0.5\times VDD),(T(Q)-0.625\times TR(Q),0)\}$$
$$QN(t)=\{(T(QN),0.5\times VDD),(T(QN)-0.625\times TF(QN),VDD)\}$$

Q Falling Case

$$N2\_1(t)=\{(TCN(VDD-VT),0),(T(Q)-0.625\times TF(Q),0.5\times VDD)\}$$
$$N2\_2(t)=\{(T(Q)-0.625\times TF(Q),VDD),(T(QN)-0.625\times TR(QN),0.5\times VDD)\}$$
$$Q(t)=\{(T(Q),0.5\times VDD),(T(Q)+0.625\times TF(Q),0)\}$$
$$QN(t)=\{(T(QN),0.5\times VDD),(T(QN)+0.625\times TR(QN),VDD)\}$$

$$\Rightarrow T_{START}=TC(VT) \tag{25}$$

$$\Rightarrow T_{PEAK}=avg\{T_{PEAK\_(G2\_1)},T_{PEAK\_(G2\_2)},T_{PEAK\_(G2\_5)}\} \tag{26}$$

$$\Rightarrow T_{END}=avg\{T_{END\_(G2\_4)},T_{END\_(G2\_5)}\} \tag{27}$$

$$\Rightarrow I_{PEAK}=\frac{2\times(\frac{E_{INT}-E_{ClockGenerator}}{VDD}+Load(Q)\times VDD)}{T_{END}-T_{START}} \tag{28}$$

4. IR-Drop aware library adjustment methods

In this section, an analytical library adjustment approach is proposed to consider the effects of the supply resistors without extra characterization. The timing and power information stored in LIB file can be modified to reflect the effect of the supply resistor by the proposed equations. Therefore, the proposed gate-level supply current estimation method can obtain the accurate waveforms with IR-drop effects. Most importantly, this method can be easily embedded into present design flow to improve the accuracy of gate-level IR-drop analysis and provide designers a fast solution to consider IR-drop effect at early design stages. In this section, the adjustment methods of combination cells, simple logic and composite logic cells are discussed first in Section 4.1. Then, in Section 4.2, the methods of sequential cell are presented. Finally, the adjustment methods of activity files (VCD) are explained in Section 4.3.

4.1 Timing and power adjustment of combination cells

4.1.1 Output transition time

Figure 17 illustrates a simple cell with a supply resistor. In the output rising case, the supply current flows through the supply resistor, which increases the transition time due to the

increased total resistance. Therefore, the RC charging model is used to calculate the increased transition time caused by the supply resistor.

R_{EFF} represents the effective resistance of the cell. C_{EFF} represents the effective capacitance of the cell. E_{INT} and E_{LOAD} represent the energy consumption caused by the cell and its output loading. In the output rising case, the C_{EFF} is approximated by the total energy divided by supply voltage. Assume $TR(Y)_{ORG}$ represents the original transition time in LIB files. $TR(Y)_{ADJ}$ represents the adjusted transition time in the output rising case. The detailed corollary and the adjustment formula can be derived as follows, in which the increased term is related to the known variables (R_{WIRE}, C_{EFF}) only. In the output falling case, the transition time is not changed because the current does not flow through the supply resistor. If there is a resistor in current path to ground, similar approach can be used to adjust TF(Y).

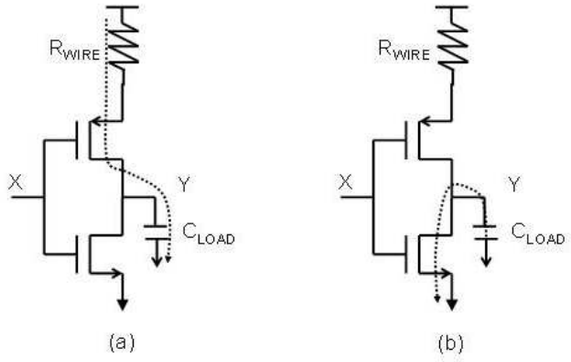


Fig. 17. The circuit structure of a simple cell (**INVETER**) with a supply resistor in (a) the output rising case (b) the output falling case

$$\begin{cases} C_{EFF} = \dfrac{E_{INT} + E_{LOAD}}{VDD} \\ TR(Y)_{ORG} = \underline{\ln 9 \times R_{EFF} \times C_{EFF}} \end{cases}$$

$$\begin{aligned} TR(T)_{ADJ} &= \ln 9 \times (R_{EFF} + R_{WIRE}) \times C_{EFF} \\ &= \underline{\ln 9 \times R_{EFF} \times C_{EFF}} + \ln 9 \times R_{WIRE} \times C_{EFF} = TR(Y)_{ORG} + \ln 9 \times R_{WIRE} \times C_{EFF} \end{aligned} \tag{29}$$

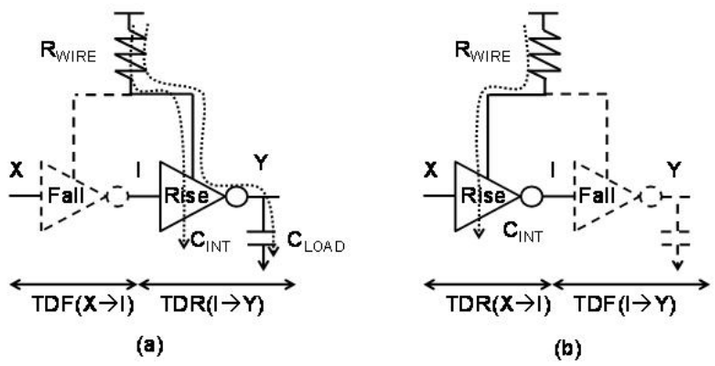


Fig. 18. The circuit structure of a composite cell (**BUFFER**) with a supply resistor in (a) the output rising case (b) the output falling case

Figure 18 illustrates a composite cell with a supply resistor. Typically, this kind of cells is composed of multiple stages of simple cells. In Fig.18(a), the supply current flows through the second stage in the output rising case. The first stage is in the output falling case. Therefore, only the increased transition time of the second stage should be considered in the output rising case. Applying the same method for the simple logic cells on the second stage can obtain the increased transition time. In the output falling case, the output transition time is still not changed because the current does not flow through the second stage. Only the propagation delay may be changed in such case, which is discussed in the next section.

4.1.2 Propagation delay time

According to the same model shown in Fig.18, the adjustment method of the propagation time for simple logic cells can be derived. Similarly, only the increased propagation time in the output rising case should be considered to adjust the original timing information. The adjustment formulas are listed as follows, in which the increased term is related to the known variables (R_{WIRE}, C_{EFF}) only.

$$\begin{cases} C_{EFF} = \dfrac{E_{INT} + E_{LOAD}}{VDD} \\ TDR(Y)_{ORG} = \underline{-\ln 0.5 \times R_{EFF} \times C_{EFF}} \end{cases}$$

$$\begin{aligned} TDR(T)_{ADJ} &= (-\ln 0.5) \times (R_{EFF} + R_{WIRE}) \times C_{EFF} \\ &= \underline{(-0.5) \times R_{EFF} \times C_{EFF}} + (-\ln 0.5) \times R_{WIRE} \times C_{EFF} = TDR(Y)_{ORG} + (-\ln 0.5) \times R_{WIRE} \times C_{EFF} \end{aligned} \quad (30)$$

For composite logic cells, the adjustment of the propagation time in the output rising case is the same with the simple logic cell as shown in Fig.18 (a). In the output falling case shown in Fig.18(b), C_{EFF} is the internal capacitance C_{INT}. This internal capacitance can be approximated as the E_{INT} divided by the supply voltage because the operation current flows through the cell only. The adjustment formulas are listed as follows, in which the increased term is related the known variables only.

$$C_{EFF} = \frac{E_{INT} + E_{LOAD}}{VDD} \Rightarrow TDR(X \to Y)_{ADJ} = TDR(X \to Y)_{ORG} + (-\ln 0.5) \times R_{WIRE} \times C_{EFF} \quad (31)$$

$$C_{EFF} = \frac{E_{INT}}{VDD} \Rightarrow TDR(X \to Y)_{ADJ} = TDR(X \to Y)_{ORG} + (-\ln 0.5) \times R_{WIRE} \times C_{EFF} \quad (32)$$

4.1.3 Internal energy

Assume $E_{INT(ORG)}$ represents the internal energy stored in standard libraries, and $E_{INT(ADJ)}$ represents the modified internal energy. This internal energy can be viewed as the short-circuit energy by ignoring the effect of internal capacitances. Therefore, $E_{INT(OLD)}$ can be expressed as the short-circuit current (I_{SC}) times the duration of the short-circuit current (T_{SC}). Since I_{SC} can be rewritten as VDD/ R_{INT}, the $E_{INT(ADJ)}$ can be derived by the ratio of R_{EFF} and R_{ADJ}, as shown in the following equations. Please be noted that the R_{EFF} can be calculated from the original propagation time because the short-circuit current happens at the logic transition period.

$$E_{INT(ORG)} = I_{SC} \times T_{SC} = \frac{VDD}{R_{EFF}} \times T_{SC}$$
$$E_{INT(ADJ)} = \frac{VDD}{(R_{EFF} + R_{WIRE})} \times T_{SC} = \frac{R_{EFF}}{R_{EFF} + R_{WIRE}} \times E_{INT(ORG)} \quad (33)$$

4.2 Timing and power adjustment of sequential elements

Only the output Q rising case is to explain the adjusted formulas because the formulas fir other cases can be derived by similar ways. One difficulty of the adjustment of DFF cases is to estimate the effective capacitance of the gate because the internal capacitance is unavailable. In this work, the internal energy is used to approximate the effective capacitance. The other difficulty is the adjustment of effective supply resistance because more than one gates switch in the DFF. Therefore, the simple parallel connection formula is applied first to approximate the effective supply resistance seen by each switching gate. The details of the adjusted formulas in the timing and internal energy are discussed in the following subsections.

4.2.1 Output transition time

Only the increased transition time caused by the output stage (G9) should be added to adjust the output transition time of output Q. The E_{INT} ($CK_{RISE} \rightarrow Q_{RISE}$) represents the internal energy consumption stored in the library for the output Q rising case when CK actives, which is composed of the energy of G1, G2, G6, G7, G9 and G10. The $E_{INT}(CK_{RISE})$ represents the internal energy consumption of G1 and G2 when only CK actives. It implies that the energy consumption of G6, G7, G10 and G9 in Fig.19 can be calculated by E_{INT} ($CK_{RISE} \rightarrow Q_{RISE}$)-$E_{INT}(CK_{RISE})$. Therefore, the C_{EFF} of the path through G9 can be approximated as a half of E_{INT} ($CK_{RISE} \rightarrow Q_{RISE}$)- $E_{INT}(CK_{RISE})$ divided by VDD because the energy are separated into two rising gates (G7 and G9).

When measuring the output transition time, three current paths travel through the R_{WIRE}. Assume the three inverters G2, G7 and G9 have similar sizes, the equivalent supply resistor of each cell must be three times the lumped supply resistor (R_{WIRE}) according to the parallel connection formula. Therefore, the adjusted formula is modified a little bit as follows. The falling time of QN (TF(QN)) is not necessary to be adjusted because it is a falling gate. The adjustment formulas for the output transition time in output Q falling case are also listed as follows, which can be derived by similar way as in the output Q rising case.

$$\begin{cases} C_{EFF} = \dfrac{E_{INT}(CK_{RISE} \rightarrow Q_{RISE}) - E_{INT}(CK_{RISE})}{2 \times VDD} + C_{LOAD} \\ R_{EFF} = 3 \times R_{WIRE} \end{cases}$$
$$TR(Q)_{ADJ} = TR(Q)_{ORG} + \underline{\ln 9 \times R_{WIRE} \times C_{EFF}} \quad (34)$$
$$TF(QN)_{ADJ} = TF(QN)_{ORG}$$

$$\begin{cases} C_{EFF} = \dfrac{E_{INT}(CK_{RISE} \rightarrow Q_{FALL}) - E_{INT}(CK_{RISE})}{2 \times VDD} + C_{LOAD} \\ R_{EFF} = 3 \times R_{WIRE} \end{cases}$$
$$TF(Q)_{ADJ} = TF(Q)_{ORG} \quad (35)$$
$$TR(QN)_{ADJ} = TR(QN)_{ORG} + \underline{\ln 9 \times R_{WIRE} \times C_{EFF}}$$

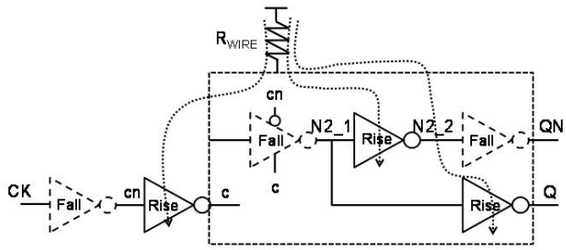


Fig. 19. The current flows of the DFF in the output rising case

4.2.2 Propagation delay time

In the signal propagation path from CK to Q, only G2 and G9 are rising in the output Q rising case. Therefore, the increased delay time of the two gates are added by the similar method shown in Section 4.1.2 to adjust the CK to Q delay of DFF circuits. The effective capacitance of G2, $C_{EFF}(G2)$, can be approximated as the $E_{INT}(CK_{RISE})$ divided by VDD. The effective capacitance of G9, $C_{EFF}(G9)$, and the R_{EFF} of G2 and G9 are obtained by the same approach for the output transition time. The adjusted propagation delay time $TDR(CK\rightarrow Q)_{ADJ}$ can be calculated by the following formulas, in which the increased term is related to known variables only.

$$\begin{cases} C_{EFF}(G2) = \dfrac{E_{INT}(CK_{RISE})}{VDD} \\ C_{EFF}(G9) = \dfrac{E_{INT}(CK_{RISE} \rightarrow Q_{RISE}) - E_{INT}(CK_{RISE})}{2 \times VDD} + C_{LOAD} \\ R_{EFF} = 3 \times R_{WIRE} \end{cases} \tag{36}$$

$$TDR(CK \rightarrow Q)_{ADJ} = TDR(CK \rightarrow Q)_{ORG} + \underline{(-\ln 0.5) \times R_{EFF} \times (C_{EFF}(G2) + C_{EFF}(G9))}$$

The propagation delay time of the output QN $TDF(CK\rightarrow QN)_{ADJ}$ can be calculated by the similar approach of $TDR(CK\rightarrow Q)_{ADJ}$. The adjustment formula is listed as follows, except that G7 is used instead of G9 for different output.

$$\begin{cases} C_{EFF}(G2) = \dfrac{E_{INT}(CK_{RISE})}{VDD} \\ C_{EFF}(G7) = \dfrac{E_{INT}(CK_{RISE} \rightarrow Q_{RISE}) - E_{INT}(CK_{RISE})}{2 \times VDD} + C_{LOAD} \\ R_{EFF} = 3 \times R_{WIRE} \end{cases} \tag{37}$$

$$TDF(CK \rightarrow Q)_{ADJ} = TDF(CK \rightarrow Q)_{ORG} + \underline{(-\ln 0.5) \times R_{EFF} \times (C_{EFF}(G2) + C_{EFF}(G7))}$$

4.2.3 Setup time

Figure 20 illustrates the internal status of a DFF when data is setting up. Following the same assumption of the setup time in Section 3, the data must reach N1_2 before the internal node c rises to ensure that the data can enter the next stage successfully. Therefore, the setup time of the D rising case TSR(D) can be expressed as the following formula.

$$TSR(D)_{ORG} = TDF(D \rightarrow N1\_2)_{ORG} - TDR(CK \rightarrow c)_{ORG} \tag{38}$$

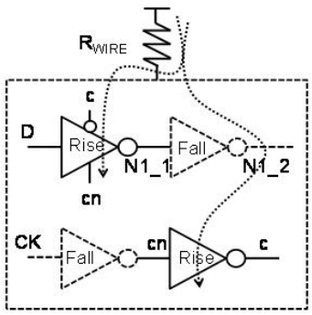


Fig. 20. The internal status of a DFF when D is setting up.

The propagation delay time TDF(D→N1_2)$_{ADJ}$ and TDR(CK→c)$_{ADJ}$ can be calculated with the similar method for the propagation delay time. Because there are two current paths in this case as shown in Fig.20, the equivalent supply resistor of each cell is two times R_{WIRE}. The formulas are listed as follows.

$$\begin{cases} C_{EFF}(G3) = \dfrac{E_{INT}(D_{RISE})}{VDD} \\ C_{EFF}(G2) == \dfrac{E_{INT}(CK_{RISE})}{VDD} \\ R_{EFF} = 2 \times R_{WIRE} \end{cases}$$
$$TDF(D \rightarrow N1\_2)_{ADJ} = TDF(D \rightarrow N1\_2)_{ORG} + \underline{(-\ln 0.5) \times R_{EFF} \times C_{EFF}(G3))} \tag{39}$$
$$TDR(CK \rightarrow c)_{ADJ} = TDR(CK \rightarrow c)_{ORG} + \underline{(-\ln 0.5) \times R_{EFF} \times C_{EFF}(G2))}$$

Therefore, the formula of the adjusted setup time TSR(D)$_{ADJ}$ can be obtained as follows. The setup time in the D falling case can be obtained by the similar way. The formula is also listed as follows.

$$\begin{aligned} TSR(D)_{ADJ} &= TDF(D \rightarrow N1\_2)_{ADJ} - TDR(CK \rightarrow c)_{ADJ} \\ &= TSR(D) + (-\ln 0.5) \times R_{EFF} \times [C_{EFF}(G3) - C_{EFF}(G2)] \\ TSF(D)_{ADJ} &= TDR(D \rightarrow N1\_2)_{ADJ} - TDR(CK \rightarrow c)_{ADJ} \\ &= TSF(D) + (-\ln 0.5) \times R_{EFF} \times [C_{EFF}(G4) - C_{EFF}(G2)] \end{aligned} \tag{40}$$

4.2.4 Internal energy

The internal energy of DFF cannot be separated to each cell. Therefore, the entire DFF is viewed as a super-gate to adjust its internal energy. The same formulas of the composite logic cells are used directly to adjust the internal energy of DFF.

4.3 Timing correction of cell switching activities

During gate-level simulation, the signal events are recorded in activity files (.vcd). Figure 21(a) shows the ideal timing diagram of four events, T(A), T(B), T(C), T(Y). With non-ideal

supply lines, these events will occur at different time thus incurring different current waveforms. Therefore, the modification of activity files is also proposed in this paper, as illustrated in Fig.21(b). First, the modified propagation delay time $TD(G1)_{ADJ}$ can be obtained by the modification method of the signal cell. Then, Diff(G1) can be implied by $TD(G1)_{ADJ}$-$TD(G1)_{ORG}$ and be propagated to next event T(B). $T(B)_{ADJ}$ is derived by the summation of T(B) and Diff(G1). The other events can be modified in the similar way. After the timing errors are corrected, the accuracy of the constructed waveforms based on those events can be further improved.

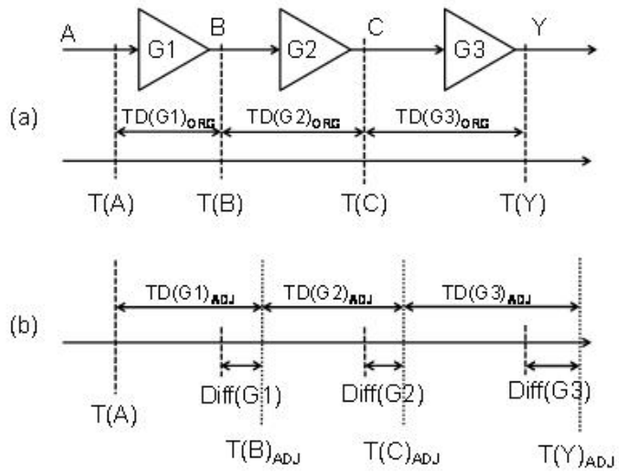


Fig. 21. Illustration of VCD events with (a) ideal (b) non-ideal supply lines

5. Experimental result

5.1 Experimental result of supply current waveform estimation method

We have implemented a supply current waveform estimation tool in C/C++. Given an input pattern, this tool can calculate the triangle that simulates the supply current waveform of each cell. The overall supply current waveform is then obtained by combining all triangles of every changed cell in time. All the input files of this tool follow standard formats, which are Verilog netlist file of the gate-level design, value changed dump (VCD) file of the design under given input patterns, and the LIB file of the standard cell library. The output format is a (time, voltage) pair that can be used to plot the dynamic supply current waveform. Those input/output files are compatible with current EDA tools. It allows our solution to be plugged into the existing EDA flow smoothly.

Very few commercial tools can provide the current waveform information at gate level. We choose PrimeTime- PX (Synopsys, 2009) for comparison, which can be used to estimate cycle-accurate peak power at gate level. Divided by the supply voltage, the peak power can be transformed to the peak current. Besides traditional LIB format, this tool also supports CCSM library format, which can be used to demonstrate the help from new library format. The results with and without CCSM data are shown in the rows "CCSM" and "LIB" of Table 1 respectively. Because 0.13 μm library does not have CCSM data yet, those CCSM data are characterized from HSPICE simulation by ourselves. Therefore, only combinational

cells are characterized in our preliminary experiments. The previous approach (Shimazaki et al., 2000) is also rebuilt in our environment and tested in the same experiments to show our improvements on accuracy. Because they did not mention how to apply their approach on sequential cells, only combinational circuits are compared.

In the experiments, ISCAS'85 and ISCAS'89 benchmark circuits, which are implemented with TSMC 0.13um process, are used to test the accuracy. For each benchmark circuit, 200 random patterns are generated to trigger the circuit. After all, the average errors of the peak current and position with 200 pattern-pairs are shown in the row "eI_p" of Tables 1 and 2. The standard deviation of the peak current and position with the 200 results is shown in the row "sI_p" of Tables 1 and 2. The last column "AVG" in Tables 1 and 2 shows the average values of all cases. Figure 22 shows the estimated current waveforms of c7552 and s9234 as examples, which are very similar to HSPICE results.

According to the results estimated by PrimeTime-PX, the CCSM libraries significantly improve the accuracy of peak current estimation. However, the cycle-accurate results are still not accurate enough for analyzing the peak power or the IR-drop noise. The estimation results of the proposed methods, which are listed in the row "GCM" of Tables 2 and 3, demonstrates that the proposed approach can provide accurate estimations on the supply current waveforms by using the same information provided in traditional LIB libraries. The average estimation errors on eI_{PEAK} and eT_{PEAK} are about 10% with small standard deviation. The correlation between the estimated waveforms and HSPICE waveforms is higher than 0.97, which shows the similarity between the two waveforms. Compared to the rough estimation in (Shimazaki et al., 2000), the proposed approach does have a significant improvement on the estimation accuracy. Most importantly, the proposed approach can deal with sequential circuits, which enables this approach to be applied to modern designs.

The run time of the current waveform estimation for each benchmark circuit is provided in Table 3, which is measured on a XEON 3G machine with 2G RAM. The row "GCM" shows the run time of the proposed approach in seconds. The row "HSPICE" shows the run time of HSPICE simulation with the same patterns in hours. The row "Ratio" shows the ratio of the run time between HSPICE and GCM, which demonstrates a significant speed improvement.

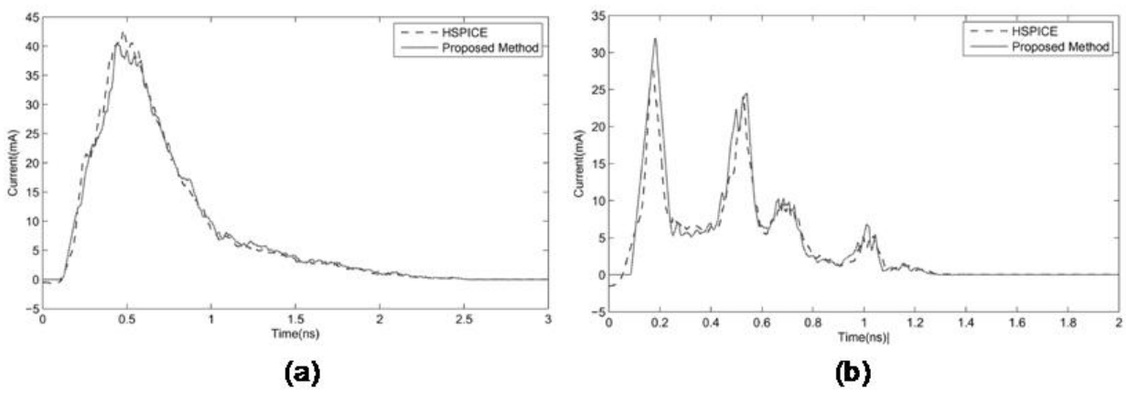


Fig. 22. The estimation supply current waveforms of (a)c7552 (b)s9234.

Circuit		c432	c499	c880	c1355	c1908	c2670	c3540	c5315	c6288	c7552	AVG
LIB	$eI_{P(\%)}$	60.63	203.96	44.51	111.75	64.72	812.42	69.66	1396.90	46.67	537.70	281.12
	$sI_{p(\%)}$	0.62	0.46	0.22	0.18	0.34	2.09	0.25	4.04	0.06	1.75	1.00
CCS	$eI_{P(\%)}$	25.25	38.41	33.49	42.43	52.22	255.50	50.68	299.00	51.94	73.05	92.29
	$sI_{p(\%)}$	0.16	0.11	0.10	0.07	0.13	0.91	0.14	0.94	0.08	0.26	0.29
(Shimazaki et al., 2000)	$eI_{P(\%)}$	42.16	35.81	59.85	81.11	64.88	41.01	51.61	38.48	27.73	31.67	47.43
	$sI_{p(\%)}$	15.92	14.58	19.68	16.47	16.99	10.21	15.70	9.96	18.56	10.02	14.80
	$eT_{P(\%)}$	2.80	1.04	4.48	1.58	5.25	1.48	6.00	4.88	11.02	7.11	4.56
	$sT_{p(\%)}$	7.50	1.18	4.98	1.19	4.50	2.42	7.72	5.82	8.13	10.14	5.36
	Corr	0.959	0.977	0.961	0.928	0.973	0.981	0.971	0.988	0.993	0.980	0.971
GCM	$eI_{P(\%)}$	12.87	7.42	6.24	9.95	8.80	9.47	6.17	5.20	6.06	3.97	7.61
	$sI_{p(\%)}$	8.18	4.99	4.96	4.69	5.21	5.82	4.77	3.98	2.55	2.99	4.81
	$eT_{P(\%)}$	6.52	1.79	5.09	4.21	4.52	5.34	5.51	5.64	2.31	3.04	4.39
	$sT_{p(\%)}$	13.16	1.14	7.02	2.45	2.45	6.67	7.80	6.29	3.16	5.31	5.64
	Corr	0.964	0.985	0.985	0.976	0.987	0.977	0.982	0.989	0.992	0.988	0.983

Table 1. Experimental results of ISCAS85 benchmark circuits

Circuit		s298	s444	s526	s820	s1196	s1238	s1494	s5378	s9234	s15850	AVG
GCM	$eI_{P(\%)}$	8.96	12.52	10.96	12.96	8.92	9.32	2.84	10.81	13.77	13.04	10.40
	$sI_{p(\%)}$	6.11	1.51	8.56	10.60	5.23	6.63	3.57	2.01	1.14	0.97	4.63
	$eT_{P(\%)}$	10.99	4.12	7.25	6.97	5.87	5.12	8.25	2.12	1.52	3.29	5.55
	$sT_{p(\%)}$	12.38	1.78	7.53	5.98	6.79	5.54	6.96	0.39	0.26	1.36	4.89
	Corr	0.967	0.976	0.966	0.968	0.977	0.977	0.975	0.973	0.982	0.979	0.974

Table 2. Experimental results of ISCAS89 benchmark circuits

Circuit	c432	c499	c880	c1355	c1908	c2670	c3540	c5315	c6288	c7552	AVG
GCM (sec)	13.17	23.05	20.05	43.79	55.39	46.43	90.60	179.77	1083.94	414.68	-
HSPICE(hr)	9.73	17.58	16.44	27.45	26.54	40.61	54.82	86.76	69.16	128.38	-
Ratio	2661	2746	2951	2256	1725	3419	2178	1737	230	1115	2074
Circuit	s298	s444	s526	s820	s1196	s1238	s1494	s5378	s9234	s15850	AVG
GCM(sec)	4.38	1.78	3.15	2.76	6.89	6.12	4.88	28.55	35.35	71.75	-
HSPICE(hr)	13.49	10.33	12.05	14.50	23.03	23.88	28.68	107.83	183.15	495.78	-
Ratio	11089	20883	13770	18914	12034	14048	21161	13596	18652	24876	16902

Table 3. Experimental results of run time

5.2 Experimental result of library adjustment method

In order to demonstrate the accuracy of the IR-drop-aware adjustment approach, the same ISCAS85 and ISCAS89 benchmark circuits are used to perform some experiments. For each benchmark circuit, 200 random pattern pairs are generated to trigger the circuit. The average results of all circuits are illustrated in Fig.23. The average peak current errors using the method without adjustment the library information is draw with dash lines (w/o). The proposed library method is draw with bold line(w). According to the results, the proposed

method can reduce the estimation errors successfully. Figure 24 shows the estimated supply current waveforms of c7552 circuit as example, which also confirm the accuracy of the proposed approach ($GCM_{(ADJ)}$). The waveforms obtained without IR-drop consideration (GCM) are also used to estimate the IR-drop directly with the same input pattern. The results show that estimation without considering R_{wire} effects suffers large errors when the resistance on supply lines is getting larger. The proposed adjustment can consider the R_{wire} effects and have a significant improvement on accuracy.

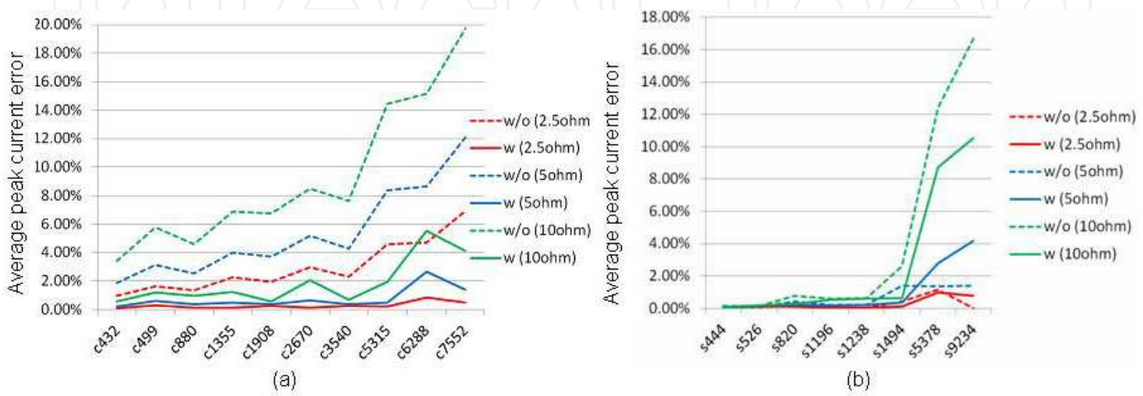


Fig. 23. The experimental results of library-adjustment methods on (a) ISCAS'85 (b) ISCAS'89.

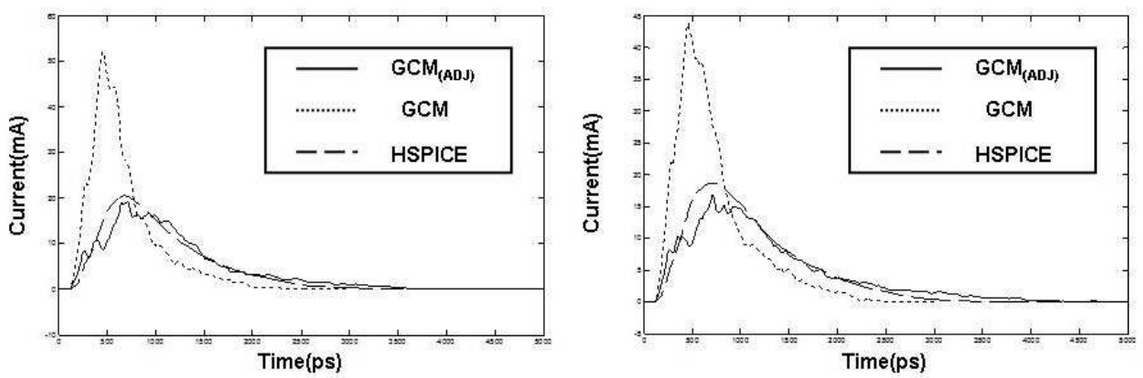


Fig. 24. The estimation supply current waveforms of c7552 with R_{WIRE}=10ohm

6. Conclusion

In this article, a library-based IR-drop estimation method is presented. This method concludes two parts, one is a gate-level supply current waveform estimation method using standard library information and the other is an analytical library adjustment method with IR-drop effect consideration. Extra characterization efforts and regression cost can be avoided to obtain accurate IR-drop estimation with less overhead. As shown in the experimental results, such an efficient modification method can provided good accuracy on IR-drop estimation with limited information. The estimation errors of our approach are about 5% compared with HSPICE results.

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8. References

Blakiewicz, G. & Chrzanowska-Jeske, M. (2007). Supply current spectrum estimation of digital cores at early design. *IET Circuits Devices Syst.*, vol.1, no.3 (Jun. 2007), pp. 233-240, ISSN: 1751-858X

Boliolo, A.; Benini, L.; de Micheli, G. & Ricco, B.(1997). Gate-level power and current simulation of CMOS integrated circuits. *IEEE Trans. Very Large Scale Integr.(VLSI) Syst.* , vol.5, no.4 (Dec. 1997), pp.473-488, ISSN: 1063-8210

Cadence (2006), *Open Source ECSM Format Specification Version 2.1*, Cadence

Chen, H.-M.; Huang, L.-D.; Liu, I-M. & Wong, M.D.F (2005). Simultaneous power supply planning and noise avoidance in floorplan design. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 24, no.4 (Apr. 2005), pp. 578-587, ISSN: 0278-0070

Juan, D.-C.; Chen, Y.-T.; Lee, M.-C. & Chang, S.-C. (2010). An Efficient Wake-Up Strategy Considering Spurious Glitches Phenomenon for Power Gating Designs. *IEEE Trans. Very Large Scale Integr.(VLSI) Syst.*, vol. 18, no. 2 (Feb. 2010), pp. 246-255, ISSN: 1063-8210

Kawa, J. (2008). Low Power and Power Management for CMOS-An EDA Perspective. *IEEE Trans. Electron Devices*, vol. 55, no. 1 (Jan. 2008), pp.186-196, ISSN: 0018-9383

Lee, M.-S.; Lin, C.-H.; Liu, C.-N.J., & Lin, S.-C. (2008). Quick supply current waveform estimation at gate level using existed cell library information. *Proceedings of ACM Great Lakes Symp. on VLSI*, pp. 135-138, Orlando, FL, May 4-6 2008, ISBN: 978-1-59593-999-9

Lee, M.-S.; Lai, K.-S.; Hsu; C.-L., & Liu, C.-N.J. (2010). Dynamic IR drop estimation at gate level with standard library information. *Proceedings of IEEE Intl. Symp. Circuits and Systems*, pp. 2606-2609, Paris, France, May 2010, ISBN: 978-1-4244-5308-5

Michael, K.; David, F.; Rob, A.; Alan G. and Shi, K. (2008). *Low Power Methodology Manual for System-on-Chip Design.* Springer, ISBN-10: 0387718184, New York, USA

Popovich, M.; Sotman, M.; Kolodny, A. & Friedman, E. (2008). Effective radii of on-chip decoupling capacitors. *IEEE Trans. Very Large Scale Integr.(VLSI) Syst.*, vol. 16, no. 7 (July 2008), pp. 894-907, ISSN: 1063-8210

Shimazaki, K.; Tsujikawa, H.; Kojima, S. & Hirano, S. (2000). LEMINGS: LSI's EMI-noise analysis with gate level simulator. *Proceedings of IEEE Int. Symp. Quality Electronic Design*, pp. 129-136, San Jose, CA, Mar. 2000, ISBN: 0-7695-0525-2

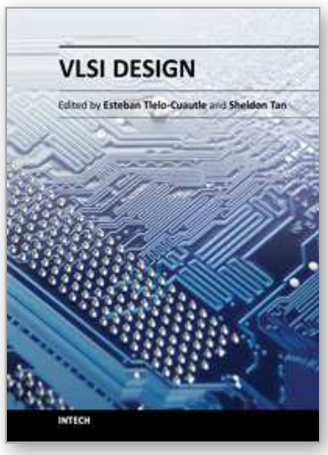
Synopsys (2003), Library *Compiler User Guide: Modeling Timing and Power Technology Libraries*, Synopsys

Synopsys (2008), *CCS Timing Library Characterization Guidelines Version 3.2*, Synopsys

Synopsys (2009), *PrimeTime PX User Guide Version C-2009.06*, Synopsys

Xu, H. ; Vemuri, R. & Jone, W. (2011). Dynamic Characteristics of Power Gating During Mode Transition. *IEEE Trans. Very Large Scale Integr.(VLSI) Syst.*, vol. 19, no. 2 (Feb. 2011), pp. 237-249, ISSN: 1063-8210

Zhao, S.; Roy, K. & Koh, C.-K. (2002). Decoupling capacitance allocation and its application to power-supply noise-aware floorplanning. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 21, no.1 (Jan. 2002.), pp. 81-92, ISSN: 0278-0070



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