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Some Basic Issues and Applications of Switch-Mode Rectifiers on Motor Drives and Electric Vehicle Chargers

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1. Introduction

Switch-mode rectifier (SMR) or called power factor corrected (PFC) rectifier (Erickson & Maksimovic, 2001; Mohan et al, 2003; Dawande & Dubey, 1996) has been increasingly utilized to replace the conventional rectifiers as the front-end converter for many power equipments. Through proper control, the input line drawn current of a SMR can be controlled to have satisfactory power quality and provide adjustable and well-regulated DC output voltage. Hence, the operation performance of the followed power electronic equipment can be enhanced. Taking the permanent-magnet synchronous motor (PMSM) drive as an example, field-weakening and voltage boosting are two effective approaches to enhance its high-speed driving performance. The latter is more effective and can avoid the risk of magnet demagnetization. This task can naturally be preserved for a PMSM drive being equipped with SMR.

Generally speaking, a SMR can be formed by inserting a suitable DC-DC converter cell between diode rectifier and output capacitive filter. During the past decades, there already have a lot of SMRs, the survey for single-phase SMRs can be referred to the related literatures. Since the AC input current is directly related to the pulse-width modulated (PWM) inductor current, the boost-type SMR possesses the best PFC control capability subject to having high DC output voltage limitation. In a standard multiplier based high-frequency controlled SMR, its PFC control performance is greatly affected by the sensed double-frequency voltage ripple. In (Wolfs & Thomas, 2007), the use of a capacitor reference model that produces a ripple free indication of the DC bus voltage allows the trade off regulatory response time and line current wave shape to be avoided. A simple robust ripple compensation controller is developed in (Chen et al, 2004), such that the effect of double frequency ripple contaminated in the output voltage feedback signal can be cancelled as far as possible. In (Li & Liaw, 2003), the quantitative digital voltage regulation control for a zero-voltage transition (ZVT) soft-switching boost SMR was presented. As to (Li & Liaw, 2004b), the robust varying-band hysteresis current-controlled (HCC) PWM schemes with fixed and varying switching frequencies for SMR have been presented. In (Chai & Liaw, 2007), the robust control of boost SMR considering nonlinear behavior was presented. The adaptation of voltage robust compensation control is made according to the observed nonlinear phenomena. The development and control for a SRM drive with front-end boost SMR were presented in (Chai & Liaw, 2009). In (Chai et al, 2008), the novel random

switching approach was developed for effectively reducing the acoustic noise of a low-frequency switching employed in a PMSM drive. In the bridgeless SMRs developed in (Huber et al, 2008), the higher efficiency is achieved by reducing loop diode voltage drops.
In some occasions, the galvanic isolation of power equipment from AC source is required. In (Hsieh, 2010), a single-phase isolated current-fed push pull (CFPP) boost SMR is developed, and the comparative evaluation for the PMSM drive equipped with standard, bridgeless and CFPP isolated boost SMRs is made.
From input-output voltage magnitude relationship, the buck-boost SMR is perfect in performing power factor correction control (Erickson & Maksimovic, 2001; Matsui et al, 2002). And it is free from inrush current problem owing to its indirect energy transfer feature. However, the traditional non-isolated buck-boost SMR possesses some limitations: (i) without isolation; (ii) having reverse output voltage polarity; (iii) discontinuous input and output currents; and (iv) having relatively high voltage and current stresses due to zero direct power transfer. As generally recognized, the use of high-frequency transformer isolated buck-boost SMR can avoid some of these limitations. The performance comparison study among Cuk, single ended primary inductor converter (SEPIC), ZETA and flyback SMRs in (Singh et al, 2006) concludes that the flyback SMR is the best one in the control performance and the required number of constituted component. In (Lamar et al, 2007), in addition to the power rating limits, the limitations of flyback SMR in PFC characteristics and output voltage dynamic response are discussed.
In (Papanikolaou et al, 2005), the design of flyback converter in CCM for low voltage application is presented. In the power circuit developed in (Lu et al, 2003), a dual output flyback converter is employed to reduce the storage capacitor voltage fluctuation against input voltage and load changes of flyback SMR in DCM. Similarly, two flyback converters are also used in the flyback SMRs developed in (Zheng & Moschopoulos, 2006) and (Mishra et al, 2004) to achieve direct power transfer and improved voltage regulation control characteristics. As to the single-stage SMR developed in (Lu et al, 2008), it combines a boost SMR front-end and a two-switch clamped flyback converter. Similarly, an intermediate energy storage circuit is also employed. In (Rikos & Tatakis, 2005), a new flyback SMR with non-dissipative clamping is presented to obtain high power factor and efficiency in DCM. The proposed clamping circuit utilizes the transformer leakage inductance to improve input current waveform. In (Jang et al, 2006), an integrated boost-flyback PFC converter is developed. The soft switching of all its constituted switches is preserved to yield high efficiency. On the other hand, the improved efficiency of the flyback converter presented in (Lee et al, 2008) is obtained via the use of synchronous rectifier.
It is known that digital control for power converter is a trend to promote its miniaturization. In (Newsom et al, 2002), the control scheme realization is made using off-the-shelf digital logic components. And recently, the VLSI design of system on chip application specific integrated circuit (SoC-ASIC) controller for a double stage SMR has also been studied in (Langeslag et al, 2007). It consists of a boost SMR and a flyback DC-DC converter. The latter is controlled using valley-switching approach operating in quasi-resonant DCM, which has fixed on-time and varying off-time according to load.
As far as the switching control strategies are concerned, they can be broadly categorized into voltage-follower control (Erickson & Madigan, 1990) and current-mode control (Backman & Wolpert, 2000). The former belongs to open-loop operation under DCM, and thus the current feedback control is not needed. As to the latter, the multiplier-based current control loop is necessary to achieve PFC control. Basically, the commonly used PWM switching control approaches for a flyback SMR include peak current control (Backman & Wolpert,

2000), average current control, charge control and its modifications (Tang et al, 1993). In the peak current controlled flyback converter presented in (Backman & Wolpert, 2000), the proper choice of magnetizing inductance is suggested to reduce the distortion of input current. In (Tang et al, 1993; Larouci et al, 2002), after turning on the switch at clock, the switch is turned off as the integration of switch current is equal to the control voltage. As to (Buso et al, 2000), a modified nonlinear carrier control approach is developed to avoid the sense of AC input voltage. For easily treating the dynamic control of a single-stage PFC converter, its general dynamic modeling and controller design approaches have been conducted in (Uan-Zo-li et al, 2005). In addition, there were also some special control methods for flyback SMR. See for example, a simplified current control scheme using sensed inductor voltage is developed in (Tanitteerapan & Mori, 2001). In (Y.C. Chang & Liaw, 2009a), a flyback SMR in DCM with a charge-regulated PWM scheme is developed.

For a SMR, the nonlinear behavior and the double-frequency voltage ripple may let the closed-loop controlled SMR encounter undesired nonlinear phenomena (Orabi & Ninomiya, 2003). The key parameters to be observed in nonlinear behavior of a SMR will be the loading condition, the value of output filtering capacitor and the voltage feedback controller parameters. In the flyback SMR developed in (Y.C. Chang & Liaw, 2009a), the simple robust control is proposed to avoid the occurrence of nonlinear phenomena, and also to improve the SMR operating performance.

Random PWM switching is an effective means to let the harmonic spectrum of a power converter be uniformly distributed. Some typical existing studies concerning this topic include the ones for motor drives (Liaw et al, 2000), DC-DC converters (Tse et al, 2000), SMRs (Li & Liaw, 2004b; Chai et al, 2008), etc. In the flyback SMR developed by (Y.C. Chang & Liaw, 2011), to let the harmonic spectrum be dispersdly distributed, a random switching scheme with fixed turn-on period and varying turn-off period is presented.

Although flyback SMR possesses many merits, it suffers from the major limitation of having limited power rating. To enlarge the rating, the parallel of whole isolated converter of flyback SMR was made in (Sangsun & Enjeti, 2002). In the existing interleaved flyback converters, the researches made in (Forest et al, 2007, 2009) are emphasized on the use of intercell transformers. However, the typical interleaving of flyback SMR requires multiple switches and diodes, which increases the cost and complexity of power circuit. For a single-phase flyback SMR, the major DC output voltage ripple is double line frequency component. Hence PWM interleaving control is not beneficial in its ripple reduction. Moreover, the power limitation of flyback transformer is more critical than the other system active components. It follows that sole parallel of transformer (Manh & Guldner, 2006; Inoue et al, 2008) will be the convenient way to enlarge the rating of whole flyback SMR. In (Y.C. Chang & Liaw, 2009b), the rating enlargement is made by parallel connection of transformer.

For the power equipments with higher ratings, the three-phase SMR is a natural choice for higher rated plants. The systematic surveys for the existing three-phase SMRs can be found in (Hengchun et al, 1997; Shah et al, 2005). Similar to transformers, three-phase SMRs can also be formed using multiple single-phase SMR modules via proper connection (Hahn et al, 2002; Li & Liaw, 2004c). For simplicity and less stringent performance, the three-phase single-switch (3P1SW) SMR will be a good choice. In the 3P1SW SMR presented in (Chai et al, 2010), a robust current harmonic cancellation scheme and a robust voltage control scheme are developed. The undesired line current and output voltage ripples are regarded as disturbances and they are reduced via robust controls. In voltage control, a feedback controller is augmented with a simple robust error canceller. The robust cancellation

weighting factor is automatically tuned according to load level to yield compromised voltage and power quality control performances.
Similar to single-phase bridgeless SMRs (Zhang et al, 2000; Youssef et al, 2008), there were also some researches being emphasized on the development of three phase bridgeless SMRs (Reis et al, 2008; Oliverira et al, 2009). In (Wang, 2010), a bridgeless DCM three phase SMR is developed and used as a front-end AC-DC converter for the SRM drive.
As generally recognized, soft-switching can be applied for various converters to reduce their switching lossess, voltage stresses and electromagnetic interference. The applications of soft-switching in 3P1SW SMRs have also been conducted in (Gataric et al, 1994; Ueda et al, 2002). For the 3P1SW SMR operating under DCM, only the zero-current switching (ZCS) at turn-off is effective in reducing its switching losses. In (Wang, 2010), the zero-current transition (ZCT) (Gataric et al, 1994) is utilized to the developed 3P1SW to achieve the ZCS of the main switch at turn-off. In realization, an auxiliary resonant branch is added, and the proper switching signals are generated for the main and auxiliary switches. The soft-switching can be achieved without adding extra sensors. And also in (Wang, 2010), the comparative performance evaluation is made for the SRM drive powered using standard 3P1SW SMR, ZCT 3P1SW SMR and bridgeless DCM three phase SMR.

2. Power factor correction approaches

For facilitating the research made concerning power quality, the commonly referred harmonic standard is first introduced. Then the possible power factor correction approaches are described to comprehend their comparative features.

2.1 Harmonic ccurrent emission standard

IEC 61000-3-2 (previously, IEC-555) is the worldwide applied harmonic current emission standard. This standard specifically limits harmonics for equipments with an input current up to 16A, connected to 50Hz or 60Hz, 220V to 240V single phase circuit (two or three wires). The IEC 61000-3-2 standard distinguishes the loads into four classes with different harmonic limits (Erickson & Maksimovic, 2001; Mohan et al, 2003). From the contents one can find that for the equipments below 600W, the harmonic limits of Class A are larger than those of Class D. This advantage will be more significant for lower power level. Taking the third harmonic under 100W as an example, the limit in Class A is 2.3A compared to 0.34A in Class D. Power converter can apply Class D or Class A regulation depending on its input current wave shape. The peaky line drawn current of a diode rectifier with larger filtering capacitor definitely belongs to Class D. However, if the simple low-frequency switching SMR (Chai et al, 2008) is employed, the modified line drawn current may fall into Class A and thus possesses the advantage mentioned above.

2.2 Possible power factor correction methods

Depending on rating, schematic and control complexities, control performance and cost, there are many possible power factor correction approaches. The suited and cost effective one can be chosen according to the desired performance for specific application.

2.2.1 Passive filter

Various series L-C resonant trap filters are connected across the line terminal to attenuate the specific order harmonics. This approach is simple, rugged, reliable and helpful in

reducing EMI. However, it is bulky and cannot completely regulate nonlinear loads, and it is needed the redesign adapted to load changes.

2.2.2 Active power filter

Compared with passive filter, active power filter (APF) has the higher control ability to compensate load reactive and harmonic current components. According to the types of connections, active power filters can be categorized into series, shunt and hybrid types (Erickson & Maksimovic, 2001; Mohan et al, 2003). Taking the shunt type active power filter as an example, a controlled current is generated from the APF to compensate the load ripple current as far as possible.

2.2.3 Passive PFC circuits

Fig. 1(a) shows the sketched key waveforms of a full-bridge rectifier with large and small filtering capacitors. One can be aware that if a very small filtering capacitor is employed, the line drawn power quality is improved, and thus the Class A rather than the Class D is applied. However, the effects of DC-link voltage ripple should be considered in making the control of the followed power stage. Recently, to reduce the rectified DC voltage ripple, some plants employ the valley-fill filter as shown in Fig. 1(b) (Farcas et al, 2006).

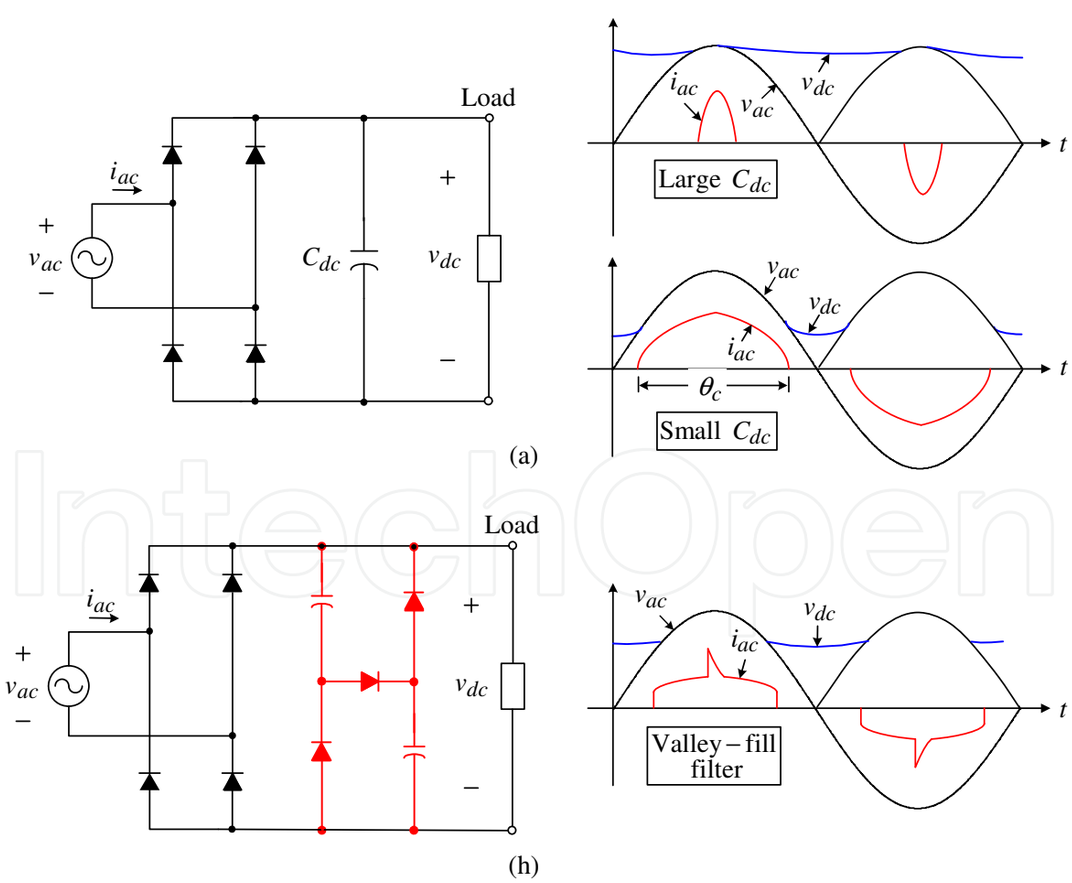

Fig. 1. Some passive PFC circuits: (a) rectifier with small filtering capacitor; (b) rectifier using valley-fill filter

2.2.4 Switch-mode rectifier

The SMRs possess many categories in circuit topology and switching control approaches. A single-phase boost-type SMR is shown in Fig. 2(a), and the typical waveforms of i_{ac} using low-frequency (LF) and high-frequency (HF) switchings are sketched in Figs. 2(b) and 2(c). The features of HF-SMR comparing to LF-SMR are: (i) more complicated in control; (ii) high control performances in line drawn current, power factor and output voltage; (iii) lower efficiency. More detailed survey for SMRs will be presented in the latter paragraphs.

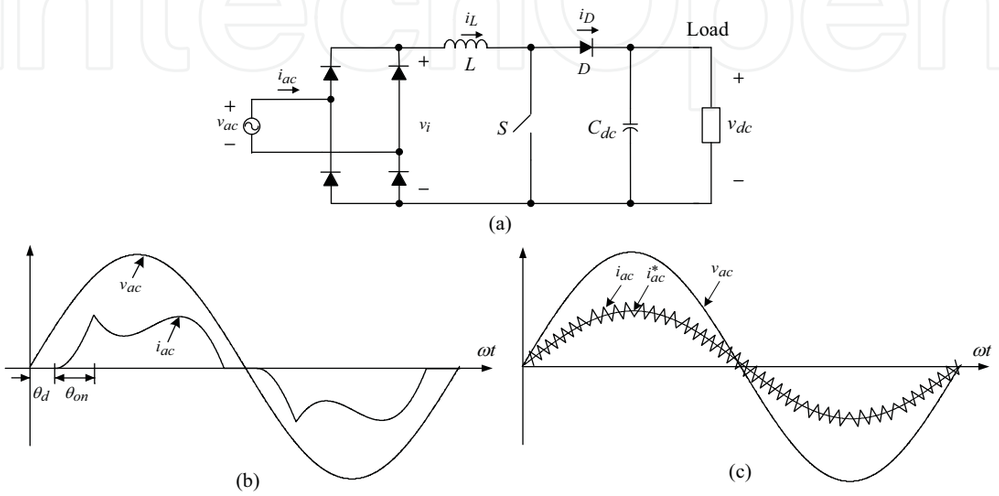

Fig. 2. Boost-type SMR: (a) circuit; (b) sketched key waveforms for low-frequency switching; (c) sketched waveforms for high-frequency switching

3. Classification of SMRs

Basically, a SMR is formed by inserting a suited DC/DC converter between diode rectifier and capacitive output filter, under well regulated DC output voltage, the desired AC input line drawn power quality can be achieved. The existing SMRs can be categorized as:

1. **Schematics**

a. Single-phase or three-phase: each category still possesses a lot of types of SMR schematics. The three-phase SMR will be a natural choice for larger power plants.
b. Non-isolated or isolated: although the former SMR is simpler and more compact, the latter one should be used if the galvanic isolation from mains is required. See for example, the flyback SMR is gradually employed in communication distributed power architecture as a single-stage SMR front-end, or called silver box, to establish -48V DC-bus voltage.
c. Voltage buck, boost or buck/boost: depending on the input-output relative voltage levels, suited type of SMR and its control scheme should be chosen. Basically, the boost-type SMR possesses the best current control ability subject to having high DC output voltage level.
d. Single-stage or multi-stage: generally speaking, the stage number should be kept as small as possible for achieving higher efficiency and system compactness. Hence, single-stage SMR is preferable if possible.

e. One-quadrant or multi-quadrant: multiple quadrant SMR may possess reverse power flow from DC side to AC source, such as the regenerative braking of a SMR-fed AC motor drive can be performed by sending braking energy back to the utility grid.
f. Hard-switching or soft-switching: Similarly, suited soft switching technique can also be applied to reduce the switching loss, switching stress and EMI of a SMR (Li & Liaw, 2003; Wang, 2010).

2. Control methods

a. Low-frequency control: only v-loop is needed and only one switching per half AC cycle is applied. It is simple but has limited power quality characteristics.
b. High-frequency control- voltage-follower control: without current control loop, only some specific SMRs operating in DCM possess this feature, see for example, buck-boost SMR and flyback SMR.
c. High-frequency control- standard control: it belongs to multiplier-based current-mode control approach with both v- and i- control loops.

3.1 Single-phase SMRs

The typical existing single-phase SMR circuits include: (a) boost SMR; (b) buck SMR; (c) buck- boost SMR; (d) Ćuk SMR; (e) SEPIC SMR with coupled inductors; (f) SEPIC SMR; (g) ZETA SMR; (h) buck-boost cascade SMR; (i) boost-buck hybrid SMR; (j) flyback SMR; (k) isolated Ćuk SMR; and (l) isolated ZETA SMR. Some comments are given for these circuits: (i) The SMRs of (a) to (i) belong to non-isolated types, whereas (j) to (l) are isolated ones; (ii) Among the non-isolated SMRs, the boost-type SMR possesses the best PFC control performance, since its AC input current is directly related to the switched inductor current; (iii) The circuits of (d), (i) and (k) possess the common features of having both continuous input and output currents, and hence needing less stringent filter design requirement.
In addition to the SMRs of (j) to (l) mentioned above, some isolated SMRs specifically for PMSM drives (Singh B. & Singh S., 2010) include: (a) push-pull buck; (b) push-pull boost; (c) half-bridge buck; (d) half-bridge boost; (e) full-bridge buck; (f) full-bridge boost. The push-pull boost SMR possesses excellent PFC control ability and high voltage boost ratio.

3.2 Three-phase SMRs

Detailed surveys for the existing three-phase SMR circuits can be referred to (Hengchun et al, 1997; Shah & Moschopoulos, 2005). The complexities of schematic and control mechanism depend on the control ability and the desired performances. Some commonly used boost-type SMRs are briefly introduced as followed.

3.2.1 Three-leg six-switch standard SMR

The standard three-phase six-switch SMR (Hengchun et al, 1997; Shah & Moschopoulos, 2005) possesses four operation quadrants and high flexibility in power conditioning control. For a motor drive equipped with such SMR, it may possess regenerative braking ability. However, the switch utilization ratio of this SMR is low, and its control is complicated.

3.2.2 Four-leg eight-switch SMR

In the four-leg three-phase SMR (Zhang et al, 2000) with eight switches, the additional fourth leg can be arranged to regulate the imbalance caused by source voltage and switching operation, and it can provide fault tolerant operation.

3.2.3 Three-switch Vienna SMR

The Vienna three-phase SMR (Youssef et al, 2008) uses only three switches to achieve good current command tracking control. It can be regarded as a simplified version of three single-phase PFCs connected to the same intermediate bus voltage. The major features of this SMR are: (i) three output voltage levels ($0.5v_o$, v_o, $-0.5v_o$) providing larger switching control flexibility; (ii) lower switch voltage rating, $0.5\,v_o$ rather than v_o; and (iii) lower input current distortion. However, it has only unidirectional power flow capability, and needs complicated power switch and two serially connected capacitors. The specific power switch (VUM 25-05) for implementing this SMR is avaiable from IXYS Corporation, USA.

3.2.4 Single-switch SMR

The three-phase single-switch SMR (3P1SW) possesses the simplest schematic and control scheme. By operating it in DCM, the PFC is naturally preserved without applying current PWM control. However, it possesses the limits: (i) Having higher input peak current and switch stress; (ii) The input line current contains significant lower-frequency harmonics with the orders of $6n \pm 1$, n=1, 2, …, and the dominant ones are the 5th and 7th harmonics. Thus suitably designed AC-side low-pass filter is required to yield satisfactory power quality; (iii) The line drawn power quality is limited, typically the power factor is slightly higher than 0.95; (iv) Similarly, this 3P1SW SMR possesses only one-quadrant capability.

To improve the input power quality of this three-phase single-switch SMR, many existing researches have been conducted, see for example: (i) Fifth-order harmonic band-stop filtering; (ii) Harmonic-injection approach; (iii) Variable switching frequency controls; (iv) Passive filtering and input current steering; (v) Optimum PWM pattern; and (vi) Injected PWM robust compensation control. In (Chai et al, 2010), the robust current harmonic cancellation scheme is developed to yield improved line drawn power quality. The robust cancellation weighting factor is automatically tuned according to load level.

3.2.5 Two-switch SMR

This SMR (Badin & Barbi, 2008) is constructed by two serially connected DC/DC boost converter cells behind the rectifier. It possesses only unidirectional power flow capability. The boost converters are applied to shape the input currents, and the current injection device is used to inject the third-harmonic currents in front of the diode bridge to improve the line drawn power quality. This converter uses fewer switches but possesses higher input current harmonics.

3.2.6 Modular connection using single-phase SMRs

Similar to three-phase transformers, three-phase SMRs can also be formed by suitable connection of multiple single-phase modules (Hahn et al, 2002; Li & Liaw, 2004c). Fig. 3(a) shows a Y-connected three-phase boost-type SMR. For $\Delta-$connected three-phase SMR, when one module is faulted, the remaining two modules can continuously provide DC power output subject to the reduction of rating.

3.2.7 Bridgeless SMR

As shown in Fig. 3(b) (Reis et al, 2008; Oliverira et al, 2009), the SMR uses three diodes and three switches rather than using diode bridge rectifier. Obviously, one diode drop is

eliminated in each line-current path resulting to increase the efficiency compared to single-switch SMR. However, two additional power switches are employed.

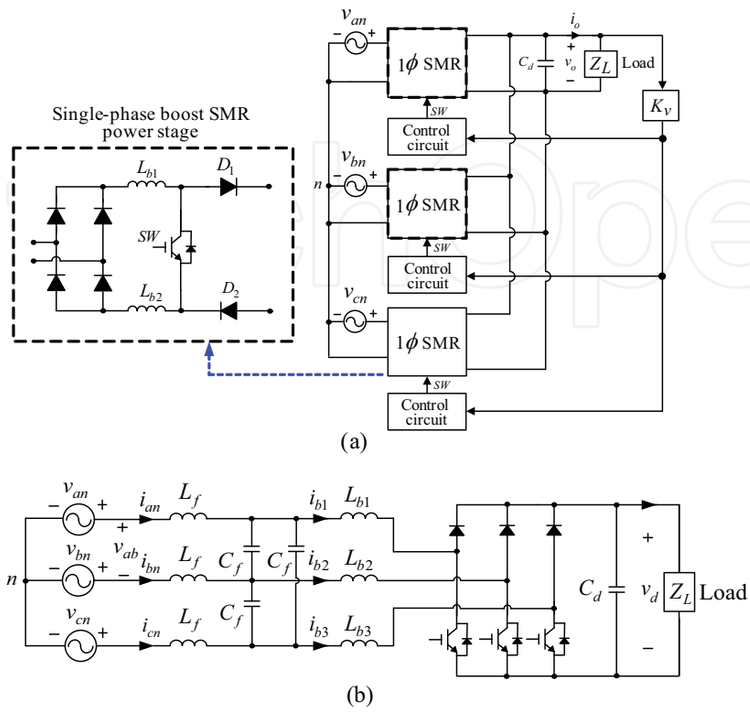

Fig. 3. Two types of SMRs: (a) modular connection of three single-phase SMRs;
(b) bridgeless DCM three-phase SMR

3.3 Three-phase single-switch ZCT SMRs

The soft-switching SMRs using auxiliary switching circuit can be generally classified into zero-voltage-transition (ZVT) and zero-current-transition (ZCT). The choice depends on the semiconductor devices to be used. The ZVS approaches are generally recommended for MOSFET. On the other hand, ZCS approaches are effective for IGBT. Some existing soft-switching SMRs are introduced as follows:

3.3.1 Classical three-phase single-switch ZCT SMR

The classical 3P1SW ZCT SMR (Wang et al, 1994) is simple in structure and easy to realize. However, the auxiliary switch is not operated on ZCS at turn-off. The efficiency is limited.

3.3.2 Modified three-phase single-switch ZCT SMR

In the modified 3P1SW ZCT SMR presented in (Das & Moschopoulos, 2007). The addition of the transformer in the auxiliary circuit let the circulating energy from the auxiliary circuit be transferred to the output. Hence it possesses higher efficiency than the classical type.

3.3.3 Three-phase three-switch bridgeless ZCT SMR

As to the three-phase bridgeless ZCT SMR (Mahdavi & Farzanehfard, 2009), the auxiliary circuit provides soft-switching condition through ZCT approach for all semiconductor devices without any extra current and voltage stress.

4. Operation principle and some key issues of SMR

4.1 Single-phase SMRs

Fig. 4 shows the conceptual configuration of a single-phase SMR. The AC source input voltage is expressed as $v_{ac} = V_m \sin \omega t = \sqrt{2} V_{ac} \sin \omega t$. If the AC input current i_{ac} can be regulated to be sinusoidal and kept in phase with v_{ac}, then the ideal SMR is similar to an emulated resistor with the effective resistance of R_e viewing from the utility grid. In reality, the double line frequency output voltage ripple always exists for an actual SMR with finite value of output filtering capacitor. This ripple may contaminate to distort the current command, and hence to worsen the power quality control performance. The output power $p(t)$ of the SMR shown in Fig. 4 can be expressed as:

$$\begin{aligned} p(t) = P_{ac} &= \frac{V_m^2}{R_e} \sin^2 \omega t = \frac{V_m^2}{2R_e}(1 - \cos 2\omega t) = \frac{V_{ac}^2}{R_e} - \frac{V_{ac}^2}{R_e} \cos 2\omega t \\ &= \frac{V_d^2}{R_d} - \frac{V_{ac}^2}{R_e} \cos 2\omega t \triangleq P_d + P_{ac2} \end{aligned} \tag{1}$$

where P_d and P_{ac2} respectively denote the output DC and the double-frequency power components. From the average power invariant property in (1), one can obtain the following equivalent resistance transfer relationship:

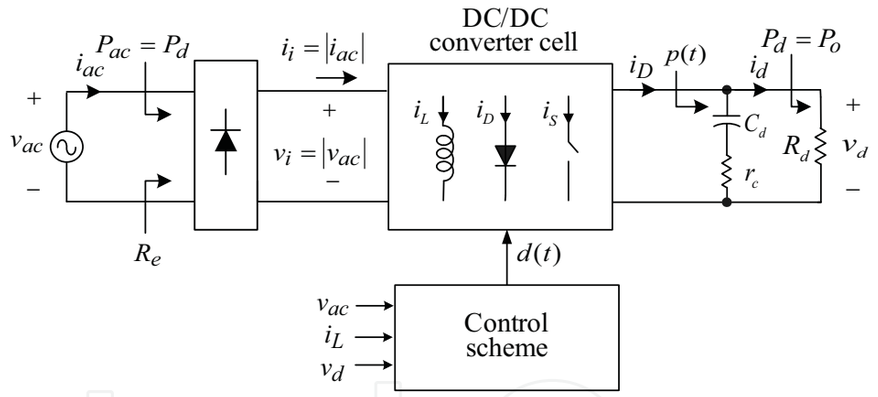

Fig. 4. Conceptual configuration of a single-phase SMR

$$\frac{V_d}{V_{ac}} = \sqrt{\frac{R_d}{R_e}} \tag{2}$$

By neglecting the capacitor ESR r_c in Fig. 4, the current $i_d(t)$ can be found from (1):

$$i_d(t) \cong \frac{p(t)}{V_d} = \frac{V_{ac}^2}{R_e V_d}(1 - \cos 2\omega t) = I_d + i_{d2} \tag{3}$$

The AC component i_{d2} is approximately regarded flowing through the capacitor:

$$C_d \frac{d\Delta v_d(t)}{dt} = -\frac{V_{ac}^2}{R_e V_d} \cos 2\omega t \tag{4}$$

Then the voltage ripple $\Delta v_d(t)$ can be found by integrating the above equation:

$$\Delta v_d(t) = \frac{1}{C_d}\int -\frac{V_{ac}^2}{R_e V_d}\cos 2\omega t dt = \frac{1}{2\omega C_d V_d}\frac{V_{ac}^2}{R_e}\sin 2\omega t = \frac{V_d}{2\omega C_d}\frac{1}{R_d}\sin 2\omega t \tag{5}$$

From (5) one can get the peak to peak value of output ripple voltage:

$$\Delta v_d = \frac{V_d}{\omega C_d R_d} \tag{6}$$

4.2 Three-phase SMRs

4.2.1 Three-Phase Single-Switch (3P1SW) SMR

For a well-regulated three-phase single-switch (3P1SW) DCM SMR shown in Fig. 5, it can be regarded as a loss-free emulated resistor R_e viewing from the phase AC source with line drawn current having dominant 5th and 7th harmonics (Chai et al, 2010). Hence, the three-phase line drawn instantaneous power can be approximately expressed as:

$$\begin{aligned} p_{ac} &= v_{an}i_a + v_{bn}i_b + v_{cn}i_c = \frac{V_m^2 \sin\omega t}{R_e}[\sin\omega t - \frac{1}{5}\sin 5\omega t - \frac{1}{7}\sin 7\omega t] + \\ &\frac{V_m^2 \sin(\omega t - 2\pi/3)}{R_e}[\sin(\omega t - 2\pi/3) - \frac{1}{5}\sin 5(\omega t - 2\pi/3) - \frac{1}{7}\sin 7(\omega t - 2\pi/3)] + \\ &\frac{V_m^2 \sin(\omega t + 2\pi/3)}{R_e}[\sin(\omega t + 2\pi/3) - \frac{1}{5}\sin 5(\omega t + 2\pi/3) - \frac{1}{7}\sin 7(\omega t + 2\pi/3)] \\ &= \frac{3V_m^2}{2R_e} - \frac{3V_m^2}{35R_e}\cos 6\omega t \triangleq P_{ac} + \delta p_{ac} \end{aligned} \tag{7}$$

where P_{ac} = average AC power, δp_{ac} = ripple AC power. By neglecting all power losses, one has $P_o = P_d$, i.e.,

$$P_{ac} = \frac{3V_m^2}{2R_e} = \frac{V_d^2}{R_d} \tag{8}$$

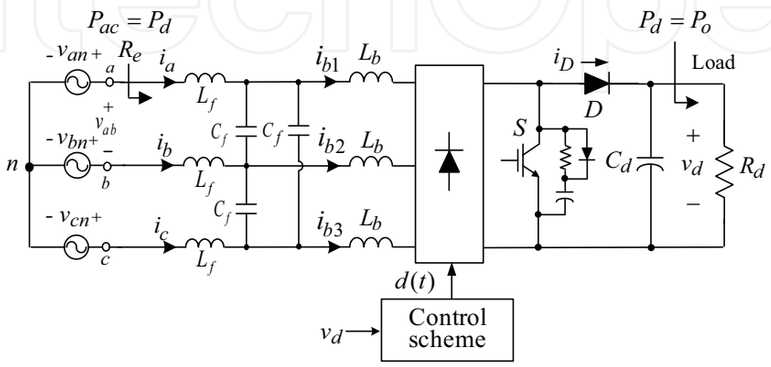

Fig. 5. Conceptual configuration of a three-phase DCM SMR

Then from (7) and (8), the AC charging current flowing the output filtering capacitor is:

$$C_d \frac{dv_d}{dt} = -\frac{2V_d}{35R_d}\cos 6\omega t \tag{9}$$

Thus one can derive the peak-to-peak output voltage ripple:

$$\Delta v_d = \frac{2V_d}{105\omega R_d C_d} \tag{10}$$

4.2.2 Three-phase three-switch and six-switch SMRs

For the Vienna SMR and three-phase six-switch standard SMR with ideal current mode control, the three-phase line drawn currents will be balanced without harmonics. Hence, from (7) one can find that the DC output voltage ripple will be nearly zero.

4.3 Some key issues of SMR

Taking the DSP-based single-phase standard boost SMR as an example, some key issues are indicated in Fig. 6. In power circuit, the ripples and ratings of the constituted components must be derived, and accordingly the components are properly designed and implemented. Some typical examples can be referred to (Li & Liaw, 2003; Chai & Liaw, 2007; Y.C. Chang & Liaw, 2009a; H.C. Chang & Liaw, 2009).

As to the control scheme, the sensed inductor current and output voltage should be filtered. The feedback controller must first be properly designed considring the desired perfromance and the effects of comtaiminated noises in sensed variables. For satisfying more strict control requirements, in addition to the basic feedback controls, the robust tracking error cancellation controls (Chai & Liaw, 2007; Y.C. Chang & Liaw, 2009a) can further be added. In making DSP-based digital control, the sampling rates are selected according to the achievable loop dynamic response. Other issues may include: (a) random switching to yield spread harmonic spectral distribution (Li & Liaw, 2004b; Chai & Liaw, 2008; Y.C. Chang & Liaw, 2011); (b) the effects of DC-link ripples on the motor drive operating performance (Chai & Liaw, 2007, 2009; Chai et al, 2010); (c) rating enlargement via parallel connection of transformers (Y.C. Chang & Liaw, 2009b) and SMR modules (Li & Liaw, 2004a).

5. Comparative evaluation of three single-phase boost SMRs

Three single-phase boost SMRs are comparatively evalued their prominences experimentally in serving as front-end AC/DC converters of a PMSM drive. For completeness, the traditional diode rectifier is also included as a reference.

5.1 Standard single-phase boost SMR

5.1.1 System configuration

The power circuit and control scheme of the developed SMR are shown in Fig. 6, wherein the two robust controllers are removed. This control system belongs to multi-loop configuration consisting of inner RC-CCPWM scheme and outer voltage loop. The low-pass filtering cut-off frequencies for the sensed current and voltage are respectively set as $f_{ci} = 12\text{Hz}$ and $f_{cv} = 600\text{Hz}$. And the digital control sampling rates of the two loops are chosen as $f_{si} = f_s = 25\text{kHz}$ and $f_{sv} = 2.5\text{kHz}$.

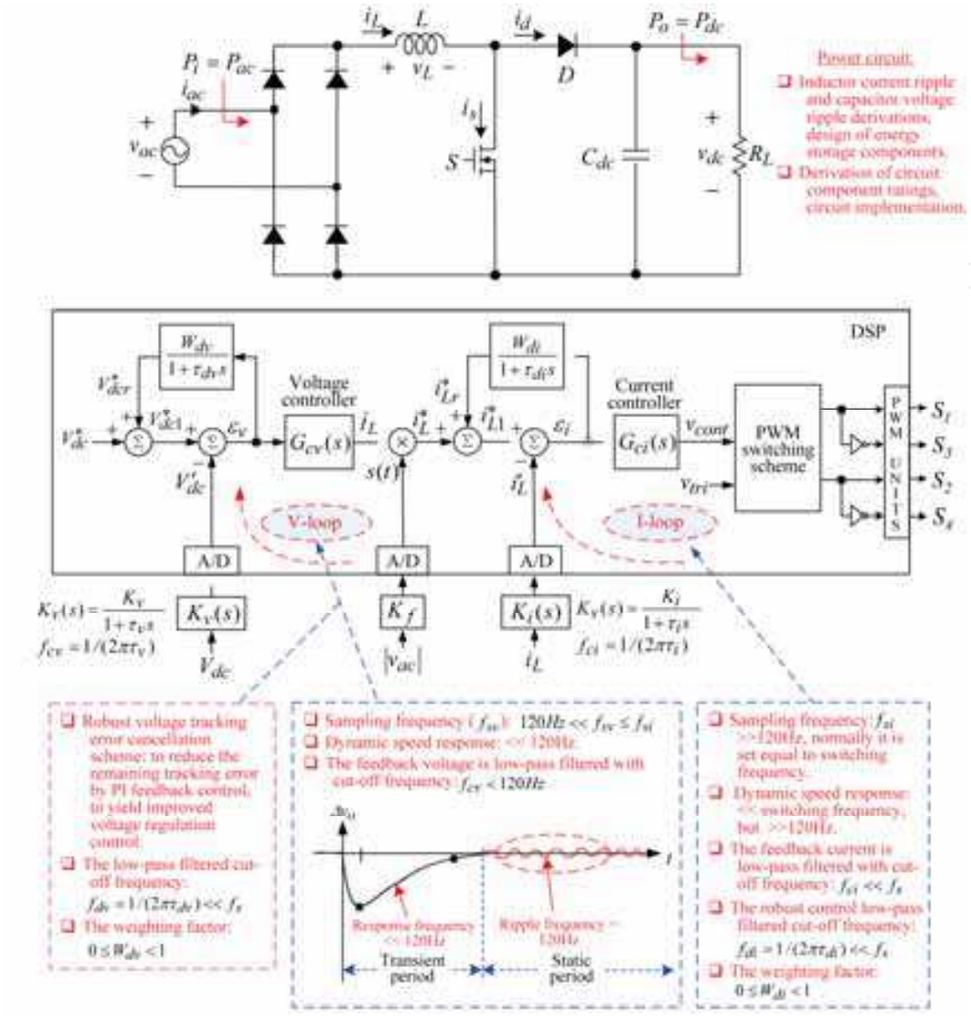

Fig. 6. Key issues of a DSP-based single-phase standard boost SMR

The system variables and specifications of the established SMR are given as follows:

AC input voltage: $V_{ac} = 110\text{V} \pm 10\% / 60\text{Hz}$.

DC output: $V_{dc} = 300\text{V} \sim 350\text{V}$ $(\ge 110\text{V} \times 1.1 \times \sqrt{2} = 171\text{V})$, $P_{dc} = 1500\text{W}$.

Switching frequency: $f_s = 25\text{kHz}$.

Efficiency: $\eta \ge 90\%$. Power factor: $PF \ge 0.95$ (Lagging).

5.1.2 Design of circuit components

The design of energy storage inductor, output filtering capacitor and power devices for this type of SMR are made according to the given specifications.

a. Boosting inductor

Some assumptions are made in performing the inductor design: (i) continuous conduction mode (CCM); (ii) all constituted components are ideal; (iii) $v_{dc} = V_{dc} = 350\text{V}$; (iv) $v_{ac} \triangleq \sqrt{2}V_{ac}\sin\omega t$, $V_{ac,\min} = 110\text{V} \times 0.9 = 99\text{V}$, $\hat{V}_{ac,\min} = \sqrt{2}V_{ac,\min} = 140\text{V}$; (v) the inductor current ripple is treated at $\omega t = 0.5\pi$, since at which the current ripple is maximum.

The maximum inductor current occurred at $\omega t = 0.5\pi$ can be calculated as

$$(\hat{i}_L)_{\max} = \frac{P_{dc}}{\hat{V}_{ac,\min}\eta} \times 2 = \frac{1500}{110 \times \sqrt{2} \times 0.9 \times 0.9} \times 2 = 23.81\text{A} \tag{11}$$

Let the inductor current ripple be:

$$\Delta i_L = \frac{\hat{V}_{ac,\min} D T_s}{L} \le 0.1(\hat{i}_L)_{\max} = 2.38\text{A} \tag{12}$$

The instantaneous duty ratio at $\omega t = 0.5\pi$ can be found as:

$$D = \frac{V_{dc} - \hat{V}_{ac,\min}}{V_{dc}} = \frac{350 - 140}{350} = 0.6 \tag{13}$$

Hence from (12) and (13), the condition of boosting inductance L is obtained as:

$$L \ge \frac{\hat{V}_{ac,\min} D}{f_s \Delta i_L} = 1.41\text{mH} \tag{14}$$

The inductor L is formed by serially connected two available inductors L_1 and L_2. The measured inductances using HIOKI 3532-50 LCR meter are L_1 = (2.03mH, ESR = 210mΩ at 60Hz, and 1.978mH, ESR= 5.68Ω at 25kHz) and L_2 = (2.11mH, ESR= 196mΩ at 60Hz, and 1.92mH, ESR= 62Ω at 25kHz). Hence $L = L_1 + L_2$ =4.14mH, which is suited here.

b. Output capacitor

By choosing the output filtering capacitor $C_d = 2200\mu\text{F}/450\text{V}$, the peak-to-peak output voltage ripple can be found as:

$$\Delta V_{dc} = \frac{V_{dc}}{\omega_1 R_L C_d} = \frac{P_{dc}}{\omega_1 C_d V_{dc}} = \frac{1500}{2\pi \times 60 \times 2200 \times 10^{-6} \times 350} = 5.17\text{V} \tag{15}$$

c. Power semiconductor devices

The maximum current of the main switch S and the diode D is $(\hat{i}_L)_{\max} + 0.5\Delta i_L = 25\text{A}$, which is calculated from (11) and (12), and their maximum voltage is 350V. Accordingly, the MOSFET IXFK44N80P (IXYS) (800V, ID= 44A (continuous), IDM = 100A (pulsed)) and the fast diode DSEP60-06A (IXYS) (600V, average current IFAVM = 60A) are chosen for implementing the main switch S and all diodes respectively.

5.1.3 Control schemes

Current controller:

he current feedback controller $G_{ci}(s)$ in Fig. 6 is chosen to be PI-type:

$$G_{ci}(s) = K_{Pi} + \frac{K_{Ii}}{s} \tag{16}$$

The upper limit of the P-gain is first determined based on large-signal stability at switching frequency:

$$\frac{dv_{cont}}{dt} = K_{Pi}K_i \frac{\left|V_{dc} - |v_{ac}|\right|}{L} < \frac{dv_{tri}}{dt} \tag{17}$$

The parameters of the developed SMR shown in Fig. 6 are set as: $V_{dc} = 300\text{V}$, $K_i = 0.04\text{V/A}$, $f_s = 25\text{kHz}$, $L = 4.14\text{mH}$ and $dv_{tri}/dt = 25\text{kV/sec}$. Using the given data, the upper value of the K_{Pi} can be found from (17) to be $K_{Pi} < \overline{K}_{Pi} = 8.625$ ($v_{ac} = 0$ is set here). Accordingly $K_{Pi} = 4.0$ is set.

In making the determination of integral gain, the magnitude frequency response of the loop gain $LG(s = j\omega) \triangleq i_L(s) / \varepsilon_i(s)\big|_{s=j\omega}$ is measured using the HP 3563A control systems analyzer as shown in Fig. 7, wherein V_{inj} denotes an injected swept sine signal. Fig. 8 shows the measured magnitude frequency response of the loop gain. The measurement conditions are set as: (i) $v_{inj,peak} = 10\text{mV}$; (ii) swept sine frequency range is from 400Hz to 11kHz; (iii) the voltage loop is opened, and the current command is set as $I_L^* = \hat{I}_L \times |v_{ac}|$ with $\hat{I}_L = 8\text{A}$; (iv) $R_L = 200\Omega$; (v) $v_{ac} = 110\text{V}_{\text{rms}}$; (vi) the current feedback controllers are set as $K_{Pi} = 4$ and $K_{Ii} = 45000$. The measured result in Fig. 8 indicates that the crossover frequency is $f_c = 1.47\text{kHz} < f_s / 2$, which is reasonable for a ramp-comparison current-controlled PWM scheme. Hence finally,

$$G_{ci}(s) = K_{Pi} + \frac{K_{Ii}}{s} = 4 + \frac{45000}{s} \tag{18}$$

If the measurement of loop-gain frequency response is not convenient, one can also use the derived small-signal dynamic model (Chai & Liaw, 2007), or using trail-and-error approach to determine the integral gain.

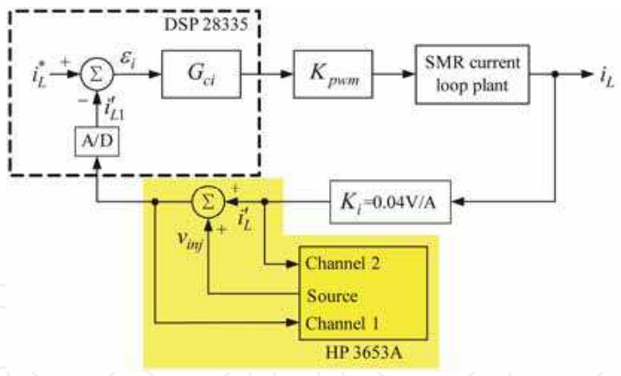

Fig. 7. System configuration in current loop gain measurement

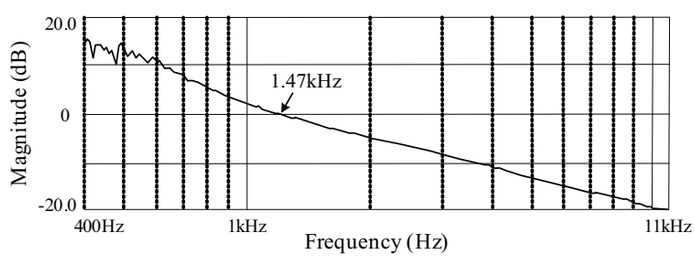

Fig. 8. Measured magnitude frequency response of current loop gain

Voltage controller:
Although the quantitative controller design can be achieved (Y.C. Chang & Liaw, 2009a), the PI voltage feedback controller is chosen trial-and-error here to be:

$$G_{cv}(s) = K_{Pv} + \frac{K_{Iv}}{s} = 8 + \frac{200}{s} \tag{19}$$

5.1.4 Experimental results

Let V_{ac} =110 V /60Hz and $V_{dc} = 300\text{V}$, the measured efficiencies η, THD_i of i_{ac} and PF at ($R_L = 400\Omega$, P_{dc} =227.7W) and ($R_L = 200\Omega$, P_{dc} =473.6W) are summarized in Table 1. And the measured (i_L^*, i_L') and (v_{ac}, i_{ac}) under ($R_L = 200\Omega$, P_{dc} =473.6W) are shown in Figs. 9(a) and 9(b). The results indicate that the input current i_{ac} is nearly sinusoidal and kept almost in phase with the utility voltage v_{ac}. Good line drawn power quality can also be observed from Table 1.

Load cases / Variables	Resistive load ($R_L = 400\Omega$)	Resistive load ($R_L = 200\Omega$)
V_{ac}	110V/60Hz	110V/60Hz
P_{ac}	241.6W	502.2W
V_{dc}	300.8V	300.2V
P_{dc}	227.7W	473.6W
η	94.25%	94.31%
THD_i	6.61%	6.11%
PF (Lagging)	0.992	0.994

Table 1. Measured steady-state characteristics of the standard boost SMR under two loads

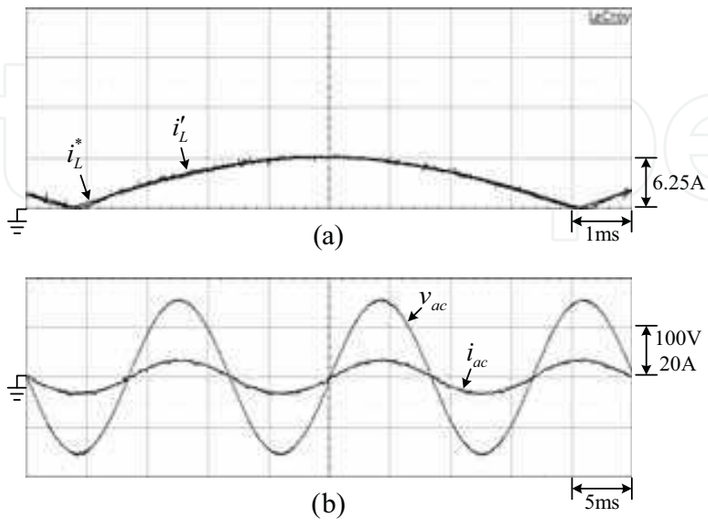

Fig. 9. Measured results of the standard boost SMR at $R_L = 200\Omega$: (a) (i_L^*, i_L'); (b) (v_{ac}, i_{ac})

5.2 Bridgeless boost SMR

5.2.1 System configuration

Fig. 10 shows the bridgeless boost SMR, its control scheme is identical to those shown in Fig. 6 with the two switches being respectively operated in positive and negative half cycles. Although the efficiency of bridgeless SMR can be slightly increased, it possesses the common mode EMI problem due to the large parasitic capacitance between the output and ground, which provides a relatively low impedance path. To reduce this problem, the boosting inductor is divided into two equal inductors, and they are placed at AC source side.

5.2.2 Circuit design

The specifications are identical to those listed above. The two inductors L_1 and L_2 in Sec. 5.1.2 are used here as the two bridgeless boost SMR inductors, i.e., $L_1 = L_2 = 0.5L$.

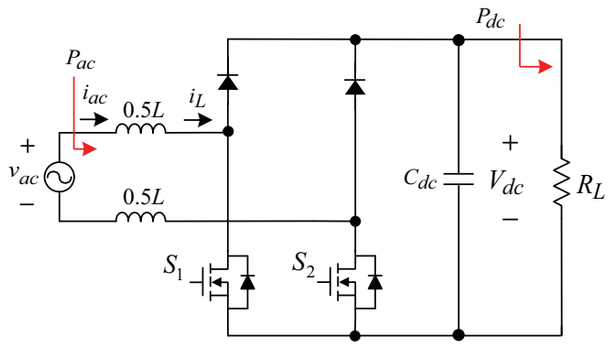

Fig. 10. Schematic and control scheme of the developed bridgeless boost SMR

5.2.3 Control schemes

Current controller: Following the similar process introduced in Sec. 5.1.3 one can get $K_{Pi} < \overline{K}_{Pi} = 8.625$. Hence, $K_{Pi} = 3.0$ is set and the integral gain is chosen via trial-and-error. Finally:

$$G_{ci}(s) = K_{Pi} + \frac{K_{Ii}}{s} = 3 + \frac{2000}{s} \tag{20}$$

Voltage controller: The PI voltage feedback controller is chosen to be:

$$G_{cv}(s) = K_{Pv} + \frac{K_{Iv}}{s} = 8 + \frac{200}{s} \tag{21}$$

5.2.4 Experimental results

The measured key waveforms are almost identical to Fig. 9 and are not repeated here. Table 2 lists the measured efficiencies η , THD_i of i_{ac} and PF at two loads. From Tables 1 and 2 one can find the slight higher efficiencies being yielded by the bridgeless SMR.

5.3 Current-Fed Push-Pull (CFPP) isolated boost SMR

5.3.1 System configuration and operation

The power circuit and control scheme of the CFPP isolated boost SMR are shown in Figs. 11(a) and 11(b). In making the analysis, some assumptions are made: (i) all circuit

components are ideal; (ii) the active voltage clamp circuits including S_3, S_4 and C_a are neglected; (iii) $v_{in} = |v_{ac}| = V_m \sin \omega t = \sqrt{2} V_{ac} \sin \omega t$; (iv) the circuit is operated under CCM. In the established current-fed push-pull SMR, the duty ratio $D \triangleq t_{on} / T_s$ $(0.5 < D < 1)$ is set. The gate signal of S_2 is generated from S_1 by shifting 180°. Detailed analysis process can be referred to (Hsieh, 2010), only a brief description and some key formulas are given here. During analysis, the voltage transfer ratio from v_{in} to V_{dc} can be derived as:

$$\frac{V_{dc}}{v_{in}} = \frac{N_s}{N_p} \frac{1}{2(1-D)} \tag{22}$$

It should be noted that the duty ratio D is a time varying function for the constant V_{dc} and time varying input DC voltage $v_{in} = |v_{ac}|$. Moreover, the variations of V_{dc} and V_{ac} should be considered in making the derivation of component ratings.

Load Cases / Variables	Resistive load ($R_L = 400\Omega$)	Resistive load ($R_L = 200\Omega$)
V_{ac}	110V/60Hz	110V/60Hz
P_{ac}	233.1W	497.5W
V_{dc}	300.6V	300.2V
P_{dc}	223.5W	475.9W
η	95.88%	95.66%
THD_i	6.02%	6.11%
PF (Lagging)	0.996	0.996

Table 2. Measured characteristics of the developed bridgeless boost SMR under two loads

5.3.2 Circuit design

a. Specifications

The system variables and specifications of the established SMR are given as follows:

AC input voltage: $V_{ac} = 110\text{V} \pm 10\% / 60\text{Hz}$.

DC output: $V_{dc} = 300\text{V} \sim 350\text{V}$ $(\geq 110\text{V} \times 1.1 \times \sqrt{2} = 171\text{V})$, $P_{dc} = 1200\text{W}$.

Switching frequency: $f_s = 25\text{kHz}$, Efficiency: $\eta \geq 75\%$, $PF \geq 0.95$ (Lagging).

b. Boosting inductor

To provide magnetization path of the inductor, duty cycle must be greater than 0.5 at any time, and from (22):

$$n \triangleq \frac{N_s}{N_p} \leq \frac{300}{\sqrt{2} \times 110} \frac{2(1-0.5)}{1} \tag{23}$$

Thus the turn ratio can be found to be $n \leq 1.935$. By choosing $n = 1$, the instantaneous duty ratio at $\omega t = 0.5\pi$ can be found from (22) as:

$$D_{\max} = 1 - \frac{\hat{V}_{ac,\min}}{2V_{dc,\max}} = 1 - \frac{140}{2 \times 350} = 0.8 \tag{24}$$

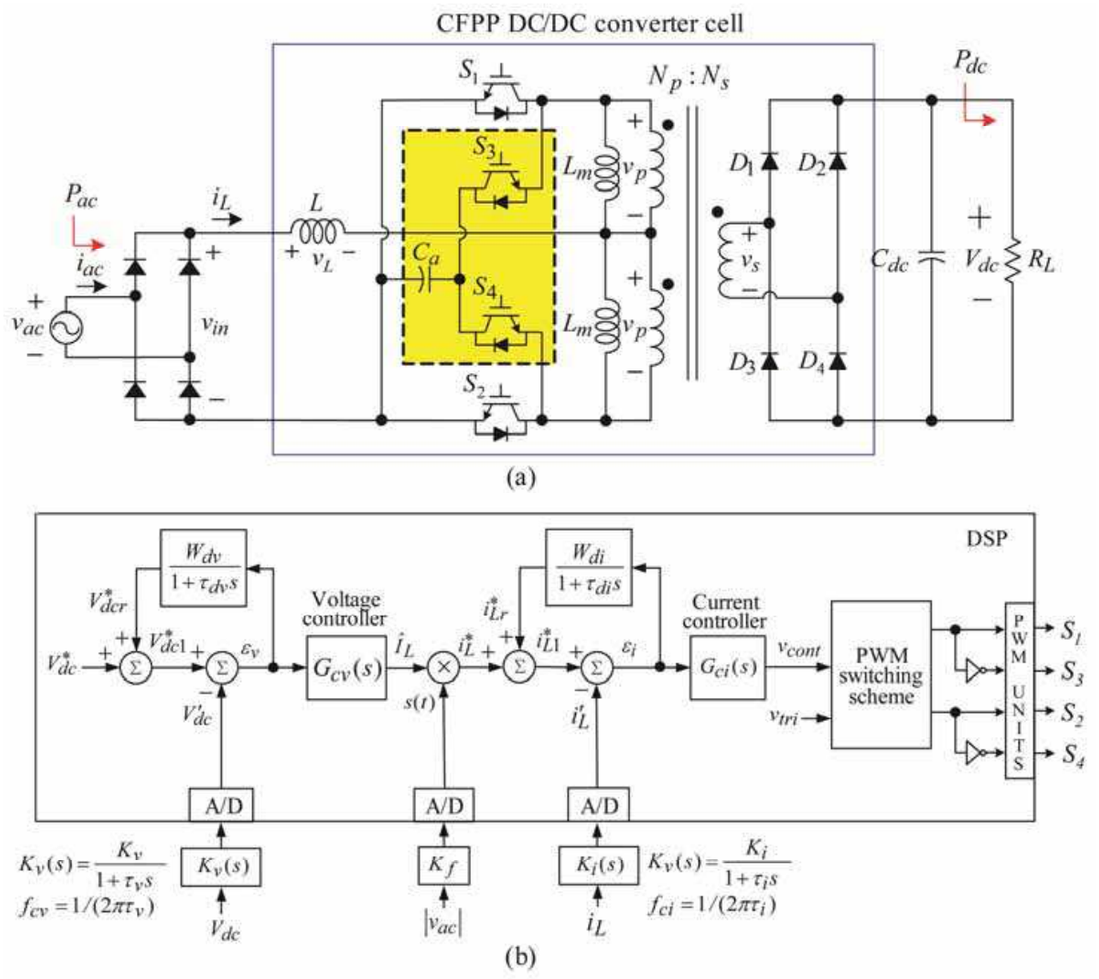

Fig. 11. The current-fed push-pull isolated boost SMR: (a) power circuit; (b) control scheme

The maximum inductor current occurred at $\omega t = 0.5\pi$ can be calculated as:

$$(\hat{i}_L)_{\max} = \frac{P_{dc}}{\hat{V}_{ac,\min}\eta} \times 2 = \frac{1200}{110 \times \sqrt{2} \times 0.9 \times 0.75} \times 2 = 22.856\text{A} \tag{25}$$

Let the inductor current ripple be:

$$\Delta i_L = \frac{\hat{V}_{ac,\min}(D-0.5)T_s}{L} \le 0.1(\hat{i}_L)_{\max} = 2.2856\text{A} \tag{26}$$

The condition of boosting inductance L is obtained as:

$$L \ge \frac{\hat{V}_{ac,\min}(D-0.5)}{f_s \Delta i_L} = 0.735\text{mH} \tag{27}$$

The inductances of an available inductor measured using HIOKI 3532-50 LCR meter are $L =$ (2.03mH, ESR = 210mΩ at 120Hz) and (1.978mH, ESR = 5.68Ω at 25kHz). Hence this

inductor is suited and employed here. Using the inductance of $L = 1.978\text{mH}$ at $f = 25\text{kHz}$, the inductor current ripple given in (26) becomes $\Delta i_L = 0.85\text{A}$.

c. Output capacitor

The output filtering capacitor $C_d = 2200\mu\text{F}/450\text{V}$ is chosen to yield the following peak-to-peak voltage ripple:

$$\Delta V_{dc} = \frac{V_{dc}}{\omega_1 R_L C_d} = \frac{P_{dc}}{\omega_1 C_d V_{dc}} = \frac{1200}{2\pi \times 60 \times 2200 \times 10^{-6} \times 350} = 4.13\text{V} \tag{28}$$

d. Power semiconductor devices

From (25) and (26), the maximum current flowing through the switches and all the diodes can be calculated as $i_{S,\max} = (\hat{i}_L)_{\max} + 0.5\Delta i_L = 22.856 + 0.5 \times 0.85 = 23.28\text{A}$. The maximum voltage for the switches is 700V which is found from Fig. 11, and voltage rating for the load side rectifier diodes is 350V. Accordingly, the IGBT K40T120 (Infineon) (1200V, ID= 40A ($100°\text{C}$, continuous), IDM = 105A (pulsed)) and the fast diode DSEP60-06A (IXYS) (600V, average current IFAVM = 60A) are chosen for implementing the switches and all the diodes, respectively.

e. Transformer design

The AMCU series UU core AMCU-80 manufactured by AMOSENSE Cooperation is used to wind the push-pull transformer here. The designed results (Hsieh, 2010) are summarized as followed. To lower the core loss, B = 0.25T is set, and thus the maximum flux density variation will be $\Delta B = 2 \times 0.25\text{T} = 0.5\text{T}$. From Faraday's law, the turns of the primary side can be expressed as follows:

$$N_p = \frac{n \times V_{dc,\max}(1 - D_{\min})T_s}{A_e \times \Delta B} \tag{29}$$

The known parameters in (29) are: $n = 1$, $V_{dc,\max}$ =350V, $D_{\min} = 0.5$, $A_e = 5.21\text{cm}^2$, $T_s = 40\mu\text{s}$. Hence $N_p = 26.87$ is found, and $N_p = N_s = 32$ are chosen here. The measured parameters of the designed transformer at $f = 25\text{kHz}$ using HIOKI 3532-50 LCR meter are: $L_m = 1.086\text{mH}$, $L_{ls1} = 10.795\mu\text{H}$, $L_{ls2} = 8.838\mu\text{H}$, $\text{ESR} = 20.4\Omega$, where L_{ls1} and L_{ls2} denote the leakage inductances of the two transformer primary windings.

f. Active voltage clamp

As generally known that a current-fed push-pull boost converter may possess serious problems due to the voltage spikes caused by transformer leakage inductances, the problems lie in having lower efficiency and increased voltage stress of power switches. The active voltage clamp circuit (Kwon, 2008; Sangwon & Sewan, 2010) is used to solve this problem. As shown in Fig. 11(a), the active voltage clamp circuit consists of two auxiliary switches (S_3, S_4) and one capacitor C_a. These two auxiliary switches are switched in complement fashion to the two main switches (S_1, S_2) but with a small dead-time. The used components for active voltage clamp circuit are: $C_a = 0.4\mu\text{F}/1000\text{V}$, S_3 and S_4 are IGBT K40T120 (Infineon) (1200V, ID= 40A ($100°\text{C}$, continuous), IDM = 105A (pulsed)), the dead-time $t_d = 1\mu\text{s}$ is set here.

5.3.3 Controller design of CFPP Isolated boost SMR

a. Current controller

Similarly, the upper value of K_{Pi} can be found from (17) to be $K_{Pi} < \overline{K}_{Pi} = 1.53$ (V_{dc} is replaced by v_p and $v_{ac} = 0$ is set). Accordingly $K_{Pi} = 0.5$ is set. Then the integral gain is chosen via trial-and-error, and finally it is found that:

$$G_{ci}(s) = K_{Pi} + \frac{K_{Ii}}{s} = 0.5 + \frac{2500}{s} \tag{30}$$

The robust current tracking error cancellation controller shown in Fig.11(b) is not applied here.

b. Voltage controller

The voltage loop dynamic model and the proposed feedback control scheme are shown in Fig. 12, the SMR is reasonably represented by a first-order process in main dynamic frequency range. The voltage feedback sensing factor is set as $K_v = 0.002\text{V/V}$. The desired voltage response due to a step load power change is also sketched in Fig. 12, which possesses the key features: (i) no overshoot and steady-state error; (ii) the typical key response points indicated in Fig. 12 are: ($t_1 = t_f$, $\Delta V_{dc1} = 0.5\Delta v_{om}$), ($t_2 = t_m$, $\Delta V_{dc2} = \Delta v_{om}$), ($t_3 = t_{re}$, $\Delta V_{dc3} = 0.1\Delta v_{om}$), with t_f = fall time, t_m = the time at which maximum dip being occurred, t_{re} = restore time, Δv_{om} = maximum voltage dip.
For the ease of implementation, the PI voltage feedback controller is chosen:

$$G_{cv}(s) = \frac{K_{Pv}s + K_{Iv}}{s} \tag{31}$$

The quantitative design technique presented in (Y.C. Chang & Liaw, 2009a) is applied to here to find the parameters of $G_{cv}(s)$ to have the desired regulation response shown in Fig. 12. The details are neglected and only a brief description is given here.

a. Dynamic model estimation

i. Let the $G_{cv}(s) = K_{Pv} + K_{Iv}/s = 6 + 10.5/s$ be arbitrary set, and the SMR is normally operated at the chosen operating point ($V_{dc}^* = 300\text{V}$, $P_{dc} = 302.8\text{W}$).

ii. A step load resistor change of $R_L = 300\Omega \rightarrow 200\Omega$ ($\Delta P_{dc} = 149.3\text{W}$, $P_{dc} = 302.8\text{W} \rightarrow 452.1\text{W}$) is applied and the response of V_{dc} is recorded. By choosing three typical response points as indicated in Fig. 12 to be (-4.4V, 27.5ms), (-7.6V, 55ms) and (-1V, 1500ms), through careful derivation (Y.C. Chang & Liaw, 2009a), one can obtain the estimated dynamic model parameters are obtained:

$$a = 7.95,\ b = 2975.71,\ K_{pl} = 0.00084542 \tag{32}$$

b. Controller design

At the given operating point ($V_{dc} = 300\text{V}$, $R_L = 300\Omega$), the voltage regulation control specifications are defined as: $\Delta V_{dc,\max} = 5.0\text{V}$, $t_{re} = 800\text{ms}$ for a step load power change of $\Delta P_{dc} = 149.3\text{W}$. Following the quantitative design process presented in (Y.C. Chang & Liaw, 2009a) one can solve to obtain:

$$G_{cv}(s) = K_{Pv} + \frac{K_{Iv}}{s} = 10.0036 + \frac{33.8878}{s} \tag{33}$$

The simulated and measured output voltage responses (not shown here) are confirmed their closeness and satisfying the specified control specifications.

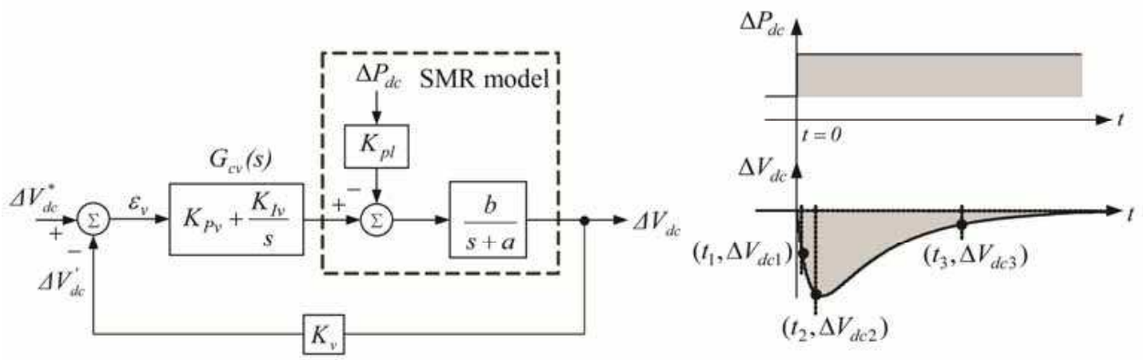

Fig. 12. The established current-fed push-pull boost SMR control scheme and the desired regulation response

c. Robust voltage error cancellation controller

A simple robust voltage error cancellation controller (RVECC) presented in (Chai & Liaw, 2007) is applied here to enhance the SMR voltage regulation control robustness. In the control system shown in Fig. 11(b), a robust compensation control command V_{dcr}^* is generated from the voltage error ε_v through a weighting function $W_d(s) = W_d / (1 + \tau_d s)$ with W_d being a weighting factor. The low pass filter process with cut-off frequency $f_{cd} = 1/(2\pi\tau_d) = 120\text{Hz}$ ($\tau_d = 0.0013263$) is used to reduce the effects of high-frequency noises on dynamic control behavior.

From Fig. 11(b) one can derive that the original voltage tracking error $\varepsilon_v = V_{dc}^* - V_{dc}'$ will be reduced to

$$V_{dc}^* - V_{dc}^{'} = (1 - \frac{W_d}{1 + \tau_d s})\varepsilon_v \approx (1 - W_d)\varepsilon_v \ , \ 0 \le W_d < 1 \tag{34}$$

where the approximation is made for the main dynamic signals. Hence the original voltage error can be reduced by a factor of $(1 - W_d)$ within main dynamic frequency range. The selection of W_d must be made considering the compromise between control performance and effects of system noises.

Figs. 13(a) and 13(b) show the simulated and measured output voltage responses by PI control without ($W_d = 0$) and with ($W_d = 0.5$) robust control due to a step load power change of $\Delta P_{dc} = 149.3\text{W}$ ($P_{dc} = 302.8\text{W} \rightarrow 452.1\text{W}$, $V_{dc}^* = 300\text{V}$). The results show that they are very close and the effectiveness of robust control in the improvement of voltage regulation response.

Let V_{ac} =110V/60Hz and V_{dc}^* =300V, and the PI feedback and robust controls are all operated, the measured steady-state characteristics at ($R_L = 400\Omega$, P_{dc} = 234.6W), ($R_L = 200\Omega$, P_{dc} = 465.8W), ($R_L = 133\Omega$, P_{dc} = 623.8W) and ($R_L = 100\Omega$, P_{dc} = 908.5W) are

summarized in Table 3. And the measured (i_L^*, i_L) and (v_{ac}, i_{ac}) under ($R_L = 100\Omega$, P_{dc} = 908.5W) are shown in Figs.14(a) and 14(b), respectively. From the results, one can find that the developed SMR possesses good power quality control performances under wide load range. The lower efficiencies compared with the previous two types of SMRs are observed, this is mainly due to the addition of isolated HF transformer.

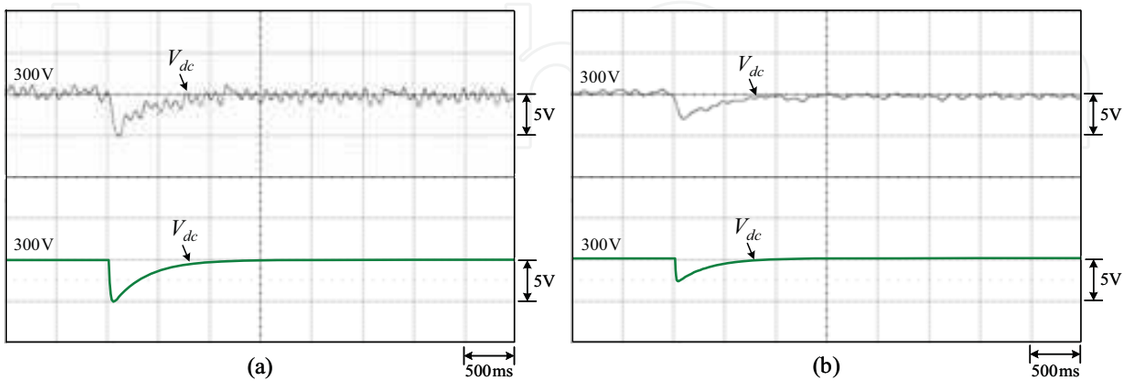

Fig. 13. Measured (upper) and simulated (lower) V_{dc} by PI control without ($W_d = 0$) and with ($W_d \neq 0$) robust control due to a step load power change of $\Delta P_{dc} = 149.3$W ($P_{dc} = 302.8\text{W} \rightarrow 452.1\text{W}$, $V_{dc}^* = 300\text{V}$): (a) $W_d = 0$; (b) $W_d = 0.5$

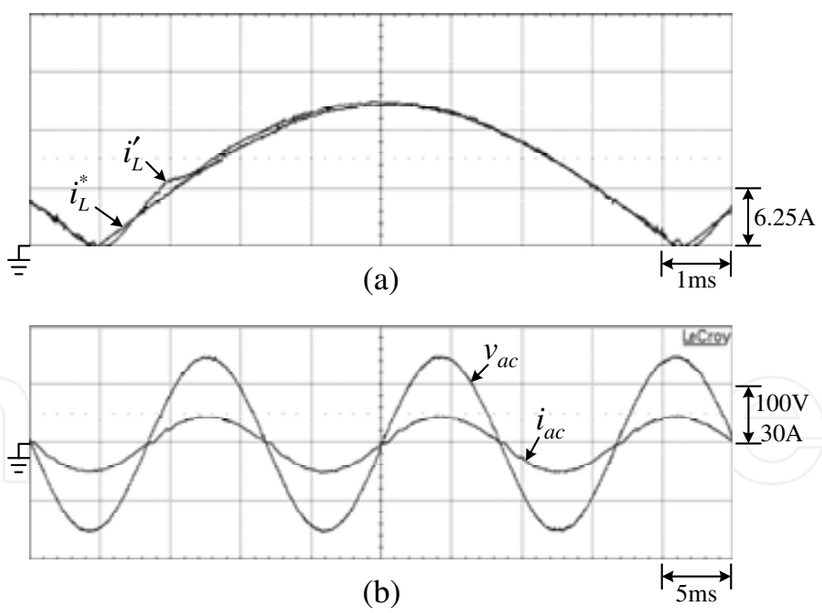

Fig. 14. Measured steady-state results of the current-fed push-pull boost SMR at $V_{ac} = 110\text{V}/60\text{Hz}$ and $R_L = 100\Omega$: (a) (i_L^*, i_L'); (b) (v_{ac}, i_{ac})

5.4 Evaluation for the PMSM drive with different front-end AC/DC converters

Figs. 15(a) to 15(d) show the standard PMSM drives equipped with different front-end AC/DC converters. In making experimental works, the following inputs are set: (i) Diode

rectifier: $V_{ac} = 220\text{V}/60\text{Hz}$, V_{dc} will vary with loading conditions; (ii) SMRs: $V_{ac} = 110\text{V}/60\text{Hz}$, $V_{dc} = 300\text{V}$ with satisfactory regulation control, the switching frequency $f_s = 25\text{kHz}$ is set. The measured results are summarized as follows:

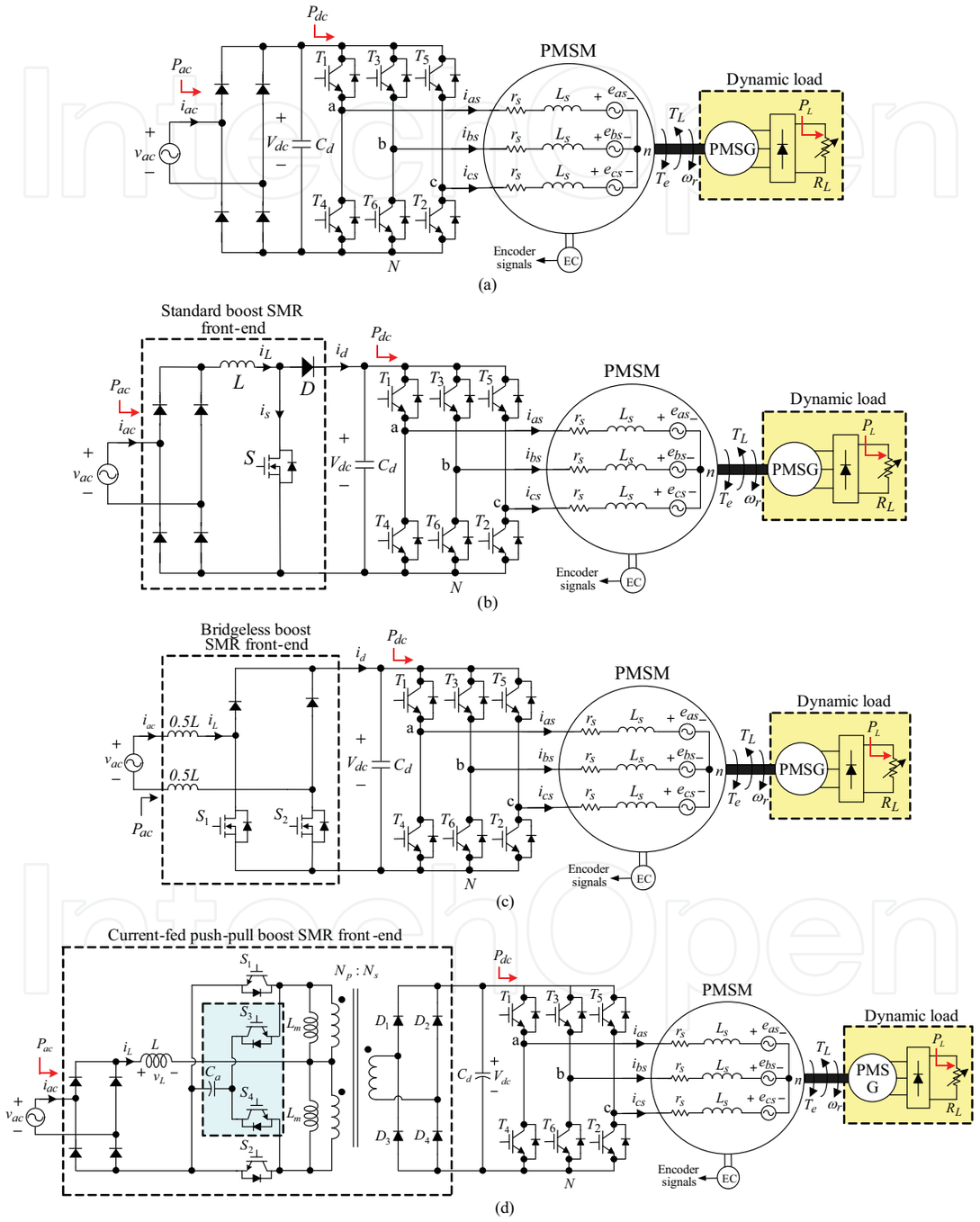

Fig. 15. The circuit configuration of established standard PMSM drive with SMR front-end: (a) diode rectifier front-end; (b) standard boost SMR front-end; (c) bridgeless boost SMR front-end; (d) current-fed push-pull boost SMR front-end

Load Cases / Variables	Resistive load ($R_L = 400\Omega$)	Resistive load ($R_L = 200\Omega$)	Resistive load ($R_L = 133\Omega$)	Resistive load ($R_L = 100\Omega$)
V_{ac}	110V/60Hz	110V/60Hz	110V/60Hz	110V/60Hz
P_{ac}	298.6W	557.4W	697.4W	1082.2W
V_{dc}	301.2V	300.8V	300.5V	300.3V
P_{dc}	234.6W	465.8W	623.8W	908.5W
η	78.57%	83.57%	89.45%	83.95%
THD_i	8.83%	6.62%	6.53%	3.82%
PF (Lagging)	0.997	0.998	0.998	0.998

Table 3. Measured characteristics of the current-fed push-pull boost SMR under four loads

5.4.1 Diode rectifier front-end

The measured (ω_r^* , ω_r), (H_A , i_{as}^* , i'_{as}) and (v_{ac} , i_{ac}) at ($\omega_r^* = 2000$rpm , $R_L = 44.7\Omega$) and ($\omega_r^* = 3000$rpm , $R_L = 44.7\Omega$) are shown in Fig. 16(a) and Fig. 16(b), and the corresponding steady-state characteristics are listed in Table 4. One can notice the normal operation of the PMSM drive under $\omega_r^* = 2000$rpm . However, the results in Fig. 16(b) indicate that large tracking errors exist in speed and phase current under $\omega_r^* = 3000$rpm . This is mainly due to the insufficient DC-link voltage ($V_{dc} = 278.4$V) established by rectifier for encountering the back-EMF effect. In addition, the peaky i_{ac} leads to poor power factor and high THD_i .

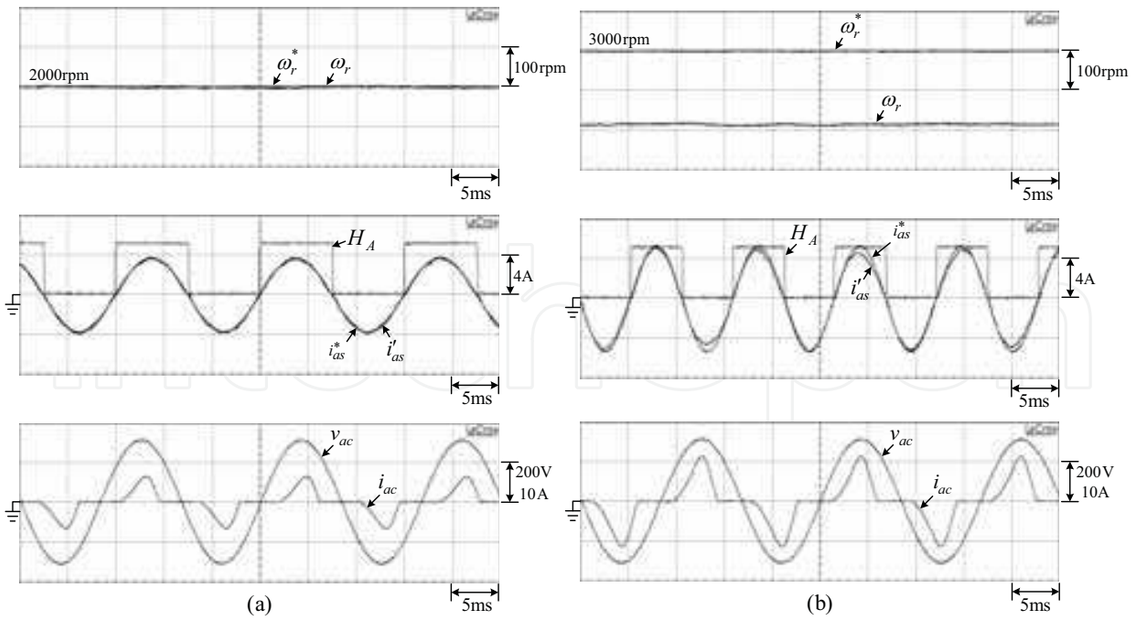

Fig. 16. Measured (ω_r^* , ω_r),(H_A , i_{as}^* , i'_{as}) and (v_{ac} , i_{ac}) of the standard PMSM drive with diode rectifier front-end at: (a) ($V_{ac} = 220$V/60Hz , $\omega_r^* = 2000$rpm , $R_L = 44.7\Omega$);
(b): ($V_{ac} = 220$V/60Hz , $\omega_r^* = 3000$rpm , $R_L = 44.7\Omega$)

Variables \ Cases	$\omega_r^* = 2000$rpm	$\omega_r^* = 3000$rpm
V_{ac}	220V/60Hz	220V/60Hz
P_{ac}	527.5W	969.4W
V_{dc}	295.9V	278.4V
P_{dc}	366.7W	706.3W
η	69.52%	72.86%
THD_i	72.95%	65.54%
PF (Lagging)	0.751	0.758

Table 4. Measured characteristics of the standard PMSM drive fed by diode rectifier front-end under two speeds ($V_{ac} = 220\text{V}/60\text{Hz}$, $R_L = 44.7\Omega$)

5.4.2 Three boost SMR front-ends

(i) Standard boost SMR: Fig. 17(a), Fig. 17(b) and Table 5; (ii) Bridgeless boost SMR: Fig. 18(a), Fig. 18(b) and Table 6; (iii) CFPP boost SMR: Fig. 19(a), Fig. 19(b) and Table 7. The results indicate that for all cases, the close winding current tracking performances are obtained, and thus good line drawn power quality characteristics are achieved.

Further observations find that: (i) the efficiencies of bridgeless SMR are slightly higher than those of standard boost SMR; (ii) the efficiencies of the CFPP SMR are lower than the other two SMRs. This is mainly due to the increased losses in the high-frequency transformer.

Fig. 20(a) and Fig. 20(b) show the measured (ω_r^* , ω_r), (i_{qs}^* , i'_{qs}) and V_{dc} of the whole PMSM drive with CFPP boost SMR front-end at ($V_{dc} = 300\text{V}$, $\omega_r = 2400$rpm, $R_L = 44.7\Omega$) due to a step speed command change of 100rpm and due to a step load resistance change from $R_L = 75\Omega$ to $R_L = 44.7\Omega$. The results indicate that good speed tracking and regulating responses are obtained by the developed SMR-fed PMSM drive. And the DC-link voltages V_{dc} are well regulated under these two cases.

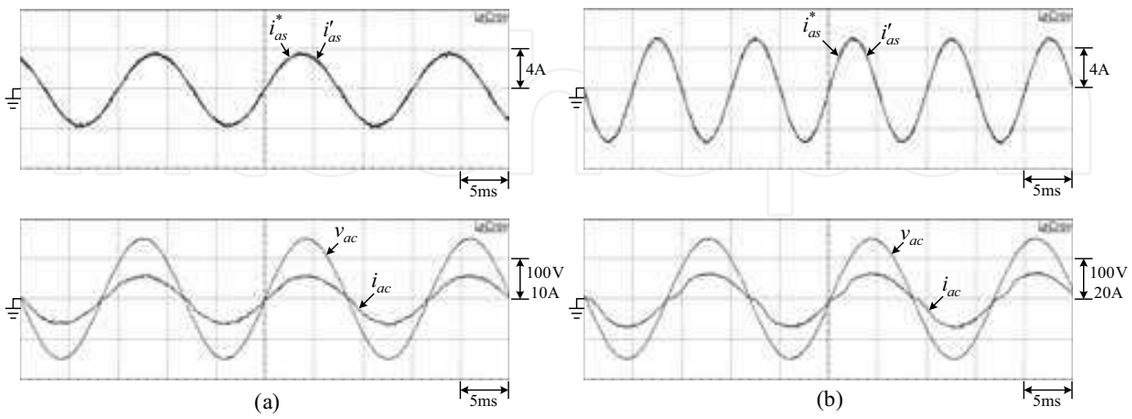

Fig. 17. Measured (ω_r^* , ω_r), (H_A , i_{as}^* , i'_{as}) and (v_{ac} , i_{ac}) of the standard PMSM drive with standard boost SMR front-end at: (a) ($V_{ac} = 220\text{V}/60\text{Hz}$, $\omega_r^* = 2000$rpm , $R_L = 44.7\Omega$); (b): ($V_{ac} = 220\text{V}/60\text{Hz}$, $\omega_r^* = 3000$rpm , $R_L = 44.7\Omega$)

Variables \ Cases	$\omega_r^* = 2000$rpm	$\omega_r^* = 3000$rpm
V_{ac}	110V/60Hz	110V/60Hz
P_{ac}	546.5W	1145.3W
V_{dc}	300.6V	300.3V
P_{dc}	365.9W	791.2W
η	66.95%	69.08%
THD_i	8.493%	7.085%
PF (Lagging)	0.998	0.997

Table 5. Measured characteristics of the standard PMSM drive fed by standard boost SMR front-end under two speeds ($V_{dc} = 300$V , $R_L = 44.7\Omega$)

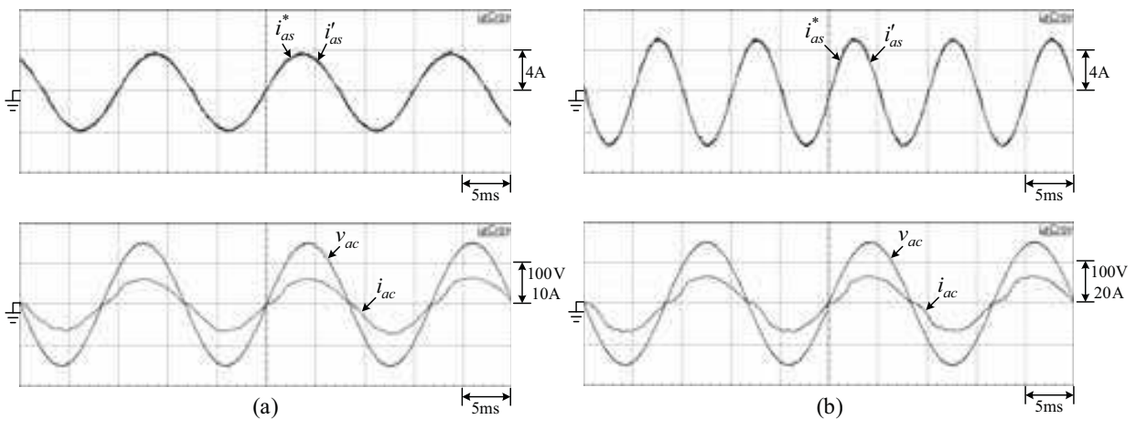

Fig. 18. Measured (ω_r^* , ω_r), (H_A , i_{as}^* , i'_{as}) and (v_{ac} , i_{ac}) of the standard PMSM drive with bridgeless boost SMR front-end at: (a) ($V_{ac} = 220$V/60Hz , $\omega_r^* = 2000$rpm , $R_L = 44.7\Omega$); (b): ($V_{ac} = 220$V/60Hz , $\omega_r^* = 3000$rpm , $R_L = 44.7\Omega$)

Variables \ Cases	$\omega_r^* = 2000$rpm	$\omega_r^* = 3000$rpm
V_{ac}	110V/60Hz	110V/60Hz
P_{ac}	543.9W	1142.4W
V_{dc}	300.4V	300.1V
P_{dc}	364.8W	790.3W
η	67.07%	69.18%
THD_i	8.238%	7.022%
PF (Lagging)	0.998	0.996

Table 6. Measured characteristics of the standard PMSM drive fed by bridgeless boost SMR front-end under two speeds ($V_{dc} = 300$V , $R_L = 44.7\Omega$)

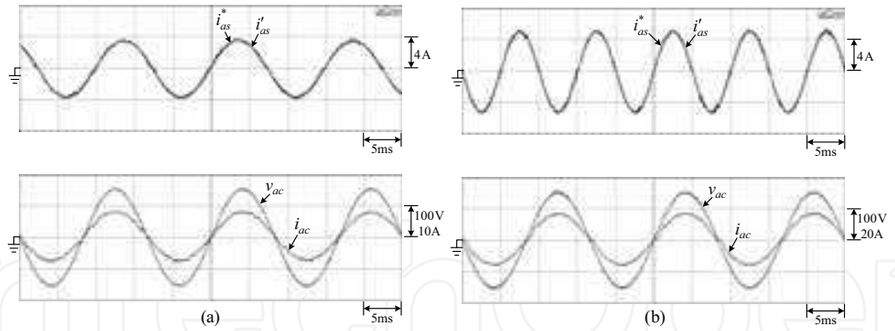

Fig. 19. Measured (ω_r^* , ω_r), (H_A , i_{as}^* , i'_{as}) and (v_{ac} , i_{ac}) of the standard PMSM drive with current-fed push-pull SMR front-end at: (a) ($V_{ac} = 220\text{V}/60\text{Hz}$, $\omega_r^* = 2000\text{rpm}$, $R_L = 44.7\Omega$); (b): ($V_{ac} = 220\text{V}/60\text{Hz}$, $\omega_r^* = 3000\text{rpm}$, $R_L = 44.7\Omega$)

Variables \ Cases	$\omega_r^* = 2000\text{rpm}$	$\omega_r^* = 3000\text{rpm}$
V_{ac}	110V/60Hz	110V/60Hz
P_{ac}	597.8W	1231.8W
V_{dc}	301.2V	300.7V
P_{dc}	365.3W	792.1W
η	61.10%	64.30%
THD_i	3.90%	4.02%
PF (Lagging)	0.998	0.998

Table 7. Measured characteristics of the standard PMSM drive fed by current-fed push-pull boost SMR front-end under two speeds ($V_{dc} = 300\text{V}$, $R_L = 44.7\Omega$)

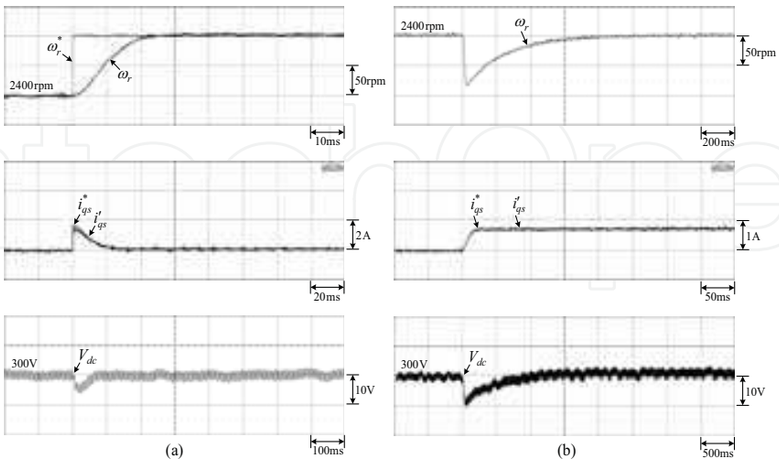

Fig. 20. Measured (ω_r^* , ω_r), (i_{qs}^* , i'_{qs}) and V_{dc} of the whole PMSM drive with current-fed push-pull boost SMR front-end at ($V_{dc} = 300\text{V}$, $\omega_r^* = 2400\text{rpm}$, $R_L = 44.7\Omega$): (a) due to a step speed command change of 100rpm: (b) due to a step resistive load change from $R_L = 75\Omega$ to $R_L = 44.7\Omega$

6. Some specific applications of Switch-Mode Rectifier

The applications of three types of single-phase SMRs as the AC-DC front-end converters of PMSM drives and their comparative evaluation have been introduced in the previous section. In this section, a SMR fed switched-reluctance motor (SRM), a SMR based electric vehicle battery charger and a flyback SMR based battery plug-in charger are presented to further comprehend the advantages of using SMR.

6.1 Switch-Mode Rectifier fed Switched-Reluctance Motor drive

6.1.1 System configuration

Fig. 21 shows the power circuit and control scheme of a three-phase single-switch (3P1SW) fed SRM drive (Chai et al, 2010). The two power stages possess the following key features:

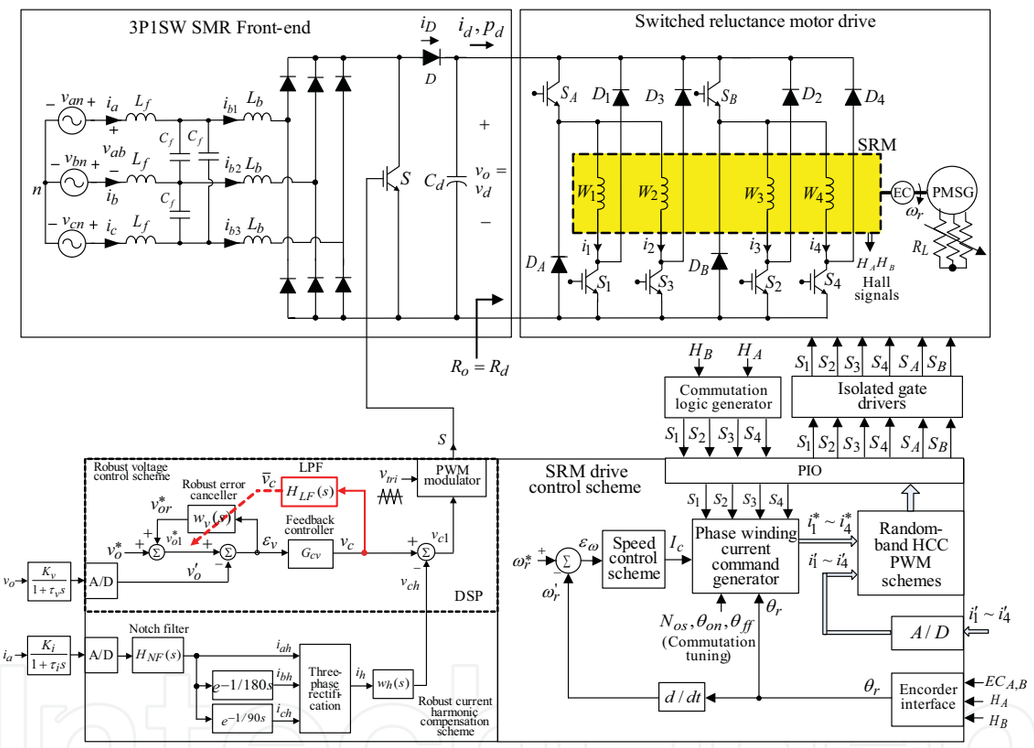

Fig. 21. A three-phase single-switch SMR fed drive and its control scheme

a. SRM drive: The SRM drive is manufactured by TASC Drives Ltd., which is rated as 4-phase, 8/6 pole, 400V, 1500rpm, 4kW. Its windings are excited by a 2(n+1) Miller's converter from the SMR established DC-link voltage. The lower switches S_1 to S_4 are in charge of commutation, and the upper switches S_A (phase windings 1 and 3) and S_B (phase windings 2 and 4) are used for performing PWM switching control.

b. 3P1SW SMR: The ratings of the 3P1SW SMR are: (1) AC input: three-phase, $V_L = 220 \pm 10\%\, V_{rms}$, 60Hz; (2) DC output: $V_o = V_d = 400\text{V}$, $P_o = 4kW$ $(R_o = 40\Omega)$. The energy storage inductor is $L_b = 15.459\mu H(10kHz)$. The output filtering capacitor is $C_o = 2000\mu F / 500V$ with the corresponding peak-to-peak DC output voltage ripple: $\Delta v_o = 2V_o / (105\omega R_o C_o) = 0.253V$. Input filter: $C_f = 3.3\mu\text{F}$ and $L_f =$ $123.679\mu H$.

6.1.2 SMR control scheme

The SMR control scheme shown in Fig. 21 consists of a robust current harmonic cancellation scheme and a robust voltage control scheme. The undesired line current and output voltage ripples are regarded as disturbances and they are reduced via robust controls. Owing to the boostable and regulated DC-link voltage provided by the SMR, the dynamic responses of the followed SRM drive are enhanced, and its vibration and speed ripple are also reduced.

a. Robust current harmonic compensation scheme: The three-phase total current harmonic current i_h is synthesized from the sensed phase-a line current i_a. Then an injected PWM robust compensating control voltage $v_{ch} = w_h(s)i_h$ is yielded, where $w_h(s)$ denotes a robust harmonic compensation weighting function.
b. Robust voltage control scheme: A compensation control command $v_{or}^* = w_v(s)\varepsilon_v$ is generated from the tracking error ε_v. The weighting factor in the weighting function $w_v(s)$ is updated according to load level, which is identified from the low-pass filtered control voltage $\overline{v}_c = H_{LF}(s)v_c$. The chaotic phenomena can be avoided automatically, better SMR control performance and voltage response are obtained simultaneously.

6.1.3 Performance evaluation

The SMR fed SRM drive is shown in Fig. 21. At the operation condition of ($V_d = 400V$, $\omega_r = 1500$rpm, $R_L = 13.2\Omega$, $P_d = 2135W$), the measured DC-link voltages $v_d(t)$ and vibrations $a(t)$ using different AC/DC front-end converters are compared in Figs. 22(a) and 22(b). The results show that the DC-link voltage ripple and the stator vibration using conventional rectifier as a front-end (measured line power quality parameters are $PF = 0.631$, $THD_i = 134\%$) are slightly reduced by employing the three-phase SMR ($W_h = 1$) with PI control only ($W_v = 0$)($PF = 0.953$, $THD_i = 18.82\%$). Larger performance improvement is achieved by applying the robust voltage control scheme with the weighting factor being automatically set to be $W_v = 0.989$. The results in Figs. 22(a) and 22(b) ($PF = 0.968$, $THD_i = 10.33\%$) indicate the further improvements both in DC-link voltage ripple and stator vibration.

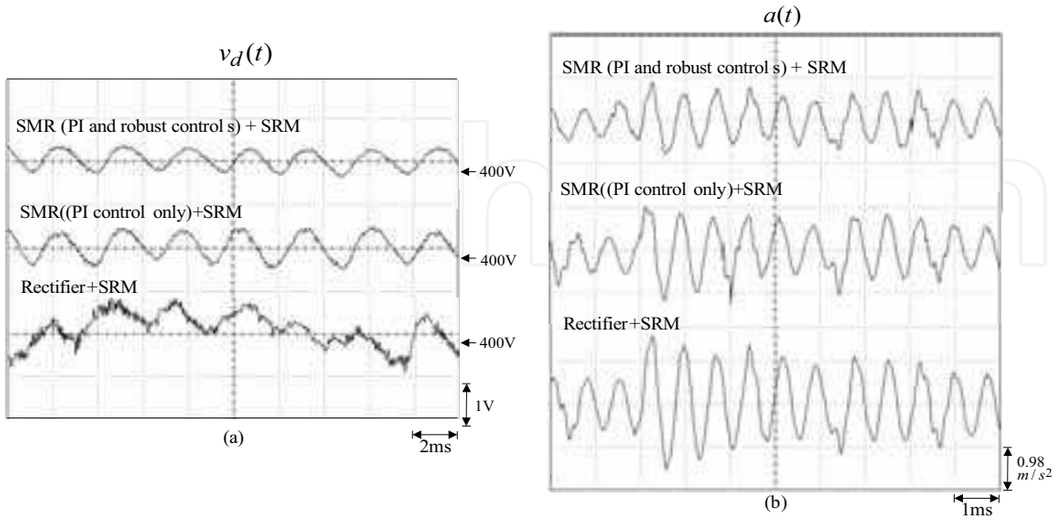

Fig. 22. Measured DC-link voltages $v_d(t)$ and vibrations $a(t)$ of the SRM drive fed by different AC/DC front-end converters at ($V_d = 400V$, $\omega_r = 1500rpm$, , $R_L = 13.2\Omega$, $P_d = 2135W$ (a) $v_d(t)$; (b) $a(t)$

At three cases of ($\omega_r = 1500rpm$, $R_L = 13.2\Omega$, $P_d = 2135W$), ($\omega_r = 1000rpm$, $R_L = 22\Omega$, $P_d = 1396W$) and ($\omega_r = 100rpm$, $R_L = 3.4\Omega$, $P_d = 807W$), and the SMR robust voltage control scheme and the SRM drive control schemes are normally operated, the measured power quality characteristics of the established SMR without ($W_h = 0$) and with ($W_h = 1.0$) current harmonic compensation are listed in Table 8.The results show that the fundamental and all other harmonic currents are all reduced and the efficiency of the SMR is increased accordingly by the harmonic compensation approach. Moreover, the line drawn power quality improvements at all cases are also obtained.

$P_d = 2.135kW$, $\omega_r = 1500rpm$, $R_L = 13.2\Omega$								
	PF	P_{ac} (kW)	$THDi$ (%)	I_{a1} (Arms)	I_{a5} (Arms)	I_{a7} (Arms)	I_{a11} (Arms)	Efficiency (%)
$W_h = 0$	0.953	2.414	18.82	5.18	0.81	0.55	0.08	88.44
$W_h = 1.0$	0.968	2.362	10.33	5.01	0.42	0.31	0.04	90.39
$P_d = 1.396kW$, $\omega_r = 1000rpm$, $R_L = 22\Omega$								
$W_h = 0$	0.941	1.598	19.13	3.58	0.62	0.29	0.05	87.36
$W_h = 1.0$	0.951	1.579	11.01	3.03	0.28	0.18	0.04	88.41
$P_d = 0.807kW$, $\omega_r = 100rpm$, $R_L = 3.4\Omega$								
$W_h = 0$	0.935	0.959	23.47	2.16	0.44	0.25	0.08	84.15
$W_h = 1.0$	0.943	0.932	19.54	1.91	0.33	0.17	0.06	86.59

Table 8. The measured power quality characteristics under SRM drive active load at various power levels without and with current harmonic compensation

6.2 Switch-Mode Rectifier based EV battery charger

6.2.1 System configuration

A battery powered SRM drive for electric vehicle propulsion is shown in Fig. 23(a) (H.C. Chang & Liaw, 2009). In driving mode, the switches are set as: $S_m \rightarrow$ M and $S_d \rightarrow$ closed. The SRM (DENSEI company Japan) is rated as 4-phase, 8-6, 48V, 6000rpm, 2.3kW. The components S_b, D_b, L_b and C_d in Fig. 23(a) form a DC/DC boost converter. The nominal battery voltage is $V_b = 12 \times 4 = 48\text{V}$, it is boosted and establishes the DC-link voltage with $48\text{V} \le V_{da} \le 72\text{V}$. During demagnetization of each communication stroke, the winding energies can be directly sent back to the battery bank via the diodes D_1, D_3, D_5 and D_7.

In charging mode, the switches in Fig. 23(a) are set as: $S_m \rightarrow$ C and S_d permanently off. With the insertion of off-board part, a buck-boost SMR based charger is formed and drawn in Fig. 23(b) with the employed embedded motor drive components being highlighted. The diode D_e is added to avoid the short circuit of battery when Q_6 is turned on. The inductances of the first two motor windings are used as the input filter components during each half AC cycle. And the third motor winding inductance is employed as the energy storage component of the SMR.

The SMR control scheme shown in Fig. 23(b) consists of outer charging control scheme and inner current controlled PWM scheme. Initially, the battery is charged in constant current

mode to let the batteries be charged under maximum current (0.25C/9.5A) until the condition of $V_b \geq 52\text{V}\ (=13\text{V}\times 4)$ reaches. Then the charging enters constant voltage floating mode.

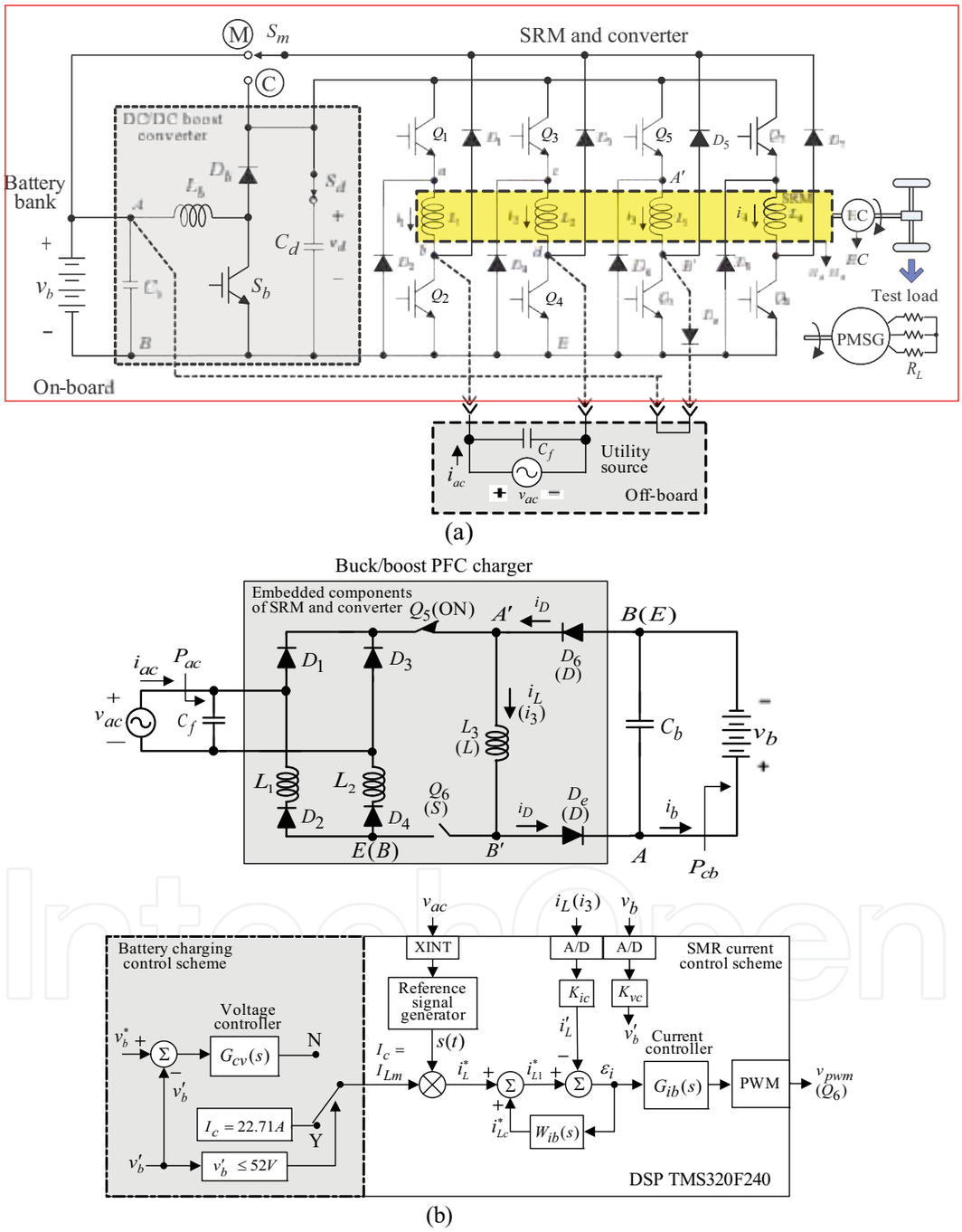

Fig. 23. A battery powered SRM drive with voltage boosting for electric vehicle propulsion: (a) system configuration; (b) schematic and control scheme of the formed on-board buck-boost SMR based battery charger in idle status

6.2.2 Performance evaluation

The derivation of circuit component ratings and the implementation affairs of the SRM drive shown in Fig. 23(a) and Fig. 23(b) can be referred to (H.C. Chang & Liaw, 2009). Some results concerning charging mode are observed here. Under the constant current charging mode with $I_{Lm} = I_c = 21.3\text{A}$ and switching frequency $f_s = 12.5kHz$, the measured i_L and its command i_L^* by PI control and robust control (W_{ib} = 0.85) are shown in Fig. 24(a) ($v_b = 47.65\text{V}$, $I_b = 9.45\text{A}$). The close inductor current tracking control is observed from the results. Fig. 24(b) shows the corresponding AC source voltage v_{ac} and current i_{ac} (PF = 0.989, THD_i = 4.23 %). Good line drawn waveform and power quality by the buck-boost SMR charger can be seen from the results.

To observe the effects of switching frequency on the SMR control performance, Table 9 lists measured performance parameters corresponding to the switching frequencies of $f_s = 12.5kHz$, $15kHz$, $7.5kHz$ and $2.5kHz$ ($W_{ib} = 0.85$). Some facts are observed from the results: (i) The current loop is normally operated at each switching frequency; and (ii) As the switching frequency becomes smaller, the inductor current will gradually become partial and then total discontinuous current mode (DCM) within the AC cycle. Accordingly, the power quality becomes worse.

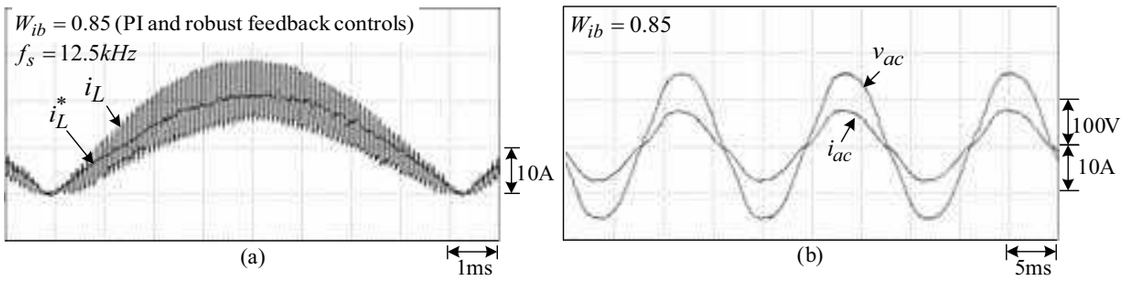

Fig. 24. Measured results of the buck-boost SMR based charger in constant-current charging mode at ($v_b = 47.65\text{V}$, $I_b = 9.45\text{A}$): (a) i_L and i_L^* by PI and robust controls ($W_{ib} = 0.85$, $f_s = 12.5kHz$); (b) v_{ac} and i_{ac} (PF=0.989, THD_i =4.23%)

f_s / Variables	2.5kHz	7.5kHz	12.5kHz	15kHz
P_{ac} (W)	579.7	563.4	547.8	560.6
I_{ac} (A)	5.56	5.15	5.11	5.14
P_b (W)	388.4	427.3	453.3	459.4
V_b (V)	46.32	47.12	47.65	47.73
I_b (A)	8.22	9.02	9.45	9.45
η(%)	67.00	75.84	82.75	81.95
PF	0.972	0.981	0.989	0.991
$THD_{i_{ac}}$ (%)	10.02	7.84	4.23	4.04

Table 9. Measured power quality parameters of the buck-boost SMR based charger under different switching frequencies

6.3 Flyback Switch-Mode Rectifier based auxiliary plug-in charger

6.3.1 System configuration

Fig. 25 shows a switched-reluctance generator (SRG) based DC microgrid distributed power system (Y.C. Chang & Liaw, 2011). The SRG establishes a 48V DC-link voltage, and a common 400V DC-grid is formed through a current-fed push-pull (CFPP) DC-DC converter. To preserve the microgrid power quality, a lead-acid battery energy storage system is equipped. The battery bank (48V) is interfaced to the common 400V DC-grid via a bidirectional buck-boost converter. The battery bank can also be charged from the utility grid by a flyback SMR based auxiliary plug-in charger. For the flyback converter employed in the SMR, three paralleled transformers are used to enlarge its power rating. The The specifications of the developed flyback SMR are given as: (i) AC input: 110V/60Hz; (ii) DC output: $V_o = V_b = 48\text{V}/300\text{W}$; and (iii) power factor: PF > 0.97. The flyback SMR is operated under discontinuous current mode using the charge-regulated PWM scheme developed in (Y.C. Chang & Liaw, 2009a). The turn-on time in is set as $t_{on} = dT_s = 9.2\mu s$, which is constant for the employed PWM switching scheme.

6.3.2 Performance evaluation for the flyback SMR based auxiliary plug-in charger

For the battery bank shown in Fig. 25, the constant charging current $I_b = 6\text{A}$ (i.e., $\hat{I}_{Sc} = 6 / K_{ic} = 6 / 1.107 = 5.42\text{A}$) is set. The measured ($v_{ac}$, i_{ac}) and (v_b, i_b) at steady state of $I_b = 6\text{A}$ during charging process are plotted in Figs. 26(a) and 26(b). The measured static characteristics under two charging currents ($I_b = 6\text{A}$ and 5A) are listed in Table 10. The results show that good charging characteristics with satisfactory line drawn power quality are obtained by the developed flyback SMR based auxiliary plug-in charger.

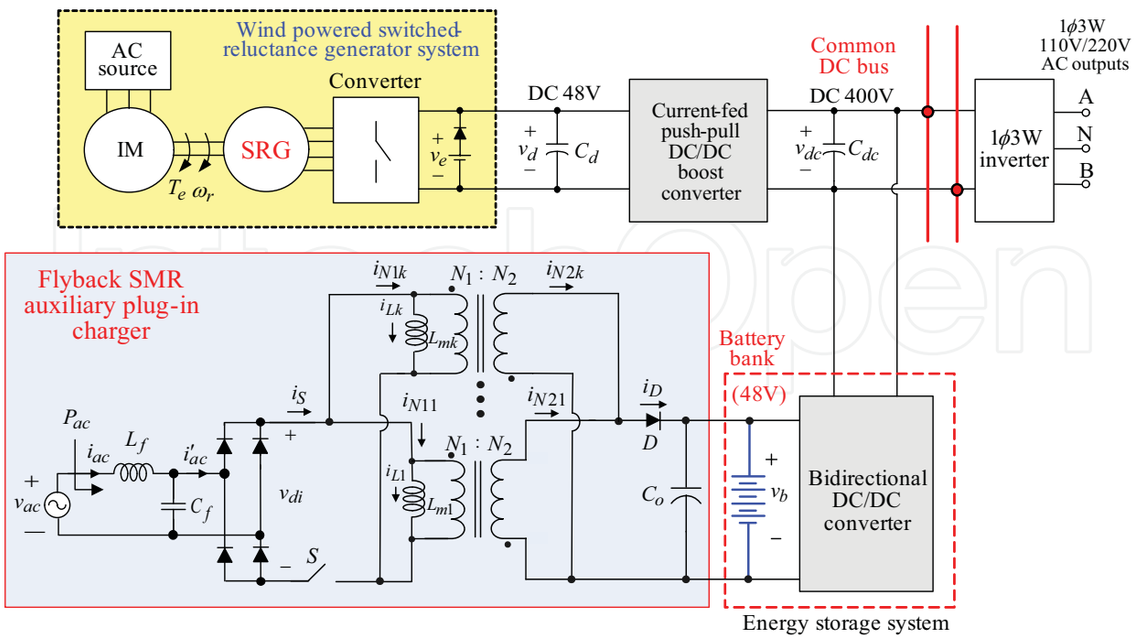

Fig. 25. System configuration of a switched-reluctance generator based DC micro-grid system with flyback SMR auxiliary plug-in charger

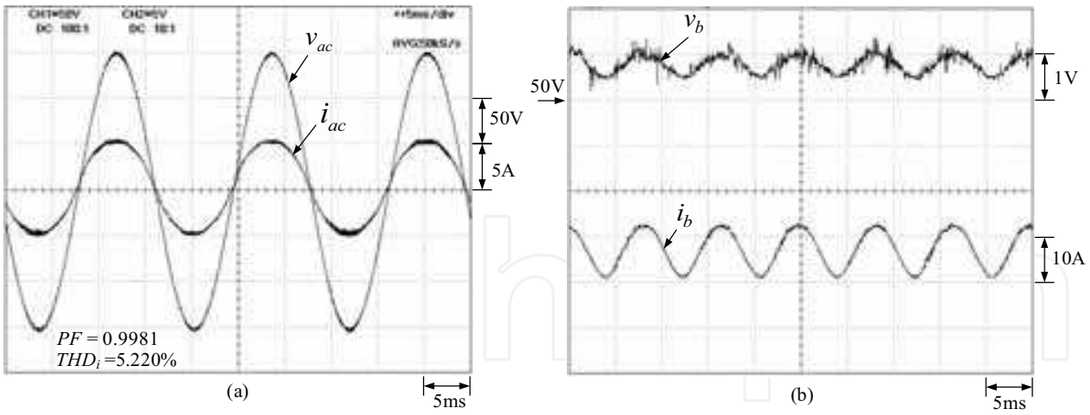

Fig. 26. Measured results of the developed flyback SMR based auxiliary plug-in charger under steady-state charging current of $I_b = 6\text{A}$: (a) (v_{ac} , i_{ac}); (b) (v_b , i_b)

I_b	5A	6A
P_b	265.28W	306.56W
P_{ac}	364.17W	415.98W
η	72.85%	73.70%
PF	0.9986	0.9981
THD_i	3.742%	5.220%

Table 10. Measured results of the developed flyback SMR based auxiliary plug-in charger at two charging current levels

7. Conclusions

This article has presented the basic issues of switch-mode rectifiers for achieving batter performance. The schematic type and control scheme should be properly chosen according to the specific application and the desired operation characteristics. The considering issues include input-output relative voltage levels, operation quadrant, galvanic isoltation, phase number, DCM or CCM operation, voltage mode or current mode control, dynamic control requirement, etc. In power circuit establishment, the ratings of circuit components and the ripples of energy storage components should be analytically derived, and accordingly, the constituted components are designed and implemented.

As to the control affairs, the sensed inductor current and output voltage should be filtered with suited low-pass cut-off frequencies. Then the basic feedack controllers are designed considring the desired perfromance and the effects of comtaiminated system noises. If more stringent control requirements are desired. The simple advanced control, such as the robust tracking error cancellation controls (Chai & Liaw, 2007; Y.C. Chang & Liaw, 2009a), can further be applied. Other possible affairs lie in the digital control with properly chosen sampling intervals, random switching, the considrations of DC-link ripple effects on the followed power stage, parallel opeartion to enlarge SMR ratings, etc.

In this article, the applications of various SMRs to PMSM drive, SRM drive, electric vehicle plug-in battery charger and microgrid plug-in battery charger were presented. The

treatments of basic issues in power circuit and control scheme have been decribed. And their comparative performances have also been assessed to demonstrate the effectiveness of the introduced issues. It is believed that the cost-effective SMR fed power palnt with satisfactory performance can be achieved if the suggested basic issues can be considered.

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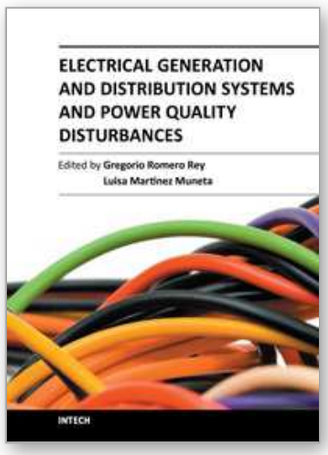

Electrical Generation and Distribution Systems and Power Quality Disturbances

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The utilization of renewable energy sources such as wind energy, or solar energy, among others, is currently of greater interest. Nevertheless, since their availability is arbitrary and unstable this can lead to frequency variation, to grid instability and to a total or partial loss of load power supply, being not appropriate sources to be directly connected to the main utility grid. Additionally, the presence of a static converter as output interface of the generating plants introduces voltage and current harmonics into the electrical system that negatively affect system power quality. By integrating distributed power generation systems closed to the loads in the electric grid, we can eliminate the need to transfer energy over long distances through the electric grid. In this book the reader will be introduced to different power generation and distribution systems with an analysis of some types of existing disturbances and a study of different industrial applications such as battery charges.

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