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Statistical Analog Circuit Simulation: Motivation and Implementation

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1. Introduction

New technologies are continually being developed that enable designers to create faster, more complex circuits, packed within a shrinking die. However, along with the promise of speed and density comes the challenge of variability, as intra-die device mismatch looms proportionately greater. Analog designs typically employ multiple core building block circuits, including current mirrors, band gap references, differential pairs and op amps, that are especially sensitive to device mismatch. Understanding the impact and potential interactions of variations between these matched devices can be critical in producing a commercially viable product.

The first part of this chapter will provide a background on the statistical nature of the semiconductor manufacturing process, with a particular focus on their implications on device performance. Due to the complexity of interactions coupled with circuit-specific design sensitivities, traditional corner models do not provide the designer with sufficient accuracy and visibility to thoroughly assess and improve the quality of their designs. Corner models also do not account for mismatch, which is a major concern for analog designs. A statistical simulation system that realistically replicates process variability will provide the designer with insights to optimize the design.

The second part of the chapter will delve into the extraction and use of statistical models within a statistical simulation system. A properly implemented statistical design tool can become one of the greatest assets available to the designer. Following a discussion of various published statistical model formulations and extraction methodologies from literature, we will consider how they might be incorporated and used within commercially available simulators.

We conclude the chapter with a demonstration that systematically evaluates the components of a band gap circuit to isolate matching sensitivities and refine the design for optimized results. With the assistance of statistical design analysis, a designer can make informed choices that will produce better circuit performance and manufacturability.

2. Semiconductor process variation

Semiconductor device and circuit performance will fluctuate due to the inherent underlying statistical variation in the process itself. This variation can include both random and systematic components. As illustrated in Figure 1, the overall total variance can be

partitioned into components reflecting the physical separation of the material during processing.
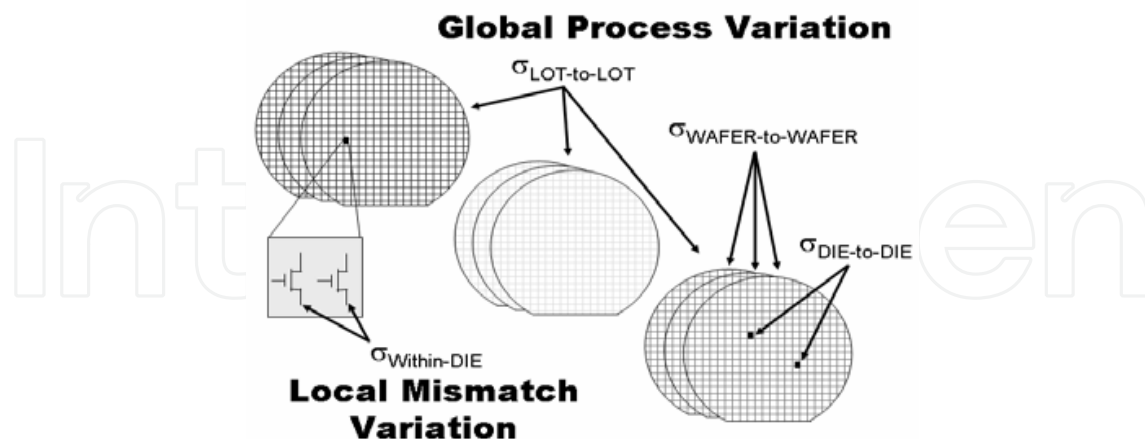

Fig. 1. Classifications of Statistical Variation

Lot-to-lot variance is generally the largest of the components as it reflects significant sources of variation not seen in the other groups, including variation across different tools that may be used at a given process step, variation between batches of raw materials, along with time-based trends and cycles relating to tool aging, preventive maintenance, upgrades and adjustments. Wafer to wafer variance can result from the slight differences experienced between wafers at single wafer processing steps as well as from gradients across batch processed wafers, such as induced by temperature and flow gradients within a furnace tube. Die-to-die variance can be an artifact of differences in exposures in stepper based lithography or gradients or localized disturbances of wafer uniformity. Lot-to-lot, wafer-to-wafer and die-to-die variance combined are often referred to as Global Variation, because all devices found on any particular die will be simultaneously and equally affected by them in the same way. In other words, in the world of that particular die, this is a global effect.

Within-die (device-to-device) variation may include a more localized contribution of some of the wafer uniformity effects driving die-to-die variance, as well as individual device definition effects resulting in slight non-uniformities in film thicknesses and edge definitions, dopant distributions, junction depths, surface roughness, and so on. Within-die variance is generally referred to as Local Variation, because the performance of each individual device on a given die will be affected slightly differently by it.

This variation can include both random and systematic components. The designer may have some limited control over certain systematic components relating to device layout, but needs to be aware of and have some means to estimate the effects of variation on circuit performance. Traditionally, this was done using so-called 'corner' models, intended to represent the worst case corners of the process variation.

3. Issues with traditional corner models

In traditional corner methodologies, 'worst case' models were typically created by evaluating the sensitivities of critical model parameters individually and then setting each of them to their worst case values simultaneously. The accuracy of this approach, however, would be highly dependent on the actual physical correlation between the parameters as

well as the cumulative probability that all would be worst case at the same time (Nardi et al., 1999). The corner method also assumes a 'one-size-fits-all' solution, when in reality different designs and circuit architectures will exhibit different worst case sensitivities. Finally, fixed corner models do not account for the intra-device variations that can have a major impact on analog circuit performance.

3.1 The issue of correlation

To demonstrate the impact of correlation, consider two standard normal variables, X and Y, which are summed and scaled to create Z. Figure 2 depicts the results for 3 cases representing negative, zero and positive correlation between X and Y:
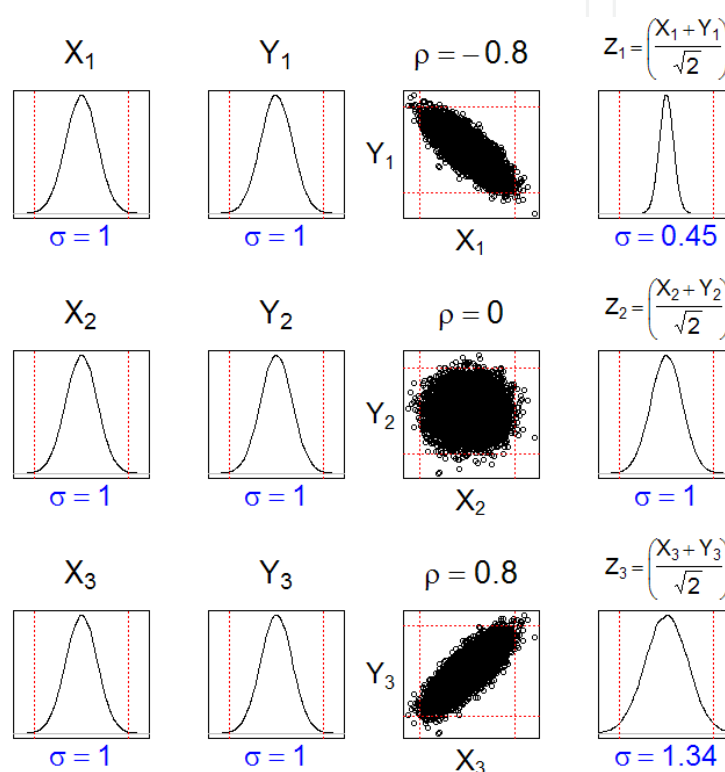

Fig. 2. The Impact of Correlation

In this simple example, it is intuitively obvious that when X and Y are negatively correlated, they would tend to cancel each other out, thus minimizing the resulting variability of Z. Conversely, when they are positively correlated, they would tend to reinforce each other, creating greater variability. Semiconductor processes, of course, are much more complex with a great number of interacting variables. The fact that there are a large number of variables brings in the next problem: how to determine which combinations of these variables best define the corners?

3.2 The issue of corner selection

Assume we have a normally distributed process and we want to define a set of worst case corners that encompass an interval of ± 3 standard deviations about its mean ($\mu \pm 3\sigma$). In other words, the probability the process would fall outside of our $\mu \pm 3\sigma$ corners would be about 0.0027. The probability that two different uncorrelated normally distributed variables

would both simultaneously fall outside their respective $\mu \pm 3\sigma$ is only $(0.0027)^2 = 0.00000729$. As the number of independent variables increases, the probability that they would all simultaneously fall outside their respective $\mu \pm 3\sigma$ windows drops off rapidly, as shown in Figure 3a.

Instead of putting all variables at $\pm 3\sigma$, we might prefer to find a $\pm k\sigma$ window such that the probability of falling outside remains constant at 0.0027 (for n variables, this corresponds to the standard normal z score for area of $(0.0027^{1/n})/2$). As the number of independent variables increases, the k value drops, as shown in Figure 3b.

Of course, there is nothing that forces us to select a corner that puts each variable at the same k value. Figure 3c show the line that plots possible solutions of k values when there are only 2 variables to consider (for 3 variables, the solution would be a surface and for n variables, it would be an n dimensional space).
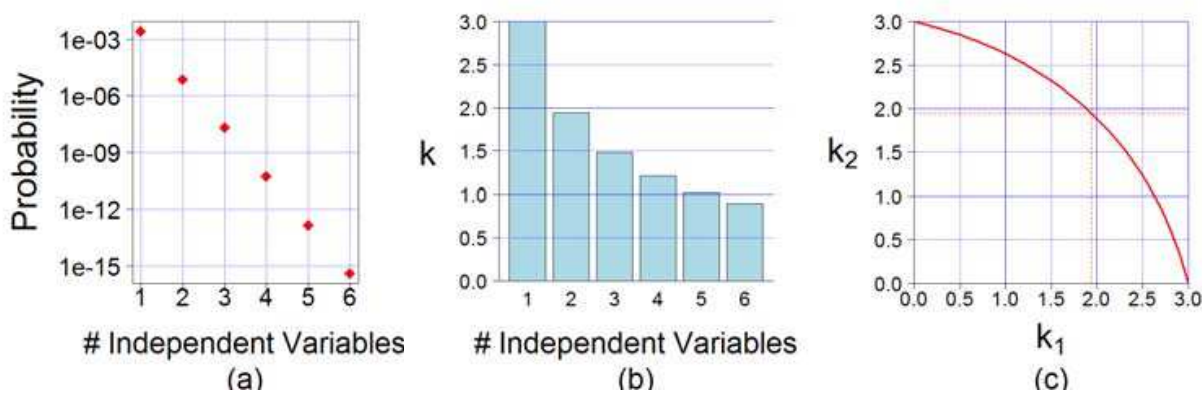

Fig. 3.
(a) Probability of Multiple Variables Falling Outside Their Respective $\mu \pm 3\sigma$ Windows
(b) k Values vs. # Variables for Cumulative Probability Outside $\mu \pm k\sigma = 0.0027$
(c) Possible Solutions for k_1 and k_2 for Constant Probability Outside $\mu_n \pm k_n\sigma_n = 0.0027$

The more variables there are in a given process, the less likely that the uncorrelated components within them will all be worst case at the same time. Ideally, a worst case corner would place those parameters that have greatest impact on circuit performance at more extreme values, while letting other less important parameters remain at more nominal levels.

In the context of semiconductor device and circuit performance, the relative importance of a given process parameter often depends on the device architecture and operating conditions. Figure 4 depicts the sensitivities of several simulated MOS I_{DS} conditions to SPICE model parameters lint (channel length offset fitting parameter), wint (channel width offset fitting parameter), vth0 (threshold voltage @ Vbs=0), tox (gate oxide thickness) and rdsw (parasitic resistance per unit width).

The underlying independent process variables that would contribute to that variation include poly gate lithography, gate oxide deposition and source drain implant and anneal (Mutlu & Rahman, 2005). Being independent, the probability of all of them being worst case at the same time is quite low. Figure 5 further demonstrates this effect, showing the results of a 10000 trial Monte Carlo simulation of the propagation delay of a simple inverter cell. Although the Monte Carlo completely covers the range of values defined by the worst case corner models for the individual model parameters, the resulting propagation delay distribution falls well inside the values predicted by the corners, simply because the occurrence of those simultaneous worst case conditions is so improbable:
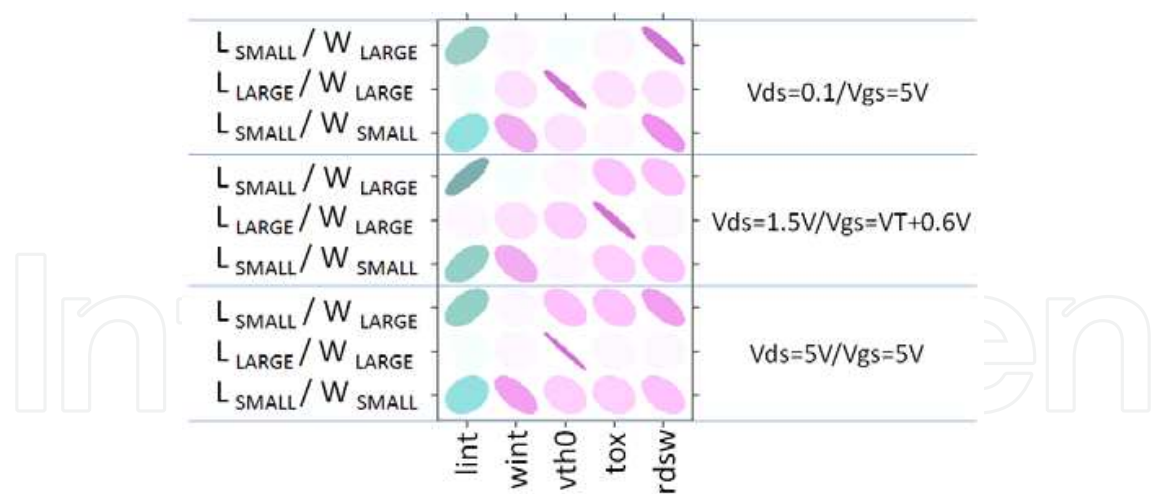
Fig. 4. Some Underlying MOS I_{DS} Sensitivities vs. Device Size and Bias Conditions
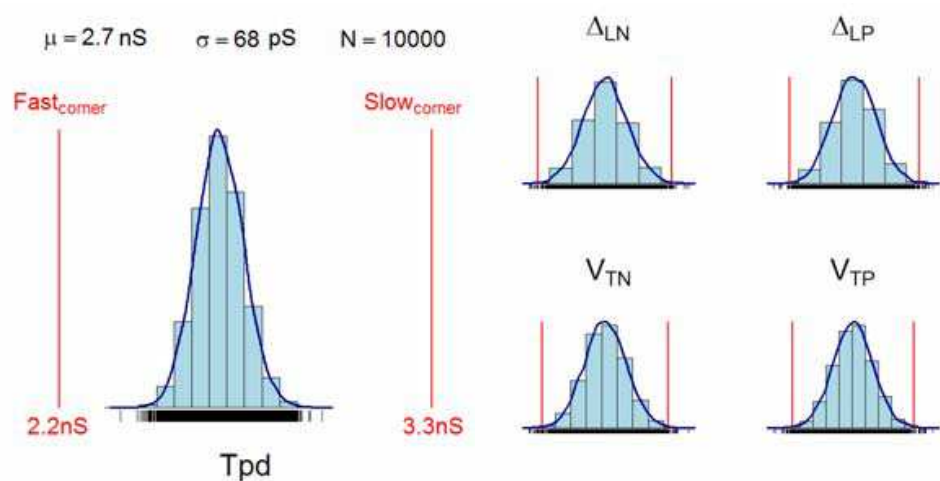

Fig. 5. All Parameters Simultaneously at Worst Case Yields Unrealistic Corners

Complicating the issue of corner selection is the fact that the worst case conditions may be completely different for circuit performance criteria that are sensitive to different process perturbations, such as the propagation delay of a CMOS digital logic circuit versus the gain of an operational amplifier. Even between related circuit performance parameters within the same circuit cell there can be notable differences. Consider the enable and disable propagation delays of a sample CMOS digital logic circuit as present in Table 1. When set to the worst case corners for disable (HZ/LZ) delay, TpZH encompasses less than 25% of the delay window obtained when using worst case enable corners (0.4nS vs. 1.8nS). The difference between the two corners is the placement of Tox. Ordinarily, Tox would be reduced for a Fast corner as it provides higher drive. However, thinner Tox also means higher oxide capacitance. The benefit of higher drive more than compensates for the penalty of higher capacitance in active delays, but the impact of the higher capacitance dominates for disable delays.

Statistical models are not tied to a particular fixed choice of conditions as corner models are. They are generally formulated to reflect underlying process interactions by re-expressing the correlated model parameters as functions of an appropriate set of uncorrelated

Worst Case Corner Setting	TpHZ (nS)	TpLZ (nS)	TpZH (nS)	TpZL (nS)
Corner 1: Worst Case Disable Times	**3.2/4.6**	**3.3/4.1**	2.3/2.7	2.0/2.5
Corner 1: Δ Slow - Fast	**1.6**	**0.8**	0.4	0.5
Corner 2: Worst Case Enable Times	3.6/4.2	3.5/3.9	**1.6/3.4**	**1.5/2.9**
Corner 2: Δ Slow - Fast	0.6	0.4	**1.8**	**1.4**

Table 1. Different Circuit Parameters may have Opposing Corner Conditions

parameters. When exercising a statistical model, the uncorrelated parameters are perturbed, rather than the model parameters directly. These changes are then propagated through to the model parameters to generate properly correlated model decks. While statistical models do not inherently resolve the issues of circuit dependencies in and of themselves, they do enable the use of exploratory statistical simulation strategies including design of experiments and response surface model (DOE/RSM) techniques that can efficiently evaluate the response of a given circuit over the entire process/design space to determine the particular worst case conditions for a given circuit (Rappitsch et al., 2004; Sengupta et al., 2004; Zhang et al., 2009).

3.3 The issue of localized matching variation
It is imperative for analog/mixed-signal designs, and is becoming increasingly important for digital designs as well, that today's simulation methodologies have the means to evaluate the effects of localized device mismatch on circuit performance. Fixed corner models applied uniformly across all device instances in a circuit do not provide any allowance for mismatch. As seen in Figure 6, the impact of mismatch on analog circuit blocks can easily exceed the variation that would otherwise be expected due to global variation over the entire process range. Simulating under the effects of global process variation only, the current mirror output current, I_O, exhibited a standard deviation of ~50nA, traced predominantly to V_T, with some residual sensitivity to L_{EFF}/W_{EFF} and
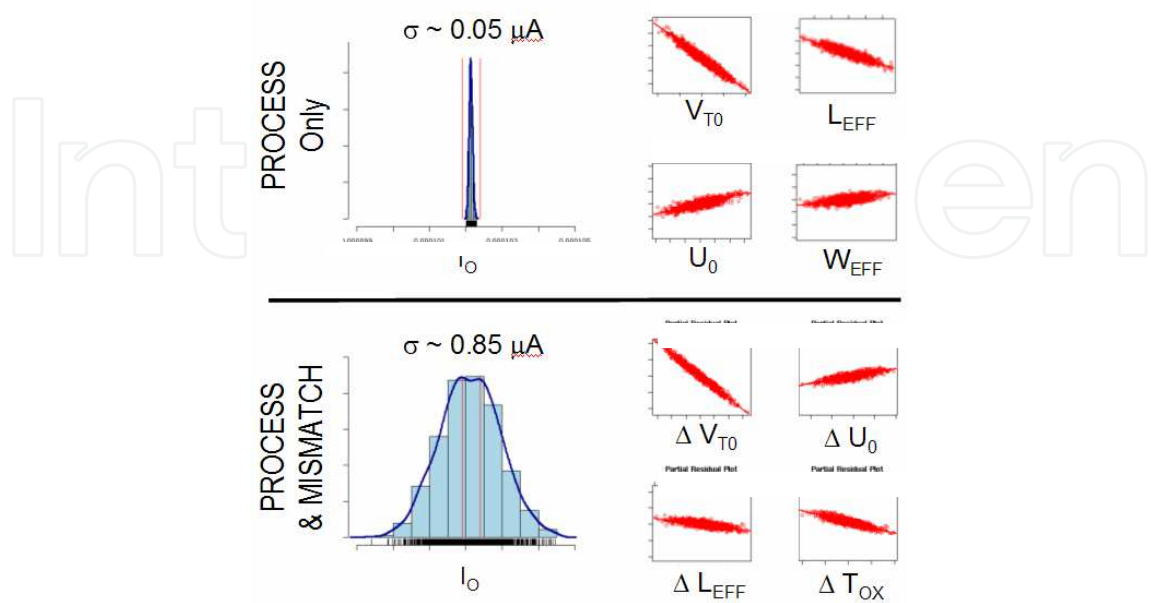

Fig. 6. Statistical Simulation of Basic Current Mirror

mobility. Adding in additional slight perturbations to the values of these parameters as applied each individual device in the circuit, the standard deviation of I_O increased about 17x to 0.85uA, almost entirely attributed to the slight difference in V_T applied between the critically matched MOS devices:

Local mismatch variation is observed by comparing two or more identical devices on a die. In the absence of systematic variation, a normally distributed random mismatch variation would induce a normal distribution upon a given parameter, P, such that P would be expected to have a mean of μ_P, the average value of P across that die, and a standard deviation of σ_P:

$$P \sim \eta(\mu_P, \sigma_P^2) \tag{1}$$

The observed difference in P between any two identical devices would be expected to be distributed with a mean of 0 and standard deviation of $\sqrt{2}\sigma_P$ (variance of $2\sigma_P^2$):

$$\Delta_P \sim \eta(0, 2\sigma_P^2) \tag{2}$$

(Lakshmikumar et al., 1986) derived a $1/\sqrt{(LW)}$ scaling dependence for threshold voltage and conductance mismatch. Using Fourier techniques, (Pelgrom et al., 1989) postulated a generalized expression for the variance of Δ_P between two rectangular devices as:

$$\sigma^2(\Delta_P) = \frac{A_P^2}{WL} + S_P^2 D_x^2 \tag{3}$$

where: W and L are the width and length of each rectangle

D_x is the separation distance between the rectangles

A_P, also known as *A factor*, is the area coefficient and

S_P is the spacing coefficient

As indicated that model, the variance of Δ_P would be expected to increase as the device sizes decrease and as the devices are spaced farther apart from one another. The magnitude of the A factor is typically a reflection of the process design itself as opposed to specifically controllable manufacturing components (Tuinhout, 2002). For MOS devices, V_T, g_m and I_D matching is affected by multiple process architectural components, including S/D and channel doping (Tuinhout et al., 2000 & Dubois et al., 2002) and gate poly/oxide definition (Difrenza et al. 2003; Brown et al., 2007; Cathignol et al., 2008).

For analog designs in MOS technologies, threshold voltage mismatch is of particular concern. (Pelgrom et al., 1998) presents a physical representation of A_{VT}, the A factor for MOS threshold voltage mismatch, as:

$$A_{VT} = \frac{q \cdot t_{ox}\sqrt{2Nt_{depl}}}{\varepsilon_0\varepsilon_{ox}} \tag{4}$$

where: *N* represents the total number of doping in the depletion region ($N_a + N_d$)

t_{depl} represents the width of the depletion region

t_{ox} represents the gate oxide thickness

A direct relationship between t_{ox} and A_{VT} is clearly evident. A former rule of thumb for technology nodes over 0.1μm gate length suggested A_{VT}, in saturation regions, would run at about 1 mVμm per nm of gate oxide thickness (Pineda de Gyvez & Rodríguez-Montañés,

2003). Within equation (4), the reduction of t_{ox} is somewhat offset by the required increases in doping levels at reduced geometries. Deep sub-100nm processes bring increasing effects from lithography and other gate region uniformity challenges (Brown et al., 2007; Cathignol et al., 2008 & Lewyn et al., 2009). Layout effects and neighbouring topology can all induce additional mismatch deviations beyond those accounted for in A_{VT} (Drennan et al., 2006 & Wils et al., 2010).

From a design perspective, it is important to take in account the relationship of circuit bias selections on resulting mismatch performance (Kinget, 2004). For instance, as V_{GS} approaches V_T, the relative mismatch variation in I_D increases, peaking in subthreshold region as shown in Figure 7:
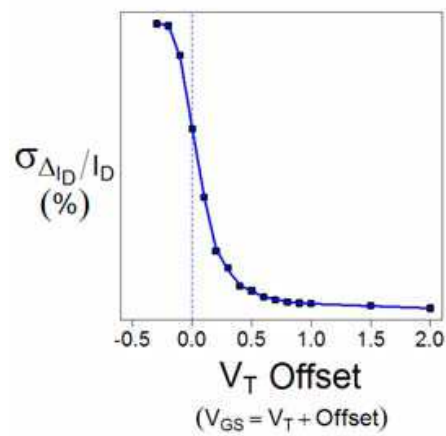

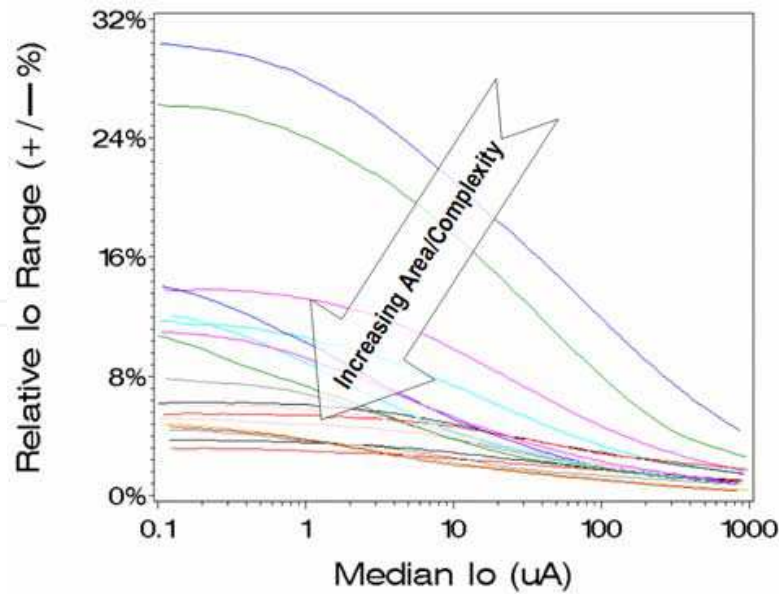Fig. 7. MOS I_D Relative Mismatch Variation Increases in Subthreshold Region

Fig. 8. Comparison of Current Mirror Data

The influence of biasing impacts can be seen in sample current mirror data. Figure 8 shows results, measured over multiple mirror configurations and sizes, for the total observed range of Io (expressed as +/- %) relative to the median operating Io value under various test conditions. Mirrors intended to run at very low currents will be exhibit proportionately

greater mismatch sensitivities. Reducing this variation requires larger devices and/or more complex mirror configurations, either of which can adversely impact manufacturing costs due to a larger die area.

Statistical models can offer the designer the opportunity to evaluate and compare the effects of mismatch on circuit performance under different design scenarios. Relative to corner models, statistical models offer improved accuracy, by properly retaining key parameter correlations, improved coverage, by not being tied to some arbitrary set of corners, and improved capability, by incorporating localized mismatch as well as global process variation effects.

4. Implementing statistical design

Implementing statistical design requires the development or procurement and integration of 3 key components: a simulation tool capable of exercising statistical models, the statistical models themselves and finally the appropriate methodologies to use them efficiently and cost effectively to validate and improve a circuit's design (Duvall 2000). The goal of statistical circuit modeling is to be able to replicate the observed pattern of global and local variances such that their effects on a particular circuit design can be simulated and, if necessary, design enhancements introduced prior to committing the design to silicon.

4.1 Extracting statistical models

Statistical models are formulated to retain correlation by re-expressing the correlated model parameters as functions of an appropriate set of uncorrelated parameters. When exercising a statistical model, the uncorrelated parameters are perturbed, rather than the model parameters directly. These changes are then propagated through to the model parameters to generate properly correlated model decks.

In its most generic representation, a statistical model would define the value of some parameter P within the jth device on the ith die as:

$$P_{ij} = \mu_{PROCESS} + G_{OFFi} + L_{OFFij} \tag{5}$$

where: $\mu_{PROCESS}$ = overall process mean for that parameter.

G_{OFFi} = global offset associated with the ith die:

$$(\mu=0, \sigma^2=\sigma^2_{GLOBAL})$$

L_{OFFij} = local offset for the jth device on ith die:

$$(\mu=0, \sigma^2=\sigma^2_{LOCAL})$$

As indicated in Figure 9, variations in the independent fabrication process variables (eg: implant dose and energy, furnace temperature, ramp time, flow rate, etc.), interact to create statistical distributions of the process characteristics (eg: junction depths, doping profiles, etc.). Different characteristics may exhibit some degree of correlation to one another due to common influences. For example, the annealing temperature/time of a poly implant will have some effect on the ultimate doping profiles of earlier source/drain and well implants/diffusions. The process architecture design and implementation will influence the nature and strength of these correlations. The statistical variations and inter-correlations of process characteristics will drive the statistical variations and inter-correlations of the device characteristics, as influenced by the device architecture design, and so on.
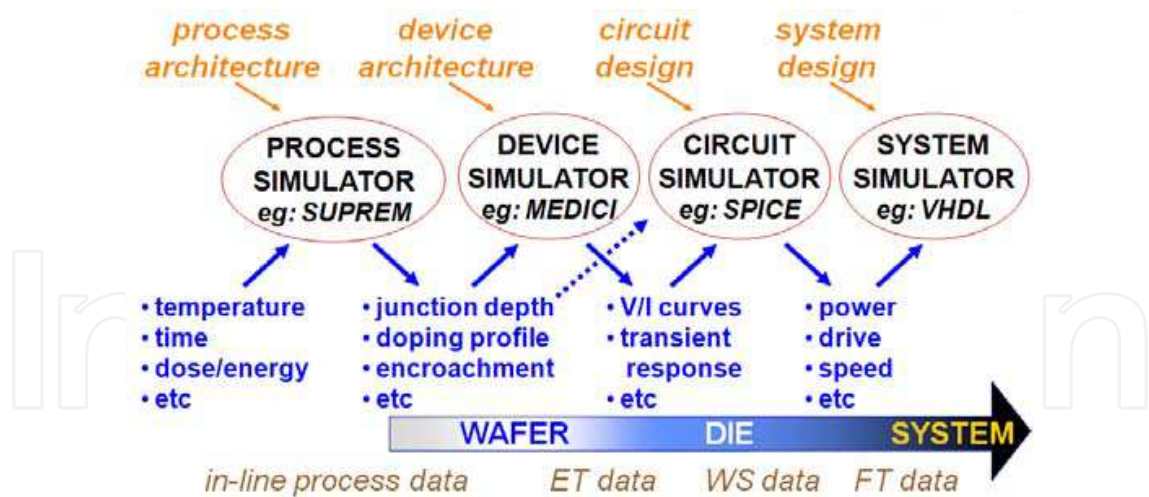
Fig. 9. Progression of Increasingly Complex Parameter Interactions

It is effectively impossible to precisely track the propagation of the variation and their impacts throughout the levels. We can get a general assessment of process variation from inline process data, device variation from wafer electrical test (ET) and circuit performance variation via wafer sort (WS) and final test (FT) data, but we have no way of knowing what specific process conditions any particular die experienced. TCAD simulators can be coupled together to cover the entire process (Hanson et al., 1996), but that requires very well calibrated models as the effects of any errors/omissions would be compounded throughout the system.

The inputs to the circuit simulator (referred to hereafter as the model parameters) are a mixture of inter-correlated pseudo-physical as well as non-physical (fitting) parameters. Since they are inter-correlated, it is not statistically (or physically) appropriate to perturb their values independently of each other. Proper correlation between the model parameters can be maintained by expressing the model parameters as functions of other independent parameters which are more suitable for applying direct statistical perturbations. These parameterized model expressions can be thought of as behavioral models, developed to provide suitable proxy for device characteristic/model parameter distributions as inputs to the circuit simulator such that reasonably realistic circuit performance projections can be expected.

Establishing appropriate distributions and intercorrelations of the model parameters can be a significant challenge. Wafer electrical test (ET) data is used to characterize a process and extract the circuit model parameters. The cumulative effect of the underlying variations in the process is manifest in the observed distribution of ET parametric data. That is:

$$E = f(\mathbf{p}) \tag{6}$$

where: E = an ET parameter

$\mathbf{p}$ = a vector of process parameters

ET data is used to extract the circuit model parameters. This is generally done by creating a large database of ET results obtained over a wide array of device geometries, architecture and operating conditions and using a specialized extraction tool, such as ICCAP, to optimize the model parameters via curve fitting. Hence, we have:

$$M = f(\mathbf{E}) \tag{7}$$

where: M = a device model parameter

E = a vector of ET parameters

For statistical modeling, the challenge is to define how to alter the model parameters in a statistically realistic manner. As stated earlier, it is not appropriate to vary the model parameters directly since they are correlated with one another. It is also not feasible to estimate the correlation between the model parameters from the model files themselves as they are usually only directly extracted for a very limited number of ET sites (and even if a suitably large set of model files were generated, there would be concerns over whether the model extraction methodology itself might have influenced the results). TCAD simulation can be used to develop models tied back to independent physical components, but this introduces additional, compounding sensitivities to the inherent accuracy of each modeled stage. Circuit designers and modelers often have less access to and familiarity with those TCAD tools. They are generally quite familiar with ET data, however, and large samples are often readily available from which the necessary statistical information can be determined and utilized for statistical modeling (Chen et al., 1996; Potts & Luk, 1998; Singhal & Visvanathan, 1999). The variation of several model parameters can be directly mapped to the variation in measured or extracted ET characteristics, including vth0 (to measured threshold voltage), xl/lint and xw/wint (to extracted L_{EFF} and W_{EFF} calculations, respectively), tox (to inverse of gate oxide capacitance) and the sheet resistances of various layers. Others can be proportionally mapped to functions of measured data, including mobility (u0 ~ Gm/Cox*[L/W]) and saturation current (is ~ ln(vbe)).

The first step of the extraction process is to validate the ET data, removing any invalid outliers, and transforming each parameter to a standardized normal distribution (keeping track of the transformations so that we know how to reverse transform it back later). Next, we perform principal component analysis (PCA) on the transformed data. PCA is a technique that can be used to re-express a correlated set of variables in terms of uncorrelated components [16]. An orthogonal transformation matrix, B, is found such that:

$$\mathbf{Y} = \mathbf{B}(\mathbf{E} - \bar{\mathbf{E}}) \tag{8}$$

$$\mathbf{Z} = \mathbf{\Lambda}^{-\frac{1}{2}} \mathbf{B}(\mathbf{E} - \bar{\mathbf{E}}) = \mathbf{A}\mathbf{X} \tag{9}$$

$$\mathbf{S} = \mathbf{B}'\mathbf{\Lambda}\mathbf{B} \tag{10}$$

where: E = matrix of correlated ET data, with means $\bar{\mathbf{E}}$

Y = matrix of principal components

Z = standardized PCA components

S = covariance matrix of $X_1, X_2, ..., X_n$

$\mathbf{B}'\mathbf{\Lambda}\mathbf{B}$ = spectral decomposition of S

$\mathbf{\Lambda}$ = diagonal matrix, diag($\lambda_1, .. \lambda_n$), with $\lambda_1 > \lambda_2 > ... > \lambda_n$ the eigenvalues of S

$\mathbf{A} = \mathbf{\Lambda}^{-\frac{1}{2}}\mathbf{B}$ and $\mathbf{X} = (\mathbf{E} - \bar{\mathbf{E}})$

Each of the principal components in Y and Z has a mean of 0 and is uncorrelated with all other principal components (that is, each Y_i is uncorrelated with all other Y_i and each Z_i is uncorrelated with all other Z_i). The variance of each Y_i is the value of the corresponding ith eigenvalue, while the standardized PCA components, Z_i, each have a variance of 1. If all X_i are normal, then each of the Z_i is standard normal, which is convenient for formulating the statistical models. For example, to run a monte carlo, the statistical simulation tool would generate vectors of Z, with each Z_i being a random normal value. These random vectors of

Z would then be reverse transformed back into corresponding vectors of E, from which we can map random, but properly correlated, perturbations of M!

Figure 10 demonstrates this technique. The black data points represent an actual sample of data collected over a 4 month period. The original 6 correlated ET parameters are decomposed into 4 uncorrelated PCA components. The matrix between them on the lower right graphically depicts that transformation relation. L_{EFFN} and L_{EFFP} are strongly related to PCA parameter A, T_{OXN} and T_{OXP} are strongly related to B, V_{TP} is strongly related to D and V_{TN} is related to C with dependance on A and D as well. While the PCA solution is entirely a mathematical construct, it may offer insights into the underlying physical relationships. Physically, L_{EFFN} and L_{EFFP} would be highly dependent on the gate poly CD, T_{OXN} and TOXP on the gate oxide thickness, V_{TN} would be dependent on multiple parameters, including N_A, T_{OX}, x_j and, for short/narrow devices, L/W, while V_{TP} would have a strong dependence on V_T adjust implant. A PCA solution that does not appear to bear any resemblance to a logical underlying physical relationship should merit greater scrutiny of the data for a possible invalid readings or a need for normality transformation.
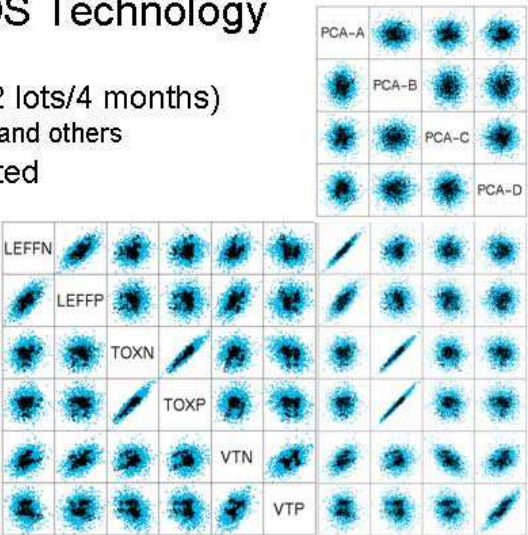

Fig. 10. Example of PCA Transformations: ET > PCA & PCA > ET

For parameters that cannot be directly mapped to physical data, it will be necessary to indirectly estimate appropriate values that will yield appropriate results when used in simulation. This includes all mismatch parameters. The backward propagation of variance (BPV) technique is quite helpful in this process (McAndrew et al., 1997; Telang & Higman, 2001, Drennan & McAndrew 2003; McAndrew et al., 2010). Measured ET data is collected over a wide spectrum of device geometries and bias conditions. Simulations are then set up covering the same set of parameters. For the first pass of simulations, a small arbitrary value of variation is assigned to each of the independent mismatch model parameter (such as 1% of its corresponding global variance). These initial simulations are used to determine the covariance matrix (or squared correlations) between the mismatch models parameters and the resulting simulated mismatch variance. Regression analysis is then performed to fit an appropriate vector of mismatch model parameter variance such that the simulated ET mismatch variances would approximate the actual measured ET mismatch variances:

$$\sigma^2_{ET} = S * \sigma^2_{Model} \tag{11}$$

where: σ^2_{ET} = vector of observed ET variance in measured data
S = covariance matrix of simulated ET results vs model parameters
σ^2_{Model} = vector of (fitted) variance to assign to model parameters
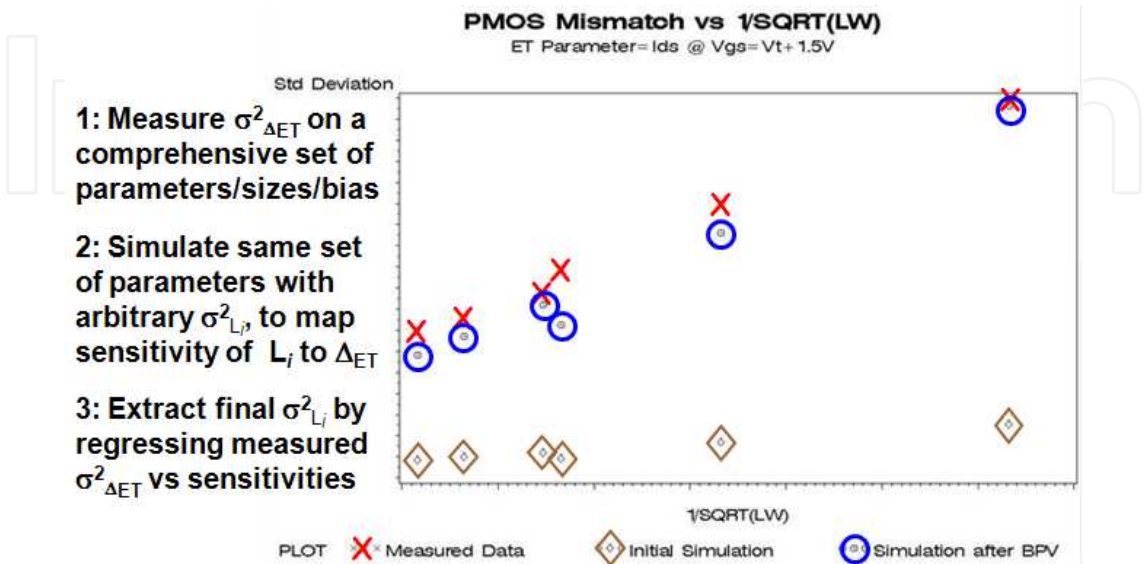

Fig. 11. Example of BPV to Fit Observed ET Data

4.2 Implementing statistical models

Over the past decade or so, Monte Carlo and other statistical simulation capabilities have been added to commercial SPICE simulators. They enable the use of specially parameterized and formulated expressions to implement the desired statistical model behavior (Lu et al., 2009). Recent compact models are also incorporating new parameters that, when combined with extracted layout information, can better predict important mismatch sensitivities, such as stress and well proximity effects (Watts et al., 2006; Yang et al., 2008).

We have implemented our parameterized statistical models within the Cadence Analog Design Environment, utilizing the monte carlo features available within their Statistical Analysis Tool (Potts & Luk, 2005). This tool offers the ability to designate random variables into two groups, process and mismatch, as declared within a statistics block within the model library, prior to the models themselves:

```
statistics {
    process {
            vary G1    dist=gauss    std=1
            ….
            vary Gn    dist=gauss    std=1
     }
    mismatch {
            vary L1    dist=gauss    std=1
            ….
            vary Lm    dist=gauss    std=1
     }
}
```

Within the models, we then encode the ith model parameter, P_i, as a functions of these independent variables by applying the statistical models we have derived for global variation , e.g.: $f_{Gi}(G_1,...,G_n)$, and mismatch, e.g.: $f_{Li}(L_1,...,L_m)$, such that:

$$P_i = P_{TYPICAL} + f_{Gi}(G_1,...,G_n) + f_{Li}(L_1,...,L_m) \qquad (5)$$

Since we have formulated our statistical models as functions of independent normal variables, each of our global variables ($G_1 - G_n$) has been declared as Gaussian distributions with a mean of 0 and a standard deviation of 1. The local variables ($L_1 – L_n$) are declared as Gaussian distributions with a mean of 0 and a standard deviation of δ_i ($0 < \delta_i < 1$), where δ_i are fitted through a backwards propagation of variance technique.

With statistical SPICE models in hand, the simplest and most generic analysis methodology, equally applicable to dc, transient or any other simulation set-up, utilizes Monte Carlo simulations to detect and isolate potential trouble spots in the circuit. With the Cadence 6.x ADE-XL/GXL platform, traceability can be enabled to monitor Monte Carlo values applied to each instance during each trail, providing a means to quickly locate any design weaknesses.

The major drawback to Monte Carlo analysis is simulation time. A large number of trails are needed, especially if one needs to accurately evaluate the tails of the distribution. This is less of an issue for small circuits or individual circuit blocks which can be simulated on the order of seconds or less per trial. As such, one strategy for larger circuits would be to break it down into blocks, and fitting behavioural macromodels to express the variation of the output of one block, which could then be applied as the input to the next block. Ignoring correlation, this could simply be done by redefining a fixed voltage or current as a design variable, say V1, set by an additional random variable of desired location and spread, e.g.:

```
parameters V1 = {desired mean value}
statistics {
    process {   ....
            vary V1    dist=gauss    std={desired standard deviation}
        }
```

A more proper solution, however, would retain correlation by expressing the V1 voltage as a function of the same Monte Carlo variables used in defining the SPICE statistical models themselves. This would be done by running Monte Carlo simulations on the circuit block that generates the V1 signal, applying regression techniques to fit the resulting V1 over the values for the Monte Carlo parameters from each trial, and then using that regression equation to define the V1 input to apply to the next block, e.g.:

$$parameters\ V1 = f_{Gi}(G_1,...,G_n) + f_{Li}(L_1,...,L_m)$$

There are alternative methods that do not require Monte Carlo, including sensitivity analysis, design of experiments (DOE) and response surface modelling (RSM) techniques. Typically, a sensitivity analysis is performed to isolate the critical model inputs and then a DOE is run over those variables (which generally requires far fewer trials than a Monte Carlo), and then RSM is employed to analyze/optimize the results. These methodologies are not as readily implemented within standard commercial SPICE simulators, requiring significant additional pre-/post-processors for set-up and analysis. Commercial solutions are available from 3rd party vendors, however, including Circuit Surfer® (PDF Solutions), Variation Designer (Solido Design Automation) and WiCkeD™ (MunEDA GmbH).

5. Demonstrational analysis of a band gap circuit

In this section, we will demonstrate the use of our statistical CAD tools and methodologies to characterize and optimize a Bi-CMOS band gap circuit consisting of a MOS bias generator, PNP band gap reference and MOS op amp, as shown in Figure 12. The circuit was initially designed and simulated to produce a stable reference voltage, V_{BGOUT}, of about 1.18 +/- 20 mV over corner models.
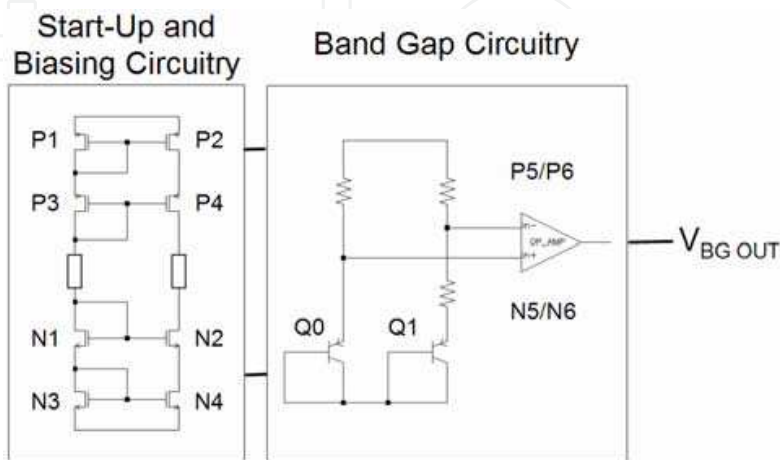

Fig. 12. Band Gap Circuit used in this Example

The baseline process Monte Carlo projected a V_{BGOUT} σ of 9.5mV – virtually all traced to PNP Is variation.
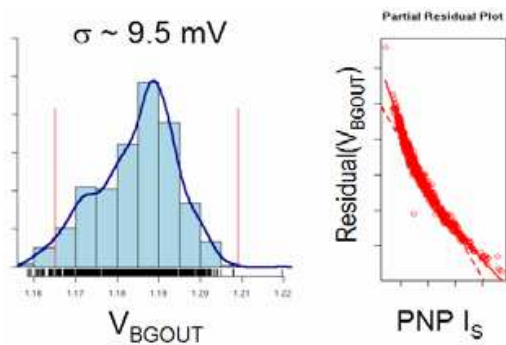
Fig. 13. Process-Only Monte Carlo Results

The combined process and mismatch Monte Carlo generated a much larger variation along with a prominent asymmetric low tail:
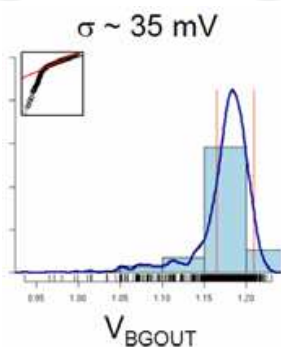
Fig. 14. Combined Process & Mismatch Monte Carlo

Partitioned mismatch Monte Carlos quickly pinpointed the source of the tail to MOS mismatch sensitivities within the start-up & biasing block:
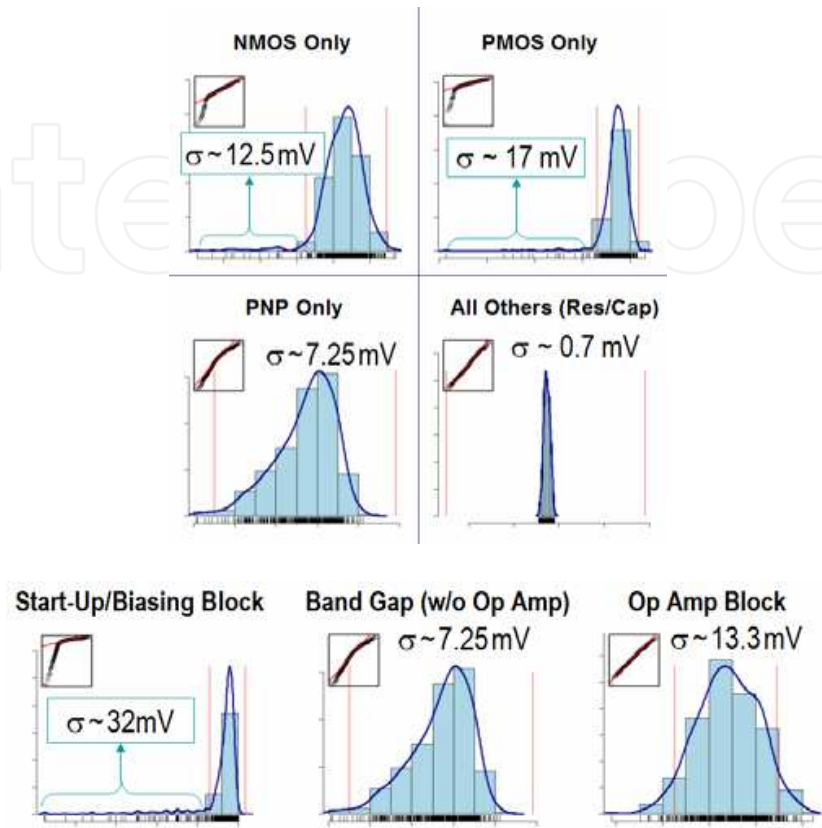

Fig. 15. Partitioned Mismatch Monte Carlo Results

Probing in the biasing block revealed "lurking cliff" ΔVt sensitivities between devices P1 & P2 and N3 & N4 (where P1,P2,... refer to devices as labelled in Figure 12):
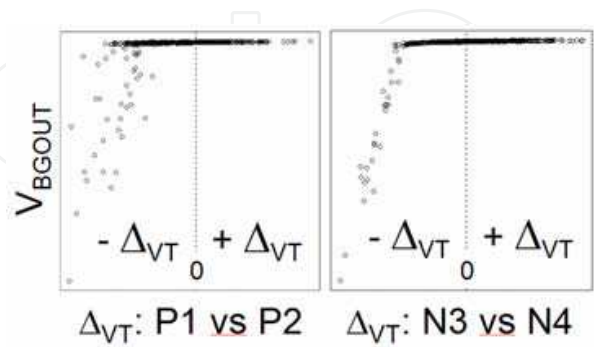

Fig. 16. Tail Traced to Δ_{VT} in Bias Circuit

After removing the outlying values in the tail, the remaining mismatch sensitivities are traced to the differential pair (P5/P6) and mirror (N5/N6) in the op amp and the PNP pair (Q0/Q1) in the band gap:
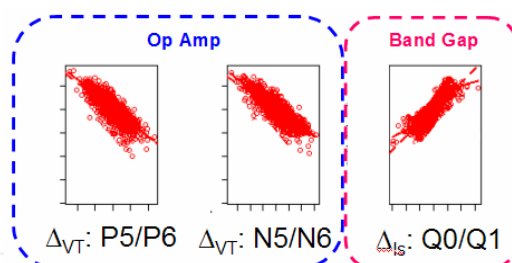
Fig. 17. Non-Tail Sensitivities: Op Amp & Band Gap

Increasing the sizes of these identified critical devices by about 2x to 3x from their original values reduces the Vbgout standard deviation under combined Process & Mismatch Monte Carlo from ~ 35mV to ~ 10mV. At that point, the PNP Is process sensitivity becomes the dominant factor in overall V_{BGOUT} variability and any additional mismatch reduction yields minimal benefit.
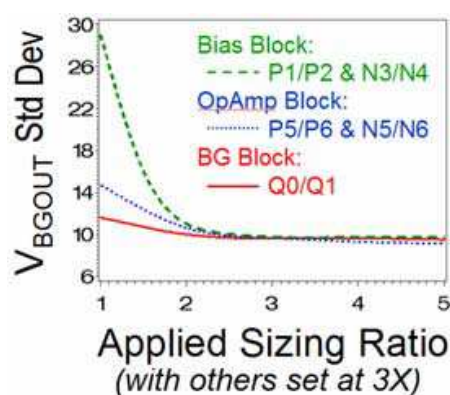

Fig. 18. Overall Variation Optimized @ 2x-3x

6. Conclusion

Statistical design offers considerable improvements over traditional worst case design methodologies. New tools and methodologies are being developed and offered in the EDA market that will enable the designer to use statistical models efficiently. A statistical design simulation framework enables the opportunity to make more intelligent design choices up front that will result in a more robust and manufacturable circuit design.

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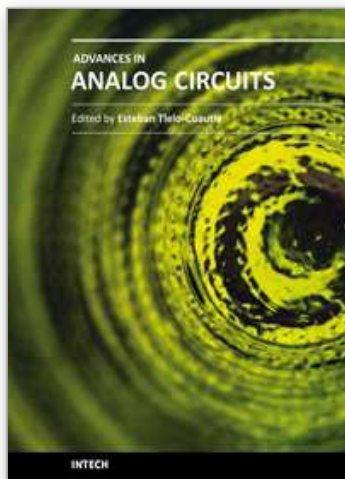
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