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Impact of Technology Scaling on Phase-Change Memory Performance

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1. Introduction

Nowadays, non-volatile storage technologies play a fundamental role in the semiconductor memory market due to the widespread use of portable devices such as digital cameras, MP3 players, smartphones, and personal computers, which require ever increasing memory capacity to improve their performance. Although, at present, Flash memory is by far the dominant semiconductor non-volatile storage technology, the aggressive scaling aiming at reducing the cost per bit has recently brought the floating-gate storage concept to its technological limit. In fact, data retention and reliability of floating-gate based memories are related to the thickness of the gate oxide, which becomes thinner and thinner with increasing downscaling. The above limit has pushed the semiconductor industry to invest on alternatives to Flash memory technology, such as magnetic memories, ferroelectric memories, and phase change memories (PCMs) (Geppert, 2003). The last technology is one of the most interesting candidates due to high read/write speed, bit-level alterability, high data retention, high endurance, good compatibility with CMOS fabrication process, and potential of better scalability. However, it still requires strong efforts to be optimized in order to compete with Flash technology from the cost and the performance points of view.

In PCMs, information is stored by exploiting two different solid-state phases (namely, the amorphous and the crystalline phase) of a chalcogenide alloy, which have different electrical resistivity (more specifically, the resistivity is higher for the amorphous, or RESET, phase and lower for the crystalline, or SET, phase). Phase transition is a reversible phenomenon, which is achieved by stimulating the cell by means of adequate thermal pulses induced by applying electrical pulses. Reading the resistance of any programmed cell is achieved by sensing the current flowing through the chalcogenide alloy under predetermined bias voltage conditions. The read window, that is, the range from the minimum (RESET) to the maximum (SET) read current, is considerably wide, which allows safe storage of an information bit in the cell and also opens the way to the multi-level approach to achieve low-cost high-density storage. ML storage consists in programming the memory cell to one in a plurality of intermediate resistance (i.e., of read current) levels inside the available window, which allows storing more than one bit per cell (the number of bits that can be stored in a single cell is $n = log_2 m$, where m is the number of programmable levels). The programming power and the read window depend on the electrical properties of the cell materials as well as on the architecture and the size of the memory cell. As the fabrication

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technology scales down the cell dimensions, new challenges arise to accurately program the cell to intermediate states and discriminate adjacent resistance levels.
In this work, we investigate the impact of technology scaling down on both the program and the read operation by means of a simple analytical model which takes the electro-thermal behavior of the PCM cell and the phase change phenomena inside the chalcogenide alloy into account.

2. Working principle of the PCM cell

The working principle of a PCM cell relies on the physical properties of chalcogenide materials, typically $Ge_2Sb_2Te_5$ (GST), that can switch from the amorphous to the crystalline phase and vice versa when stimulated by suitable electrical pulses. Basically, a PCM cell is composed of a thin GST film, a resistive element named heater (*TiN*), and two metal electrodes, i.e., the top electrode contact (TEC) and the bottom electrode contact (BEC). Only a portion of the GST layer, which is located close to the GST-heater interface and is referred to as active GST, undergoes phase transition when the PCM cell is thermally stimulated. In particular, in this work we focus our attention on the Lance heater geometry (Pellizzer et al., 2006), which is essentially composed of a thin layer of GST alloy and a pillar-shaped heater, as shown in Fig. 1. In the reference Lance heater cell implemented in the 90 *nm* technology node, the GST thickness t is 70 *nm*, the GST-heater contact area A is 3000 nm^2, and the heater height h is 180 *nm*.
The typical V-I characteristic of the PCM cell in the amorphous (RESET) and the crystalline (SET) state is shown in Fig. 2. Consider the case of a cell in its full-SET state: the differential resistance of the cell decreases as the applied voltage increases. This effect is due to the contribution of the crystalline GST to the cell resistance. In fact, the crystalline GST resistivity decreases with increasing electrical field inside the material.

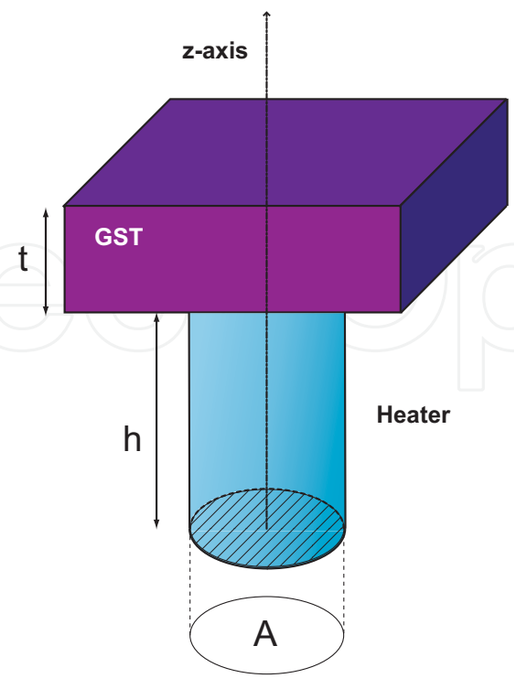

Fig. 1. Conceptual scheme of a PCM Lance heater cell.

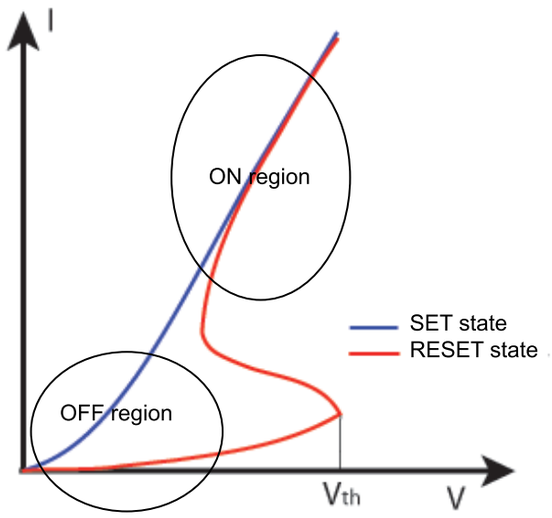

Fig. 2. V-I curve of a PCM device in the SET and the RESET state.

The V-I curve of the cell in its RESET state shows an S-shaped behavior. This effect is due to the threshold switching phenomenon (Adler et al., 1980; Ovshinsky, 1968; Pirovano et al., 2004; Thomas et al., 1976) which consists in a sudden drop of the amorphous GST resistivity as the voltage across the PCM cell exceeds a critical value, typically referred to as threshold voltage, V_{th}. Thus, when low-amplitude voltage pulses are applied to the cell, a low current flows through the device, which is in its high-resistance state (OFF region in Fig. 2). On the other hand, when a high-amplitude voltage pulse is applied to the cell, threshold switching takes place and the device shows a much lower resistance (ON region in Fig. 2). It can be noted that the V-I curves of the cell in the two states (SET and RESET) are almost superimposed in the ON region, while they are substantially different in the OFF region. Thus, readout must be carried out by operating the cell in the OFF region. Typically, a predetermined read voltage is applied to the cell and the current flowing through the device, referred to as read current, is sensed (current sensing approach). The read voltage must be low enough to avoid unintentional modification of the cell contents due to the read pulse. On the other hand, writing is carried out by operating the cell in the ON region, in order to provide the device with enough energy to induce phase change. Since phase transitions are thermally assisted, in PCM devices Joule heating is exploited to raise the temperature inside the chalcogenide material to the required value. The crystalline-to-amorphous phase transition is obtained by applying a high-amplitude electrical pulse to the cell so as to bring the temperature of the active GST material above the melting point T_m (about 600 °C) (Peng et al., 1997), and then quickly cooling the memory cell, in order to freeze the GST material into a disordered (i.e., amorphous) structure. A pulse duration on the order of few tenths of ns is sufficient (Weidenhof et al., 2000). The amorphous-to-crystalline phase transition is obtained by applying an electrical pulse with a lower amplitude and a longer time duration. In this case, the amorphous material is heated to a temperature below the melting point but above the crystallization temperature, that is the temperature necessary to activate the crystallization process in the required time scale (typically an the order of 100 ns). This way, the thermal energy is able to restore the crystalline lattice, which is a minimum-energy configuration. Typical electrical pulses for SET and RESET operations are shown in Fig. 3.

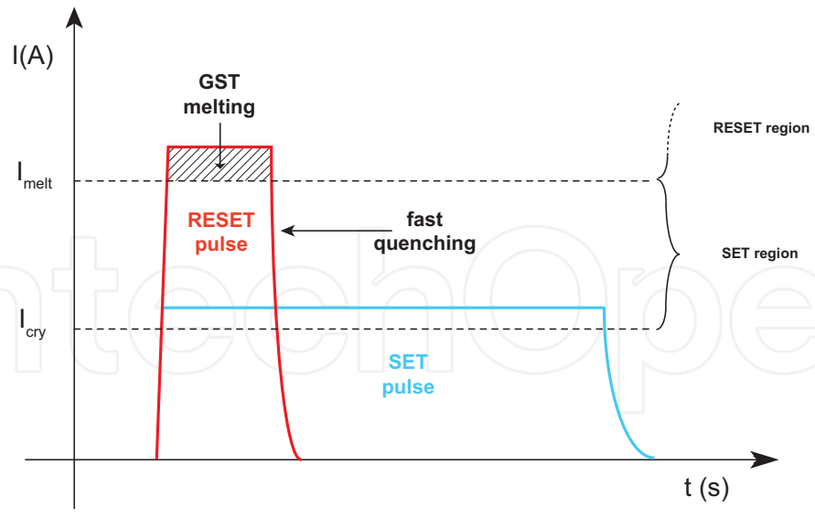

Fig. 3. Standard pulses for bi-level PCM programming.

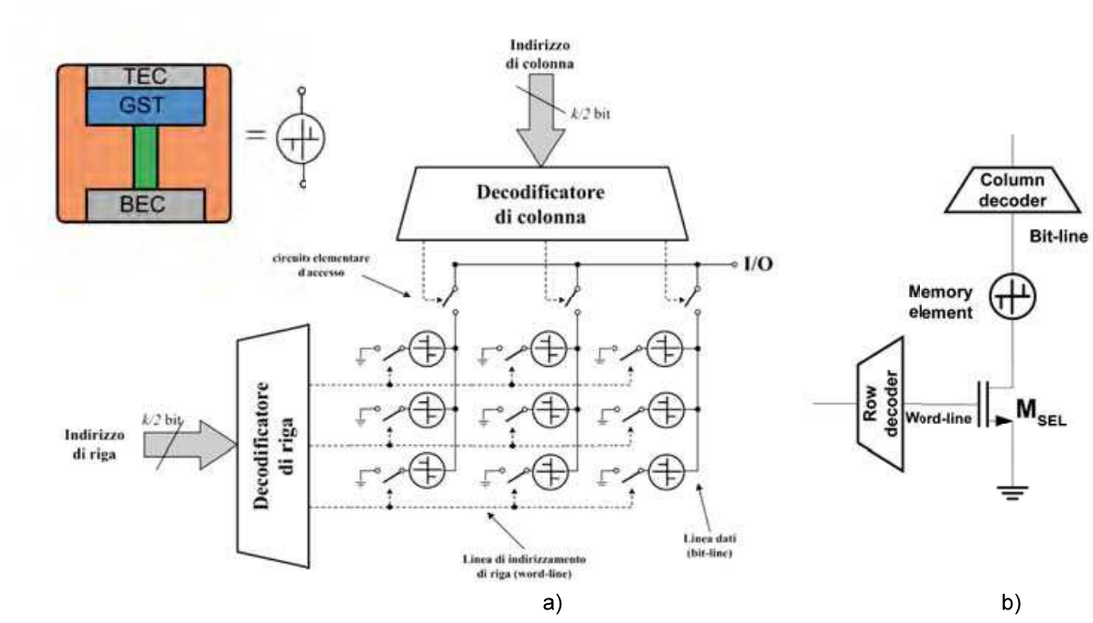

Fig. 4. Architecture of a PCM matrix (a) and schematic of the circuit used to program and read the memory cell (b). Transistors M_{SEL} is the row select transistor.

A PCM memory chip is made of a large number of PCM cells organized in a bi-dimensional array. As opposed to the case of Flash memories, in which the elementary storage consists of a floating-gate transistor, the PCM memory cell is a programmable resistor and, hence, is a two-terminal device. For this reason, a NOR type architecture is adopted (Fig. 4a). As shown in Fig. 4b, each memory cell consists of a PCM storage element connected to a selection transistor M_{SEL} which can be either an MOS or a bipolar device. The gate or the base of all

select transistors of the same row are connected to the same word-line, while the TECs of the PCM cells belonging to the same column are connected to the same bit-line. The memory cell is selected by means of row and column decoders that generate the electrical control signals required for read and write operations.

3. Programming operation

We analyzed first the impact of technology scaling on the programming operation, focusing our attention on the electical power (hereinafter referred to as programming power). The maximum programming power is obviously required by the RESET operation, where the highest temperatures are needed to melt the active GST volume. The RESET pulse duration must be higher than the minimum required time for melting \cite{Weidenhof00}, while the cooling time must be short enough to prevent the crystallization process from taking place. The minimum current required to melt a portion of the active GST layer is referred to as melting current, I_m. When the current flowing through the memory cell during a write operation is higher than I_m, the obtained RESET resistance increases with the amplitude of the current pulse. In fact, the maximum temperature inside the cell increases with the pulse amplitude, thus leading to the amorphization of a larger GST volume.

The maximum temperature reached inside a Lance heater cell of given sizes can be estimated by means of an approximated electro-thermal model. In general, the temperature increase in the active GST volume is due to the current flow both through the heater (heater heating) and through the GST layer itself (GST self-heating). Nevertheless, GST self-heating can be neglected when considering high-amplitude RESET pulses. In fact, the resistance of the GST layer (both in the crystalline and in the amorphous state) is negligible with respect to the heater resistance due to high-field effects (the PCM cell is operated in the ON region). Thus, in this case we can estimate the temperature profile inside the PCM cell by considering only the Joule power generated inside the heater when a current I flows through the cell. We assume, for simplicity, a cylindrical geometry of the heater and calculate the temperature along the cell axis. The power generated in a volume $A\delta\tilde{z}$ located at a distance $\tilde{z}$ from the heater-BEC contact is equal to $\delta Q = \frac{I^2\rho_h}{A}\delta\tilde{z}$, ρ_h being the heater electrical resistivity, and contributes to the temperature increase ΔT at the heater-GST interface with a term δT given by

$$\delta T = \left[(R_{th,GST} + R_u(\tilde{z})) \,||\, R_d(\tilde{z}) \right] \frac{R_{th,GST}}{R_{th,GST} + R_u(\tilde{z})} \delta Q, \tag{1}$$

where $R_u(\tilde{z}) = \frac{h-\tilde{z}}{\kappa_h A}$ and $R_d(\tilde{z}) = \frac{\tilde{z}}{\kappa_h A}$ (κ_h being the thermal conductivity of the heater material) are the heater thermal resistance from the coordinate $\tilde{z}$ to the heater-GST contact and to the heater-BEC contact, respectively, and $R_{th,GST}$ is the equivalent thermal resistance of the GST layer.

By integrating Eq. (1) along the cell axis from the BEC-heater contact ($\tilde{z}$ = 0) to the heater-GST contact ($\tilde{z}$ = h), we obtain the temperature T at the interface:

$$T = \frac{I^2 \rho_h h}{A} \cdot \frac{R_{th,GST} R_{th,h}}{2(R_{th,GST} + R_{th,h})} + T_0 \tag{2}$$

$$= Q_J \frac{1}{2} (R_{th,GST} \parallel R_{th,h}) + T_0 \tag{3}$$

In the above equations, T_0 is room temperature, $Q_J = \frac{I^2 \rho_h h}{A}$ is the Joule power delivered to the cell during the RESET pulse, and $R_{th,h}$ the thermal resistance of the heater, which can be expressed as $\frac{h}{\kappa_h A}$.
From Eq. (2), taking the expression of $R_{th,h}$ into account, I_m is given by

$$I_m = \sqrt{2 \cdot \frac{(T_m - T_0)}{\rho_h k_h} \frac{(R_{th,GST} + R_{th,h})}{R_{th,GST} R_{th,h}^2}}. \tag{4}$$

In order to estimate the dependence of $R_{th,GST}$ on the geometrical features of the memory cell, we simulated the temperature profile along the cell axis inside the GST layer (Fig. 5a). Fig. 5b shows the simulation results for different values of the GST layer thickness obtained with our previously proposed 3D model (Braga et al., 2008). It can be noticed that the temperature decreases almost linearly inside the GST layer with increasing distance from the GST-heater contact. Moreover, the accuracy of the linear approximation increases as the ratio between the GST layer thickness and the heater radius decreases. Since this behavior suggests that heat flow inside the GST is substantially directed along the cell axis, from the heater-GST interface along the cell axis, a reasonable approximation for the thermal resistance of the GST layer is $R_{th,GST} = \frac{t}{\kappa_{GST} A}$, where κ_{GST} is the thermal conductivity of the GST. Thus, we can rewrite Eq. (4) as

$$I_m = \frac{A}{h} \sqrt{2 \cdot \frac{(T_m - T_0)}{\rho_h} \left(\kappa_h + \kappa_{GST} \frac{h}{t} \right)}. \tag{5}$$

As highlighted by Eq. (5), the melting current depends on the ratios $\frac{A}{h}$ and $\frac{h}{t}$.
Due to fabrication process constraints, heater geometries with a high aspect ratio (i.e., geometries having a high ratio between the GST-heater contact diameter and the heater height), may not be easily manufacturable. Several fabrication solutions have been proposed to overcome lithographic limits and, thus, realize heater structures with minimized contact area (Lam, 2006; Pirovano et al., 2008). In the following, we will consider heater geometries with a high aspect ratio with the purpose of investigating the scaling perspective, even if they may require advanced fabrication techniques. Given a scaling factor $\epsilon < 1$, I_m turns out to be proportional to ϵ in the case of isotropic scaling, where all the linear dimensions are scaled by the same amount, while $I_m \propto \epsilon^2$ in the case of shrinking, where only planar dimensions are scaled. The comparison of melting current reduction in the cases of isotropic scaling and shrinking is shown in Fig. 6.
In order to compare PCM cells having different dimensions, we chose to consider the full-RESET state to be achieved when the maximum temperature inside the PCM cell reaches a

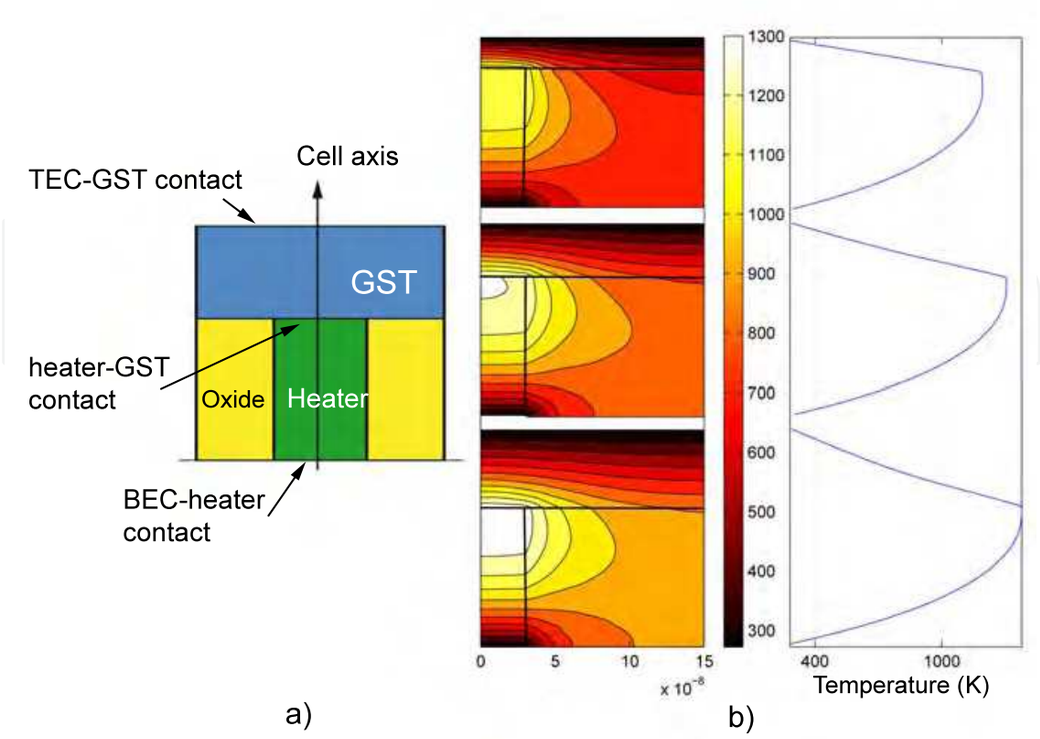

Fig. 5. Cell structure (a) and simulated temperature Maps inside a Lance heater PCM cell with different values of GST layer thickness: 40 nm, 70 nm, and 100 nm (b). Notice that the temperature profile is almost linear inside the GST layer. The maps were obtained by means of our 3D electro-thermal model (Braga et al., 2008).

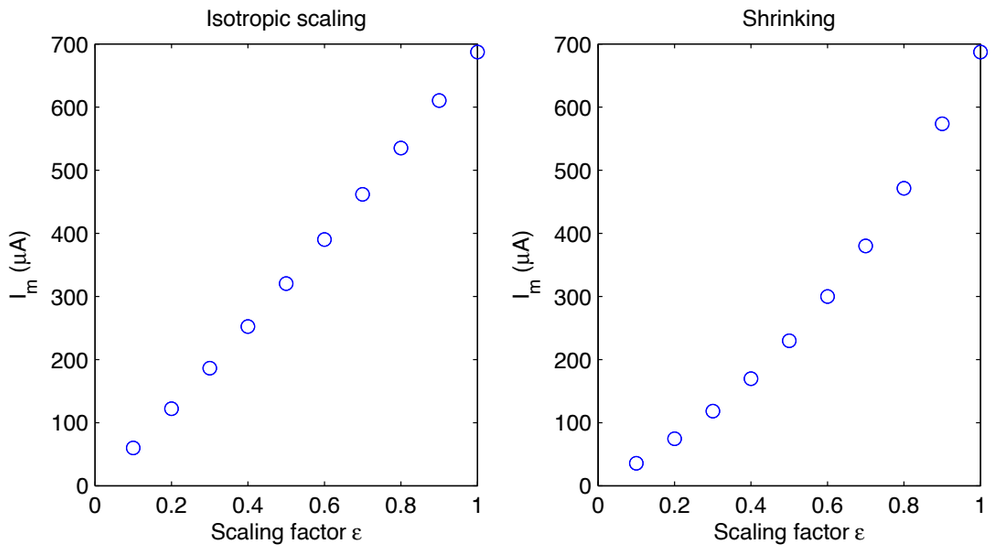

Fig. 6. Melting current reduction in the case of isotropic scaling (left) and shrinking (right). The dimensions are scaled with respect to a reference lance heater cell realized in 90 nm technology

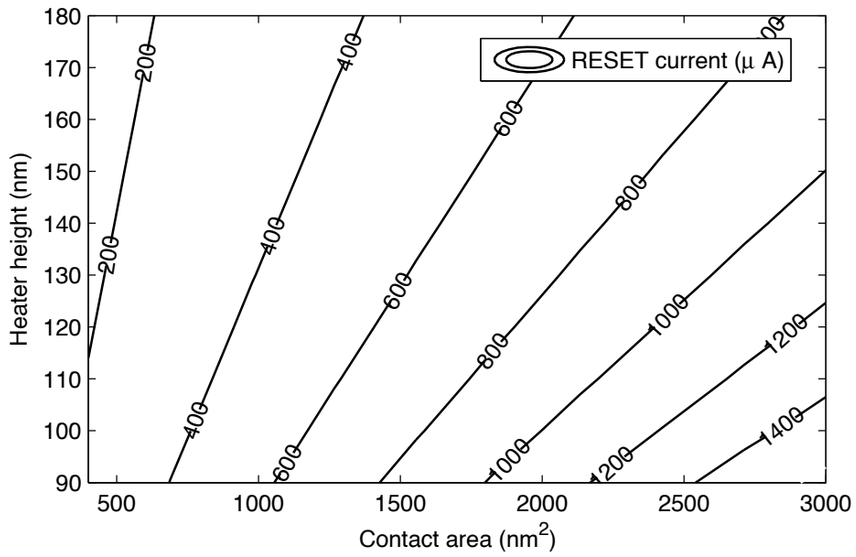

Fig. 7. Map of the RESET current as a function of the GST-heater contact area and the heater height (the GST layer thickness was set to 70 nm).

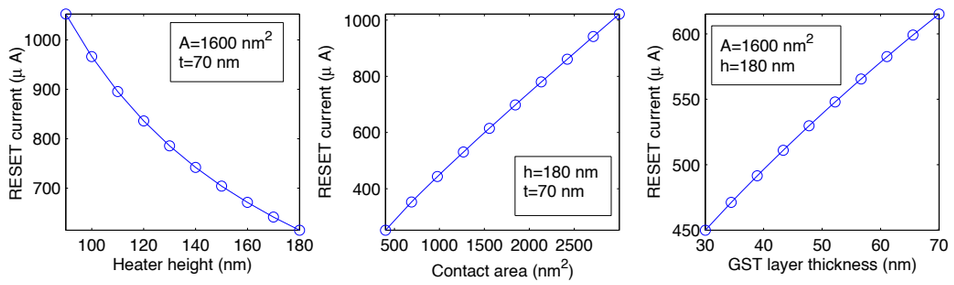

Fig. 8. RESET current dependence on the geometrical parameters of the memory cell.

predetermined value, T_{RST}, which is obtained with a current pulse of amplitude I_{RST}. Typically, I_{RST} is 50% higher than I_m. Different cells require different pulse amplitudes (I_{RST}) to reach T_{RST}, due to the different values of the electrical and the thermal resistance of the device. The dependence of the RESET current on cell sizes obtained by means of Eq. (4) is sketched in Fig. 7 and Fig. 8. The reduction of the heater height leads to a significant increase of I_{RST} due to the decrease of the Joule power and heater thermal resistance. On the contrary, the reduction of the contact area only, that is the shrinking approach, leads to a linear decrease of the RESET current, due to the increase of the Joule power and the thermal resistance of the cell. The same behavior is obtained when considering the scaling of the GST layer thickness.

The values of the electrical and thermal properties used in the above simulations are summarized in Tab. 1. For simplicity, the field dependence of the crystalline GST resistivity was neglected. In order to validate the described analytical compact model, we compared the temperature profiles along the cell axis obtained with this model and our 3D finite-element model (Fig. 9).

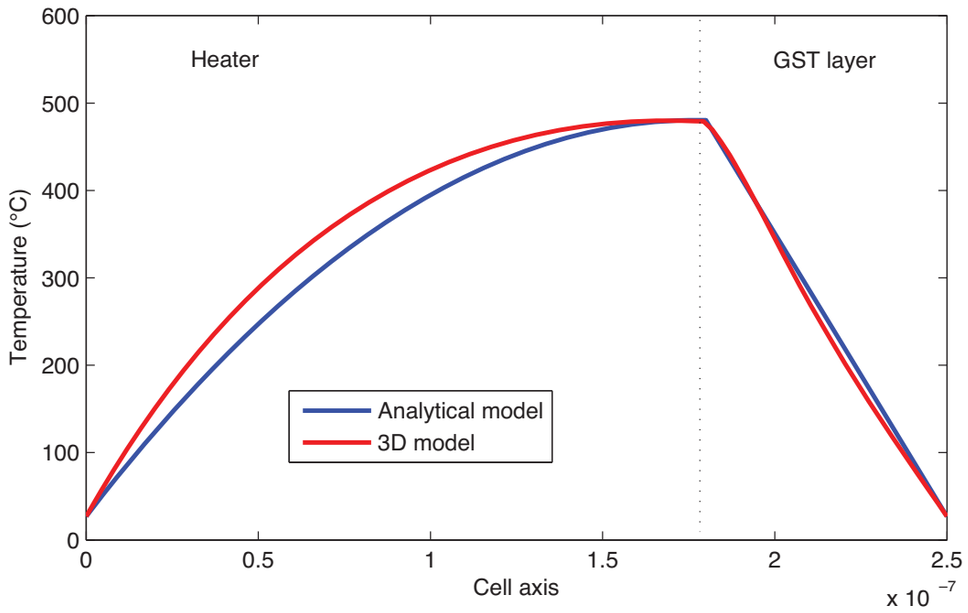

Fig. 9. Comparison of the thermal profile along the cell axis obtained by means of the analytical model and the 3D finite-element model.

Heater thermal conductivity	κ_h	$36\ \frac{W}{m^{\circ}C}$
GST layer thermal conductivity	κ_{GST}	$0.5\ \frac{W}{m^{\circ}C}$
Heater electrical resistivity	ρ_h	$30\ \mu\Omega m$
Cryst. GST electrical resist.	ρ_C	$0.1m\ \Omega m$
Amorph. GST electrical resist.	ρ_A	$10m\ \Omega m$

Table 1. Electrical and Thermal Properties of Cell Materials–

A good agreement is observed especially inside the GST layer. The slight temperature disagreement inside the heater is ascribed to the inhomogeneous heat flow in the material that surrounds the heater. To take this thermal evacuation contribution into account, the value of κ_h used in the compact model was set higher than the actual physical value.

4. Read operation

The GST layer undergoes crystalline to amorphous phase transition in the region where the temperature exceeds the melting point. As pointed out above, the temperature profile along the cell axis inside the GST decreases almost linearly with the distance from the GST-heater interface. By approximating the thermal profile inside the GST along the cell axis with a straight line, we derived the analytical expression for the thickness of the amorphous cap x_a obtained when a full-RESET pulse is applied to the cell:

$$x_a = t\frac{(T_{RST} - T_m)}{T_{RST} - T_0}. \tag{6}$$

Thus, the thickness of the amorphous cap obtained by means of the RESET operation is a fraction $f = \frac{(T_{RST} - T_m)}{T_{RST} - T_0}$ of the GST layer thickness (Braga et al., 2009). The volume of amorphous GST determines the value of the GST resistance in the RESET state and, thus, the lower edge of the read window. Since the temperature gradient is much higher along the cell axis than along the other two axis, the ratio between the thickness and the width of the amorphous cap is quite high, thus allowing us to estimate the amorphous GST resistance in the full-RESET state as

$$R_{RST} = \rho_A \frac{ft}{A} + R_h \approx \rho_A \frac{ft}{A}, \tag{7}$$

where ρ_A is the amorphous GST resistivity and R_h has been neglected since it is much lower than the resistance of the GST layer after the full-RESET pulse.
In order to estimate the cell resistance in the full-SET state, by neglecting the current spread inside the crystalline GST, we can write:

$$R_{SET} = \frac{\rho_C t}{A} + R_h, \tag{8}$$

where ρ_C is the resistivity of crystalline GST.
When considering the current sensing approach, we can calculate the minimum and the maximum read current:

$$I_{rd,min} = \frac{V_{read}}{R_{RST}}, \tag{9}$$

$$I_{rd,max} = \frac{V_{read}}{R_{SET}}, \tag{10}$$

where V_{read} is the amplitude of the read voltage. V_{read} must be lower enough to avoid unintended programming during readout. The read current window is affected by both the scaling of V_{read} and the geometrical scaling strategy. It must be pointed out that when V_{read} is kept constant (this approach will be referred to as constant voltage approach), the electrical field E_{read} during readout inside the amorphous GST increases as the size of amorphous cap scales ($E_{read} \approx \frac{V_{read}}{ft}$), thus impacting on the electrical resistivity of the amorphous GST. In this case, in order to calculate the read current, the exponential dependence of the amorphous GST resistance on the electrical field must be taken into account (Ielmini & Zhang, 2007; Kim et al., 2007). For a given PCM cell in the RESET state, neglecting the heater resistance, we have

$$R_{RST} \propto e^{-\frac{E_{read}}{E_{ref}}}, \tag{11}$$

where E_{ref} is the electrical field which activates the electrical resistivity inside the amorphous GST. The value of V_{read} must be chosen so as to ensure that the PCM device is operated in the read region (OFF zone) and the electrical field during readout is below the critical switching field for every considered cell size. In this respect, we chose $V_{read} = 0.3\ V$ and calculated the cell resistance and the read current for both the SET and the RESET state. E_{ref} was set to $30M\ V/m$ (Buckley & Holmberg, 1974).

Several studies (Adler et al., 1980; Buckley & Holmberg, 1974) have shown that V_{th} decreases linearly with the amorphous GST thickness which, in our case, is a fraction of the GST layer thickness. Then, we can scale V_{read} and t consistently, so as to keep the electrical field during readout inside the amorphous GST roughly constant and below the critical value for threshold switching (Buckley & Holmberg, 1974). This scaling approach will be referred to as constant field scaling.

It can be noticed from the simulation results in Fig. 10, that constant voltage approach leads to an increase of the SET read current as the thickness of the GST layer decreases, due to the reduction of the SET resistance. Moreover, a significant increase of the minimum current (RESET state), mainly due to the dependence of amorphous GST resistivity on the electrical field, is apparent. The increase of the RESET read current depends on E_{ref} and is affected by the value of V_{read}. Rather different results are obtained when considering constant

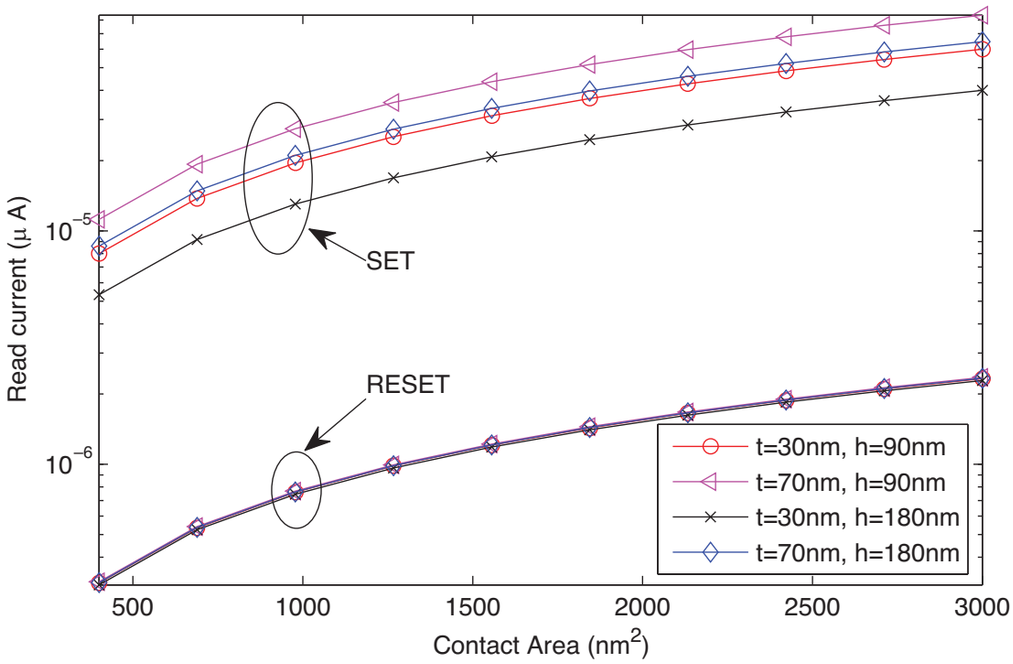

Fig. 10. Constant voltage approach: read current as a function of the contact area A for different values of GST layer thickness t and heater height h. The read voltage is assumed to be 0.3 V.

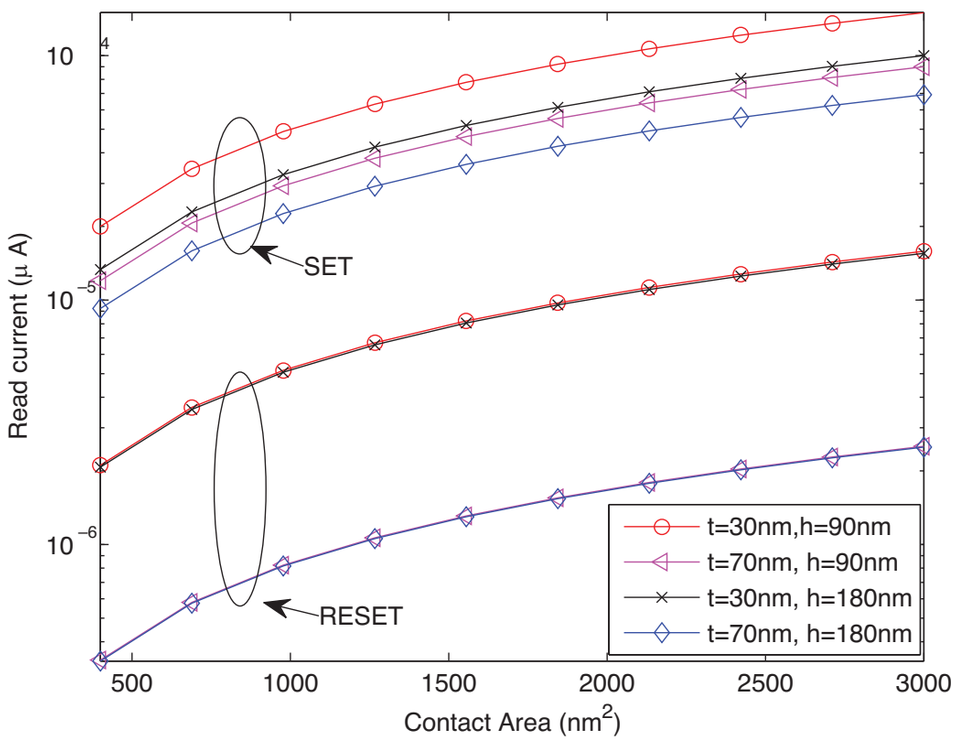

Fig. 11. Constant field approach: read current as a function of the contact area A for different values of GST layer thickness t and heater height h. The read voltage is assumed to be proportional to the thickness of the GST layer (V_{read}= 0.3 V @ t=70 nm).

field scaling. In this case, the current read window scales as shown in Fig. 11. The RESET current is almost independent on t and h, since the read voltage and the cell resistance roughly scale by the same factor. As opposite to the previous approach, in constant field scaling the SET read current decreases with decreasing t due to the fact that R_{SET} is less affected than V_{read} by the reduction of t. The dependence of I_{read} on the contact area is qualitatively similar to the constant voltage case. In both approaches, I_{read} progressively decreases with decreasing A.

5. Conclusions

In this work, we addressed the impact of technology scaling on the performance of phase change memory cells by investigating its effects on both the programming current and the width of the read window. To this end we derived a simplified analytical model of the PCM cell electro-thermal behavior and validate it by means of a 3D finite-elements model of the PCM cell. We considered both constant field and constant voltage scaling approaches. Our study highlights the program-read tradeoffs challenges which aggressive scaling arises and provides analytical insight in the scaling mechanisms.

6. Acknowledgements

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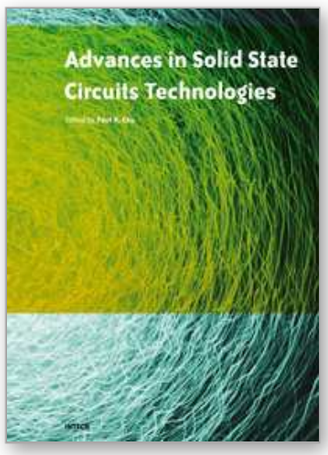

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This book brings together contributions from experts in the fields to describe the current status of important topics in solid-state circuit technologies. It consists of 20 chapters which are grouped under the following categories: general information, circuits and devices, materials, and characterization techniques. These chapters have been written by renowned experts in the respective fields making this book valuable to the integrated circuits and materials science communities. It is intended for a diverse readership including electrical engineers and material scientists in the industry and academic institutions. Readers will be able to familiarize themselves with the latest technologies in the various fields.

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