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A Time-Delay Suppression Technique for Digital PWM Control Circuit

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1. Introduction

Recently, power management has been introduced to improve the power efficiency of Micro Processing Unit (MPUs), Field Programmable Gate Array (FPGAs) and Digital Signal Processor (DSPs). The power management system includes a full operation mode, standby mode, and sleep mode. The clock frequency, core voltage and/or core current are changed in each mode accordingly. As a result, the output current of the point-of-load (POL) DC-DC converters is intermittent and has a high slew rate. A low output voltage, a large output current and a high speed response are required for the POL. In such a condition for the control circuit, highly accurate and high-speed control demands that the tolerance of the output voltage becomes internally severe, advanced by speed-up and lowering of the voltage of the MPUs, FPGAs and DSPs. A general control method is pulse width modulation (PWM) control with PID. Generally, such control circuits are composed with analog circuits and/or simple combination digital circuits.
In these days, robustness or flexible controls for versatile conditions are demanded which cannot accomplished with analog control circuit. For the control purpose, DPWM control is a one of appropriate technique (Edward Lam, Robert Bell, and Donald Ashley (2003), A.V.Peterchev and S.R.Sanders (2003), B.J.Patella, A.Prodic, A.Zirger and D.Maksimovic

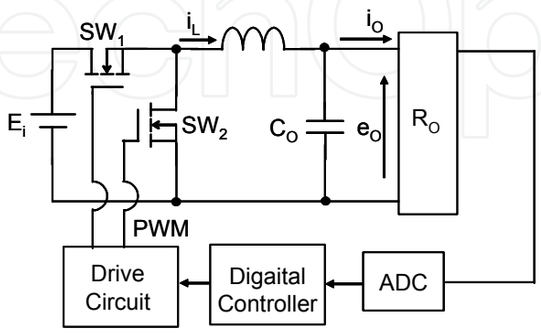


Fig. 1. Common digital control DC-DC converter.

(2004), D.Maksimovic, R.Zane, and R. Erickson (2004), S.Saggini, D.Trevisan and P.Mattavelli (2007), S.Saggini, E.Orietti, P.Mattavelli, A.Pizzutelli and Bianco(2008)).

Digital control or DPWM can accomplish robust and flexible power control with soft-tuned parameters and will become popular control technique.
Although, there are some disadvantages in cost and speed, against analog control circuit.
Especially, A/D converter circuit, which doesn't need for analog control, is the one of the key circuits which effects on cost and speed. Generally, A/D converter is located in front of digital controller as shown in Figure 1. Therefore, the transition speed of A/D converter directly effects on the response speed of the control circuit. And, the cost and speed are always trade off problem. This problem is especially serious in POL DC-DC converter which is required to design the control circuit in relatively low-cost and high speed control response. Moreover, generally, there is sample-hold circuit in front of A/D converter which degrades the response speed.
A delay in any feedback system degrades the stability and damping of the system. Especially, in DPWM, if a total of the delays described in above become larger than on-term of one switching period, a factor of A/D converter becomes Vq/Z shown in Figure 2 where Vq is a coefficient constant.
An objective of this paper is to design high speed and low cost voltage sensing circuit for DPWM control circuit for DC-DC converter. And, also real-time PID control method is proposed. In Sec. II, the details of proposed system are described. In Sec. III, the some characteristics of the system are confirmed with experimental results. Finally, in Sec. IV, the summary is described.

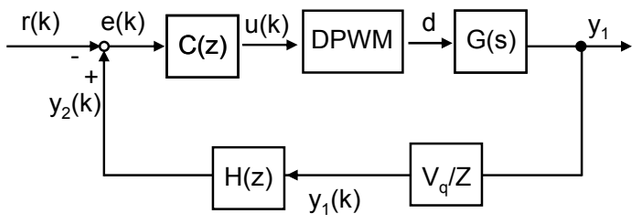


Fig. 2. Control System.

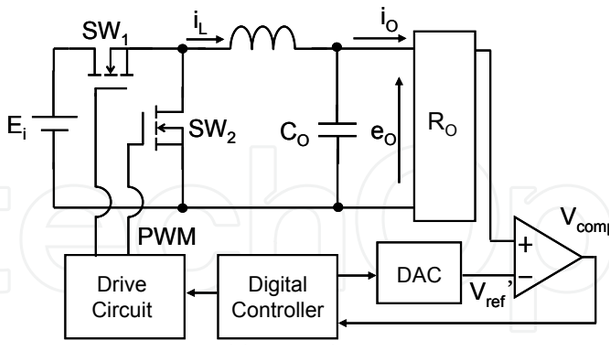
2. Proposed System

We propose a scheme of a digital control and DPWM circuit for DC-DC converter without A/D converter shown in Figs.3 and 4, respectively. In this proposed control circuit, most components are digital components. Analog components for the control circuit are essentially only D/A converter and analog comparator. Theoretical waveforms of each part are shown in Figure 5. The control circuit is composed of three major blocks.

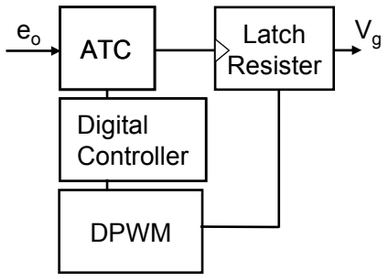
2.1 Analog-Timing Converter (ATC)

The first block is ATC block which detects the output voltage e_o and outputs the detected signal to latch register. The maximum output value of D/A converter DAC is set as a sum of the output reference voltage of DC-DC converter V_{ref} and margin $\alpha(>0)$. A digital staircase waveform data, pre-stored in memory Memory1, is output to DAC synchronized with a system clock, and converted analog staircase waveforms V_{ref}' is compared with e_o. As soon as $V_{ref}' > e_o$, the comparator outputs high.

2.2 PID Control with Look-up Table



(a) Total Systems.



(b) Control blocks.

Fig. 3. Proposed DPWM Control DC-DC converter

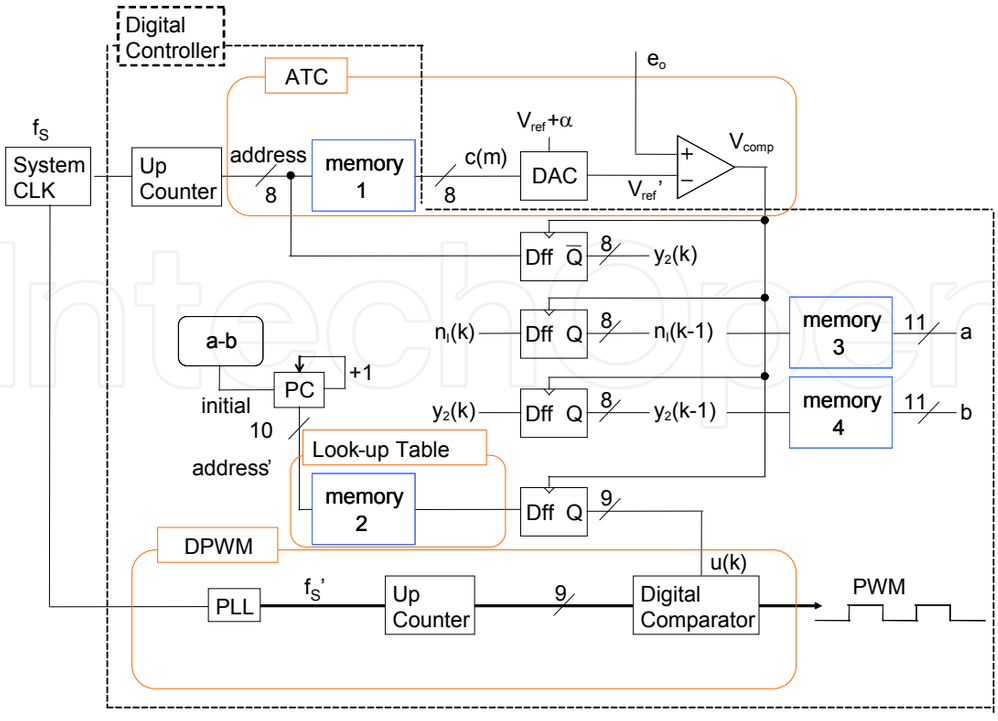


Fig. 4. Proposed digital control circuit.

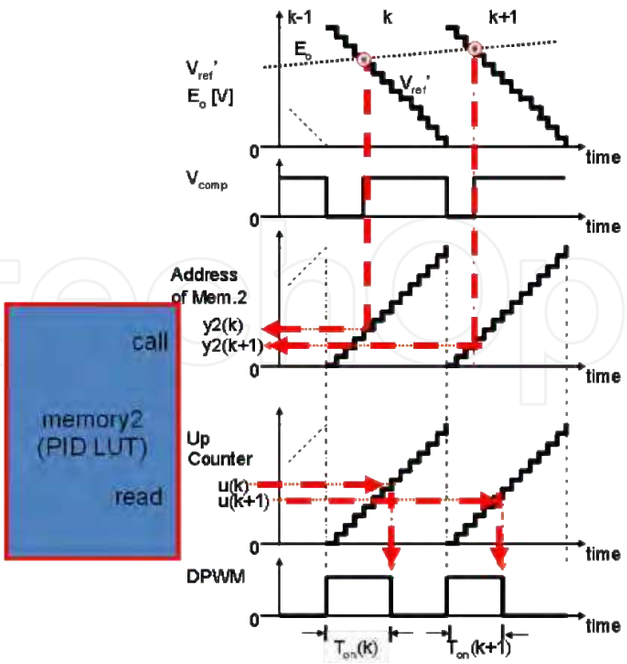


Fig. 5. Theoretical waveforms.

$u(k)$ which is output from Memory2 is calculated by general PID digital control laws as

$$u(k) = u_{Ref} + K_P e(k) + K_I n_I(k) + K_D \left(e(k) - e(k-1) \right) \tag{1}$$

where u_{Ref} is a reference value of $u(k)$, $e(k)$ is an digitalized error value between r which is digitalized reference voltage V_{ref} in switching term k, and $n_I(k)=n_I(k-1)+e(k)$(G. F. Franklin, J. D. Powell and M. L. Workman (1997)). K_P, K_I and K_D are a proportional gain, an integral gain and an derivative gain, respectively.
Equation (1) can be transformed to

$$\begin{aligned} u(k) &= u_{Ref} - (K_P + K_I) r \\ &+ A\{ y_2(k) + \frac{K_I}{A} n_I(k-1) - \frac{K_D}{A} y_2(k-1) \} \end{aligned} \tag{2}$$

where $A = K_P + K_I + K_D$ and $y_2(k)$ is digitalized output voltage e_o in switching period k.
In Figure 4,

$$a = \frac{K_I}{A} n_I(k-1) \tag{3}$$

,

$$b = \frac{K_D}{A} y_2(k-1) \tag{4}$$

.

Memory3 and Memory4 store a and b, respectively.

In Eq. (2), $a-b$ in the term k is pre-calculated in the term k-1 and the obtained value becomes the initial value of programmable counter PC of the term k. And, *address'* which indicates address of Memory2 is incremented with system clock and $u(k)$ is called from Memory2, simultaneously.

$$address'=y_2(k)+a-b \quad . \tag{5}$$

From (2) and (5),

$$u(k)=u_{Ref}-(K_P+K_I)r+A\{adress'\} \quad . \tag{6}$$

Therefore, $u(k)$ is determined as soon as $y_2(k)$ is detected.

2.3 DPWM

In this system, on-term $T_{on}(k)$ of DPWM signal is decided by $u(k)$, which is normalized $T_{on}(k)$, and system clock frequency f_S'as

$$T_{on}(k)=u(k)/f_s' \tag{7}$$

$u(k)$ is decided by latched value of Memory2.
In parallel with the processing of ATC block, the $u(k)$ is called with system clock and latched by ATC output as trigger.

3. Sensing Resolution

3.1 Resolution Increasing

As described in previous section, all blocks are synchronized with only one clock source. From this advantage, all blocks are modified in easy way.
In this paper, voltage sense resolution increase of output voltage is proposed.
In proposed system, R-2R ladder type D/A converter is used. The output voltage is set between $V_{ref}^{+}(=V_{ref}+\alpha)$ and V_{ref}^{-}. Therefore,

$$V_{ref}'=\frac{c(m)}{2^n}(V_{ref}^{+}-V_{ref}^{-})+V_{ref} \tag{2.8}$$

where n is bits. Also, least significant bit (LSB) voltage a_{LSB} becomes

$$a_{LSB}=\frac{1}{2^n}(V_{ref}^{+}-V_{ref}^{-}) \tag{2.9}$$

In this paper, V_{ref}^{-} is set to V_{ref} / 2. Almost n+1 bits resolution can be realized by n bits digital system as shown in Table 1.

3.2 Sensing Time Delay

With this method, sensing time is increased. To avoid the time delay, the reference voltage waveform data pre-set in memory1 V_{ref}' is modified as shown in Figure 6.

	bits	Reference voltage		LSB voltage value
	n[bit]	V_{ref}^{+}[V]	V_{ref}^{-}[V]	a_{LSB}[mV]
[3]	8	1.7	0	6.64
[3] with 9bits	9	1.7	0	3.32

Table 1. Relations between parameter and quantization error of D/A Converter

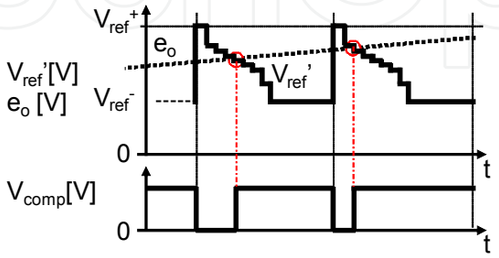


Fig. 6. Modified reference voltage waveforms

4. Prototype Circuit Experiments

4.1 Experimental Conditions

Some experiments are performed to verify the scheme. The proposed controller with prototype circuit is shown in Figure 7. The digital controller part is designed in FPGA Altera Stratix with Quartus II. 149 logic elements and 1 PLL block are used. All mem-ory blocks, Memory1, Memory2, Memory3 and Memory4, are including in the logic elements.Intersil CA3338MZ is used as 8bit DAC. National Semiconductor LMV7219 is used as an analog comparator.

The DC-DC converter topology is basically same as Figure 3. The experimental conditions are shown in Table 2.

4.2 Experimental Results

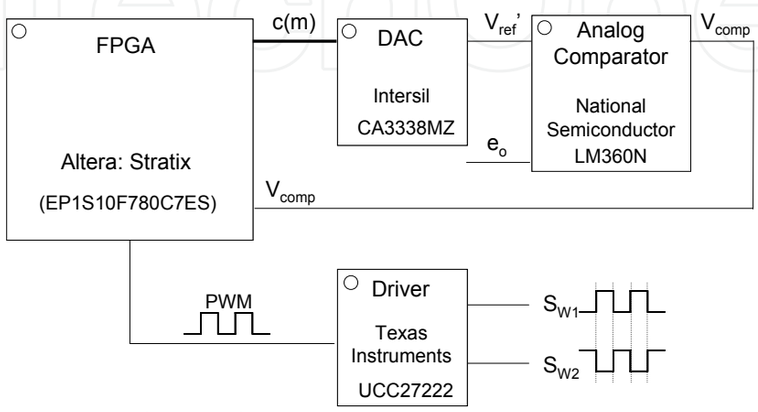


Fig. 7. Prototype proposed control circuit.

The static experimental waveforms are shown in Figure 8.

From this result, it is able to confirm that the output voltage sensing is done within the on-width of PWM signal.

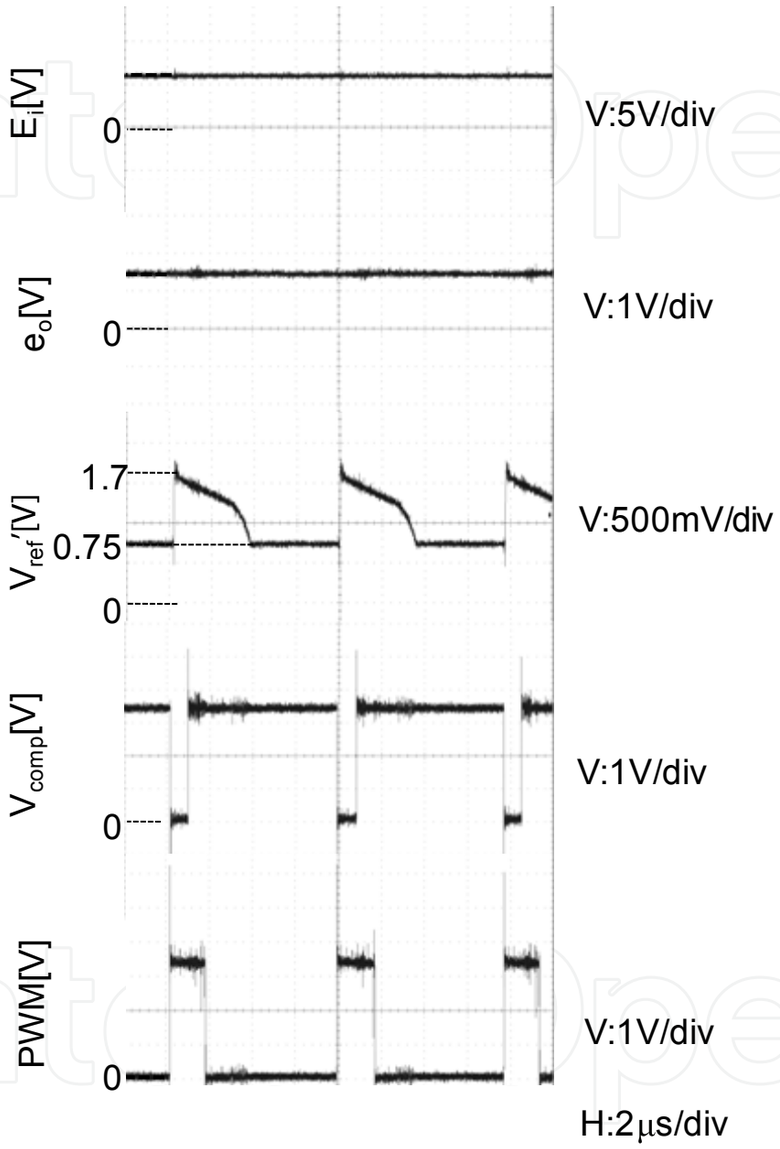
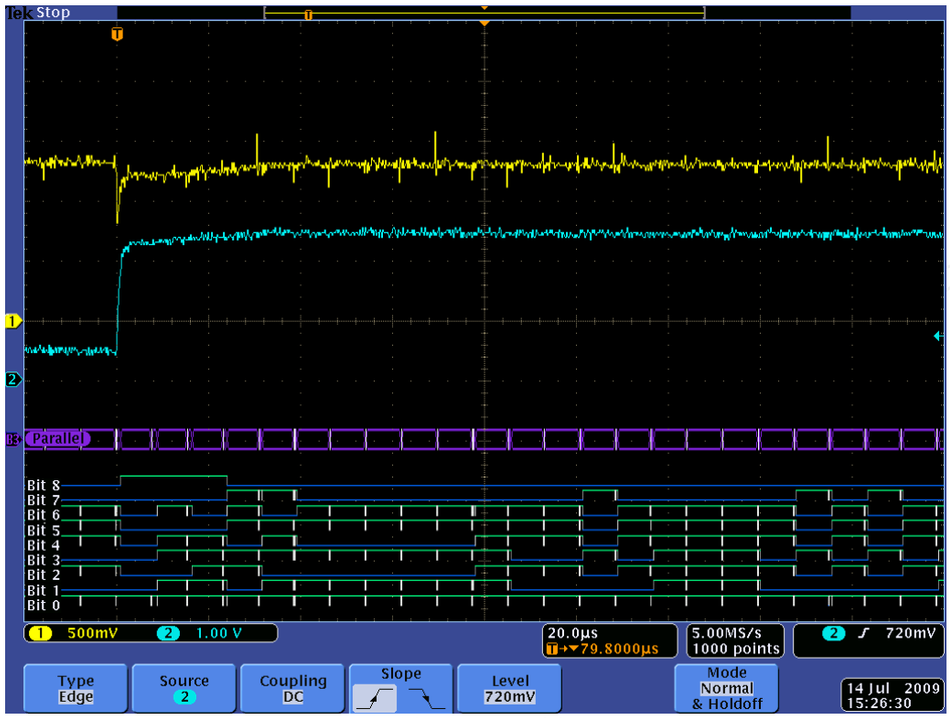


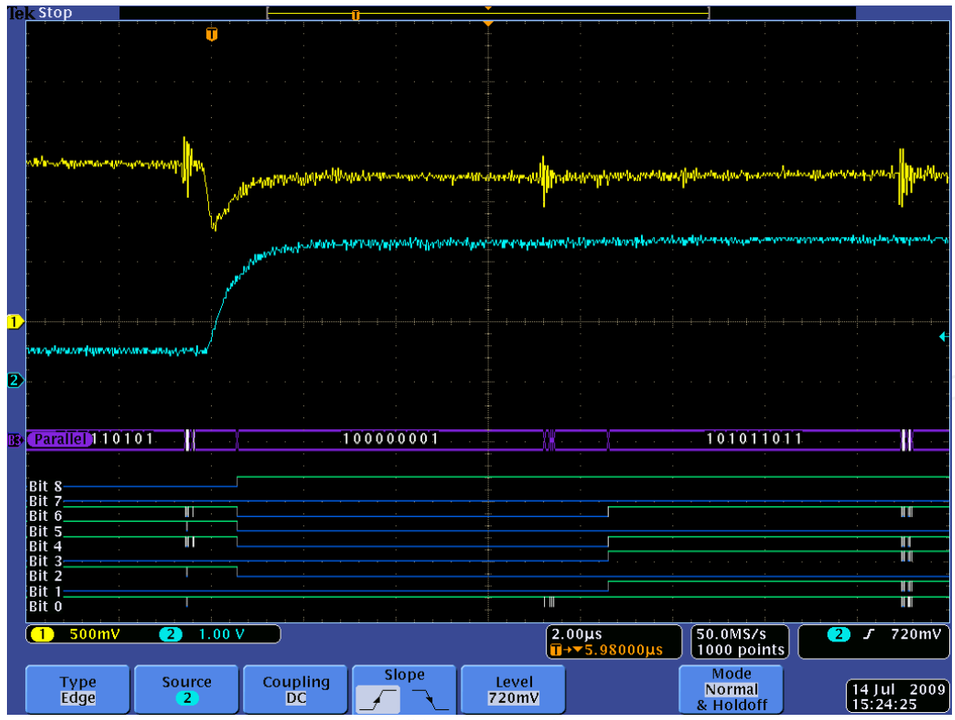
Fig. 8. Experimental waveforms

4.3 Dynamic Characteristics

Figure 9 and 10 show dynamic characteristics with load current io changing between 0.5A and 2.5A, respectively. The mixed-signal oscilloscope Textronix MSO4034 is used to measure analog and digital signal, coinstantaneously. The load current chang-ing is

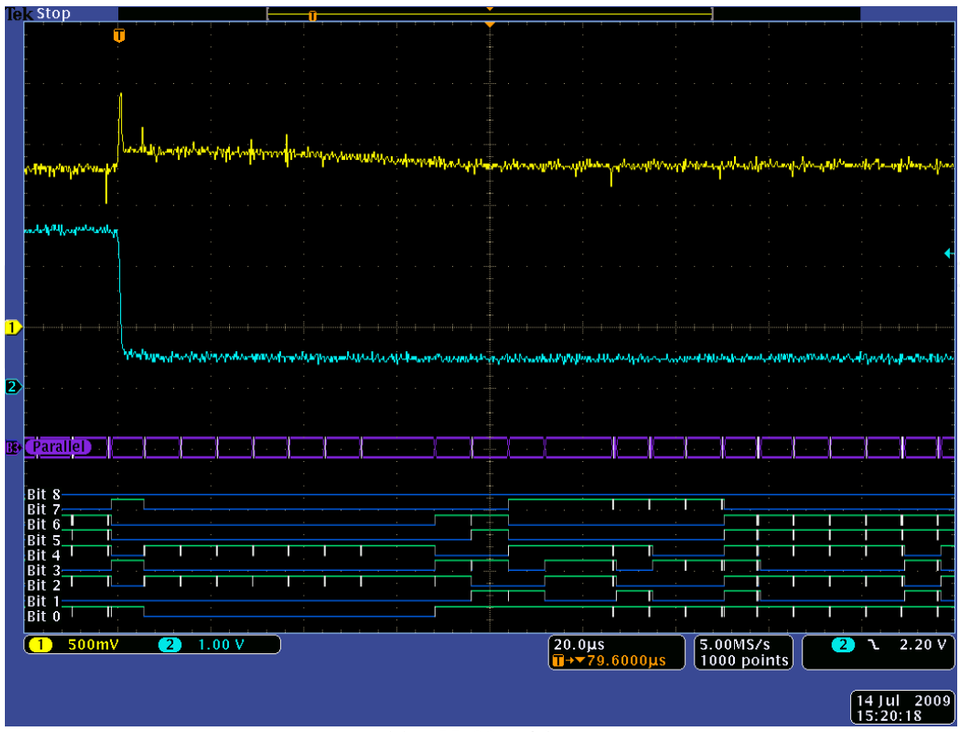


(a) H: 20µs/div.

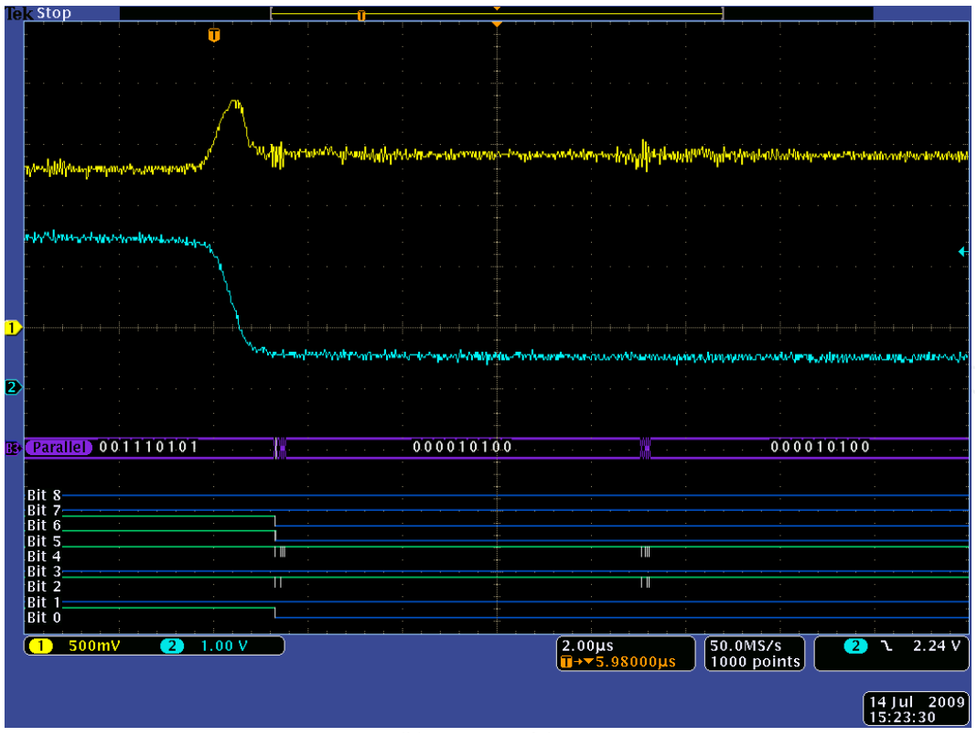


(b) H: 2µs/div.

Fig. 9. Dynamic characteristics (from 0.5A to 2.5A)



(a) H: 20µs/div.



(b) H: 2µs/div.

Fig. 10. Dynamic characteristics (from 2.5A to 0.5A).

performed with 1kHz driven power MOSFET parallely-connected to load resistance. Yellow and Blue line shows the output voltage and the output current, respectively. The 9 bits pulse waveforms shown at the bottom of Figure 9 are calculated DPWM of FPGA.
Figure 9 shows the sudden load current increasing results. From these results, after the 1μs voltage drop, the output voltage immediately recovers to the reference voltage.
Figure 10 shows the sudden load current decreasing results. From these results, after the 1μs voltage rising, the output voltage immediately recovers to the reference voltage.

5. Conclusion

This paper describes a digital PWM controller IC without A/D converters. The analog timing converter (ATC) is proposed for output voltage sensing. In this system, analog circuit are realized with an comparator and an D/A converter.

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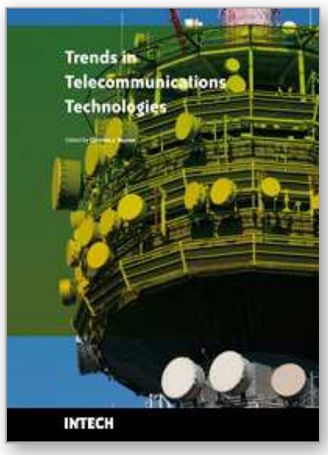

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The main focus of the book is the advances in telecommunications modeling, policy, and technology. In particular, several chapters of the book deal with low-level network layers and present issues in optical communication technology and optical networks, including the deployment of optical hardware devices and the design of optical network architecture. Wireless networking is also covered, with a focus on WiFi and WiMAX technologies. The book also contains chapters that deal with transport issues, and namely protocols and policies for efficient and guaranteed transmission characteristics while transferring demanding data applications such as video. Finally, the book includes chapters that focus on the delivery of applications through common telecommunication channels such as the earth atmosphere. This book is useful for researchers working in the telecommunications field, in order to read a compact gathering of some of the latest efforts in related areas. It is also useful for educators that wish to get an up-to-date glimpse of telecommunications research and present it in an easily understandable and concise way. It is finally suitable for the engineers and other interested people that would benefit from an overview of ideas, experiments, algorithms and techniques that are presented throughout the book.

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