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Energy Saving Drives New Approaches to Telecommunications Power System

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1. Introduction

Steady growth in the telecommunication industry providing data, voice and video is very likely to continue in the foreseeable future. This growth is supported by expansion into the new markets, especially in Asia, accelerated widespread of wireless and broadband technology, and strong demand for more efficient, power saving solutions. As the result of the growth, the telecommunication infrastructure becomes significant energy consumer and contributor to greenhouse emissions. Based on International Telecommunication Union estimation, the information and communication technology contributes 2-2.5 per cent into the worldwide greenhouse gas emissions (http://www.itu.int/themes/climate/index.html). To reduce the impact on global warming, more efficient distribution, conversion and use of electrical energy by telecommunication industry is required. Worldwide movements for energy saving and "Green power" generation and distribution, have resulted in number of voluntary initiatives and mandatory regulations by international and government organizations for increased efficiency of electronic equipment including data and telecommunication power systems. Examples of such organizations and initiatives are United States ENERGY STAR® program, German Blue Angel, Japan Environment Association, European Code of Conduct and others (http://www.energystar.gov/index.cfm?c=ent_servers.enterprise_servers; Mammano, 2006). The focus of this chapter is efficient and low power consumption DC power systems for a central office and base station of telecommunication infrastructure. According to (Fasullo et al., 2008) telecommunication industry consumes 160 Billion kWh each year, and majority of this electrical energy passes through DC power distribution system.

Telecommunication DC power systems have come long way from simple rectifier/battery system to complex switching power supplies, from centralized power to distributed architecture (Thorsell, 1990). At the same time, required tasks and functional complexity of power systems continue to grow. To effectively reduce the overall system power consumption per required functionality, all design levels from system architecture level down to each specific function and component must be optimized. This chapter limits its scope to energy saving considerations of power system at facility level, then down to power distribution in a rack, or cabinet, and finally focuses on the specific power conversion topologies and control algorithms implemented in power supplies.

At the facility level, intensive research and evaluation of 380-V DC distribution bus is reported to replace traditional 208 V (230 V) AC mains (Pratt et al., 2007; Akerlund et al., 2007). At the cabinet level, intermediate bus architecture (IBA) has become widespread to address increased requirements for supply voltage quality, accurate power sequencing, flexibility and availability of power system (Morrisson, 2002; White, 2003; Miftakhutdinov, 2008a). Currently, demand for high efficiency over wide output power range and low power consumption reshapes the telecom power distribution system once again. Typical cabinet level power system includes AC/DC front end power supply providing system bus voltage that can be –48 V, 24 V, 12 V or 130 V depending on specific system and application. The same power supply in most cases is used as a charger for the backup battery. Driven by government regulations and market demand, the telecom and server power supply is now required to be efficient over output power range from 10% (sometimes even 5%) up to 100% (http://www.energystar.gov/index.cfm?c=ent_servers.enterprise_servers).

Efficiency was always important for data and telecommunication power supply to achieve high power density and improve thermal performance. So far, only high efficiency at maximum load was required because it determines reliability, size and cost of equipment and cooling. Currently, the focus is shifted to energy saving and high efficiency over the entire output power range.

Overall, the design procedure includes power system architecture selection and identifying power conversion topologies and related control strategy. Use of the best in class components is also critical to meet the design goals. In the chapter, all these critical stages of telecom power system design are discussed in details including comparison of alternative solutions.

Optimal control algorithm is critical not only to meet static and dynamic requirements of telecom power system. It also opens new opportunities to increase the efficiency by transitioning into different optimal power saving modes depending on system conditions. Here, the flexibility, programmability and auto tuning capability of digital controllers must be weighted against the lower cost, simple, and usually faster analog control ICs. Promising control strategies along with the examples of advanced analog and digital controllers addressing new requirements for high efficiency will be provided in the chapter.

The interface between IC controller and power stage, that includes power switch drivers, current, voltage, and temperature sensing, auxiliary bias supply, has critical role and deserve careful consideration as well.

The chapter discusses requirements for telecom rectifiers and front-end server power supplies: the key functional parts of any data- and telecommunication power system.

Special attention is provided to intermediate bus converters (IBC) that are the enabling part of any IBA. The IBC requirements and parameters, popular topologies, design challengers are discussed in details. The design examples and test results of 600-W unregulated IBC converter with 48-V input and 5:1 transfer ratio are provided to illustrate and verify the recommended design approaches and solutions.

2. Strive for Efficiency and Power Saving

2.1 Energy Saving Trends and Regulations

High efficiency was always critical requirement for data and telecom power system as precondition to achieve high power density and improve thermal parameters. So far, only

the efficiency at maximum load was usually being taken into consideration. This is because the size, cost, temperature profile of components and their cooling selection is determined at the maximum output power, where power losses are the highest. However, currently the paradigm is shifted and the new requirements focus primarily on energy saving. Therefore, it is critical to have high efficiency even at mid and light loads, where, as it turned out, power system operates significant amount of time. Driven by government regulations and market demand, the data and telecommunication power supply efficiency is now specified from 10% (sometimes 5%) up to 100% of its output power range. At the same time, the power supply and entire system must not exceed the power consumption limits specified for idle operation modes. One example is ENERGY STAR®, which is a joint program of the U.S. Environmental Protection Agency and the U.S. Department of Energy. The program sets efficiency and power consumption recommendations and regulations for different types of electronic equipment. The version 1 of ENERGY STAR® Program Requirements for Computer Servers was effective starting May 15, 2009 (http://www.energystar.gov/ia/partners/product_specs/program_reqs/computer_server_prog_req.pdf). Table 1 below shows related efficiency requirements at 10%, 20%, 50% and 100% output power of single-output AC/DC and DC/DC converters.

Rated Output Power	10% Load	20% Load	50% Load	100% Load
≤ 500 W	70%	82%	89%	85%
501 – 1000 W	75%	85%	89%	85%
> 1000 W	80%	88%	92%	88%

Table 1. Efficiency requirements for single output AC/DC or DC/DC server power supply

For AC/DC Server Power Supply the ENERGY STAR® Program also defines the minimum Power Factor Coefficient as 0.9 for loads from 50% to 100%. This practically means mandatory use of active power factor corrector block in power supply. The Program also limits maximum power dissipated at Idle State to 55 W for single processor based standard server. By definition, during the Idle Operational State, the operating system and other software have completed loading and the server is capable of completing workload transactions, but not processing of any useful work. Adding redundant power supplies to the system allows extra 20 W of power per each additional power supply. Another words only 20 W power can be consumed by the power supply at no load condition.

Similar power saving programs are currently implemented or under development worldwide by government organizations like German Blue Angel, Japan Environment Association, European Code of Conduct and others (Mammano, 2006). It becomes widespread practice that large data and telecommunication providers sometimes set even stronger efficiency and power saving requirements to power system manufactures in attempt to reduce the cost of service and stay competitive.

2.2 Power System Architecture at Facility Level

To meet new efficiency and power saving requirements all system and design levels must be reviewed and optimized. These levels include general power system architecture, power stage topologies for each power conversion, optimal power stage component selection and control algorithms providing optimal and efficient operation of the entire system.

Typical power system of data center at the facility level is shown in Figure 1. Such system generates uninterruptable 208 V AC line. There is double power conversion from DC to AC in UPS and from AC back to DC in the front-end power supply.

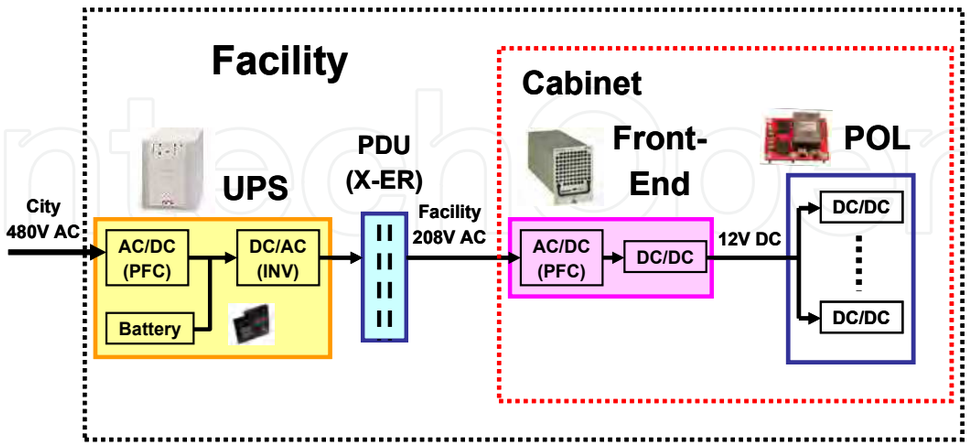


Fig. 1. Typical power system of data center

If to replace AC uninterruptable distribution power line at facility level by the DC line, as it is shown in Figure 2, more than 7% overall efficiency improvement (Pratt et al., 2007) and 10% to 30% saving in cost of operation (Akerlund et al., 2007) can be achieved.
Advantages of the power system with DC distribution bus at facility level are obvious from the power saving view however, some safety and technical questions must be resolved including certified DC power distribution units and availability of UPS with high voltage DC output. The European Standard EN 300 132-3 issued by ETSI includes DC bus up to 400 V as an option for powering telecommunication equipment, thus setting guidelines for development and use of such power architecture (ETSI, 2003).

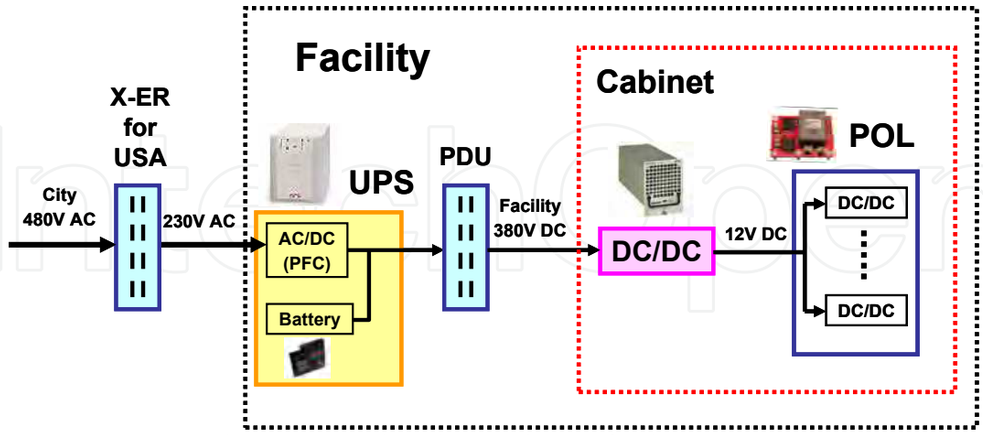


Fig. 2. Power system with 380 V DC distribution bus at facility

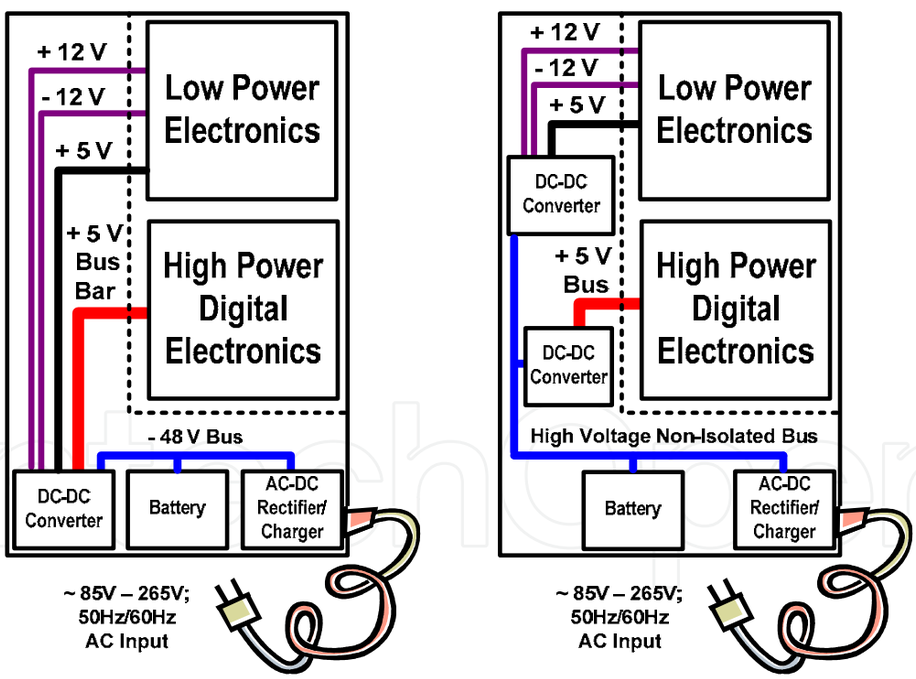
3. Evolution of Telecommunication Power System at Cabinet Level

Power distribution systems for tele- and data-communication equipment at cabinet level have undergone dramatic changes within last two decades because of fast progress of

modern digital-processing technology, requiring high quality supply voltages with specific power sequencing. significant increase in economic losses in case of service interruption was another key factor demanding highly reliable, flexible and available power system. And the most recent changes are driven by push for the efficient, "green" power with the reduced cost of ownership. The evolution of cabinet power system from centralized power to distributed power architecture (DPA) and then to the intermediate bus architecture (IBA) as subset of DPA is the focus of this section.

3.1 Centralized Power System

Originally, the only voltage needed for telecommunication electromechanical switching systems was –48 V provided by AC/DC rectifiers and back up batteries. Since 1960s, the transition from electromechanical relays to electronic semiconductor switchers added to power system the DC/DC converters generating +5 V and ±12 V from –48V supply. These centralized power supplies, typically located in the bottom of a rack or cabinet, included AC/DC front-end rectifier/charger, a power backup battery and DC/DC converter. Large and costly supply bus bars routed the required voltages to each shelf inside the cabinet, which contained replaceable line cards with switching, diagnostic and monitoring equipment. Figure 3 shows typical configuration of centralized power systems that were dominant till mid 1980s (Thorsell, 1990, Ericsson Inc., 1996)



(a) Centralized power system (b) Multilocation centralized power system

Fig. 3. Different types of centralized power system with battery backup

In multilocation centralized power systems, the DC/DC converters were physically located in different places, thus requiring safety shielding because of the presence of the high-voltage bus. The centralized power system is still used in "silver" box power supplies for

low end desktop and server computers, but it has become obsolete in relatively large telecommunication power distribution systems because of the following reasons:

- Centralized, custom power supplies require longer time to market and lack flexibility for quick modification.
- Failure of any part of the power system means failure for the electronic equipment in the whole cabinet.
- Custom, bulky power-delivery bus bars are expensive.
- Static and dynamic regulation of the supply voltage is poor and varies from shelf to shelf

3.2 Distributed Power Architecture

A dramatic step happened in early 1990s when the market largely adopted distributed power architecture (Tabisz et al., 1992; Lindman & Thorsell, 1996). The bulky centralized power supplies were replaced by AC/DC rectifier/charges providing –48-V backplane voltage to each shelf and line card. The line cards allow hot-swap replacement to reduce failure downtime. Each line card includes a number of –48-V input isolated DC/DC modules, that provide all required voltages to the electronic functional blocks (Figure 4).

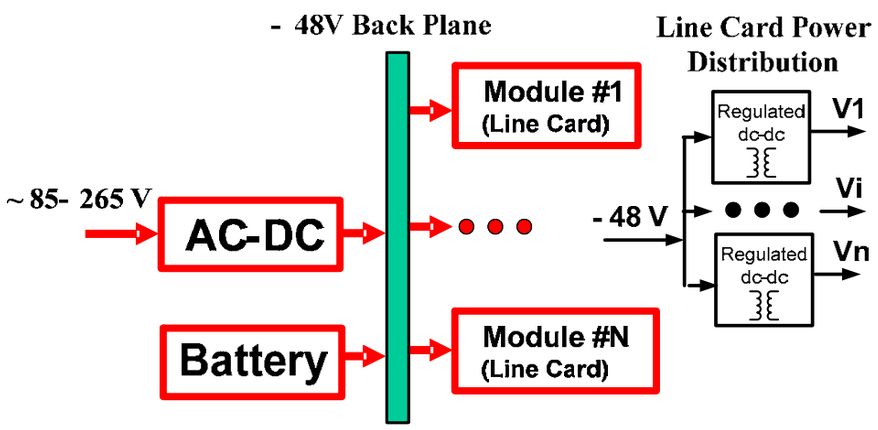


Fig. 4. Example of distributed power architecture

The introduction of distributed power architecture (DPA) was driven by the following:

- A trend towards digital processing blocks with increased power consumption, lower voltages, and specific power sequencing
- A broad market introduction of modular, high density, and reliable isolated DC/DC converters at a reasonable cost
- A demand for a more flexible, shorter design cycle power distribution systems allowing quick changes and updates
- A need for systems with high reliability and availability that supported hot swapping and had lower maintenance costs

3.3 Hybrid Power System

DPA-based systems addressed new power requirements, but the system cost remained relatively high. When the required number of supply voltages per line card exceeded the

initial four to five, the excessive number of isolated DC/DC converters was questioned (Narveson, 1996). In this paper there was suggestion to use only one isolated DC/DC converter. This converter provides most power demanding supply voltage in the system and also supplies non-isolated point-of-load (POL) regulators, which provide the remaining supply voltages to electronic blocks. This architecture, commonly called hybrid power system (Figure 5), was the first step towards the IBA. The hybrid power system reduces power distribution costs and allows placing POLs right next to the related load, thus reducing the impact of supply plane parasitics and improving high di/dt transient response. If power sequencing is needed, an additional switch can be added between the isolated converter output and the electronic load (Figure 5).

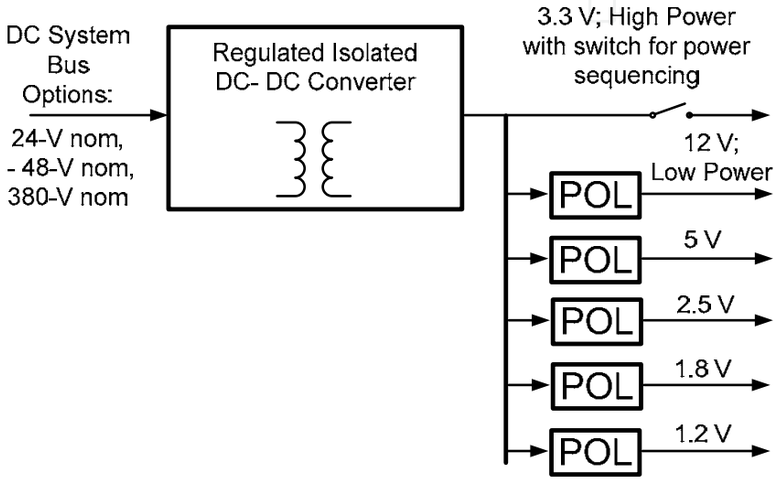


Fig. 5. Hybrid power system

The hybrid power system is preferable solution when one of the output voltages requires relatively high power. In this case, a single regulated isolated converter improves the efficiency of the whole system when the converter's output voltage is 3.3 V or higher. With the 3.3-V bus voltage, the hybrid system's overall output power might be limited to about 200 W. This limit is suggested because high currents circulating through the power and ground planes can cause significant losses and EMI issues as the system power increases.

3.4 Intermediate Bus Architecture

Driven by digital- and analog-IC industry demands for the low-level supply voltages in the 0.5-V to 3.3-V range and for the low-cost POLs, since early 2000s the market adopted the IBA (Morrison, 2002; White, 2003, Mills, 2004). In many applications, the IBA-based power system includes a front-end AC/DC power supply with a typical output of –48 V, 24 V, 12 V or 130 V. In some data-communication and medical equipment the input DC voltage can be 380 V taken directly from a power factor corrector output (Zhu & Dou, 2006) This voltage is supplied to an input of intermediate bus converter, that provides isolation and conversion to the lower level intermediate bus voltage, typically within 5 to 14 V. This intermediate bus voltage is supplied to non-isolated, POL regulators that provide high quality voltages for a variety of digital and analog electronic functional blocks (Figure 6).

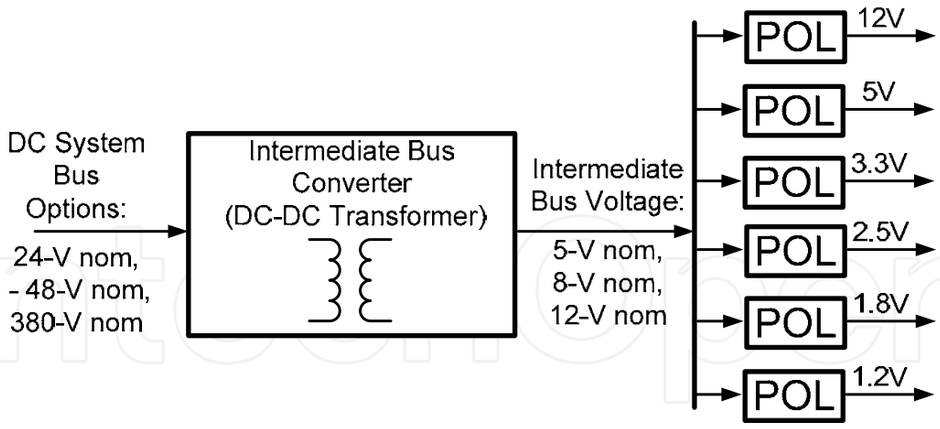


Fig. 6. Example of intermediate bus architecture

The following are advantages of IBA:

- System cost is reduced because only one isolated converter is needed and low cost, standardized, non-isolated POL regulators are available in the market.
- IBC circuit can be made simple because typically intermediate bus voltage variation is relaxed.
- Quality of supply voltages is increased because non-isolated POLs are located next to the electronic functional blocks.
- System is flexible for modifications and updates.
- Overall system reliability is higher.
- Housekeeping, power sequencing, diagnostics, optimized power saving modes are easier to implement because all major control signals are on the secondary side.

The following are challengers that IBA needs to address:

- The IBC must have highest efficiency and power density to provide a competitive edge for IBA versus DPA.
- The overall line card power can be limited because of high currents circulating through ground and bus-voltage planes.
- Parallel operation of highly efficient unregulated bus converters can be difficult.
- Specialized IBC controller ICs are needed to address specific IBC requirements.

3.5 Comparison and Trade-Offs of IBA versus DPA

IBA is a continuation of DPA at the line card level. An optimal choice between IBA and standard DPA for each specific case depends on many factors, including the number of supply voltages, the required voltage and power levels, the system-bus input voltage range, and the specified static and dynamic regulation for supply voltages. It is obvious that cost and efficiency are the most significant trade-off. Table 2 shows the pros and cons between IBA- and DPA-based systems in very general terms. A detailed analytical comparison is needed to make the right design decision. Examples of such analysis can be found in literature (Sayani & Wanes, 2003).

System Requirement		IBA	DPA
Input Voltage Range	Wide	–	Best
	Narrow	Best	–
Number of Outputs	<4	–	Best
	≥4	Best	–
One Regulated Output Demands Most of the Power		–	Good
		Hybrid system could be the best in such case	
Cost		Best	–
Efficiency		Better	Best
Load Supply Voltage Quality		Best	Good
Power Density		Best	Good

Table 2. Comparison of IBA versus DPA for different system requirements

3.6 Selection of Optimal Bus Voltage

Optimal selection of intermediate bus voltage is critical for the overall performance and lowest cost of IBA based power distribution system. For higher bus voltages, IBC is more efficient; however, POL regulators perform more efficiently at lower bus voltages. A lower bus voltage means higher currents circulating through the power and ground planes, thus adding additional losses. Obviously, there are some trade-offs to consider when defining a bus voltage optimized for the lowest overall power losses.

In general, the power losses, *Ptot,* associated with any switching power conversion can be expressed as

$$Ptot = Pconst + Kv \times V^2 + \mathrm{Re}q \times I^2 \tag{1}$$

where *Pconst* is nearly-constant power losses consumed by the control and housekeeping circuits; $Kv \times V^2$ is the power losses associated with the switching process (a function of switching voltage, frequency and in some cases, the load current); *Kv* is a coefficient measured in W/V2 that reflects module losses dependence on the switching voltage; $\mathrm{Re}q \times I^2$ is the conduction power losses that are dependent on load current, *I,* and equivalent resistances, *Req,* of the components and traces. It is assumed that the switching frequency is constant.

The optimal bus voltage has to be analyzed for each design case because the selected IBC converter and POL regulators differ in terms of their power losses dependence from the bus voltage and current. The following example of bus-voltage optimization is for a DPA consisting of an unregulated IBC converter and POLs providing five different output voltages. It is assumed that for the bus voltage ranges from 5 V up to 15 V, the MOSFET switches for the selected IBC converter and POL modules remain the same. The key optimization parameters are shown in Table 3. These data is taken from the IBC converter and the POL modules available in the market. The parameters *Req* and *Kv* are specific for the selected modules and might be different for other practical examples.

Module	Vout, V	Iout, A	Pout, W	Pconst, W	Req, mΩ	Ploss(I), W	Kv, W/V^2
POL #1	0.7	60	42	0.46	2.5	9	0.038
POL #2	1.0	120	120	0.92	1.25	18	0.076
POL #3	1.5	60	90	0.46	2.5	9	0.038
POL #4	2.5	60	150	0.46	2.5	9	0.038
POL #5	3.3	30	99	0.23	5	4.5	0.019
Total	-	-	501	2.53	-	49.5	0.209
Bus Plane	-	-	-	-	2	Pplane(Vbus)	-
IBC	Vbus	Ibus	Pbus(Vbus)	0.5	4	Req x $Ibus^2$	0.056

Table 3. IBA power system parameters for optimal bus voltage analysis

The sum of the constant losses of each POL module (2.53W) and the sum of the output-current related losses (49.5W), can be used to define the total losses in the POLs as function of *Vbus*:

$$Ppol(Vbus) = 2.53W + 0.209\frac{W}{V^2} \times Vbus^2 + 49.5W \tag{2}$$

The bus-voltage power and ground planes have a resistance, *Rbus,* equal to 2mΩ, and the overall output power, *Pout total,* is equal to 501 W. Thus, the plane losses are defined as function of *Vbus*:

$$Pbus(Vbus) = Rbus \times \left(\frac{Ppol(Vbus) + Pouttotal}{Vbus} \right)^2 \tag{3}$$

IBC converter *Vbus*-dependent losses, *Pibc(Vbus)*, are shown in Equation (4) after substituting the related parameters from Table 3 and the Equations (2) and (3):

$$Pibc(Vbus) = 0.5W + 0.056\frac{W}{V^2} \times Vbus^2 + 4m\Omega \times \left(\frac{Pbus(Vbus) + Ppol(Vbus) + Pouttotal}{Vbus} \right)^2 \tag{4}$$

Therefore, total IBA-based power system losses can be defined as:

$$Ptotal(Vbus) = Ppol(Vbus) + Pbus(Vbus) + Pibc(Vbus) \tag{5}$$

Figure 7 shows power losses plots as a function of bus voltage. The optimal bus voltage for minimal overall power losses can be chosen from the plot. In this particular case, the curve showing total power losses is relatively flat in the region of minimum losses for bus-voltages between 8 and 10.5 V. With this wide optimal bus-voltage range, the unregulated IBC converter can be good fit depending on its input voltage range.
The optimal bus voltage is usually lower for the higher switching frequencies of POLs and the lower total system power. This trend supports a balance between the voltage-dependent losses like switching losses and the current-dependent losses like conduction losses.

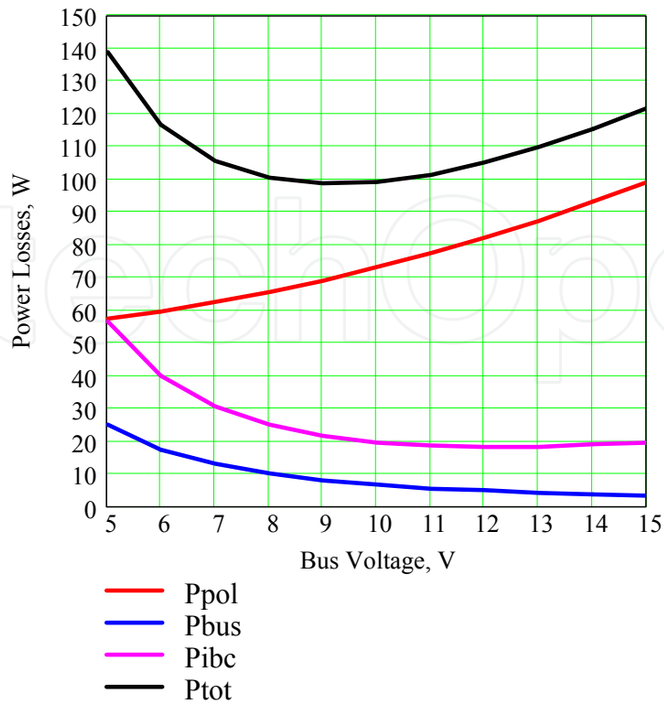


Fig. 7. Power losses over bus voltage

4. Telecom Rectifier and Front-End Server Power Supply

Practically every telecom rectifier, or server power supply have the following key functional blocks, which are usually associated with any over 500 W AC/DC power supply:

- EMI filter
- Power factor corrector (PFC) with hold up capacitor
- Isolated post-PFC DC/DC converter
- Auxiliary bias or standby power supply
- Fan and its regulator

Regulations and specifications define the overall efficiency of AC/DC power supply. It is the responsibility of designer, based on previous designs and future forecast, identify the efficiency and power losses of each functional block to meet the total efficiency goals.

4.1 Power and Efficiency Distribution

For a power and efficiency distribution analysis between the key functional blocks of AC/DC power supply the following approach can be used. Usually the EMI filter and PFC are considered together because it is convenient from the test procedure as well. The output of the PFC (typically 400 V) supplies the main isolated DC/DC converter and the standby power supply. The typical standby power-supply output-power range Can be from 5 W up to 30 W depending on application. It is much lower than the output power of main DC/DC converter. But, the efficiency and power consumption of standby power supply can not be neglected, because the regulations specify the efficiency down to 10% or even 5% of

maximum output power. The fan regulator is usually supplied from the output of DC/DC converter and thus, it is included into the efficiency of converter. Table 4 below is an example of power and efficiency distribution analysis between the PFC, main DC/DC converter and standby power supply. It is fulfilled for 12-V, 660-W output server power supply.

Rated Output Power	10% Load	20% Load	50% Load	100% Load
Efficiency from Table 1	75%	85%	89%	85%
Overall Power Consumption	89 W	158 W	376 W	788 W
PFC Efficiency	95.3%	96.4%	97.6%	97.7%
PFC Output Power	85 W	152 W	367 W	770 W
Standby Power	6 W	7 W	10 W	10 W
Standby Power Efficiency	80%	82%	85%	85%
Standby Power Consumption	7.5 W	8.5 W	12 W	12 W
DC/DC Input Power	77.5 W	143.5 W	355 W	758 W
DC/DC Output Power	66 W	132 W	330 W	660 W
DC/DC Efficiency Goal	85.2%	92.7%	93%	87.1%

Table 4. Power and efficiency analysis of 660-W server power supply

4.2 Power Factor Corrector

Efficiency of power factor corrector (PFC) depends significantly on input AC line range (Cohen & Lu, 2008). Typically, for the more than 500-W PFC, the boost converter based power stage remains the most popular option. The boost converter achieves its highest efficiency at high input line, and the efficiency gradually degrades at lower input voltages. The efficiency and power factor specified by ENERRGY STAR® test procedure for the single output server power supplies has to be confirmed by measurements at 230 Vrms AC line (http://www.energystar.gov/ia/partners/product_specs/program_reqs/computer_server_prog_req.pdf). However, if the design targets the 85 to 265 Vrms universal range, all critical thermal and electrical parameters of PFC have to be verified in the whole operating range. Usually, the output power capability rated at 230-Vrms input voltage, for the same front-end AC/DC power supply is de-rated for the 115-Vrms AC line.

Currently the interleaved PFC and bridgeless PFC are two major directions where most of the research and development is focused. The interleaved PFC is already established solution in mass production supported by available in the market controllers from different vendors (see in http://focus.ti.com/docs/prod/folders/print/ucc28070.html). Typical application diagram of the two-phase interleaved, continuous current mode PFC using UCC28070 from Texas Instruments is shown in Figure 8.

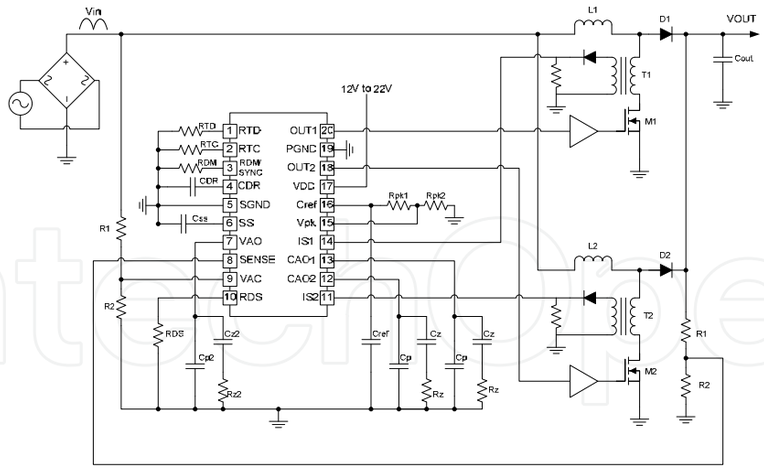


Fig. 8. Two-phase interleaved PFC converter using UCC28070 controller

Advantages of interleaved PFC include:

- Reduced input current ripple because of ripple cancellation effect caused by 180O phase shifted operation;
- Reduced EMI filter because of lower input current ripple;
- Lower RMS current through the output capacitor because of ripple cancellation effect. This means less number of capacitors is needed, or increased reliability when the output capacitance can not be reduced because of required hold up time;
- Better, equalized temperature profile because the power dissipated components are spread between phases. This also results in the higher overall efficiency.

The first bridgeless PFC circuit has been patented as far as in 1983 (Mitchell, 1983), but the concept is still mostly at the research stage. The practical implementation has been limited by the high voltage MOSFET and diode performance, EMI issues, difficulties of voltage and current sensing. Latest achievements in components technology, especially availability of CoolMOS™ transistors and Silicon Carbide diodes, renewed interest to the bridgeless PFC (Hancock, 2008). The analytical and experimental comparison of few different bridgeless PFC topologies is provided in (Huber et al., 2008). The analysis claims that the bridgeless PFC with two boost circuits (Souza & Barbi, 1999) shown in Figure 9 has the efficiency advantages and less EMI issues versus other bridgeless PFC topologies. In general, publications claim up to 1% efficiency improvement when using the bridgeless PFC versus standard approach.

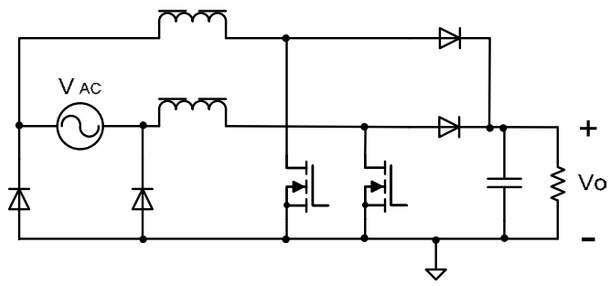


Fig. 9. Bridgeless PFC with two boost circuits (Souza & Barbi, 1999)

4.3 Isolated DC/DC Converter for Front-End Power Supply

The isolated DC/DC converter topology selection is critical for total efficiency of front-end power supply. Zero voltage switching (ZVS) enabling topologies are preferable in such applications because of the relatively high input voltage usually, from 350 to 420-V range. Attractive solutions include phase shifted full-bridge, asymmetrical half-bridge, LLC resonant converter and variations of these topologies (Zhang et al., 2004; Miftakhutdinov et al., 1999; Fu et al., 2007).

For the interleaved topology, the asymmetrical half-bridge converter suits best because of its relative simplicity (Miftakhutdinov et al., 1999). One possible example of interleaving with four phases is shown in Figure 10.

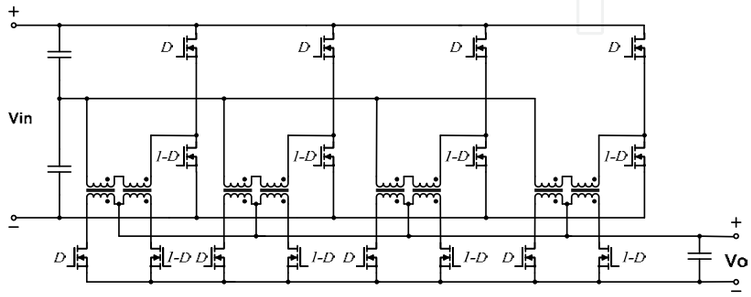


Fig. 10. Four phases interleaved asymmetrical half-bridge.

The LLC resonant topology is recently gaining popularity as post-PFC isolated DC/DC converter (Figure 11).

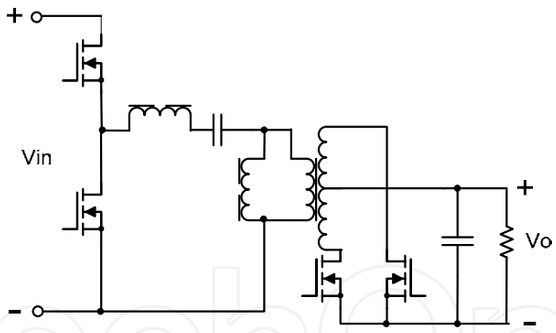


Fig. 11. LLC resonant converter power stage

Its main advantage is ZVS for the primary side switches and zero current switching (ZCS) for the secondary side synchronous rectifier MOSFETs (Fu et al., 2007). Variable switching frequency, special attention to light load operation and difficulties with interleaving limit this topology to sub-kW range.

One implementation of classical phase shifted bridge topology using specialized analog controller is shown in Figure 12. The efficiency improvement of this circuit is achieved by using synchronous rectification, adaptive control algorithm providing ZVS condition over wide operating range, accurate adaptive timing of control signals for primary and secondary power FETs and light load management block providing the highest efficiency and power savings at low output power conditions.

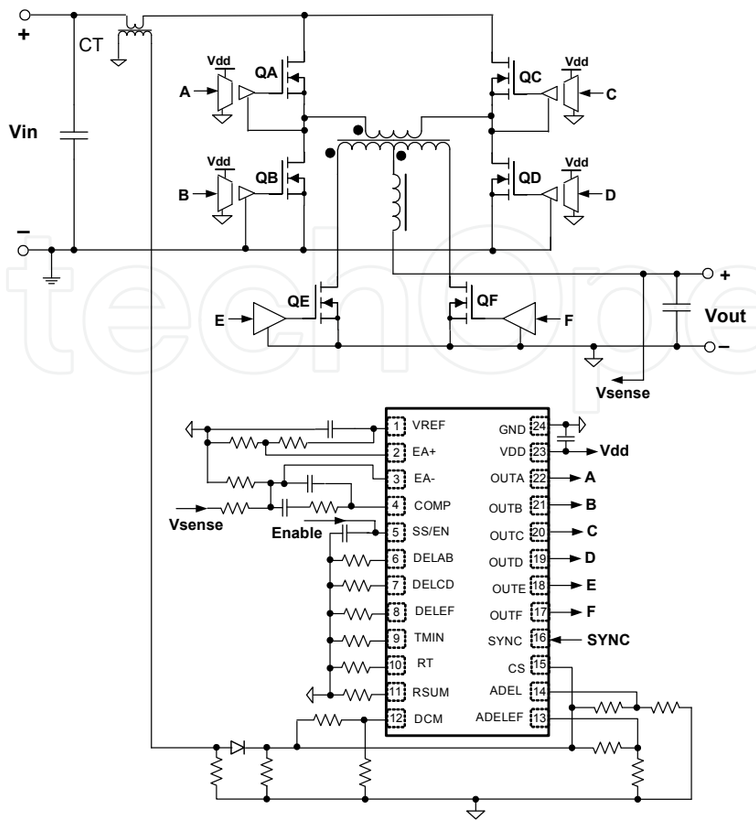


Fig. 12. Phase shifted full-bridge converter with advanced analog controller

4.4 Control Algorithms for High Efficiency

Optimal control algorithm is critical not only to meet static and dynamic requirements of telecom power system, but it also opens new opportunities to increase efficiency by transitioning into optimal power saving modes depending on system conditions. When selecting the controller, the flexibility, programmability and auto tuning capability of digital controllers have to be weighted versus lower cost, simple and generally faster analog control ICs. The list of most popular power saving control strategies is provided below.

- Interleaving of few phases for better current and temperature distribution at maximum output power and gradual phase shedding when the load is reduced (Figure 10);
- Synchronous rectification using MOSFETs with the diode emulation technique at light load to avoid current circulation. It could be beneficiary to switch off the drive circuit of rectifier MOSFETs at very light load where the drive losses exceed the conduction losses. Performance of synchronous rectifier significantly depends on accurate timing between primary and secondary side switches (Figure 12);
- Proper use of zero voltage (ZVS) and zero current (ZCS) switching technique to reduce switching losses in power MOFETs. This requires optimal adaptive or predictable set of delays between switching events depending on operation conditions (Figs. 10 - 12);

- Optimal adjustment of intermediate bus voltage, drive voltage and other system parameters to maintain highest efficiency at different operation conditions;
- Smooth transition between operation modes to maintain highest efficiency depending on operating conditions, for example from continuous mode to discontinuous, from fixed frequency to frequency foldback etc (Figure 12);
- Proper use of pulse skipping or burst mode at light load or no load to reduce the power consumption (Figure 12)

This list shows benefits of wide use of digital controllers to address power saving technique because of their programmability and flexibility. The digital controllers for power supplies are available from few vendors at reduced cost that make these devices competitive with analog controllers, even for relatively low power applications in sub-kW range (see in http://focus.ti.com/docs/prod/folders/print/tms320f28023.html). Specifically designed for these applications high end analog controllers also have their niche. Analog controller ICs remain popular in mature, high volume applications where the operating conditions are well known and established, and thus, cost is more critical than programmability and flexibility (Figure 12).

4.5 Design Considerations and Component Selection

Optimal selection of power stage components provides foundation for high efficiency power system design. Magnetics and power switches are major contributors into the total power losses budget. In this chapter the main focus is on power MOSFETs and high voltage diodes where the significant progress has been achieved lately. The new super junction technology for high voltage MOSFETs significantly reduces Rdson, drain-source and gate-source capacitances providing lower conduction losses and switching losses (Bjoerk et al., 2007). Still accurate ZVS condition analysis over operating conditions remains critical to ensure the highest efficiency. Because of significant non-linear behavior of drain-source capacitance, the super junction MOSFETs, like CoolMOS™, require new analytical model to estimate switching losses and determine ZVS conditions. The following Equation (6) is adequate for energy calculation stored in the output capacitance of high-voltage regular MOSFETs (Miftakhutdinov, 2008a)

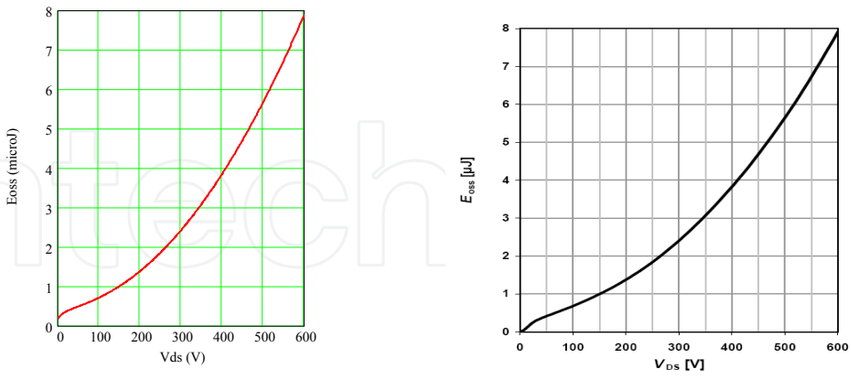
$$Ecds = \frac{2}{3} \cdot Coss \cdot \sqrt{Vdsoss} \cdot Vds^{\frac{3}{2}} \tag{6}$$

Here, *Ecds* is the energy, *Coss* is the output capacitance at *Vdsoss* = 25V from datasheet, and *Vds* is the voltage where the energy should be calculated. The new super junction MOSFETs require different model because of significant non-linear behavior of drain-source capacitance. The following approximated Equation (7) provides good practical results for super junction FETs:

$$Ecds = \frac{Coss}{Kc} \cdot (Vdsoss)^2 \cdot \ln\left(\frac{Vds + 5V}{V}\right) + \frac{Cinit \cdot (Vds)^2}{2} \tag{7}$$

where Kc = 2.2 and Cinit = 40 pF for SPA11N60FCD type MOSFET from Infineon.

The plots in Figure 13 compare calculated energy using Equation (7) with the plot provided in the datasheet.



a) analytically derived plot b) experimental plot from datasheet

Fig. 13. Energy Ecds over Vds for SPA11N60FCD type MOSFET

The pairing of super junction MOSFETs with silicon carbide diodes in PFC applications results in significant power losses reduction (Miesner et al., 2001). The use of silicon carbide diodes practically eliminated the need for complicated snubbers in PFC boost power stage. This is because these Schottky type diodes have very fast recovery time versus the p-n junction silicon diodes. Regardless of the extra cost of such diode, the industry widely accepts silicon carbide diodes for PFC applications because the overall efficiency gain could be 3% or higher.

5. Intermediate Bus Converter

This section discusses major requirements to IBC converters, compares key parameters of the available in the market products, considers preferable topologies and focuses on design challengers that must be taken into account. An example of practical implementation based on the IBC controller UCC28230 is also provided and supported by test results. Additional analysis and design information related to IBC as part of IBA can be found in publications (Barry, 2004; Miftakhutdinov & Sheng, 2007; Miftakhutdinov et al., 2008; Miftakhutdinov, 2008a; Miftakhutdinov, 2008b)

5.1 Major Requirements and Parameters of Modern IBCs

IBA includes an additional DC/DC conversion stage provided by IBC to supply intermediate bus voltage. It is important for the IBC to be highly efficient with high power density at the lowest possible cost. The first bus converters in the market were slightly modified versions of fully regulated DC/DC modules. However, the IBC's strict requirements in a short time have made it a stand-alone, specialized product in module manufacturer' portfolios. A list of major IBC parameters follows:

- Efficiency: 96% to 97% typical
- Power density: >250 W/inch^3
- Cost: $0.1 to $0.2 per watt

- Input voltage range:
  - 43 to 53 V for servers and storage
  - 38 to 55 V for enterprise systems
  - 36 to 60 V for narrow telecom range
  - 36 to 75 V for wide telecom range
  - 380 to 420 V for data center high-voltage systems
- Power range: 150 to 600 W and higher
- Mechanical form factor:
  - 1/4 brick for > 240 W of output power
  - 1/8 or even 1/16 brick for < 240 W output power
- Most popular transfer ratios: 4:1, 5:1 and 6:1 for –48-V nominal input voltage
- Switching frequency: relatively low at 100 to 200 kHz
- Most popular power stage topologies: Full-bridge, half-bridge, and push-pull
- Secondary-side rectification: Almost entirely uses synchronous MOSFETs, self- or control-driven
- Control approaches: Fully regulated, semi-regulated, or unregulated

Because of the growing popularity of IBA, the IBCs for different power levels and transfer ratios are readily available from different vendors. Table 5 shows the major parameters of currently available IBCs in the market. This data is based on review of products from the popular vendors in the first half of 2008.

Manu-facturer	Model	Input, V	Form Fact. Brick	Pout, W	Trans. Ratio	Output, V	Eff., %	Density, W/inch^3
Tyco	EUK240S9R0	36-60	1/8	240	5:1	6.5-11.5 unreg.	95.5	272
Tyco	QBK033AOB	36-60	1/4	396	4:1	11.4-12.6 reg.	94.5	285
Ericsson	PKM 4402NG PI	38-55	1/4	587	5:1	7.1-11.0 unreg.	96.4	403
Ericsson	PKM400B PI	36-75	1/4	286	4:1	11-12.5 reg.	95.9	191
Delta	Q48SB9R650NRFA	36-57	1/4	500	5:1	6.8-11.5 unreg.	96.4	312
Delta	ES8SB9R625NRFA	38-55	1/8	240	5:1	7-11 unreg.	96.5	258
Delta	V48SB12013NFRA	38-55	1/16	150	4:1	8.9-13.75 unreg.	95.2	347

Table 5. Major parameters of modern IBC converters

5.2 Control Approaches

Depending on the input voltage range and the requirements for output voltage tolerances, the IBC can be regulated with the feedback loop taken from its output; semi-regulated with the input voltage feed-forward circuit; or unregulated (Barry, 2004; Ericsson Inc., 2005).

The IBC with a closed feedback loop requires an additional isolation barrier for feedback signal transfer. It is more expensive than semi-regulated because of more complex control circuit and less efficient than unregulated IBC because it operates in a wide duty cycle range. However, full regulation is justified for the hybrid power system where the IBCs

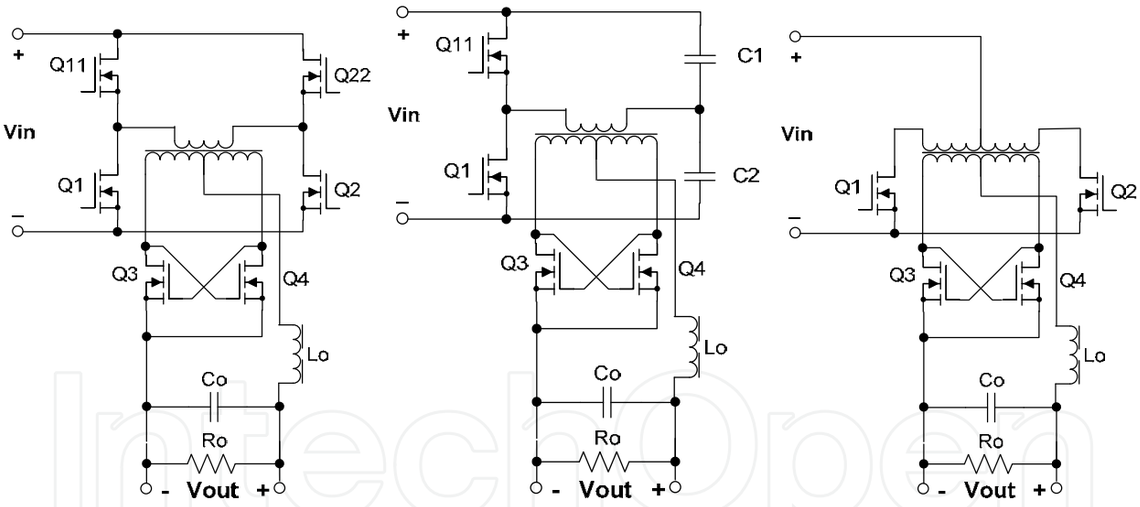
output is the supply voltage for the most power consuming load. If the power sequencing is needed, an additional switch can be added between the IBC output and the load as it is shown in Figure 5 (Ericsson Inc., 2005).

The semi-regulated IBC with input feed-forward control is usually a lower cost solution than the fully regulated converter, but it also has lower density and efficiency than the unregulated converter. This is because the semi-regulated IBC is designed to operate over a wide duty cycle range, even at steady state. The semi-regulated IBC is usually used in a system with a relatively wide input voltage range.

The unregulated IBC provides the solution with the highest efficiency and power density and the lowest cost because it operates at almost 100% duty cycle at steady state. There is no additional communication through the isolation barrier except for the energy transfer through the power transformer. The size of the transformer and output and input filters is small because converter operates at maximum duty cycle. However, overstresses during transient conditions like start up, current limiting, and shut down need to be addressed during the design.

5.3 Major IBC Topologies

IBCs usually employ forward type full-bridge, half-bridge and push-pull topologies with the synchronous MOSFET rectification technique to achieve highest efficiency. Figure 14 shows three such IBCs in their very simplified forms.



a) Full-bridge IBC b) Half-bridge IBC c) Push-pull IBC

Fig. 14. Popular power stage topologies for IBC

Using a self-driven synchronous MOSFET rectifier is a very popular choice, especially for unregulated converters, but practical solutions might require additional control windings and snubber circuits for improved efficiency and reliability. For the high power applications and, especially for the fully regulated and semi-regulated converters, the control driven MOSFET rectifiers can be preferable. The advantages of using control driven rectifiers are a simplified power transformer and a gate drive voltage that is independent from input voltage and load current variations. A detailed review, classification and comparison of synchronous rectification techniques can be found in Reference (Miftakhutdinov, 2007).

The double-ended topologies shown in Figure 14 are preferred for bus converter applications because they can operate at almost 100% duty cycle applied to the output filter, thus significantly reducing the size of the output inductor. Currently available IBCs usually operate at about 100 kHz switching frequency. IBCs with 48-V (nominal) input voltage can operate in the hard switching mode, but the zero voltage switching technique is preferred for the IBCs with 400-V (nominal) input voltage. The full-bridge topology is preferred for a 250-W or higher output power. The half-bridge topology provides a low cost solution for the output power range below 250 W. The bridge based topologies have primary MOSFETs with a drain-to-source voltage rating equal to the input voltage, with some reliability margin. These topologies are better choice for input voltages higher than 24 V. For a 24-V or lower input, the push-pull topology is attractive because of simple drive circuit of primary MOSFETs. However, the center tapped primary winding is a drawback for the planar transformer in push-pull topology.
Table 6 provides a general comparison of IBC topologies. However, to select the right topology during practical design, detailed calculations and a review of power system specifications are needed for each specific case.

Topology	Full-Bridge	Half-Bridge	Push-Pull
Primary MOSFETs	Vds = Vin	Vds = Vin	Vds > 2Vin
Transformer	Good utilization	Issue with 5:1 transfer ratio because planar transformer has to be 2.5:1	Poor utilization
Rectifier MOSFETs	Primary winding clamping to zero is possible	No primary winding clamping ability	No primary winding clamping ability
Output inductor	The Same		
Cycle-by-cycle current limit	Only a problem if a DC blocking capacitor is used	Inherent issue	Not a problem

Table 6. Comparison of popular IBC topologies

5.4 Using a Resonant Converter as an Unregulated IBC

Recently, high frequency resonant topologies for IBC application have been suggested and their high performance reported (Ren et al., 2005). In this research the resonant topology has been successfully used for a 48-V input, 12-V, 500-W output IBC at switching frequency up to 800 kHz and the 95.5% efficiency achieved. Nevertheless, the resonant IBC approach has not yet become mainstream in the industry.

5.5 Unregulated IBC Design Challenges

The design of unregulated IBC with self-driven MOSFET rectification has its own challenges and trade offs. The design goal is to achieve the highest efficiency and power density at the lowest cost. The challenges include the following:

- High ripple current during transitional states
- Start up problems
- Optimal synchronous rectification
- Reverse energy flow and self-oscillation
- Parallel operation issues
- Flux balancing of power transformer

A. Operation at Transitional States

At steady state, an unregulated converter operates at almost 100% duty cycle with very low output inductor current ripple. However, during soft start or cycle-by-cycle current limiting, the duty cycle varies from 0% to 100%, which can cause significant ripple increase in the middle of this range. This ripple can overstress the power stage and limit the start up capabilities of the IBC, especially when there is a large output capacitance. The output inductor's peak-to-peak ripple current, *ΔIL*, is defined for the whole duty cycle range with Equation (8):

$$\Delta IL = \frac{Vin \times D \times (1-D)}{2 \times Ntr \times Lo \times Fsw}, \tag{8}$$

where *Fsw* = 1/*Tsw* is the switching frequency, *D* = *Ton*/(0.5 x *Tsw*) is the duty cycle after rectification, *Ntr* = *Wpr*/*Wsec* is the transformer's turns ratio, *Wpr* is the primary winding turns, *Wsec* is the secondary winding turns, *Lo* is the inductance of the output inductor, and *Vin* is the voltage applied to the transformer's primary winding. Note that duty cycle calculations and related equations assume a D value between 0 and 1. The following discussion and plots refer to duty cycle in percent, which is D x 100. The plots in Figure 15 show that the output inductor's ripple current is very low in the vicinity of *D* = 0 and 100%, but can reach 120 A at *D* = 50%.

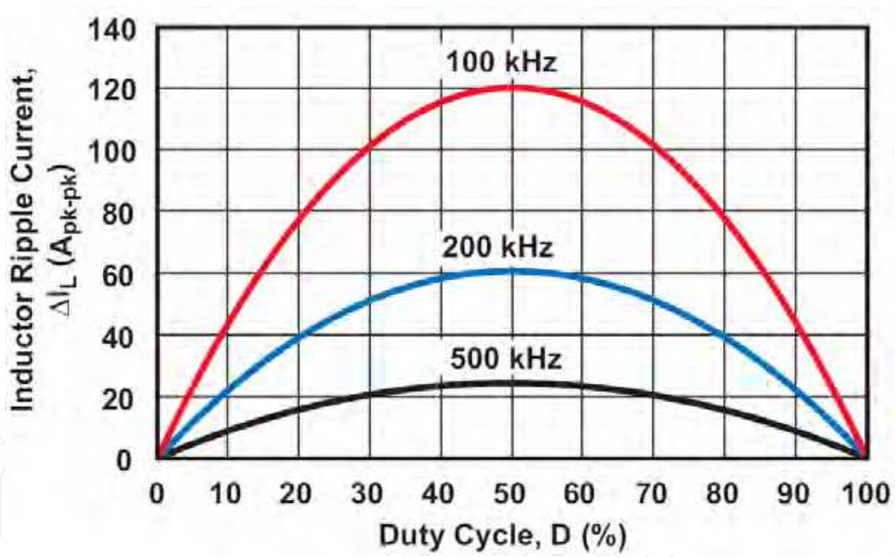


Fig. 15. Output inductor's ripple current versus duty cycle for *Vin* = 50 V, *Ntr* = 5, *Lo* = 0.1 μH, and 100, 200 and 500 kHz switching frequencies in accordance with Equation (8)

Thus, the size and cost of power stage components, especially of the output inductor, become significantly higher when this increased transitional ripple and peak current has been taken into account.

One way to avoid the issue of high ripple current is to use a special frequency control circuit that limits the output inductor's ripple current during duty cycle transitions between 0% and 100%. The desired change in switching frequency over the duty cycle range is

$$Fsw = k \times D \times (1 - D), \tag{9}$$

where k is a constant based on circuit implementation. Substitution Equation (9) into Equation (8) gives the inductor ripple current as

$$\Delta IL = \frac{Vin}{2 \times Ntr \times Lo \times k}. \tag{10}$$

The result is that the switching frequency changes as the duty cycle changes to maintain the inductor's ripple current at a constant value. This idea has been implemented in Texas Instruments UCC28230/1 controller
(http://focus.ti.com/docs/prod/folders/print/ucc28230.html).
A measured plot of the switching frequency change versus the duty cycle is shown in Figure 16. In this case, the nominal switching frequency is set at about 100 kHz.

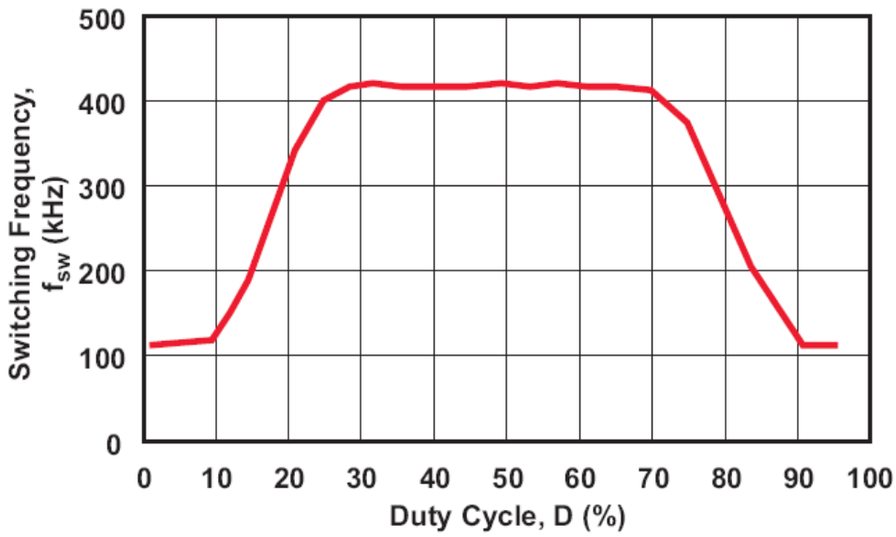


Fig. 16. Measured switching frequency versus duty cycle with frequency control circuit

The frequency is maintained constant at steady state operation when the duty cycle is above 90 % or less than 10%. During start up or cycle-by-cycle current limiting, the duty cycle varies significantly such that the inductor's ripple current reaches a maximum value at 50 % duty cycle. The frequency control circuit maintains the maximum frequency at about 420 kHz when the duty cycle is between 30 % and 70 %. The higher frequency significantly reduces ripple current and allows the output inductor to be approximately 25% of the value needed without the frequency control circuit. When the frequency control circuit is used, inductor selection is based on a maximum frequency of 420 kHz at 50% duty cycle instead of on 100 kHz as it would be without frequency control.

B. Start Up Problems

The ripple increase described in previous section also impacts IBC start up. The inductor's ripple current increase during start up may activate the over-current protection circuit,

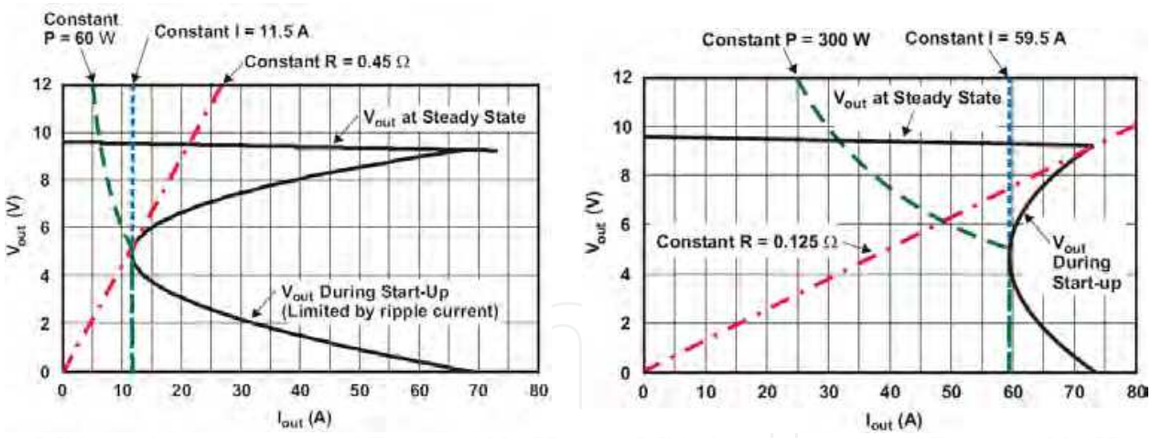
possibly causing the converter not to start at all. Increasing the over-current limit threshold and adding more filtering are not recommended for correcting a start up problem. If a real over-current or output short circuit occurs, these methods of correction will probably overstress the converter. To meet reliability and current stress margin requirements for the power stage components, a much larger output inductor must be selected or the switching frequency must be increased to reduce the ripple (Figure 15).
To further illustrate the start up issue, the plots in Figure 17 of output voltage versus average load current are presented based on the following analysis. During the cycle-by-cycle current limiting, the inductor's average output current, *Iout,* and converter's output voltage, *Vout*, can be described by Equations (11) and (12):

$$Iout = Io\lim - \frac{Ntr \times Vin \times D}{4 \times Lm \times Fsw} - \frac{Vin \times D \times (1-D)}{4 \times Ntr \times Lo \times Fsw}, \tag{11}$$

where *Io*lim is the output current limit and *Lm* is the primary magnetizing inductance of the power transformer. For any *Iout* range the output voltage, *Vout,* can be determined as follows:

$$Vout = \frac{(Vin - Iout \times Rpr / Ntr) \times D}{Ntr} - Iout \times R\sec, \tag{12}$$

where *Rpr* is the equivalent series resistance of the power stage primary side, and *Rsec* is the equivalent series resistance of the secondary side.



a) Without frequency control Fmax = 100 kHz b) With frequency control Fmax = 420 kHz
Fig. 17. IBC start up capability at 75 A current limit threshold and 100-kHz nominal switching frequency

The plots in Figure 17a show the output voltage versus the average load current at steady state and during start up operation with cycle-by-cycle current limiting. These plots were determined after substituting Equation (11) into Equation (12) with the following conditions: *Vin* = 48 V, *Fsw* = 100 kHz, *Ntr* = 5, *Lo* = 0.1 µH, *Lm* = 75 µH, *Io*lim = 75 A, *Rpr*=25 mΩ and *R*sec=4 mΩ.

Also included in Figure 17a are the load curves for the resistive load of 0.45 Ω, a constant current load of 11.5 A, and a constant power load of 60 W. The constant-resistance and constant-current load curves are touching the start up *Vout* versus *Iout* curve without crossing it. With the constant-power mode replicating POL regulator behavior, it is assumed that the POL regulator starts operating and draws current only after *Vout* exceeds the under voltage lockout threshold (UVLO) set at 5 V. Until then, the POL regulator does not draw any current. Thus, the load curves indicate the maximum start up load current of the converter designed for 60-A nominal output with a current limit set at 75 A. Obviously, the fold back type of behavior of *Vout* versus *Iout* limits the start up capability of this unregulated IBC. The load curves cross the steady state *Vout* (upper) plot at 21 A for the constant-resistance mode, at 11.5 A for the constant-current mode, and at 5 A for the constant-power mode. The start up performance of the converter is reduced dramatically because of the inductor's large ripple current at 50% duty cycle. Without the frequency control circuit suggested earlier, the only way to override this limitation is to either increase the output inductance or increase the nominal switching frequency. Either way, power losses and converter cost increase.

Figure 17b illustrates the advantage of a start-up frequency-control circuit. The conditions are the same as for Figure 17a except that the converter operates at 420 kHz for most of the start-up time and at 100 kHz when it reaches the steady-state condition. With the same 0.1-µH output inductor, the start-up capability is significantly improved over that shown in Figure 17a where Fsw(max) = 100 kHz.. The load curves cross the steady-state Vout curve at 75 A for constant-resistance mode, at 59.5 A for constant-current mode, and at 32 A for constant-power mode.

This start-up analysis is based on the assumption that the IBC's output capacitance is not very large. Obviously, if the allowable start-up time is short and the output capacitor is large, an additional current to charge the high capacitance must be taken into account. The frequency-control circuit increases the average charge current available for start-up even with a large output capacitor. The average charge current, *Ich*, for the output capacitor, *Cout*, that satisfies the selected soft-start time, *tss*, can be determined by Equation (13):

$$Ich = Cout \times \frac{Vin}{tss \times Ntr} \tag{13}$$

Figure 18 shows the IBC's average output current required for charging different output capacitances for the selected soft-start time. These curves do not account for the extra current drawn by the load. The effects of different output capacitances can be estimated with and without a frequency-control circuit by comparing the plots in Figs. 17 and 18. With the frequency-control circuit, a charge current of at least 59.5-A is available per Figure 17b. A 10-A portion of this current can be used to charge the 10,000-µF output capacitor within 10 ms per Figure 18. The remaining 49.5-A current is available to the load. Without the frequency-control circuit, the available current per Figure 17a is only 11.5 A. This current is barely sufficient to charge the 10,000-µF output capacitor within 10 ms. If the load draws more than 1.5 A in addition to the capacitor's charge current, the converter will not start because the over-current protection circuit will be activated due to the large ripple current.

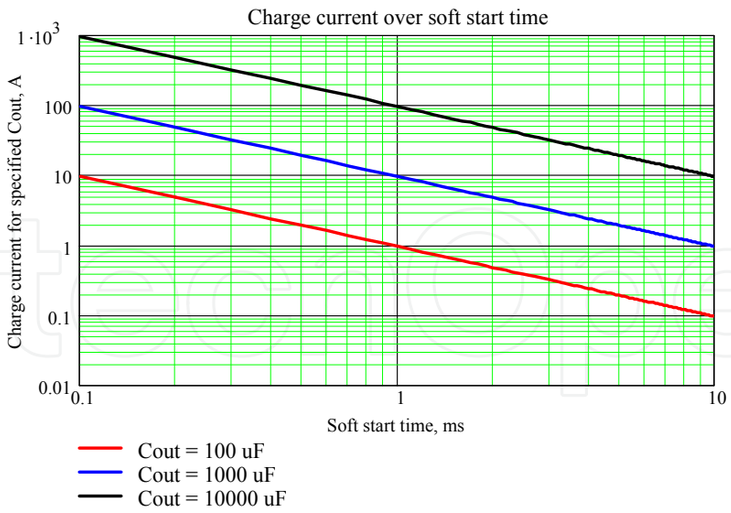


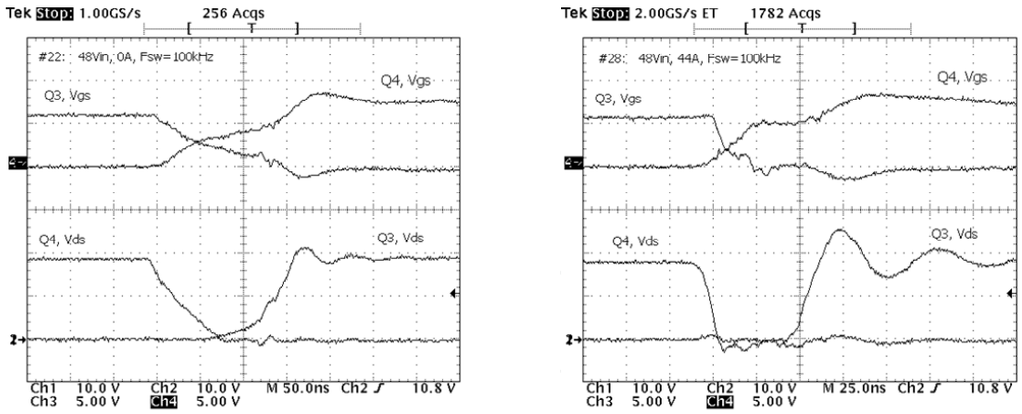
Fig. 18. IBC's required charge current for different output capacitances at selected soft start time

C. Optimal Synchronous Rectification Technique

For IBCs with a 12-V or lower output voltage, the synchronous-rectification technique is mandatory to achieve the required efficiency. Compared to Schottky diodes, low-RDS(on) rectifier MOSFETs can increase IBC efficiency by more than 5%. There are many publications and patented solutions for how to drive the rectifier MOSFETs. Most designs can be divided into self-driven, control-driven, and diode-emulator categories.

Classification of synchronous rectification and additional details can be found in Reference (Miftakhutdinov, 2007). For the unregulated IBC, a self-driven rectification approach that uses a secondary-side transformer winding (Figure 14) or an additional control winding is quite popular because of its simplicity. The proper timing in either self-driven or control-driven synchronous rectifiers is critical to reduce power losses. To avoid overshoot, it is important that the conducting rectifier MOSFET on the secondary side turn off before the primary-side MOSFET is turned on. This is achieved by proper OFF-time switching control of primary-side MOSFETs for half-bridge (Figure 14b) and push-pull (Figure 14c) topologies. For the full-bridge topology (Figure 14a), the OFF time is specified to be the time between primary current switching of MOSFETs on one diagonal to MOSFETs on the other diagonal. The optimal OFF time, Toff(opt), depends on power-stage parameters and the load current.

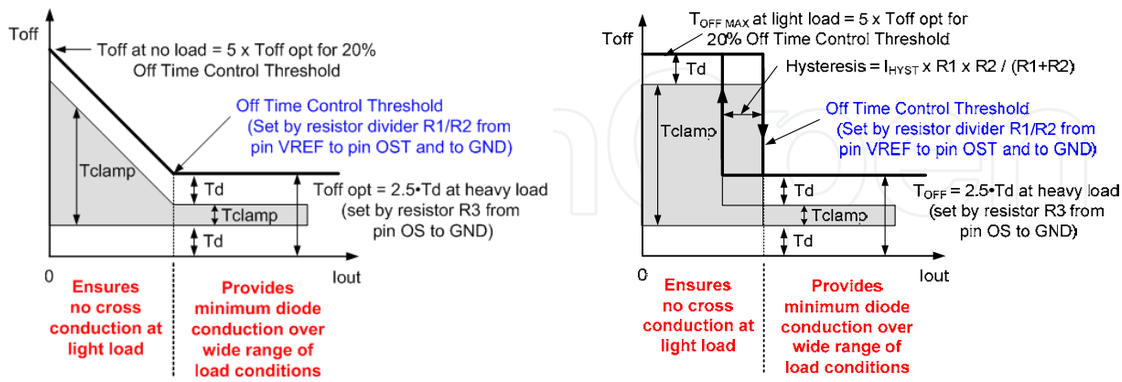
With light loads, the optimal OFF time is longer. This relationship is illustrated in the drain-source and gate-source switching waveforms of the synchronous-rectifier MOSFETs shown in Figure 19a for no load and in Figure 19b for nominal current conditions.



a) No load, 50 ns/div b) 44-A load current, 25 ns/div

Fig. 19. Secondary side MOSFET rectifier switching waveforms

Optimal switching of rectifier MOSFETS over a wide load-current range is possible when the OFF time is allowed to increase to some degree at light loads but is kept as short as possible with nominal loads. A special OFF-time control circuit can be designed to allow the desired output-current threshold to be set such that the OFF time, Toff, starts increasing and reaches its maximum at no-load condition (Figure 20). This increase can be implemented in a linear manner as shown in Figure 20a, or as a step function with hysteresis as shown in Figure 20b. The method can vary depending on the specific design and application. Texas Instruments' specialized UCC28230/1 bus-converter controller implements a comparator based approach as shown in Figure 20b. This controller has dedicated pins (OS and OST) to allow programming of the nominal OFF time, *Toff*, and the output current threshold so the OFF time steps up to the new *Toff(max)* value at the desired current level. The gray area designated "Tclamp" in Figure 20 represents the time when both rectifier MOSFETs are turned off. The purpose of *Tclamp* is to prevent reverse energy flow, which is described in detail in the following Section *D*.



a) Linear approach of controlling off time b) Step change approach of controlling off time

Fig. 20. Setting *Toff*, *Td* and *Tclamp* versus load current with off time control circuit

Since the control circuit of unregulated IBC does not have direct access to the secondary side, so the primary current sensing with a current sense transformer or resistor is usually used to monitor the output current indirectly. Primary side current sensing includes not only the

reflected load current, but also magnetizing current. However, in most applications, the magnetizing current is only a small percentage of total current and can be ignored.
The impact of increasing off time at light load to the output voltage *Vout* is shown by Equation (14):

$$Vout = \frac{Vin}{Ntr} \times \frac{Ts - Toff}{Ts} - Iout \times Rout \tag{14}$$

For the comparator based approach shown in Figure 20b, the output voltage, *Vout*, can jump a few hundred millivolts (with hysteresis) as shown in Figure 21. This jump is not desirable if IBC's operate in parallel with droop current sharing. For such applications, the off time control circuit can be disabled to allow constant-slope output voltage.

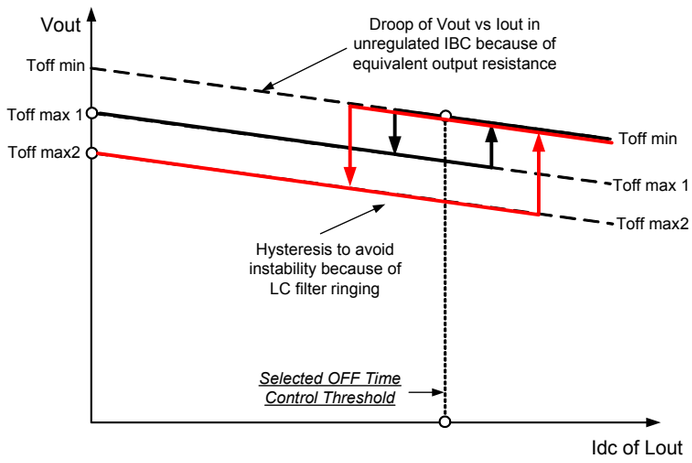


Fig. 21. Impact of comparator based off time control circuit on output voltage (not to scale)

The impact on *Vout* of changing off time is different for linear based off time control circuit. Depending on the gain of the control circuit shown in Figure 20a and the output impedance of the IBC, the slope of *Vout* versus *Iout* below the off-time-set threshold can be positive, negative or zero (Figure 22).

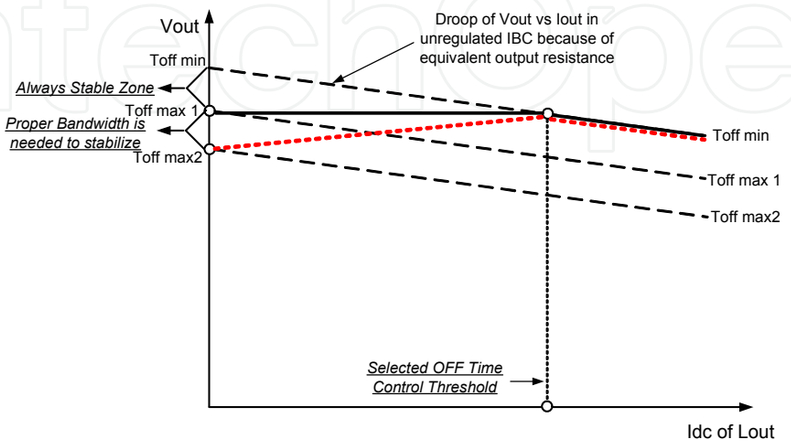


Fig. 22. Impact of linear based off time control circuit on output voltage (not to scale)

D. Reverse Energy Flow and Self-Oscillation

All topologies shown in Figure 14 are capable of transferring energy in the reverse direction, that is, from the output to input. This is because MOSFETs can conduct current in either direction when turned on. This is not true for a converter using a diode rectifier. During shutdown or a sudden input voltage drop, it is possible for the self-driven MOSFET rectifier to start oscillating and pumping energy backwards, thus causing large current and voltage spikes at the rectifier MOSFETs (Bottrill, 2007). The reverse current flow is also possible during quick converter re-start because the output bus capacitor has not been completely discharged from the previous operation. Another potential condition for reverse energy flow is the parallel operation of several bus converters.

One possible way to address this issue is to forcibly turn off the secondary side rectifier MOSFET during primary-side MOSFET off time. To understand this technique let us refer to Figs. 23 and 24. In this implementation, the controller uses additional output signals O1_DIN and O2_DIN, to turn off rectifier MOSFETs during Toff time as shown in Figure 23. Figure 24 shows the controller's push-pull outputs, O1_D and O2_D, driving the high side MOSFETs in the full-bridge power stage, and complementary 1-D outputs, O1_DIN and O2_DIN, driving the low side MOSFETs via external drivers. There is always dead time, Td, between the D and 1-D pulses that is necessary to avoid shoot-through currents in each leg on primary side. If the duty cycle is less than maximum, there is the overlapping time, T_{CLAMP}, when the primary winding is shorted by the lower MOSFETs because they are both in the ON state (Figs. 23 and 24). This specific timing algorithm has been implemented in UCC28230/1 controllers (http://focus.ti.com/docs/prod/folders/print/ucc28230.html).

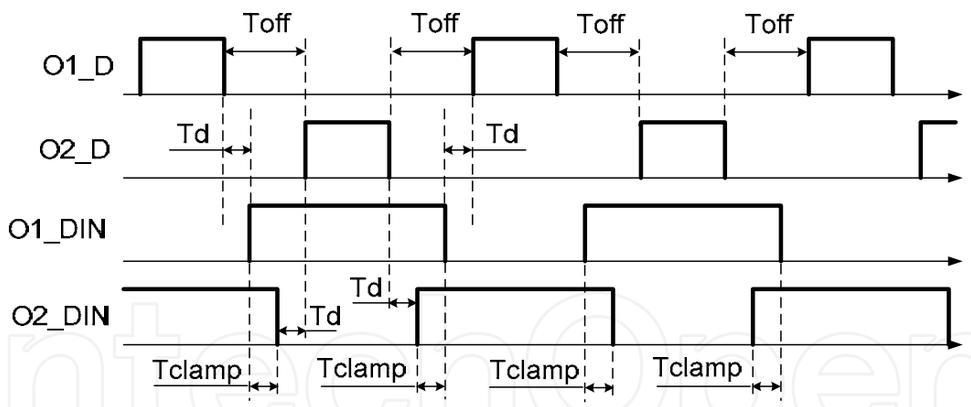


Fig. 23. Timing of UCC28230 controller's output signal

As mentioned earlier, this timing technique addresses the problem of reverse current flow during output pre-bias start up, shut down, input voltage drop, or parallel operation. For the half-bridge (Figure 14b) or push-pull (Figure 14c) IBC topologies, the primary winding of the power transformer can not be shorted by the primary power MOSFETs. To turn off the secondary side rectifier MOSFETs during the T_{CLAMP} interval, an external pulse transformer can be used as shown in Figure 25. In this case the synchronous rectifier scheme uses the control-driven technique for the unregulated IBC.

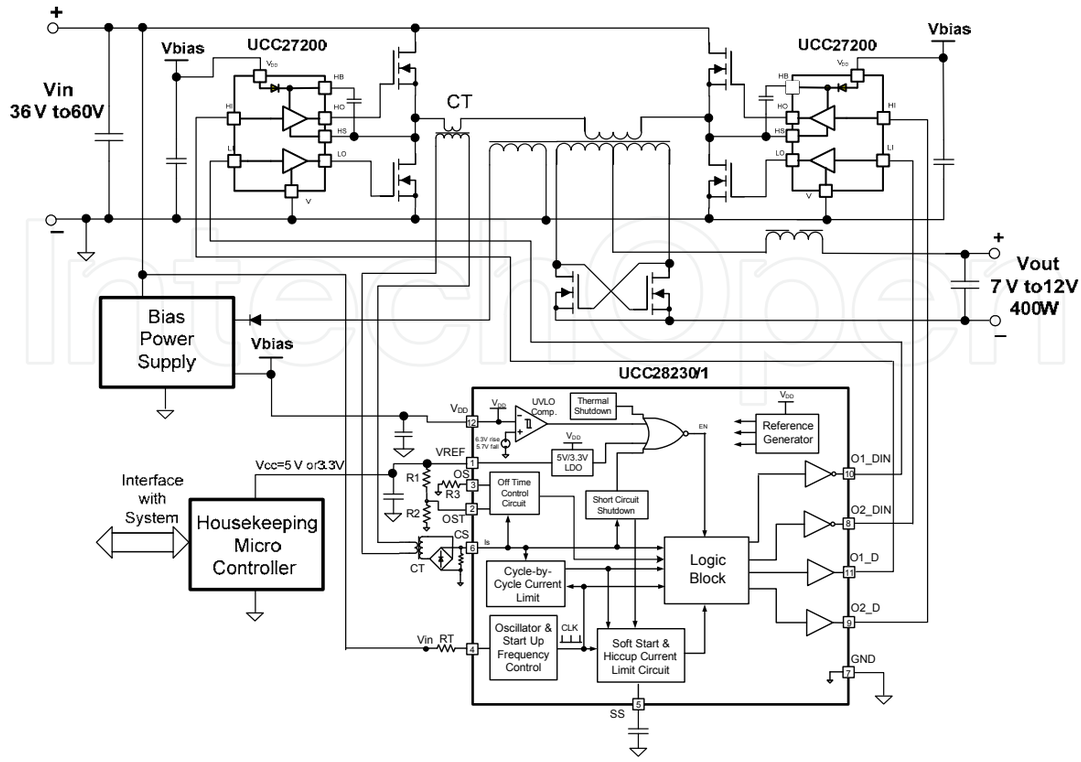


Fig. 24. Simplified diagram of typical full-bridge unregulated IBC

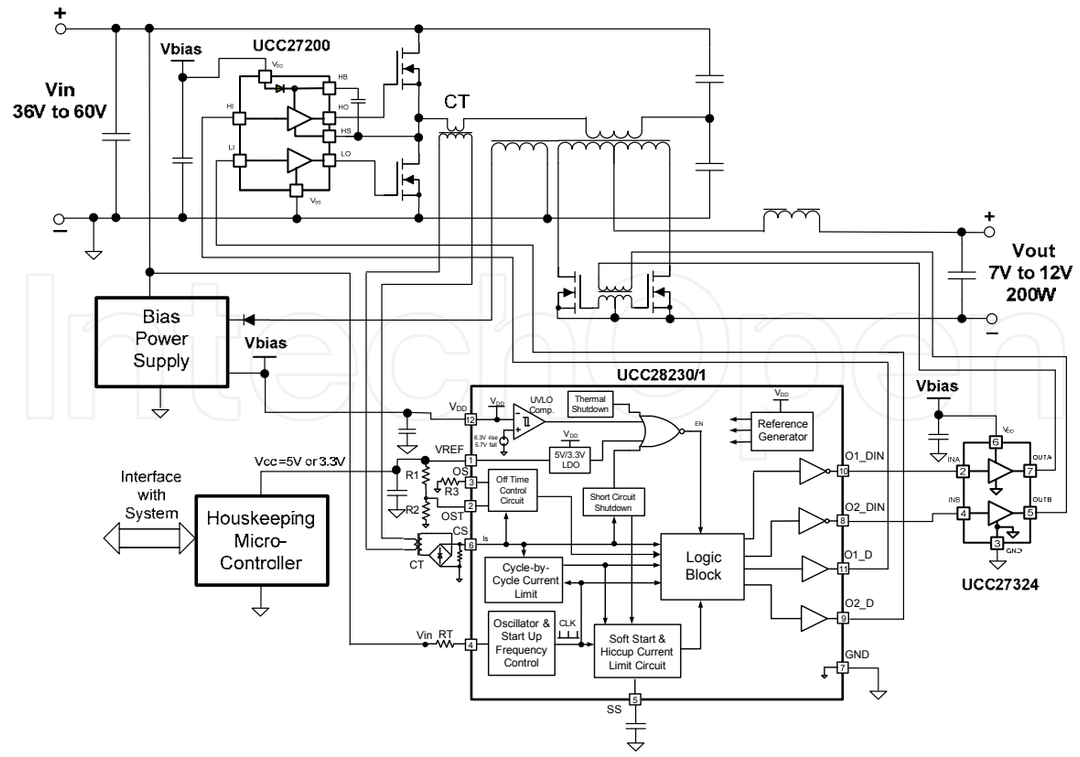


Fig. 25. Typical half-bridge unregulated IBC with control driven synchronous rectifier

E. Parallel Operation Issues

Parallel operation of IBCs is desirable in cases when the physical height is limited or when there may be a future need to easily upgrade to higher power levels. Paralleling can also be used for N+1 redundancy, but in this case, diodes in series with the outputs are needed to isolate a failed converter from the rest of the system. It is impossible to use any kind of active current-sharing technique with unregulated converters in parallel. The only option is to use a droop-current-sharing mechanism that depends on the output impedance of the converters sharing the current. Obviously, an accurate droop-current-sharing approach becomes more difficult as new IBC designs become more efficient. Additional problems related to sharing steady-state current can occur if all parallel IBCs do not start simultaneously. These problems include power circulation and tripping the over current protection circuit. Maintaining the secondary-side rectifier MOSFETs in the off state during the 1 – D cycle previously described is one way to prevent reverse current flow during parallel operation of unregulated IBCs.

F. Flux Balancing of Power Transformer

To reduce switching losses, unregulated IBCs use a relatively low 100- to 200-kHz switching frequency. The power transformers in the topologies shown in Figure 14 are expected to operate with a symmetrical B-H loop with no flux unbalancing for smaller size and reduced losses. One option to avoid flux unbalancing is using the gapped transformer. However, this approach increases a magnetizing current. Another option is to use a DC blocking capacitor in series with the primary winding of full-bridge converter shown in Figure 14a. For the half-bridge topology, this capacitor is already present as a necessary part of the power stage (Figure 14b). The potential issue with the DC blocking capacitor is that during cycle-by-cycle current limiting, significant variations in pulse amplitudes applied to the primary winding each half-cycle might occur. This pulse variation occurs because significant DC voltage can build up across the blocking capacitor that maintains volt-second balance of the transformer each half-switching cycle. Unequal amplitude pulses to the transformer windings cause over voltage stresses at the secondary side rectifier MOSFET. In many cases, careful layout and symmetrical matched output pulses from the controller and drivers can eliminate the need for DC blocking capacitor in the full-bridge converter. The simplest way to avoid unbalancing in a push-pull converter is to use cycle-by-cycle current limiting or a gapped transformer, because the DC blocking capacitor can not be used with this topology.

5.6 Experimental Results

The described advanced control improvements to an unregulated IBC were verified with a DC/DC module that had a 600-W output, a 48-V input, a 5:1 turns ratio, and a quarter-brick form factor. The controller used for these experiments was the UCC28230/1. More details about this controller can be found in (Texas Instruments, 2008. http://focus.ti.com/docs/prod/folders/print/ucc28230.html) The measured module efficiency, power losses, and output voltage are shown in Figs. 26, 27, and 28, respectively. In this example, the off time was set to a fixed time period. For this reason the output voltage shown in Figure 28 has an almost constant slope. The input-voltage measurements were Vin1 = 38 V, Vin2 = 44 V, Vin3 = 48 V, and Vin4 = 53 V. A comparison to the old controller that had an identical power stage, revealed an efficiency improvement of at least 1% over the full load-current range.

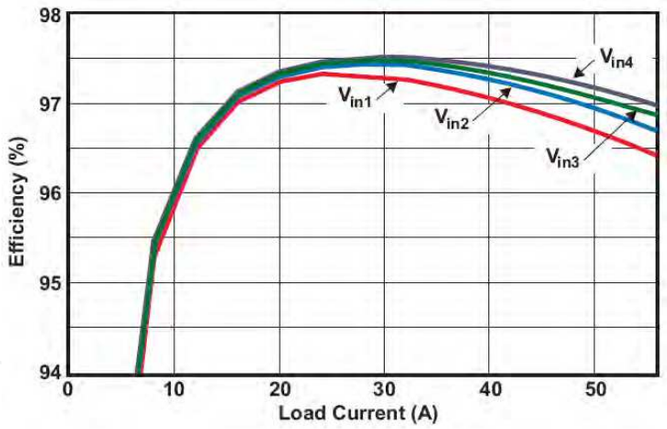


Fig. 26. Efficiency at 38V, 44V, 48V and 53V inputs over 0A to 56A output current range

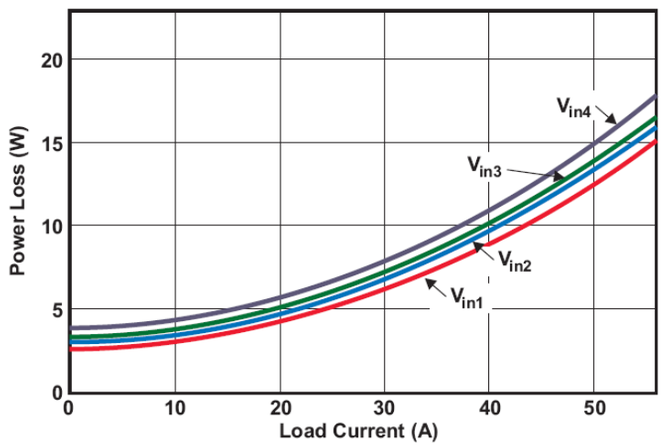


Fig. 27. Power losses at 38V, 44V, 48V and 53V inputs over 0A to 56A output current range

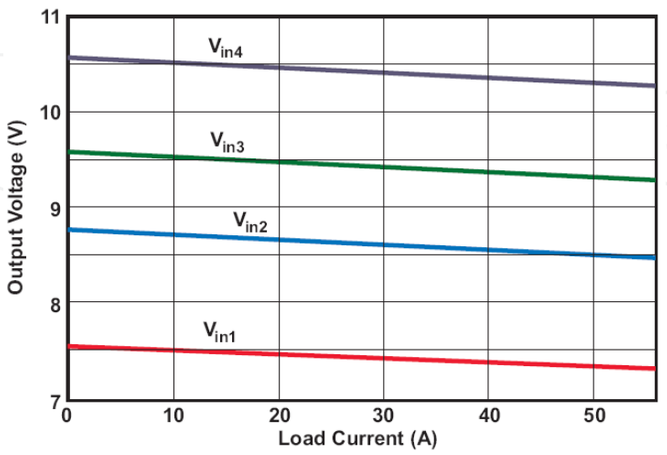


Fig. 28. Output voltage versus load current measurements

6. Conclusion

General market trends and new regulations to the telecommunication power system are discussed. It was shown, that to meet the new efficiency and power saving requirements, all system and design levels must be considered. Therefore, the focus was on review and comparison of the efficient, power saving solutions from the facility-level power system, to the cabinet level, followed by discussion of the specific requirements and solutions for the key functional blocks.

At the facility level, the new high voltage DC bus distribution system and its pros and cons have been described and compared. At the cabinet level, the brief history of power system evolution was shown. Pros and cons of different distribution power architectures were provided. Advantages and challengers of the evolving intermediate bus architecture were discussed in details including the optimal bus voltage analysis and selection.

The chapter discussed the requirements for telecom rectifiers and front-end server power supplies: the key functional parts of any data- and telecommunication power system.

Special attention was provided to the intermediate bus converters that are an enabling part of any IBA. Their requirements, key parameters, popular topologies, and design challenges were discussed in depth. The design example and test results of 600-W unregulated IBC converter with 48-V input and 5:1 transfer ratio was provided to illustrate and verify the recommended design approaches and solutions.

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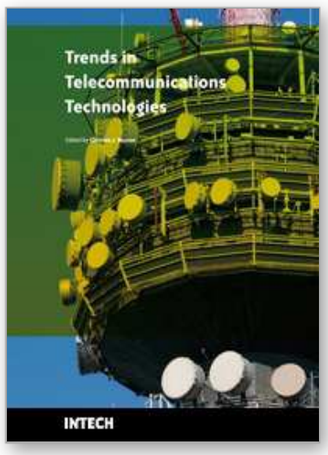

Trends in Telecommunications Technologies

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The main focus of the book is the advances in telecommunications modeling, policy, and technology. In particular, several chapters of the book deal with low-level network layers and present issues in optical communication technology and optical networks, including the deployment of optical hardware devices and the design of optical network architecture. Wireless networking is also covered, with a focus on WiFi and WiMAX technologies. The book also contains chapters that deal with transport issues, and namely protocols and policies for efficient and guaranteed transmission characteristics while transferring demanding data applications such as video. Finally, the book includes chapters that focus on the delivery of applications through common telecommunication channels such as the earth atmosphere. This book is useful for researchers working in the telecommunications field, in order to read a compact gathering of some of the latest efforts in related areas. It is also useful for educators that wish to get an up-to-date glimpse of telecommunications research and present it in an easily understandable and concise way. It is finally suitable for the engineers and other interested people that would benefit from an overview of ideas, experiments, algorithms and techniques that are presented throughout the book.

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