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A Novel PFC Circuit for Three-phase utilizing Single Switching Device

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1. Introduction

For consumer or industrial applications, electrical appliances use various types of rectifier, which give rise to distorted input current due their non linear characteristics. Problems are created by the various harmonics, generated in the power system. Under such circumstances, IEC guideline was instituted ten and several years ago, and has recently been superseded.(JISC.2005). With the spread of the use of such nonlinear equipments, it is anticipated that we can not avoid the problems due to harmonics. With the relatively increased capacity of industry applications, PWM rectifiers can be expected to be used in three phase and single phase applications. (Takahashi. 1985, IEEJ Committee. 2000). Also in office environments, OA equipments, inverter type fluorescent lamps and inverter type air-conditioners are frequently used, surely bringing harmonic problems with them. Under such conditions, various new type PFC schemes are presented and discussed. (Takahashi.1900,Fujiwara.1991,Takeuchi2005). Methods intending to improve the current towards a sinusoidal waveform by using switching devices will incur high cost performance and yet troublesome noise problems. Certain applications require a switch-less scheme to maintain the electromagnetic environmental standards. (Yamamoto. 2001, Takeuchi. 2007). Also in the future, main stream methods will intend to achieve sinusoidal waveforms. From thinking about research stream until now, more simplified method or low cost scheme would be discussed and developed in a similar manner also in the future. On the basis of the perceived requirements, in this paper, we propose and discuss a novel PFC circuit for three phase, employing a single switch in such a manner as to render the waveform as sinusoidal as possible.

2. Operational Principle

2.1 Prasad-Ziogas Circuit

Figure 1 shows a conventional circuit, comprising a three-phase circuit, using single switching device. (Prasad & Ziogas. 1991). The principle of operation is such that the three phase circuit is periodically shorted by a single switching device at a high frequency, so that the input current waveform is created in proportion to input voltage waveform. The input current waveform becomes synchronized with the input voltage, so that the circuit scheme

is constructed as PFC circuit. In this paper, this circuit is named the PZ (Prasad-Ziogas) circuit, one of these individuals being famous for contributions toward power electronics development.

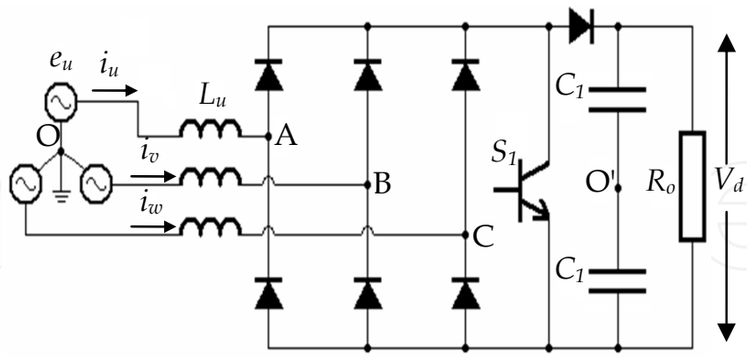
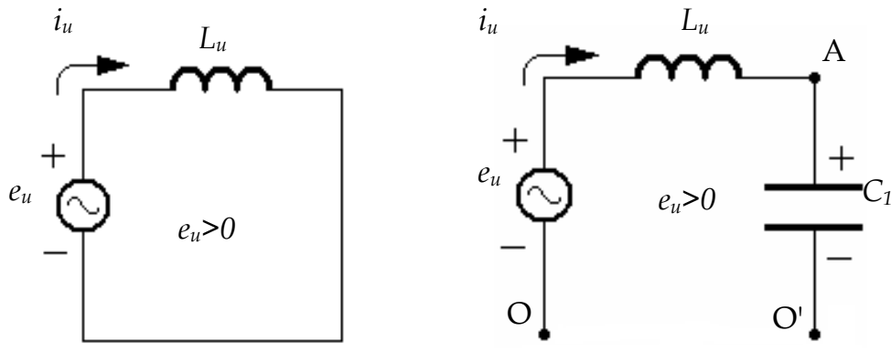


Fig. 1. Three-phase single switch PFC circuit by Prasad-Ziogas.



(*a*) S_1 turn-on (*b*) S_1 turn-off

Fig. 2. Equivalent circuit for Prasad-Ziogas.

Figure 2 shows the equivalent circuit of the PZ circuit. These characteristics may be explained as follows; In Figure 2 (*a*), when S_1 turns-on, the equivalent circuit is established as shown, where the operation will be explained as a current-discontinuous mode for simplicity of circuit analysis. In Figure 2 (*b*), the terminal voltage across O and O' of fictional neutral point can be derived from Figure 1, the amplitude being $E_0/6$ with an operational frequency three times supply frequency, where E_0 is the output dc link voltage. In Figure 2 (*a*), when S_1 is turned on, circuit equation can be established as follows;

$$e_u = L_u \frac{di_u}{dt} \tag{1}$$

The analogous equations can be described also in phase v and phase w. From Eq. (1), the input current is increasing in proportion to amplitude of e_u at S_1 turn-on. (see Figure 3 (*b*) and (*c*)). When the switch is turned-off, the equivalent circuit is established as shown in Figure 2 (*b*), where, by analogy with the other phases, the equations become as follows;

$$
\begin{aligned}
e_u - v_{AO} &= L_u \frac{di_u}{dt} \\
e_v - v_{BO} &= L_v \frac{di_v}{dt} \\
e_w - v_{CO} &= L_w \frac{di_w}{dt}
\end{aligned}
\tag{2}
$$

From these equations, it is clear that each phase current is decreasing in proportion to e_u-v_{AO} etc. These waveforms are shown for the S_1-off period in Figure 3. If the current waveforms are decreasing, as shown by the dashed lines, the resultant current values could be obtained in proportion to the input voltage values. However, the terms for attenuation, such as e_u-v_{AO}, are nonlinear. (see Figure 4 showing v_{AO}). Actual waveforms are attenuated by means of the terms like e_u-v_{AO} etc. (Murphy. 1985). If e_v, for an example, has a small value, the degree of attenuation may be small, so that a gently decaying dashed line would be obtained, as shown. In this example case, however, the attenuation term is e_v-v_{BO}, so that the attenuation degree becomes severe. As a result, the sharply decaying solid line can be obtained, because of significant attenuation, producing nonlinear waveforms.

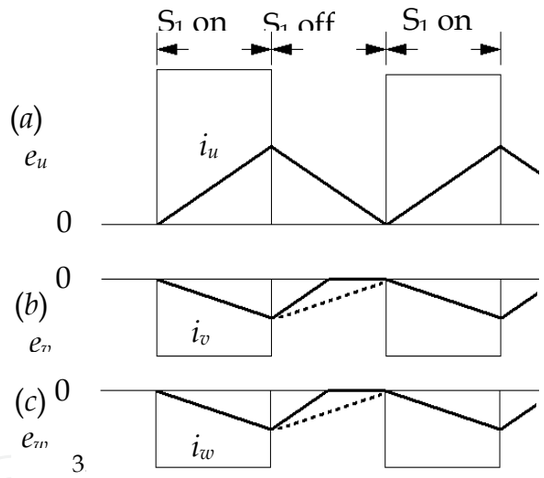


Fig. 3. Input current waveforms at S_1 switching.

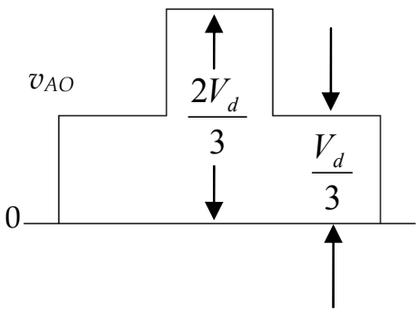


Fig. 4. Conceptual voltage waveform, v_{AO}.

Figure 4 shows conceptual waveform as v_{AO}. When S_1 is turned-off, the corresponding diode conducts. Depending on whether the amplitude of v_{AO}=2V_d/3 or V_d/3, where V_d is the output voltage, the degree of attenuation at S_1 turn-off is varied.

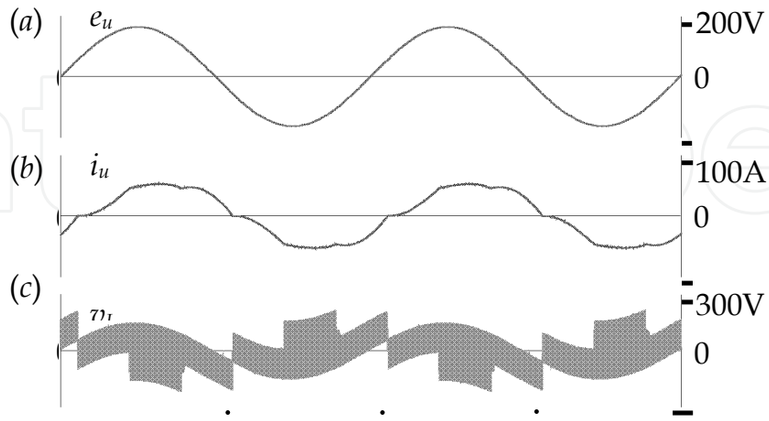


Fig. 5. Explanation of distorted input current waveform in conventional method.

Figure 5 shows the operational waveforms for Figure 1 from circuit simulation. From these figures, the reasons for waveform distortion in the conventional input current can be explained to a certain extent. From the phase voltage, e_u, in Figure 5 (*a*), the input current waveform, i_u, appears as in Figure 5 (*b*), using single device switching. It can be found that the envelope of a six stepped waveform v_{AO} appears and the distortion of i_u is generated as in Figure 5 (*b*). The term e_u-v_{AO} in (2) appears as an envelope of the applied voltage across the input inductor in Figure 5 (*c*). From equation v_L=$L_u di_u/dt$, it can be seen that the integral of v_L becomes the input current, i_u, so that the improvement scheme for input current waveform can be determined from observing the inductor voltage wave, v_L, to a certain extent.

2.2 Operation Principle of the Proposed Circuit

Figure 6 shows one of the proposed types of, three-phase, single switch converter. In this paper, we will discuss the boost type converter. In the future, however, it may be possible that a buck type converter could be realized under adequate discussion. Thus, this paper title does not restrict the concept to the boost type converter. The circuit configuration originates from the above mentioned Prasad-Ziogas circuit. The notable feature is that several electrolytic capacitors are parallel-connected to rectifying diodes. By means of this configuration, the input voltage circuit is always connected to either dc output bus, so that continuity and improvement of the input current can be realized. In such a way, a boosted dc voltage, utilizing the PFC scheme, can be obtained in comparison to the conventional circuit. The circuit operation can be roughly divided into six periods, where each period is 60 degrees. From the operation waveforms in Figure 7 and the operational periods shown in Figure 8, the circuit operation can be discussed. To simplify the analysis of the operation, we will assume a unity power factor of phase, u, where fundamental voltage and current components are almost synchronized with each other.

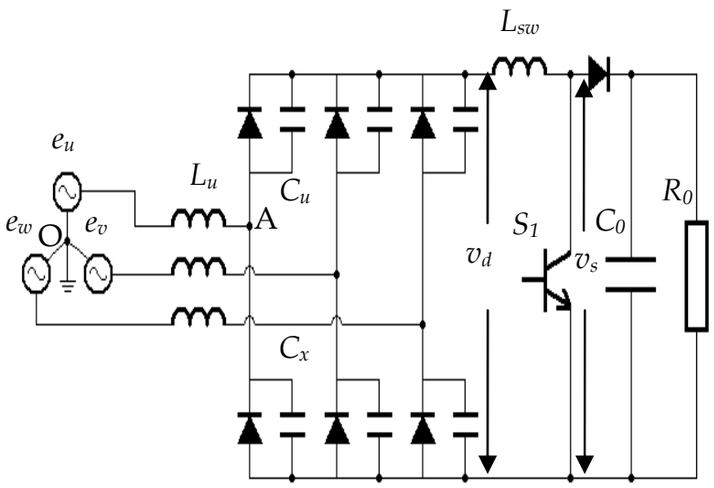


Fig. 6. Proposed circuit configuration.

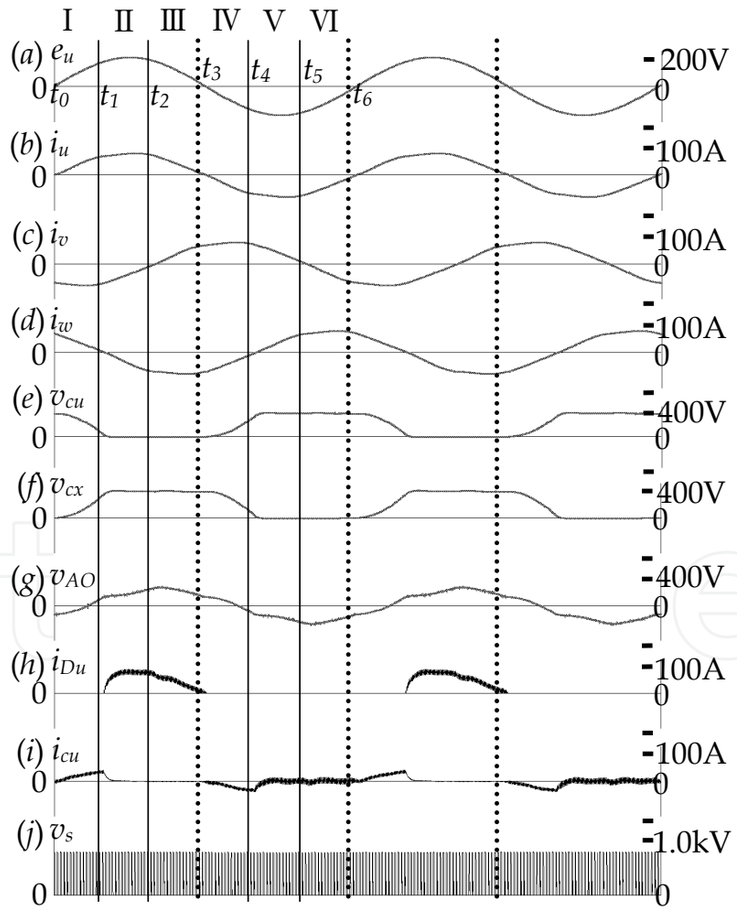


Fig. 7. Waveforms for proposed circuit.

(a) period Ⅰ (t_0<t<t_1)
The voltage in phase u is gradually increasing from e_u=0. In usual three phase circuit, the current at small values of supply voltage can not be rising due to a large dc link voltage, so that the current becomes zero for usual circuits, or suppressed to fairly reduced value, even in the Prasad-Ziogas circuit. In the proposed circuit, however, the capacitor voltage, v_{cu}, is gradually discharged from being fully charged at the dc link voltage. (see Figure 7 (*e*)). During this discharging period, diode current, i_{Du}, does not flow. In the other phases, v and w, diodes, D_v and D_w, conduct, although parallel-capacitor currents do not flow. The capacitor charge and discharge currents, i_{cu} and i_{cx}, each of which are connected to the constant dc link voltage, are equal, i.e., $|i_{cu}|=|i_{cx}|=|i_u/2|$. These results can be derived from the equation $C_u \times dv_{cu}/dt = -C_x \times dv_{cx}/dt$. In Figure 7 (*h*), (*i*) and (*b*), these results can be seen as $i_{Du}+2i_{Cu}=i_u$. The diode current in phase w is decreasing toward zero as e_w decreases. When this voltage polarity is reversed, and the D_w current is commutated to D_z circuit, this period comes to an end.

(b) period Ⅱ (t_1<t<t_2)
As the capacitor, C_z, in parallel with D_z, is charged to $v_{cz}=v_d$, this period starts from the beginning of the discharge current i_{cz}. The current, D_u, in phase u and the current, D_y, in phase v continue to flow, supplying the dc bus. At the end of this period, the voltage, e_v, is reversed and i_v is greater than zero.

(c) period Ⅲ (t_2<t<t_3)
The voltage, e_v, begins to rise and the commutation from D_y to D_v commences. The capacitor voltage, v_{cv} , is varied in a similar manner to v_{cu} in period Ⅰ. The current, i_v, rises from the zero point of e_v. In phase u, the current, i_u, is decreasing toward zero according to the decrease in e_u, when this period comes to an end.
In the subsequent period of negative e_u, an analogous operation is repeated such as a commutation of D_u to C_x and D_x etc. A remarkable characteristic of this strategy is that there is no discontinuity of the input current wave, as compared to the conventional three phase diode circuit having 120 degree current wave. In the proposed method, on the other hand, one terminal is always connected to either dc link circuit through a capacitor, achieving a continuous and improved waveform. In this paper, the boost chopper strategy has been considered and discussed, such that the stored charge is forced to flow from capacitors, so that the functions of charge and discharge become more efficient and smoothing of the input current becomes more effective. As an indication of the improvement of input current waveform, the v_{AO} waveform is shown in Figure 7 (*g*). This waveform can be derived from the conventional six step inverter circuit by an analogous procedure. In the proposed circuit, however, due to the intermediate capacitors, the v_{AO} waveform becomes smoothed, as shown in Figure 7 (*g*). Through such improved waveforms, instead of usual six step wave v_{AO} as in Figure 4, input current waveform can be improved, as shown in Figure 7 (*b*).

3. Operational Characteristics

By employing circuit constants in Table 1, various characteristics can be resolved. The operational waveforms in Figure 7 can be resolved by using these circuit constants. Figure 9

shows the relationship between output power and THD. The characteristics are compared between the conventional and

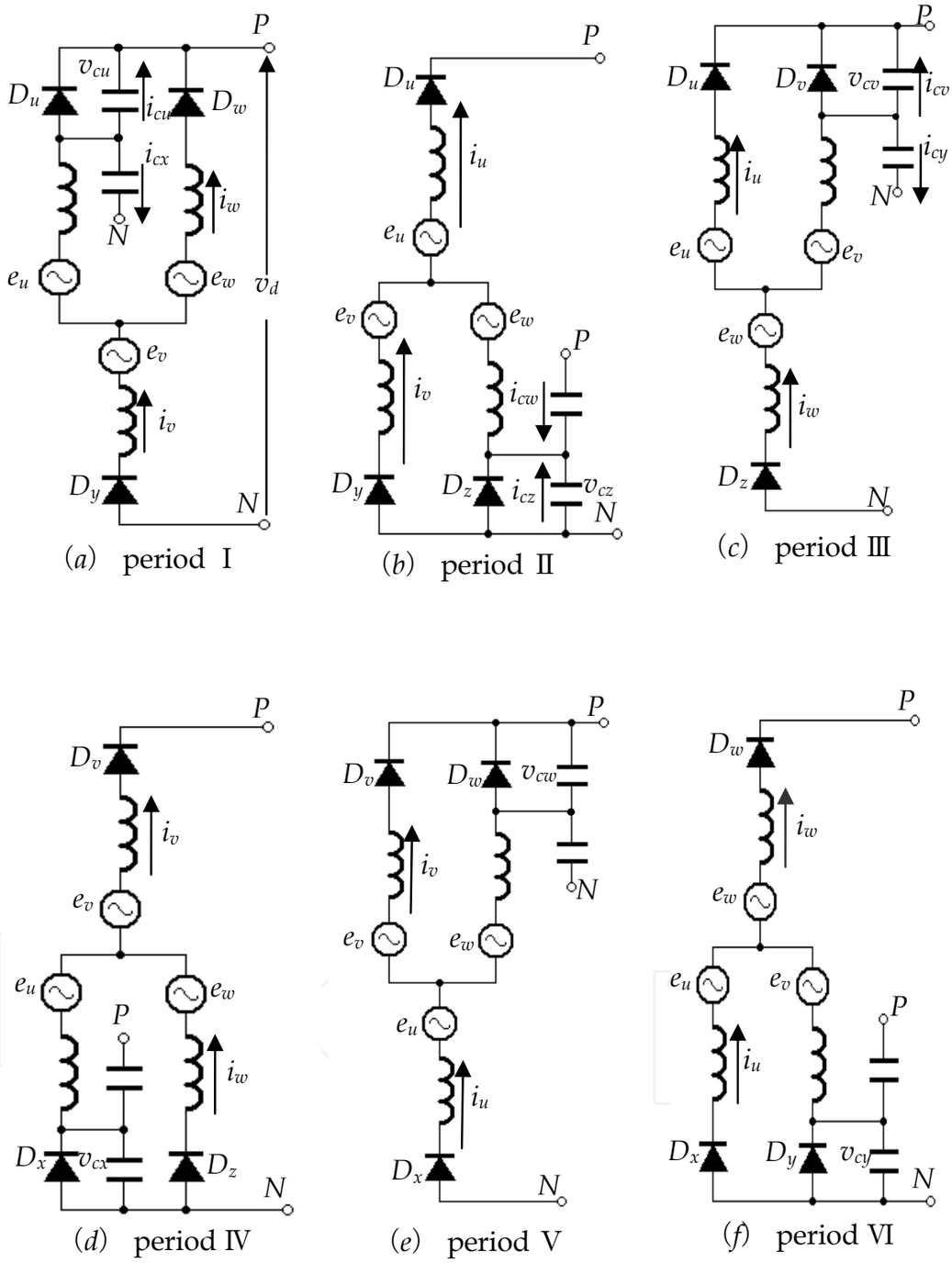


Fig. 8. Operating circuit.

proposed methods, where the input inductors are taken as parameter. In the reduced power region of conventional circuit, the THD is deteriorated. In a region of increased power of the circuit, the harmonics are relatively suppressed due to the function of the input inductor, and the THD can be improved. For the proposed circuit, in this manner, the THD can be entirely suppressed and improved.

L_L: Line inductance	0.25 mH
R_s: Line resistance	0.2 Ω
L_{in}: Input filter inductance	
proposed	5 mH
conventional	3 mH
L_{sw}: Switching inductance	0.2 mH
C_a: Auxiliary capacitance	150 μF
C_o: Output capacitance	6000 μF
R_o: Load resistance	
proposed	42 Ω
conventional	22 Ω
f_{sw}: Switching frequency	20 kHz
v_s: Supply line voltage	200 V
f_s: Supply frequency	60 Hz

Table 1. Circuit constants

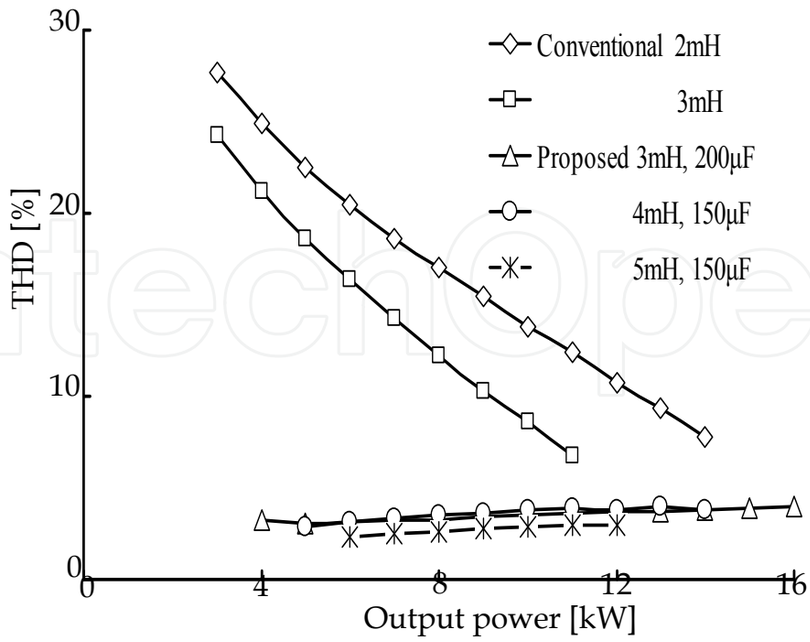


Fig. 9. Relationship between output power and THD.

In a region of more increased power for the conventional method, we might expect that a more improved THD could be obtained, but the actual result is to the contrary. Because voltage drop across the input inductor is significant in the increased power region, a more increased power can not be obtained. Due to an LC resonant operation, where the stored electric charge in the C is charged and
discharged, a little increased power can easily be obtained, offering one remarkable feature of this strategy.

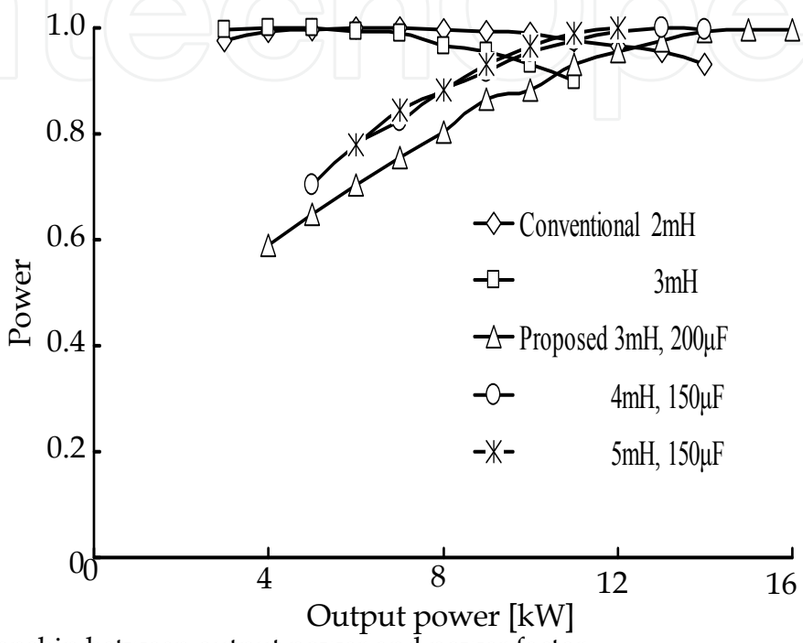


Fig. 10. Relationship between output power and power factor.

Figure 10 shows the relationship between the output power and power factor using the same circuit constants from Table 1. In the conventional circuit, as the output power is increased, the power factor is reduced a little. The reason is that the voltage drop across the input inductor is fairly significant. In the proposed method, however, though the THD characteristic is much improved, the power factor characteristic is a little deteriorated. For this reason, it could be said that this strategy is unsuitable for an application requiring the avoidance of reduced power factor over a variable wide power range. Rather, it is suitable for an application requiring constant output power or extended operation term with constant power.

Figure 11 shows the relationship between auxiliary capacitance, C_a, and the THD. Results at C_a=0 are represented for Prasad-Ziogas circuit, where THD is 12% of deteriorated value. Employing the proposed auxiliary capacitance, however, as the value of capacitance is increased, the THD characteristic is fairly improved, where output power is adjusted so as to maintain unity power factor. Consequently, as the capacitance is increased, the input current and the power are also increased, as shown by dotted line in Fig 11. Such increased current can partly contribute an improvement in the THD.

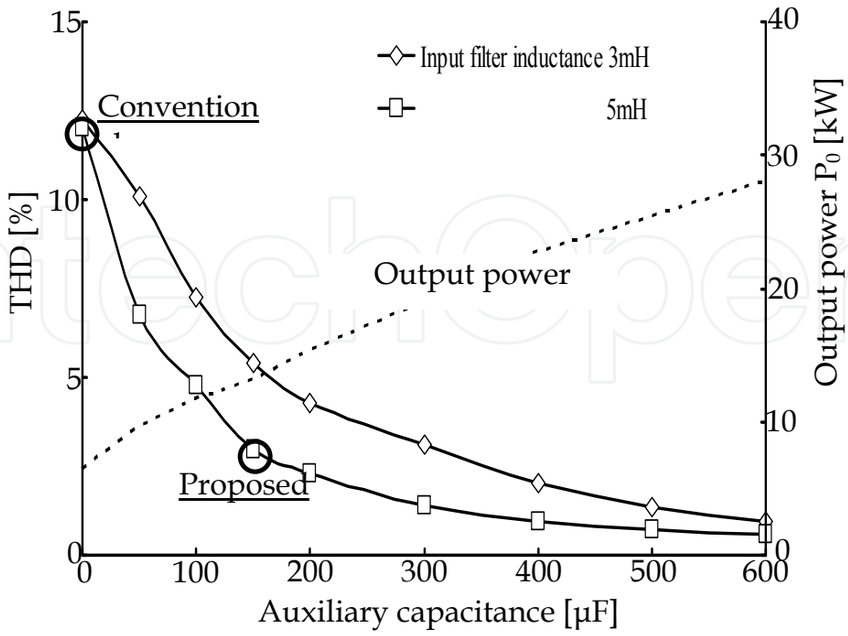


Fig. 11. Relationship between auxiliary capacitance and THD.

4. Development to Buck-converters

This paper discussed about boost type converters, but those type ones can be easily develop toward any type of converters. In this section, we will discuss about the application for buck type converter in single phase. Figure 12 shows such proposed circuit for buck converter, where previously mentioned auxiliary intermediate capacitors are installed. In this circuit configuration, the intended characteristics could be realized. The basic circuit is constructed by the conventional buck-converter. The distinctive feature of the discussed circuit is to be described as follows: Previously mentioned relatively large capacitors such as electrolytic ones are parallel-connected to diodes in a similar way. By means of those connections, the input circuit is always connected to either terminal of the dc link circuit, such as positive or negative one, which makes possible the input current continuity and the improvement of input current waveform. In general, for buck-type converter when the PFC circuits are designed both for three-phase and single-phase, it might be difficult to construct the suitable PFC ones, even with fairly large inductions or transforms. The distinctive feature of the proposed strategy employs a very simple way, in which some electrolytic capacitors are merely parallel-connected. By means of this parallel connection of capacitors, non-linearity of input current waveform becomes linear one, which brings the waveform improvement. In the usual buck chopper circuit having the constant dc link voltage, the output current does not flow in a certain period. This feature brings non-sinusoidal waveforms. In a case of the proposed circuit, the dc link voltage is constructed by the sum of series-connected double capacitor voltage such as $v_{C1} + v_{C2}$. As a result, due to assistance of each capacitor charge and discharge operation, the input current always cntinues to flow, though the dc link voltage v_R becomes constant , so that each appearance should be in sinusoidally wave.

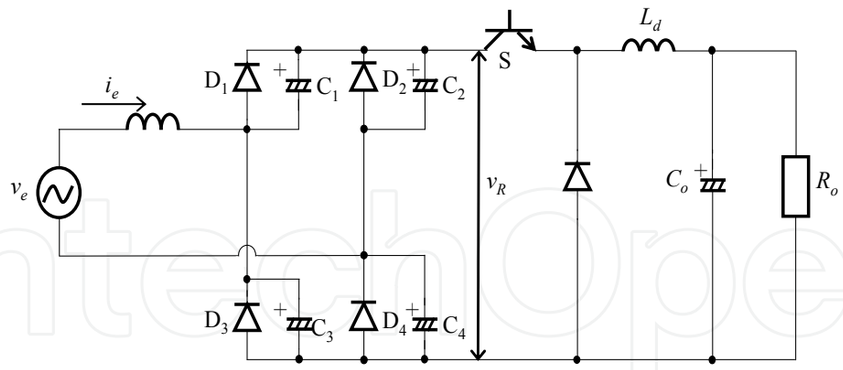


Fig. 12. Development to buck-converter.

5. Conclusions

An improved circuit strategy has been proposed and discussed, based on an extension of the Prasad-Ziogas circuit, offering significant improvement in the THD characteristic. The results have been presented and compared. The proposed circuit uses single switching device like the conventional one and the characteristics can be improved sufficiently by using a simple auxiliary capacitor connection. In this way, a three phase PFC circuit can be realized in a simple manner. Another feature in the proposed circuit is the ability to obtain a fairly increased power capacity, making the circuit suitable for high capacity converter.
However, the circuit is employs several capacitors in the series current path. As a result, a somewhat reduced power factor region is observed, particularly in the lower output power region. Consequently, the circuit is unsuitable for an application requiring a wide variable power range and a reduced power operation for a long period.
In the future, after further consideration and discussion, a novel buck-type converter using proposed method might be realized.

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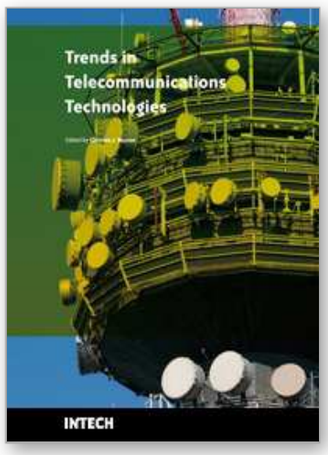

Trends in Telecommunications Technologies

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The main focus of the book is the advances in telecommunications modeling, policy, and technology. In particular, several chapters of the book deal with low-level network layers and present issues in optical communication technology and optical networks, including the deployment of optical hardware devices and the design of optical network architecture. Wireless networking is also covered, with a focus on WiFi and WiMAX technologies. The book also contains chapters that deal with transport issues, and namely protocols and policies for efficient and guaranteed transmission characteristics while transferring demanding data applications such as video. Finally, the book includes chapters that focus on the delivery of applications through common telecommunication channels such as the earth atmosphere. This book is useful for researchers working in the telecommunications field, in order to read a compact gathering of some of the latest efforts in related areas. It is also useful for educators that wish to get an up-to-date glimpse of telecommunications research and present it in an easily understandable and concise way. It is finally suitable for the engineers and other interested people that would benefit from an overview of ideas, experiments, algorithms and techniques that are presented throughout the book.

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