10

Implementation of Low Phase Noise Wide-Band VCO with Digital Switching Capacitors

Meng-Ting Hsu, Chien-Ta Chiu and Shiao-Hui Chen
Microwave Communication and Radio Frequency Integrated Circuit Lab
National Yunlin University of Science and Technology,
Department of Electronic Engineering
Yunlin, Taiwan, Republic of China

1. Introduction

In present fast-growing wireless communications, requires wide bandwidth, low-power and low-cost RF circuits [1]. In Fig. 1, it is a simple super-heterodyne transceiver [2], and in this diagram, VCO (voltage-controlled oscillator) is one of the most important building blocks in the wireless communication system. An optimum performance VCO should include low phase noise and wide bandwidth to support several communication standards of wireless transceiver, and low power design technique to enhance the battery lifetime. Recently, the standard CMOS process technology is better choice to overcome low-cost challenge. The choice is also favored by the possibility of system-on-chip integration with digital parts, which should save the total chip area and cost. The VCO with multi-band and wideband are the current trend [3] - [8]. The methods of increasing tuning range are classified as follows, switching inductors or variable inductor [3], switching capacitor modules [4], [5], varactors in parallel [6], [7] and capacitive source degeneration [8]. It is a well-known fact that the Lesson's model of the single-sideband power spectral density is given by [9]:

$$L\{\Delta w\} = 10\log\left[\frac{2FKT}{P_s}\left[1+\left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right]\cdot\left(1+\frac{\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \quad (1)$$

Where FKT is the effective thermal noise with the multiplicative factor F, Boltzmann's constant K, the absolute temperature T; P_S is the average power dissipated in the resistive part of the tank; Aft is the offset frequency; Q_L is the effective quality factor of the tank and is dominated by quality factor of spiral inductor; ω_0 is the center frequency and ω_{1/f^3} is the corner frequency of the flicker noise. The model describes well the shape of the spectrum, and realizes that many parameters affect phase noise performance. Circuit design tradeoff of the device parameters is required.

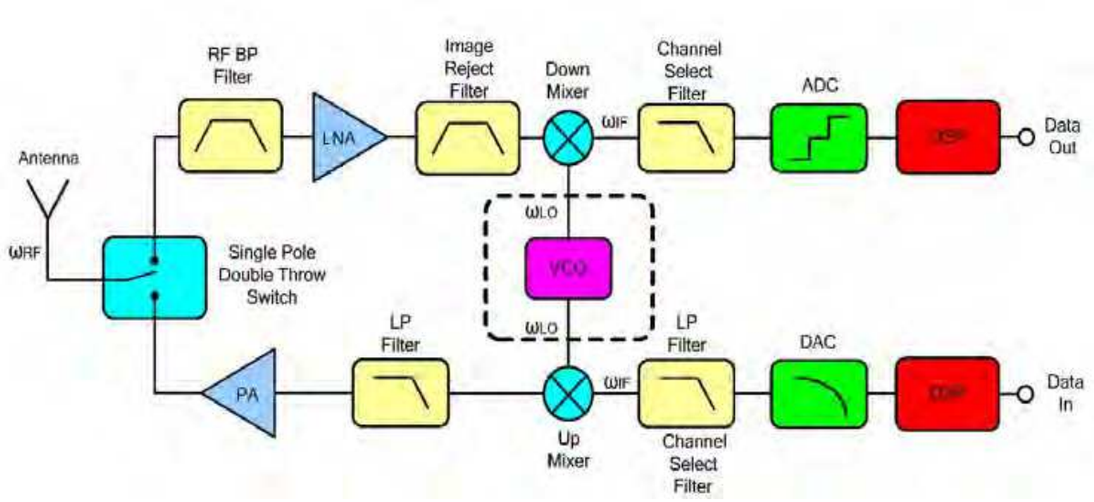


Fig. 1. Building blocks of super-heterodyne transceiver [2]

2. VCO Design

VCO must be designed carefully, its performance affects the stability of the VCO in the transceiver. This section studies how to optimize the circuit design and establish the design procedure for a voltage-controlled oscillator (VCO) in the front end of a transceiver. It promotes the better quality of communication by decreasing the power dissipation and phase noise. This VCO has good data performance between the simulation and measurement.

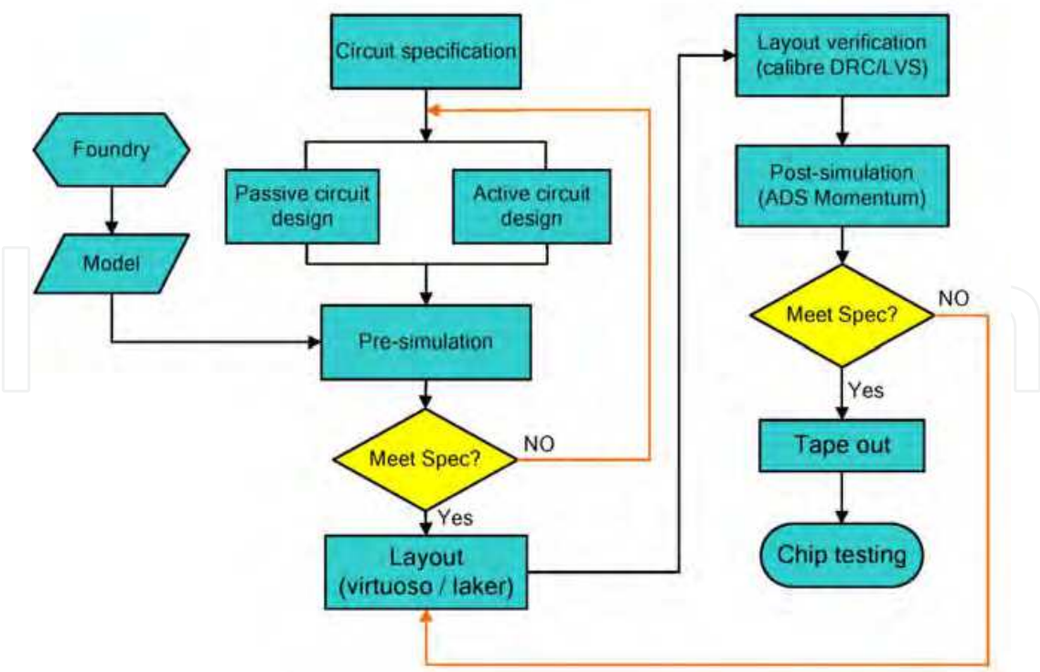


Fig. 2. Design flow of VCO

2.1 Design flow of VCO

This VCO was made by TSMC (Taiwan Semiconductor Manufacturing Company) standard 0.18|μm 1P6M CMOS process technology. In Fig. 2, design process can be divided into the following steps: Step 1: Review of related literature, and make design specification. Step 2: Design passive and active circuit of the VCO topology.
Step 3: It is pre-simulated by Agilent Advanced Design System (ADS) with TSMC 0.18|μm RF CMOS process model and fabricated by TSMC 0.18|μm CMOS technology. It is need to redesign if the pre-simulation result and design goal are different.
Step 4: IC layout design using cadence virtuoso and laker.
Step 5: Layout verification using Calibre DRC (Design Rule Check) and LVS (Layout Versus Schematic).
Step 6: Using the EM simulator with ADS Momentum to perform a numerical electromagnetic analysis of the layout. It is
need to re-layout if the post-simulation and pre-simulation results are different.
Step 7: The chip is fabricated by TSMC (Taiwan Semiconductor Manufacturing Company) 0.18|μm 1P6M standard CMOS process technology.
Step 8: The chips are measured on PCB board or on-wafer.

2.2 Simple LC Tank VCO Structure

In Fig. 3, we can analyze several important parts of this simple LC tank VCO structure:
The part A-LC tank: The tank circuit consists of a high-Q inductor and varactor components. Select the model values of inductor and varactor for control oscillatory frequency. Where, *Rp* denotes the passive element loss of LC tank. The part B-Active circuit: Active circuit is used to provide negative resistance to compensate for the loss of the LC tank. The part C-Buffer: The buffer is designed to drive the 50 ohm load of the testing instruments.

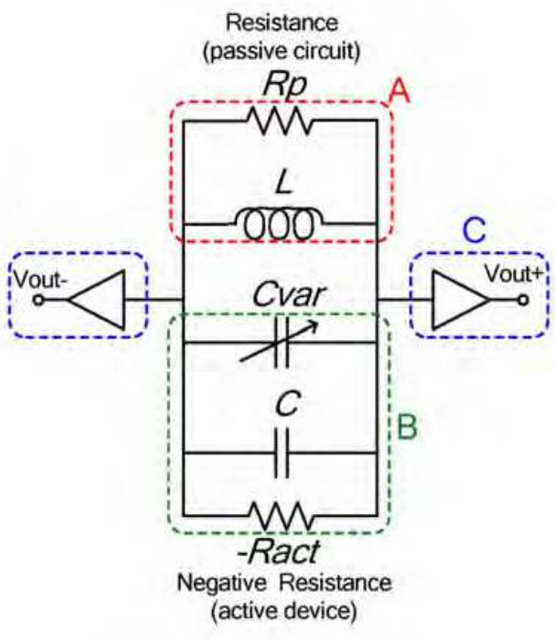


Fig. 3. Simple LC tank VCO structure

2.3 Schematic of the proposed VCO

In Fig. 4(a) shows the narrowband VCO which is composed of the complementary cross-coupled pair MOSFETs, LC tank and switching tail current transistors. In addition, we add the switching capacitor modules for wideband application in Fig. 4(b). A wide-tuning range VCO usually accompanies large Kvco (gain of VCO, Kvco=dω/dVtune). But large Kvco of VCO will amplify noise on the control node (Vtune) and hence will degrade the phase noise performance. We design the small size of PMOS varactors which are capable of providing a small gain of VCO, an array of binary switching capacitor modules were used to extend the tuning range. In this section we discuss several components such as complementary cross-couple pair, LC tank, switching tail current and switching capacitor modules.

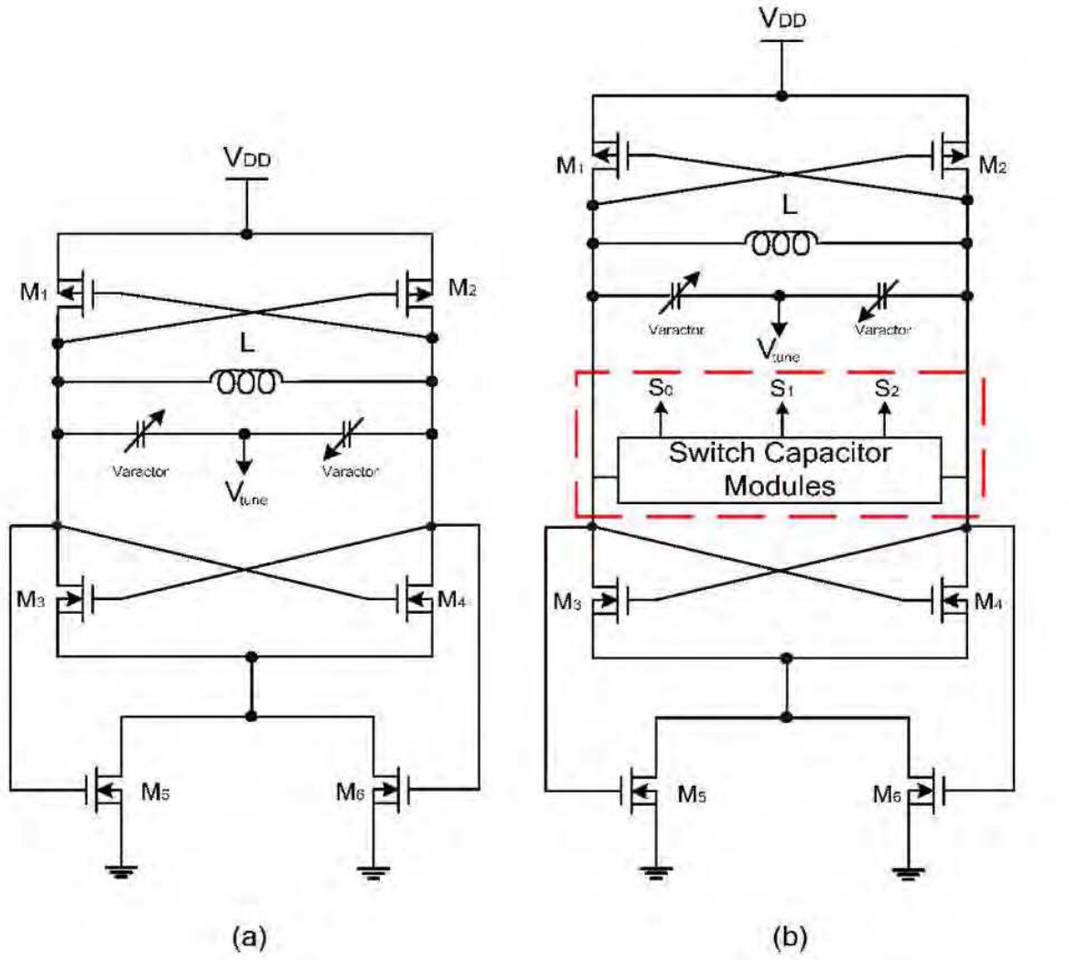


Fig. 4. Circuit schematics of (a) narrow band VCO without switching capacitor modules; (b) wide band VCO with switching capacitor modules

2.3.1 Complementary cross-couple pair

There are three merits in the complementary cross-coupled pair which described as follows [10]:
A. Same current existing, the complementary cross-coupled pair offers higher transconductance and faster switching speed on each side.

B. The output wave are more symmetrical on each other for rise-time and the fall-time, as debate the noise which comes from low frequency noise, 1/f, transferring to high frequency.
C. In all NMOS structure, the channel voltage is larger than complementary case, Therefore, it causes faster saturation speed and larger γ value [11].
The simple schematic of NMOS cross-coupled pair is shown in Fig. 5. T1 and T2 indicate NMOS transistors. The high frequency equivalent circuit with capacitive parasitic is shown in Fig. 6(a). And the calculation of input impedance or admittance of the simplified equivalent circuit is shown in Fig. 6(b).

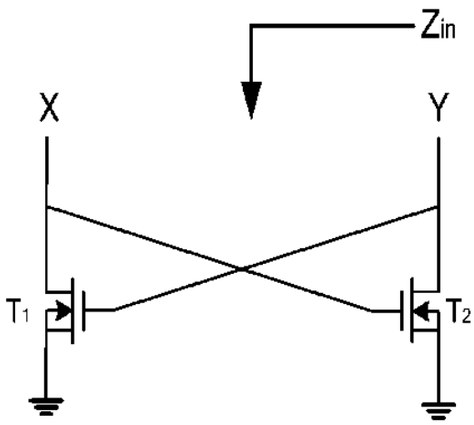


Fig. 5. Simplified schematic of NMOS cross coupled pair

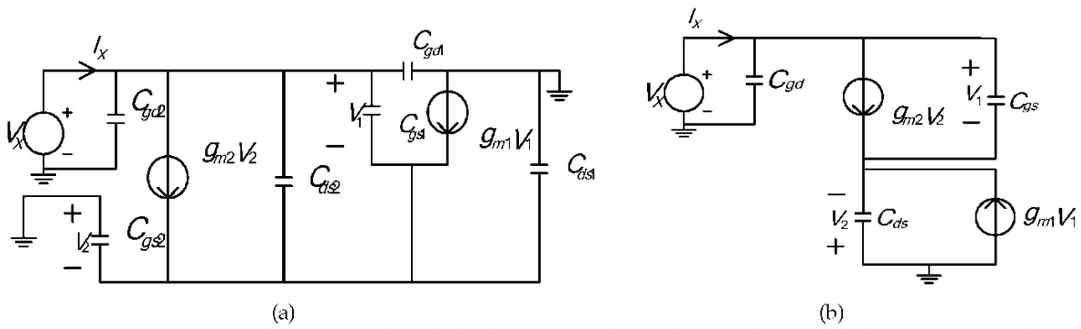


Fig. 6. Small signal model of Fig. 5 for (a) high frequency equivalent circuit; (b) equivalent circuit of impedance calculations

Let $C_{gd} = C_{gd1} // C_{gd2}, C_{gs} = C_{gs1} // C_{gs2}, C_{ds} = C_{ds1} // C_{ds2}$ for simple calculation of the circuit.
We can obtain the input impedance Z_{in} as following:

$$Z_{in} = \frac{V_X}{I_X} = \frac{\dfrac{1}{g_{m1} + sC_{ds}} + \dfrac{1}{g_{m2} + sC_{gs}}}{1 + \dfrac{sC_{gd} - g_{m1}}{g_{m1} + sC_{ds}} + \dfrac{sC_{gd} - g_{m2}}{g_{m2} + sC_{gs}}} \tag{2}$$

If the transistors size are the same, we can assume that $g_{m1} = g_{m2} = g_m$ and $C_{gs} \approx C_{ds}$ for microwave range in simplified calculation with small dimension device [12]. The Eq. (2) becomes as following:

$$Z_{in} = \frac{2}{-gm + 2sC_{gd} + sC_{ds}} \tag{3}$$

If $s = j\omega$ is used, then Eq. (3) can be written as following:

$$Z_{in} = \frac{-2gm}{gm^2 + \omega^2 \left(2C_{gd} + C_{ds}\right)^2} - j\frac{2\omega\left(2C_{gd} + C_{ds}\right)}{gm^2 + \omega^2 \left(2C_{gd} + C_{ds}\right)^2} \tag{4}$$

If Eq. (4) $Z_{in} = R_a - jC_a$, then R_a and C_a can be expressed as :

$$R_a = \frac{-2gm}{gm^2 + \omega^2 (2C_{gd} + C_{ds})^2}, \quad C_a = \frac{2\omega(2C_{gd} + C_{ds})}{gm^2 + \omega^2 (2C_{gd} + C_{ds})^2},$$

where, R_a is the real part and C_a is the imaginary part, respectively. And the parameters of active device are represented in Fig. 7.

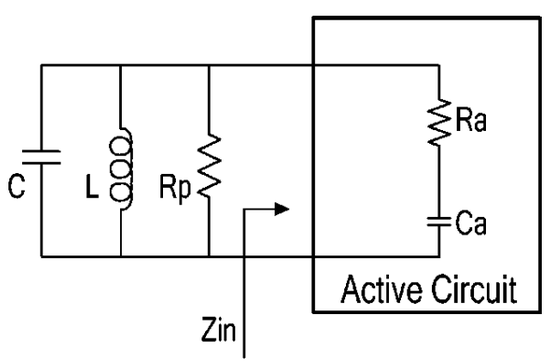


Fig. 7. Parallel LC oscillator model

When the parasitic is ignored, the traditional negative resistance of the input port is indicated by *-2/gm*. Although the complementary topology has more devices than the NMOS pair, the differential voltage swing is larger for the same current consumption resulting in reduce phase noise. The M1 ~ M4 transistors of a complementary cross-coupled pair are shown in Fig. 4, which yield $-\left(\frac{2}{g_{mn}} // \frac{2}{g_{mp}}\right)$ negative resistance to compensate the passive element loss of LC tank.
It can be achieved to start up for oscillation [13] and output signals of the circuit are differential.

2.3.2 Switching tail current

The circuit with a tail current can improve the effect of various noise sources and supply sensitivity [11], and some researchers discovered that a square wave cycling a MOS transistor from strong inversion to accumulation reduces its intrinsic 1/f noise [14]. Therefore, switched biasing can be useful in many circuits to reduce the up-conversion of noise 1/f [15]. The flicker noise from tail current source, especially in MOSFET transistors, makes a great deal of phase noise. Gradually switching tail transistors can release trapped electrons in FET channel, which results in decreasing flicker noise. Moreover, this technique can not only reduce 1/f noise up-conversion but also save power as well. The bias of tail current source was replaced by switched bias without extra DC bias [15] [16]. Utilizing the output voltage swing V1, V2 control M5, M6 which is switched turn on. The output voltage swing is 1.16~1.18V in Fig. 8. In order to determine behavior of the switching, the tail current can't too small. If it is too large, the power consumption is increased, so we need to tradeoff switching behavior, power consumption and phase noise.

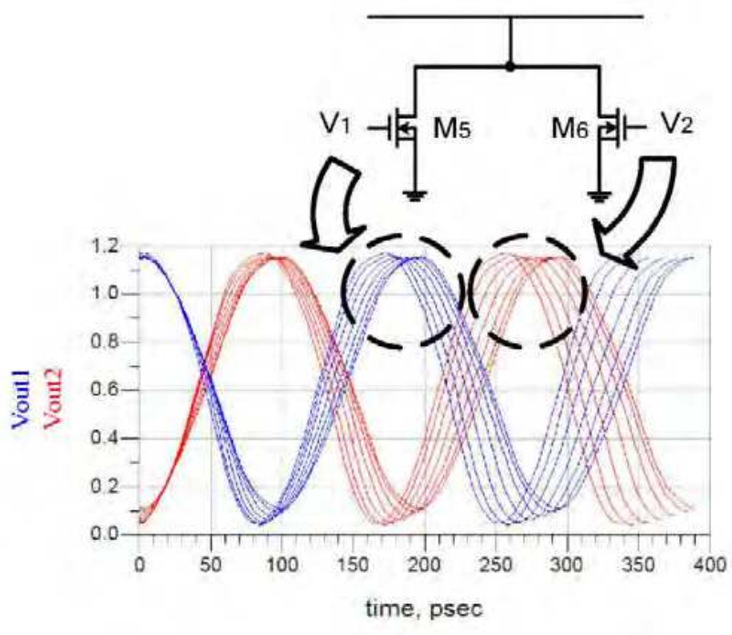


Fig. 8. The output voltage swing with switching tail transistors

The comparison of simulated phase noise performance between fixed bias and switched bias of different tail current topology is shown in Fig. 9.

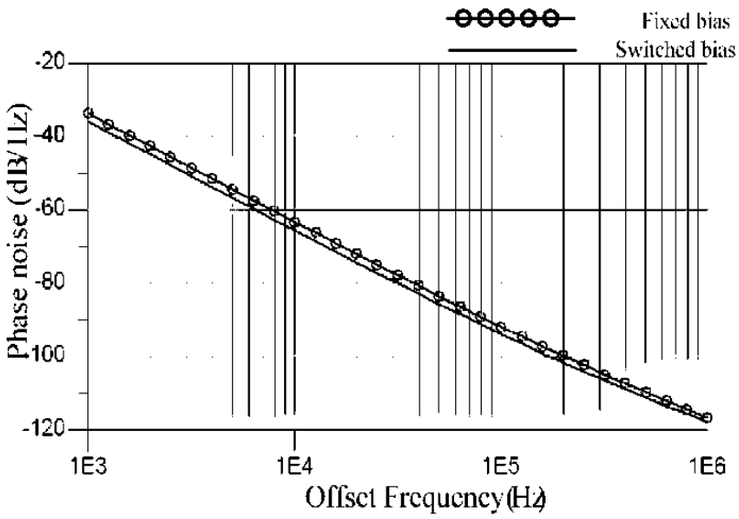


Fig. 9. Phase noise comparison between fixed bias and switched bias at 5 GHz

2.3.3 LC tank

We establish the simulation parameters of Si-substrate and the circuit models of inductors. The resonating tank causes the current in the tank to be Q times larger. Hence the metal lines connecting the LC tank need to be sufficiently large to withstand the large current [17]. In Fig. 10, the quality factor of inductor in this chip is approximately 11 over the working frequency range. The capacitance range of MOS varactor is wider than junction varactor and the equivalent series resistance of the former is smaller than that of the latter. Because using NMOS varactor that drawback is apt to be disturbed in substrate. NMOS capacitor could not implemented in the separate P-well, so NMOS capacitor has high sensitivity of noise that induced by substrate than PMOS capacitor. In view of this, we adopted PMOS varactor.

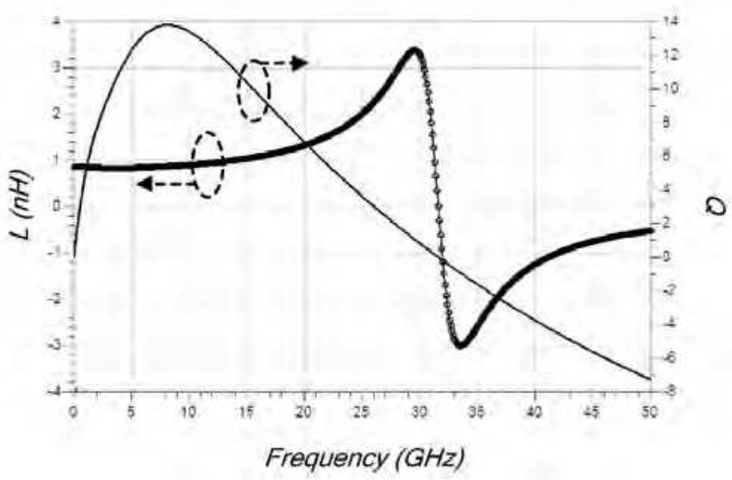


Fig. 10. Inductance and quality factor (Q)

2.3.4 Switching capacitor modules

We usually use band switching techniques to expand the tuning range. The gain of VCO (KVCO) can be reduced to improve the phase noise performance. Making use of switching capacitor modules, eight frequency channels are able to be selected. In order to enable eight channels to connect continually, we design the ratio of the capacitance C2, C1, C0 is 4.45:2.09:1. The S2, S1 and S0, digital pads of the chip, connect digital lines so as to switch different channels. The logical high is 1.8V and the logic low is 0V. The switching has less power dissipation by using NMOSFET within 0.3 mW in our practical work. The whole circuit of switching capacitor modules is shown in Fig. 11. Furthermore, the MOS varactor pair tunes the wideband operation within continuous frequency in each channel [18].

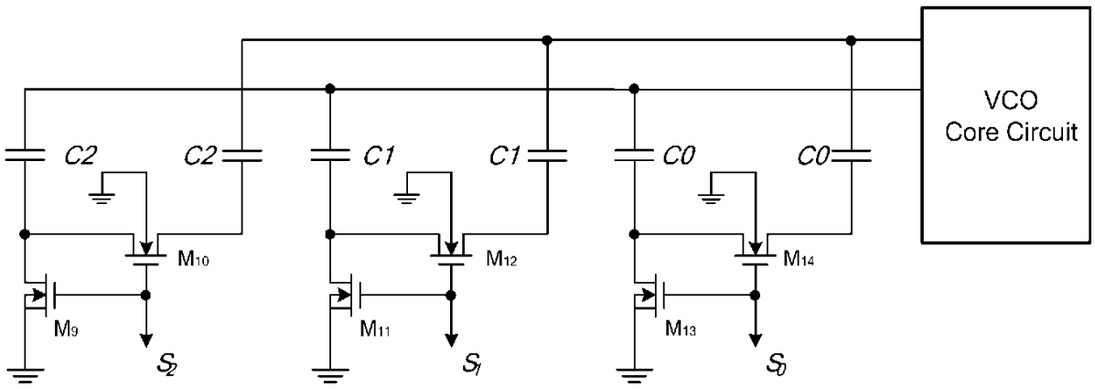


Fig. 11. A switching capacitor module

2.3.5 Output buffers

The VCO is sensitive to loading effect, and it output oscillation frequency would be changed by loading variation. If we insert the buffer between oscillator and loading, it can isolate between them, and the variation of the loading will not influence oscillator directly.

The load of the instrument for measurement is 50Q such as spectrum analyzer. Without buffers, the chip cannot directly drive instrument. The buffer is shown in Fig. 12. [16].

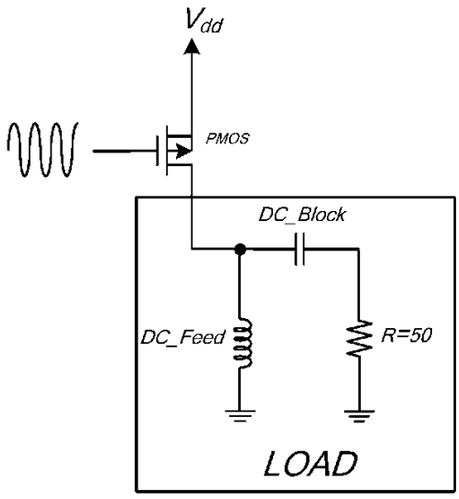


Fig. 12. A buffer schematic

2.3.6 Devices Size of the Circuit

The devices size of our proposed VCO circuit is shown in Table 1, the devices size that we take an optimization to achieve maximize quality factor and generate a negative resistance enough to oscillation, they improve the performance of this proposed VCO.

3. Experimental results

3.1 Measurement setup

A. Agilent E3631A is used as a DC source for digital switching High/Low.
B. Agilent E5052A is used as signal source analyzer and DC sources for DC supply and tuning voltage.
C. The photo of chip with pads is shown in Fig. 13(a).
D. Above a gold plated FR4 PCB is glued the chip which is bonded aluminum wires, shown in Fig. 13(b).
E. The differential outputs of PCB connect a Bias-Tee on each side and then connect two loads, Agilent E5052A and 50Q, shown in Fig. 13(c).
F. The wires which connect to instruments are shielded well and properly matched.

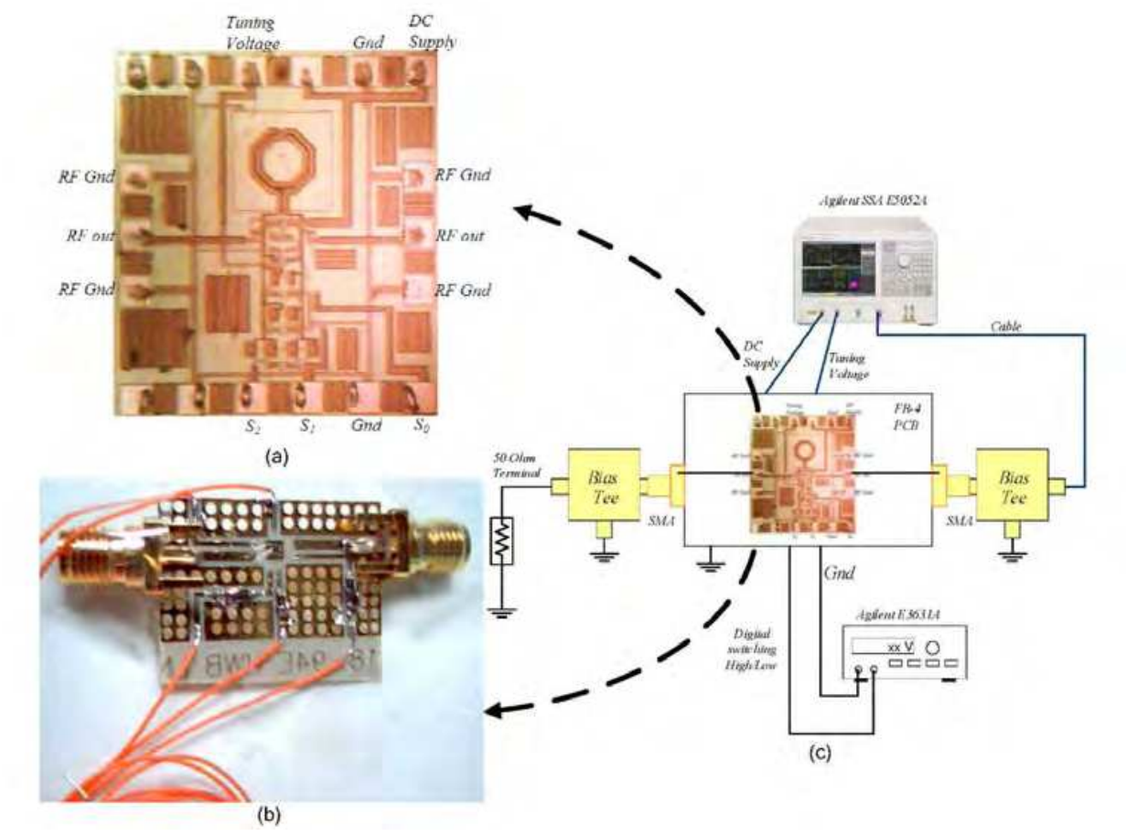


Fig. 13. Measurement setup (a) Die photo (b) Bonding on PCB (c) PCB Measurement

3.2 Measurement result

A. When switching channel is set for S_2SiS_o = "100", DC supply at 1.8V, tuning voltage from -

0.5V to 1.8V, Fig. 13 shows that the frequency range, the magnitude of carrier and the current from supply in different value of tuning voltage. From Fig. 14, we know that MOS varactor pair is able to adjust 0.24 GHz and the magnitude of carrier is -5.97 dBm at 1.15V tuning voltage.

B. Fig. 15 shows phase noise, -128 dBc/Hz with 1 MHz offset at 4.13 GHz when switching channel is set for S_2SiS_o = "100", DC supply at 1.8V, tuning voltage at 0V.

C. According to the steps above, the frequency range, phase noise, the magnitude of carrier and the current from supply in different channels are listed in Table 2. Table 2 shows that each channel works well and the current of each channel is almost the same, which means that the circuit operates in high stability within switching operation. Therefore, we may well say that the usage of switching capacitor modules is a good way to design the wide-band VCO.

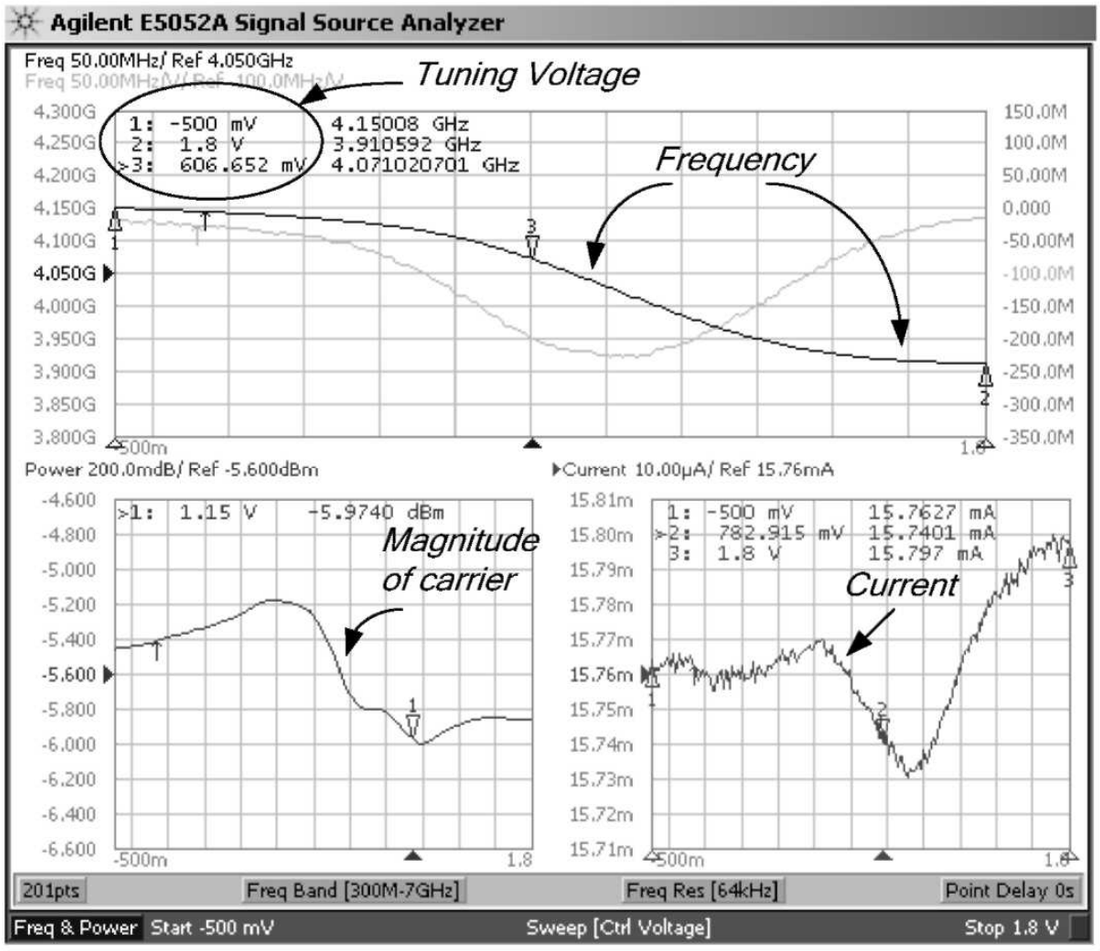


Fig. 14. S_2SiS_o = "100"; Y axes: frequency range, the magnitude of carrier and the current from supply; X axis: tuning voltage

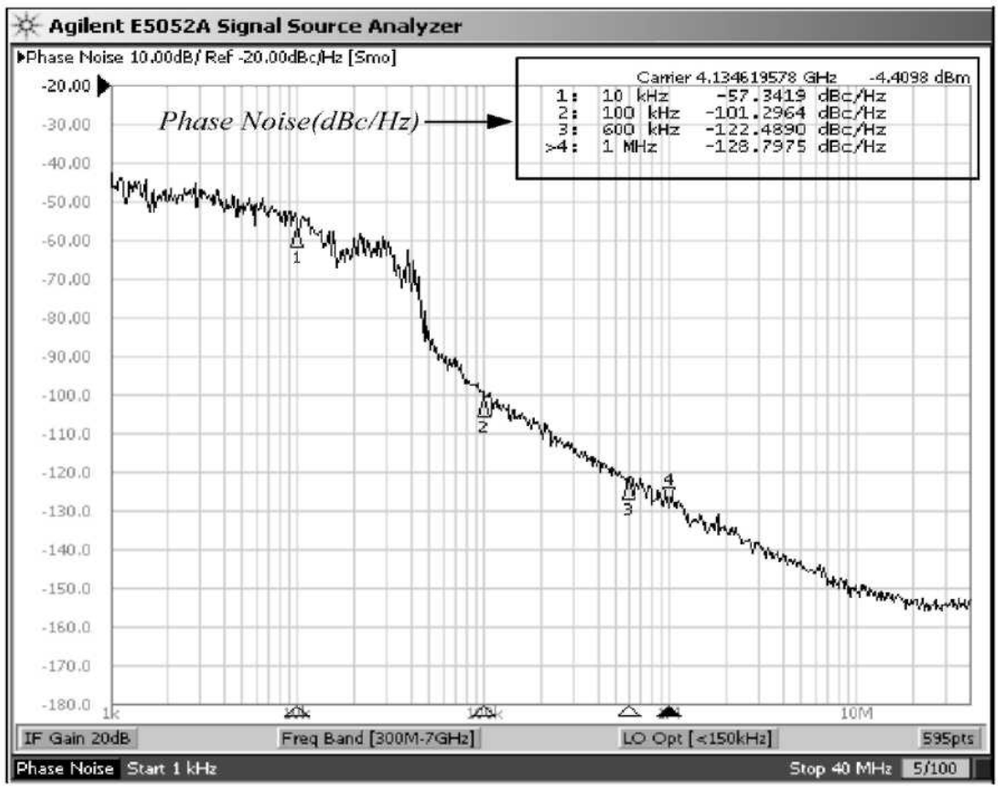


Fig. 15. Phase noise when S_2SiS_o = "100", tuning voltage = 0V

$S_2S_1S_o$	Frequency (GHz)	Phase Noise at 1MHz Offset (dBc/Hz)	Magnitude of carrier (dBm)	Current (mA)
000	5.37-4.84	-124.2 at 5.33GHz	-1.67	15.69
001	5.16-4.69	-122.1 at 5.13GHz	-1.72	15.69
010	4.80-4.43	-121.8 at 4.78GHz	-2.77	15.83
011	4.67-4.55	-124.4 at 4.64GHz	-2.68	15.90
100	4.15-3.91	-128.8 at 4.13GHz	-5.97	15.78
101	4.07-3.84	-126.4 at 4.05GHz	-6.06	15.85
110	3.89-3.69	-126.3 at 3.88GHz	-6.92	15.83
111	3.82-3.64	-122.8 at 3.81GHz	-6.78	15.84

Table 2. Performance of eight channels of the proposed VCO

The supply voltage is set at 1.8V and S_2SiS_o = "111", we attained 1.8V x 15.8mA = 28.5mW. Disconnecting two loads, we get the core power dissipation 13.7 mW at DC supply 1.8V. It is a well-known that figure of merit (FOM) is an index between different VCOs. FOM is defined as [10]

$$FOM = L\{\Delta f\} - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P}{1mW}\right) \quad (5)$$

Where $L\{\Delta f\}$ is the phase noise at *Af* offset from the carrier f_o and *P* is the core power dissipation. Table 3 shows the comparison with recently reported papers VCOs.

	This work	[3]	[4]	[5]	[6]	[7]	[19]
Process (um)	0.18	0.18	0.18	0.18	0.18	0.13	0.09
Center Freq. (GHz)	4.50	2.02	4.40	1.80	5.15	4.75	5.63
Tuning Range (%)	38	72	41	73	29	40	45
Supply voltage (V)	1.8	1.8	1.8	1.5	0.8	1	1
Core power diss. (mW)	13.7	17.7	4.9	4.8	1.2	2.5	14
Phase noise (dBc/Hz)	-121.8 -128.8	-135	-114	-126.5	-109.7	-121.7	-108.5
FOM (dBc/Hz)	-183 -189	-188	-181	-184	-183	-189	-171.5

Table 3. Comparison of VCOs performance

4. Conclusion

This VCO presents a technique of operating narrowband into wideband, employs switching tail current technique and maintains the good phase noise performance. The switching capacitor modules offered multi-channels can enhance oscillator frequency range and the K_{VCO} is still small. This VCO operated from 3.64 to 5.37 GHz with 38% tuning range. The power consumption is 13.7 mW by a 1.8 V supply voltage and measured phase noise in all tuning range is less than -122 dBc/Hz at 1 MHz offset.

5. Acknowledgment

This project is support by National Science Council, (NSC 95-2221-E-224-102). We would like to thank the Taiwan Semiconductor Manufacture Company (TSMC) and Chip Implementation Center (CIC) for the wafer fabrications. We are grateful to National Nano Device Laboratories (NDL) for on-wafer measurements and National Chung Cheng University for PCB measurements by Dr. Ting-Yueh Chih.

6. References

[1] Craninckx, Michiel S. J. Steyaert, "A 1.8-GHz low-phase-noise CMOS VCO using optimized hollow spiral inductors,"Solid-State Circuits, IEEE Journal of Volume 32, Issue 5, May 1997 Page(s):736 - 744

[2] Frank Ellinger, 2008, Radio Frequency Integrated Circuits and Technologies, Springer.

[3] Ito, Y.; Yoshihara, Y.; Sugawara, H.; Okada, K.; Masu, K.;"A 1.3-2.8 GHz Wide Range CMOS LC-VCO Using Variable Inductor". Asian Solid-State Circuits Conference, 2005 Nov. 2005 Page(s):265 - 268

[4] Fard, A.; Johnson, T.; Aberg, D.;" A low power wide band CMOS VCO for multi-standard radios". Radio and Wireless Conference, 2004 IEEE 19-22 Sept. 2004 Page(s):79 - 82

[5] Berny, A.D.; Niknejad, A.M.; Meyer, R.G.;" A 1.8-GHz LC VCO with 1.3-GHz tuning range and digital amplitude calibration". Solid-State Circuits, IEEE Journal of Volume 40, Issue 4, April 2005 Page(s):909 - 917

[6] Chung-Yu Wu; Chi-Yao Yu;" A 0.8 V 5.9 GHz wide tuning range CMOS VCO using inversion-mode bandswitching varactors". Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on 23-26 May 2005 Page(s):5079 - 5082 Vol. 5

[7] Neric H. W. Fong, Jean-Olivier Plouchart, Noah Zamdmer, Duixian Liu, Lawrence F. Wagner, Calvin Plett and N. Garry Tarr, "A 1-V 3.8-5.7-GHz Wide-Band VCO with Differentially Tuned Accumulation MOS Varactors for Common-Mode Noise Rejection in CMOS SOI Technology", IEEE Transactions on Microwave Theory And Techniques, Vol. 51, No. 8, August 2003, pp.1952-1959

[8] Byunghoo Jung; Harjani, R.;" A wide tuning range VCO using capacitive source degeneration". Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on Volume 4, 23-26 May 2004 Page(s):IV - 145-8 Vol.4.

[9] Yao-Huang Kao, Meng-Ting Hsu, Min-Chieh Hsu, and Pi-An Wu, "A Systematic Approach for Low Phase Noise CMOS VCO Design", IEICE Trans. Electron., Vol. E86-C, No.8, pp.1427-1432, August 2003

[10] Donhee Ham and Ali Hajimiri, "Concepts And Methods in Optimization of Integrated LC VCOs", IEEE Journal of Solid-State Circuits, Vol.36, Issue.6, Jun 2001, pp.896-909

[11] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential LC oscillators," IEEE J. Solid-State Circuits, vol. 34, no. 5, May 1999, pp. 717-724.

[12] Huang, P.-C.; Tsai, M.-D.; Vendelin, G. D.; Wang, H.; Chen, C.-H.; Chang, C.-S., "A Low-Power 114-GHz Push-Push CMOS VCO Using LC Source Degeneration", Solid-State Circuits, IEEE Journal, Vol.42, Issue 6, June 2007, pp.1230 - 1239

[13] Razavi, Behzad, "Design of Integrated Circuits for Optical Communications"-1st ed

[14] Eric A. M. Klumperink, Sander L. J. Gierkink, Amoud P. van der Wel, Bram Nauta, "Reducing MOSFET 1/f Noise and Power Consumption by Switch Biasing", IEEE Journal of Solid-State Circuits, Vol.35, Issue 7, July 2000, pp.994-1001

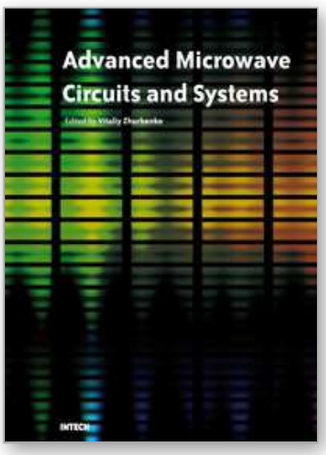
[15] C. C. Boon, M. A. Do, K. S. Yeo, J. G. Ma, and X. L. Zhang, "RF CMOS Low-Phase-Noise LC Oscillator through Memory Reduction Tail Transistor," IEEE Transactions on Circuits and Systems, Vol. 51, Feb. 2004, pp. 85-89

[16] Meng-Ting Hsu, Chung-Yu Chiang, and Ting-Yueh Chih, "Design of Low Power with Low Phase Noise of VCO by CMOS Process", IEEE International Asia-Pacific Microwave Conference 2005, December 4-7, 2005, pp. 880~883

[17] T. H. Lee, "The Design of CMOS Radio-FrequencyIntegrated Circuits", 2nd ed., Cambridge University Press, 2004

[18] Meng-Ting Hsu, Shiao-Hui Chen, Wei-Jhih Li, "Implementation of Low Phase Noise Wide-Band VCO with Digital Switching Capacitors", Microwave Conference, 2007. APMC 2007. Asia-Pacific 11-14 Dec. 2007 Page(s):1 - 4

[19] Soltanian, B.; Ainspan, H.; Woogeun Rhee; Friedman, D.; Kinget, P.R.;" An Ultra-Compact Differentially Tuned 6-GHz CMOS LC-VCO With Dynamic Common-Mode Feedback", IEEE Journal of Solid-State Circuits, Vol.42, Issue8, Aug. 2007, pp.l63S - 16418



Advanced Microwave Circuits and Systems

Edited by Vitaliy Zhurbenko

ISBN 978-953-307-087-2
Hard cover, 490 pages
Publisher InTech
Published online 01, April, 2010
Published in print edition April, 2010

This book is based on recent research work conducted by the authors dealing with the design and development of active and passive microwave components, integrated circuits and systems. It is divided into seven parts. In the first part comprising the first two chapters, alternative concepts and equations for multiport network analysis and characterization are provided. A thru-only de-embedding technique for accurate on-wafer characterization is introduced. The second part of the book corresponds to the analysis and design of ultra-wideband low- noise amplifiers (LNA).

How to reference

In order to correctly reference this scholarly work, feel free to copy and paste the following:

Meng-Ting Hsu, Chien-Ta Chiu and Shiao-Hui Chen (2010). Implementation of Low Phase Noise Wide-Band VCO with Digital Switching Capacitors, Advanced Microwave Circuits and Systems, Vitaliy Zhurbenko (Ed.), ISBN: 978-953-307-087-2, InTech, Available from: http://www.intechopen.com/books/advanced-microwave-circuits-and-systems/implementation-of-low-phase-noise-wide-band-vco-with-digital-switching-capacitors

INTECH
open science | open minds

InTech Europe
University Campus STeP Ri
Slavka Krautzeka 83/A
51000 Rijeka, Croatia
Phone: +385 (51) 770 447
Fax: +385 (51) 686 166
www.intechopen.com

InTech China
Unit 405, Office Block, Hotel Equatorial Shanghai
No.65, Yan An Road (West), Shanghai, 200040, China
中国上海市延安西路65号上海国际贵都大饭店办公楼405单元
Phone: +86-21-62489820
Fax: +86-21-62489821

IntechOpen