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Current Trends of CMOS Integrated Receiver Design

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1. Introduction

The use of CMOS technology for implementation of fully RFICs (Radio Frequency Integrated Circuits) is shown as a trend in the new devices for wireless communications. Nowadays, these circuits are found in many kind of applications, in which they can provide a lot of services including: Cellular Phones, Personal Mobile Service, Satellite, Specialized Radios (used by the Police, Fire-fighters, Emergency Services), and WLANs (Wireless Local Area Networks).

The potential of CMOS RFIC has been demonstrated in many academic works and by commercial devices. Due to the quick development of 3G and 4G technologies and the design of devices for systems that operate at standards such as WCDMA (Wideband Code Division Multiple Access), GSM/GPRS (Global System for Mobile Communication/General Packet Radio Service), WiMAX (Worldwide Interoperability for Microwave Access), and WiBro (Wireless Broadband), the CMOS RFIC has been more and more inserted, because of its good technical and commercial characteristics, becoming itself a challenge for the designers (Iniewski, 2007).

For modern and appropriated RFIC applications, new mobile systems demand antennas in small dimensions with wideband and reasonable gain, offering the possibility of a multiband operation (Liberti & Rappaport, 1999).

In addition, the UWB (Ultra WideBand) communication systems are an important advancement in wireless applications. They use a wide range of frequencies at very low power to transmit at high data rate. The low power allows these systems to use existing licensed RF bands without interfering with current users (Ismail & Gonzalez, 2006).

With the coming of the new digital standards, the data exchange over the wireless became predominant. In fact, in the 1990s, the GSM and IS-95 standards, evolved to include data transmission as an effective part of its services. Besides, the 3G and 4G are being applied and developed with voice and data integration. It has been foreseen that the data traffic will overtake the voice one. Furthermore, nowadays the costs of these devices and services for the data traffic are cheap enough to permit its continuous utilization into user's houses and offices.

In this way, the aim of this chapter is to provide a guide to the RF building blocks of smart communication receivers in accordance with the present state of the art. The goal is to show

the conception and development of several RFICs, for example, LNAs (Low Noise Amplifiers), mixer, and VCOs (Voltage Controlled Oscillators) in different applications.

The circuits presented here can supply the necessities for many mobile applications, in particular, for SMILE (Spatial MultIplexing of Local Elements) front-end receiver circuitry. As an example of a circuit developed for this technique, it is shown a multiplexed LNA with four channels to supply the necessity of multiplexing without losing the concern about noise or any other kind of design performance parameters (Capovilla et al., 2007). Page constraints have made it necessary to limit coverage in some areas to represents different areas as best as possible.

2. Smart receivers

The antenna array is one of the most promising techniques for increasing the system capacity in wireless communication. The demand for mobile systems emerges and the use of data transmission grows through applications of several protocols.

With the quick development of 3G and 4G technologies and the growth of the commercial applications for their equipments, the seeking for antenna technical solutions has increased a lot for these applications. Due to this fact, the antennas represent a fundamental role in its performance, strengthening this research area.

Using a variety of processing algorithms, usually managed by a DSP (Digital Signal Processor), the adaptive antennas adjust its radiation pattern dynamically to enhance the desired signal, null or reduce interference (Liberti & Rappaport, 1999). They are used to improve the received signals, minimizing interference and maximizing the desired receiving signal and to form dynamic beams.
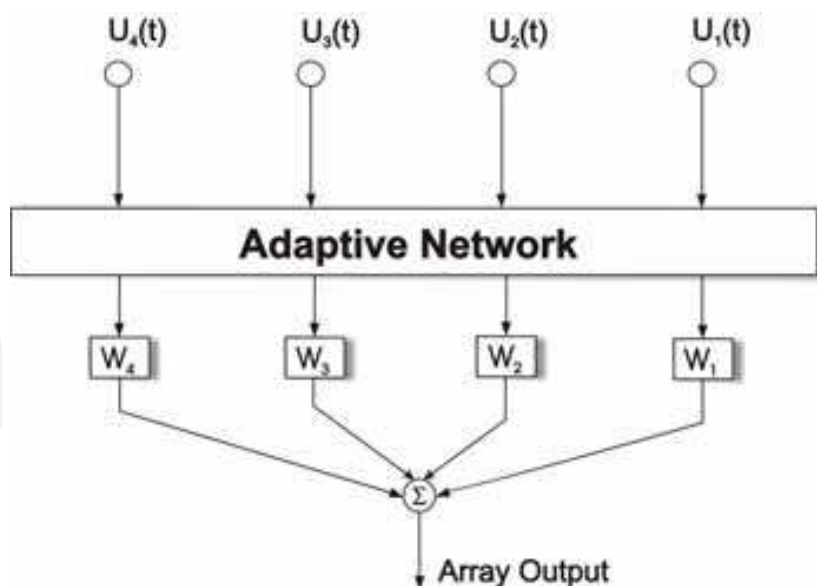

Fig. 1. – Adaptive array concept.

An adaptive system considers that the desired signal and the interfering one come from different directions. As can be seen in Fig. 1, to reduce the fading and the co-channel

interference, the system processes four input signals coming from different antennas of the array (u1(t), u2(t), u3(t), and u4(t)) to generate an output optimized signal.

This one is the work of the crossed correlation and of the relative signal levels between four received signals. The radiation pattern can be configured in real time through direct application of control algorithms as MUSIC (Multiple Signal Classification) (Ratnarajah & Manikas, 1998) and ESPRIT (Estimation of Signal Parameters via Rotational Invariance Techniques) (Roy & Kailath, 1989), which are examples of DOA (Direction Of Arrival) algorithms.

To estimate the best weight of the array (Godara, 1997a), efficient algorithms as LMS (Least Mean Squares) (Clarkson & White, 1987) and RLS (Recursive Least Squares) (Qiao, 1991) can be used. Due to this control over the radiation pattern envisaging a better management of the system, it is also possible to form dynamic cells using the multiple beams. This technique is known as SDMA (Space Division Multiple Access) (Godara, 1997b), and allows for different users the simultaneous operation of the same time/frequency slot, increasing the capacity of the system (Kuehner et al., 2001).
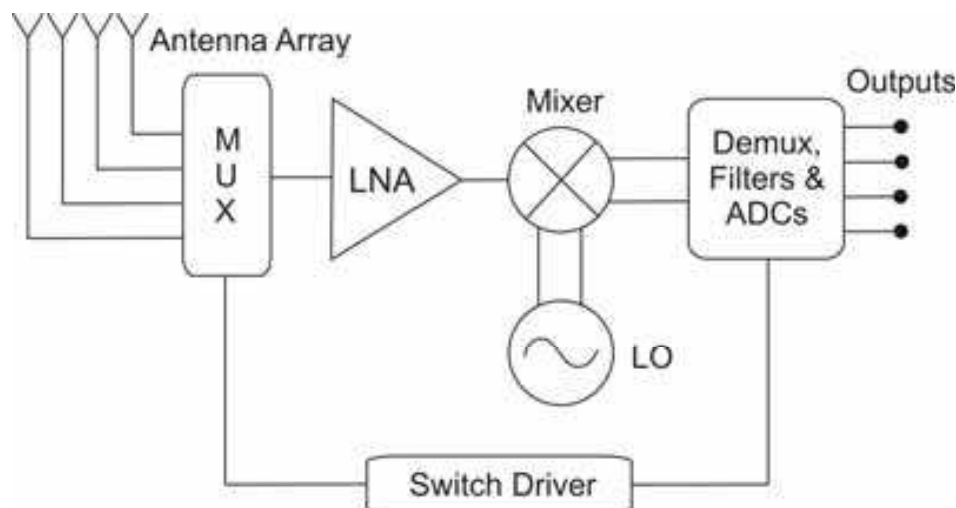

Fig. 2. – SMILE RF front-end receiver architecture.

Additionally, there are several techniques for optimization of smart antennas in spatial diversity. The DBF (Digital BeamForming) is one of those techniques that revolutionized the capabilities of antenna arrays. In the beginning, the DBF projects were motivated by military operations, however with the increasing interest in low cost WLAN, nowadays, there are studies in order to use the DBF in different applications. The DBF scheme provides a lot of advantages over analog beamforming including in hardware implementation (Doble & Litva, 1996).

For this one, the smart antenna array requires independent RF channels (RF switch, LNA, and mixer) for each array element, increasing hardware costs and the power consumption, which are proportional to the number of array elements. In this way, many efforts have been made aiming at reducing the use of repetitive RF channels. The works of Cheng (2001) and Ishii (2000) show some of the attempts in this direction, but only for limited functional environmental conditions.

The SMILE scheme is shown in Fig. 2. It appears as a new solution to solve these technical problems. This hardware technique reduces the RF channels of the smart receiver to only one without loss of signal fidelity. This functional characteristic is obtained by independently switching the array elements at a rate above the Nyquist frequency, according to the sampling theory. After processing the RF channel (through RF switch, LNA, and mixer), the spatially sampled signals are demultiplexed and low-pass filtered to form only one output (Fredrick et al., 2002).
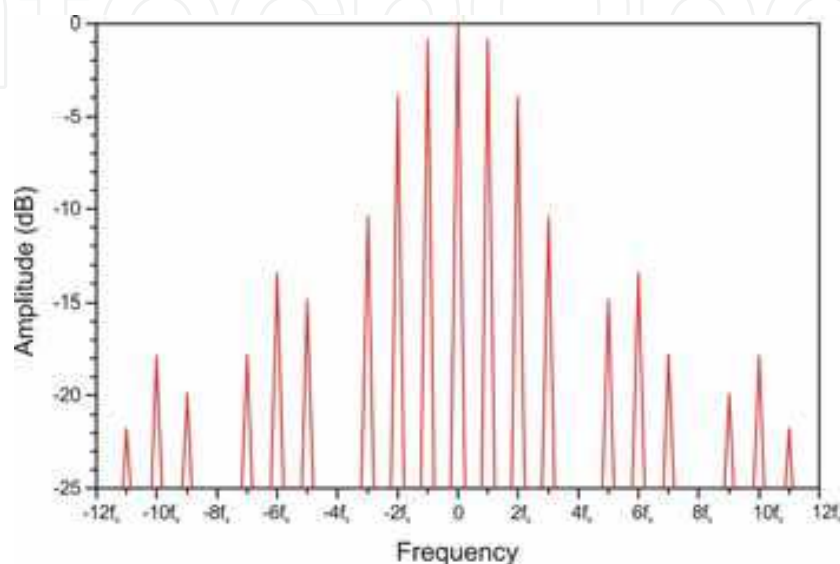

Fig. 3. – Baseband SMILE spectrum.

To test the scheme, a single-tone test was performed with an IF of 750kHz. After receiving the signal, the baseband spectrum of the multiplexed signal for the array rotate at 45º is shown in Fig. 3. Each of the four channels demultiplexed and recovered are shown in Fig. 4. The envelope shows the original data samples. This technique significantly reduces the RF hardware, getting the necessary functionality with only a fraction of the hardware requirements. Compared to N elements from a traditional system, the proposed system offers an N fold reduction in the RF hardware requirement also reducing the power consumption and the circuit size.

3. CMOS receivers

The RF basic blocks of receivers are composed by LNA, mixer, and LO (Local Oscillator). In this section, these circuits are presented and characterized in CMOS technology. Normally, at the foundry, the CMOS RF technology is derived from a process for manufacturing digital circuits, after a stabilization procedure, by adding masks and performing other slight modifications, such as, the use of thick metal technique for the top layer (Backer et al., 2001).
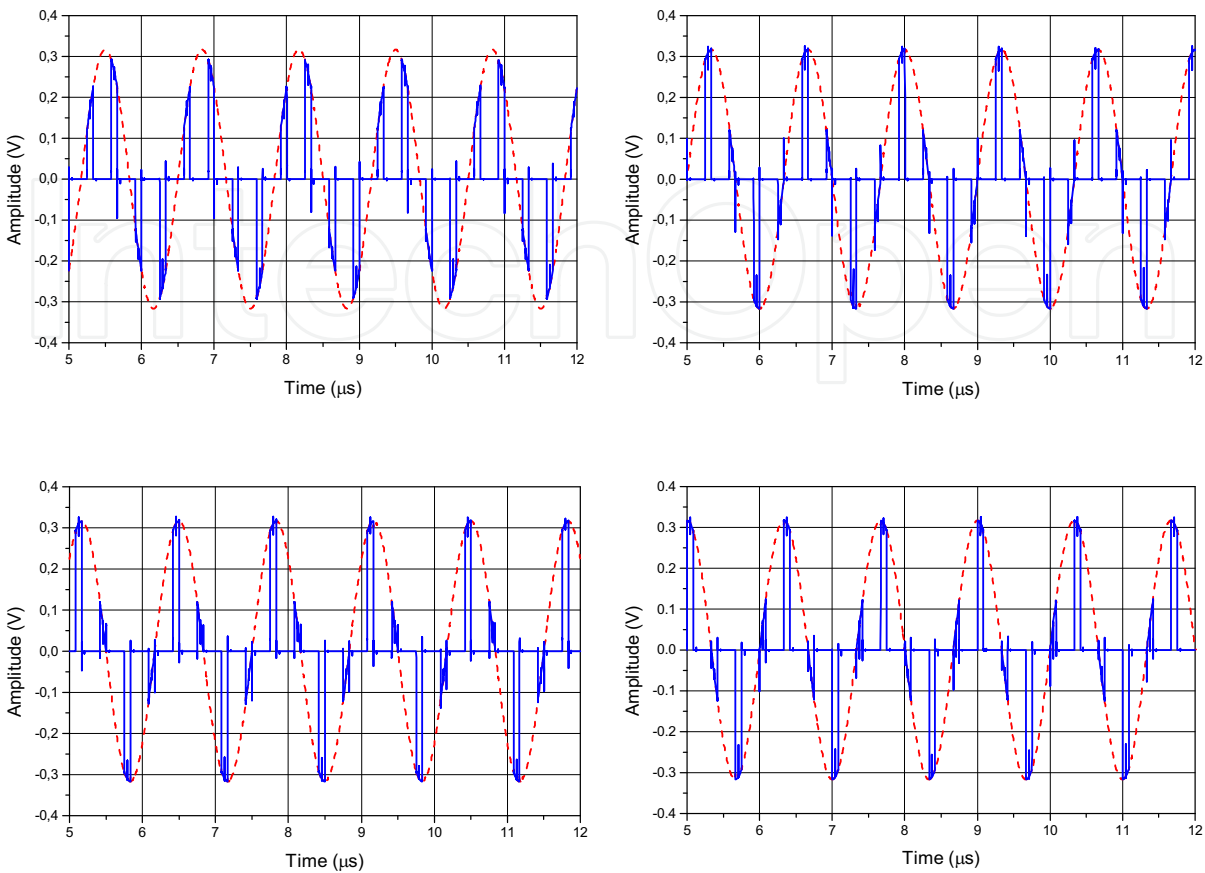
Fig. 4. – Recovered multichannel baseband data for array at 45°.

3.1 Low noise amplifier

The schematic of a basic common-source LNA is shown in Fig. 5. For simplicity, the bias network is represented only by Vbias and Rb (usually 5-10kΩ). The input and output are coupled with DC-block capacitors (not showed here). The use of inductive degeneration results in no additional noise generation since the real part of the input impedance does not correspond to a physical resistor. A mathematical representation of the noise from the whole amplifier circuit with neglected noise contribution of the transistor Mn2, is given by (Allstot et al.,2004):

$$F = 1 + \frac{\gamma}{\alpha} \frac{1}{Q} \left(\frac{\omega_0}{\omega_T} \right) \left[1 + \frac{\delta\alpha^2}{5\gamma} \left(1 + Q^2 \right) + 2 \left| c \right| \sqrt{\frac{\delta\alpha^2}{5\gamma}} \right] \tag{1}$$

with:

$$Q = \frac{1}{\omega_0 C_{gs} R_s} \qquad\qquad \alpha \equiv \frac{g_m}{g_{d0}}$$

where: Q is the quality factor, g_{d0} is the drain conductance, and, γ, δ, c are fixed transistor parameters.
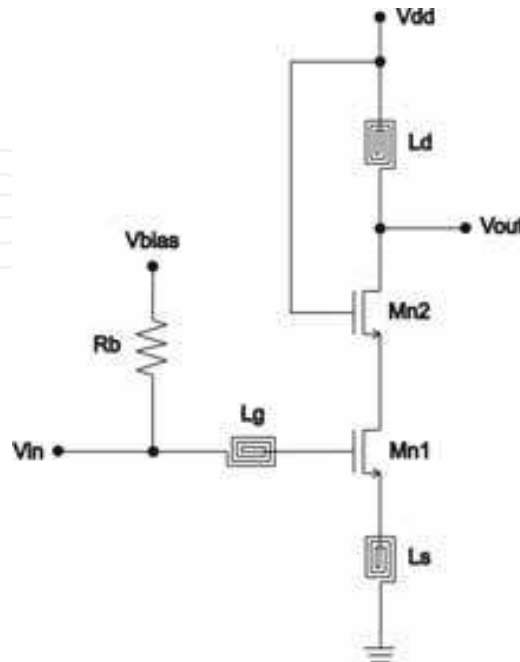

Fig. 5. – LNA schematic.

A simple analysis of the input impedance (Shaeffer & Lee, 2001) shows that:

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}} \tag{2}$$

where: L_s and L_g are source and gate inductors, respectively, and g_m and C_{gs} denote small signal parameters of transistor Mn1 (C_{gd} and C_{ds} are neglected in this first-order approximation).

The input is matched to 50Ω by using inductors L_g and L_s, with the source inductor L_s chose to match the real part, and gate inductor L_g used to set the resonance frequency. Using some assumptions taken from the long-channel theory, the optimum width of the device Mn1 is given by (Lee, 1998):

$$W_{Mn1} \approx \frac{1}{3\omega_0 L_{eff} C_{ox} R_s} \tag{3}$$

where: L_{eff} is the effective transistor length and C_{ox} is the oxide capacitance of the transistor. Equation 3 gives a definite width of the transistor, but for short channel devices, the CMOS technology leads to very large transistors. In this case, it is recommended to use multi-gates transistors to reduce the noise generated due to the resistance of the gate.

For the selection of the cascode transistor Mn2 width, two competing considerations should be made. The Miller capacitance of Mn1 can considerably reduce the gate and drain impedances of Mn1, degrading both the noise performance and the input matching.

This behaviour can be compensated by a large cascode device (C_g device), which reduces the gain of the C_s device. However, the parasitic source capacitance associated with a large C_g device increases the amplification of the C_g device. It was presented in publications that the ratio between C_s and C_g transistor widths varies from 0.5 (Guo & Hang, 2002), up to three (Goo & Dutton, 2002), based on simulations. Note that Mn2 also introduces noise in the amplifier, and that, the size of this transistor should be also constrained by the noise figure of the amplifier (Rafla & El-Gamal, 1999).
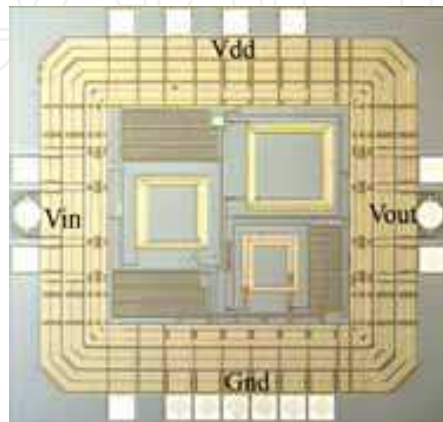

Fig. 6. – LNA die (1530 x 1425µm).

As an example, it is shown in Fig. 6 a LNA die with an area of 2.2mm². This circuit was fabricated by AMS (Austriamicrosystems) foundry with 0.35µm gate length and four metal layers (metal4 is a thick-metal layer used mainly in spiral inductors). The three spiral inductors are clearly visible. The input spiral inductors (L_g) and the input pads are at the left side of the die. The inductor at the lower right side is L_s and the one at the upper right side is L_d, which tunes the output of the LNA. The spiral inductors are fabricated with metal4 (thick-metal), which gives Q's of about eight. This value of Q is higher than a typical metal3 on-chip spiral inductor can provide (Li et al., 2004).

3.2 Mixer
The downconverter mixer translates an incoming RF signal to a lower frequency, being possible in this lower frequency to get necessary selectivity and gain for the receiver. A nonlinear device makes the multiplication of the RF signal and the LO signal in time domain. This multiplication results in output signals at sum and difference frequencies of the inputs. For selectivity reasons, the signal that always interests is the difference of the input signals and, usually, it is selected through a low-pass filter. Theoretically, to accomplish the frequency translation a nonlinear device with quadratic characteristic is used, but in implemented devices, this characteristic normally does not occur.
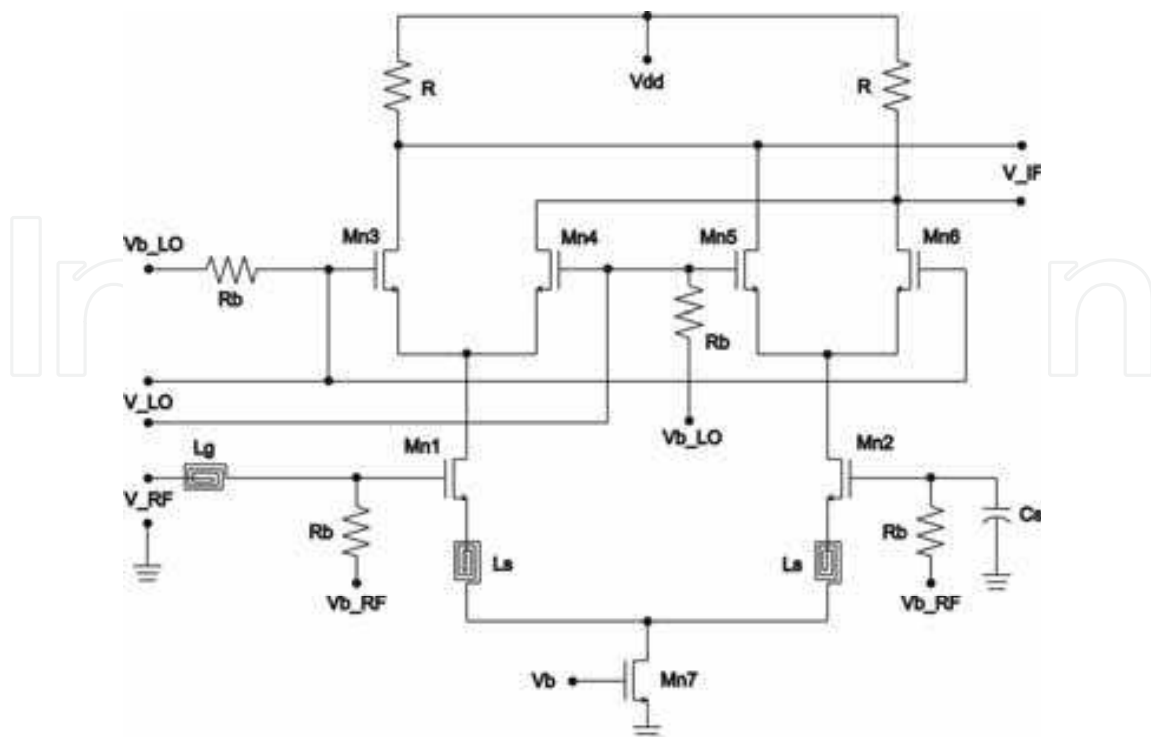
Fig. 7.– Double-balanced Gilbert cell as mixer.

So, if the nonlinear device presents N degree transfer characteristic, in the translation, other components will appear, and eventually, they can overlay the frequency of interest or to arise close to the same one, resulting in distortion. The CMOS mixers present some advantages if compared to bipolar ones. For instance, the transfer characteristic of the MOS transistor is approximately quadratic in saturation region, while the bipolar one is approximately exponential. Thus, the MOS transistor presents less harmonic distortion (Tsividis, 1999). Other advantage is that the MOSFET has better noise performance (internally generated noise). Looking through the topology, an advantage of the double-balanced structure in comparison with the single-balanced one is the good isolation between the LO and the IF port. Besides, there are other advantages such as the noise-rejection in common mode, better linearity, and less intermodulation (Lehne et al., 2000). In this way, for RFIC mixer, the Gilbert cell is the most common topology. Its choice usually is inevitable (Darabi & Chiu, 2005). Thus, due to the advantages and presented considerations, the researches with this type of mixer have been intensified in the last decade, resulting in modifications of classic structures and doing this topology almost unanimity in recent publications.

The mixer shown in Fig. 7 is a doubly balanced Gilbert cell with one arm of the RF differential pair connected to input and the other arm AC grounded. This differential input is widely used in CMOS downconverter mixers, since it provides a high impedance input to the low noise amplifier and is capable of driving a low impedance load at its output. To drive this one, the mixer output is buffered (not shown in the figure).

An example of implemented double-balanced mixer in 0.35μm CMOS technology is shown in Fig. 8. This prototype has an overall area of 2.45mm^2.
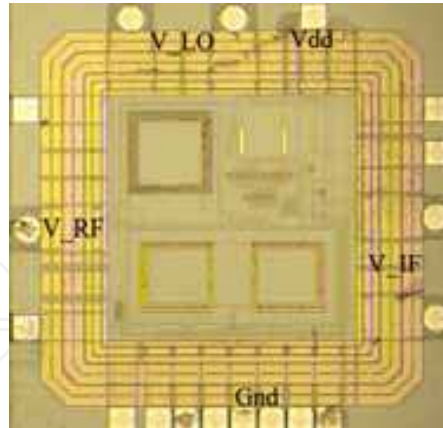
Fig. 8. – Double-balanced mixer die (1570 x 1560μm).

3.3 Local oscillator

The voltage controlled oscillator is a kind of oscillator in which the frequency of oscillation can be modified inside of a pre-determined band. Usually, there are three types of integrated VCO topologies: Ring oscillators, relaxation oscillators, and tuned oscillators (Razavi, 2001). The ring oscillators are implemented by digital inverter cells at feedback closed loop (odd number of inverters). Its integrated design is simple and compact. The frequency control is made through the current variation into the inverter cells, or eventually, for the modification of the inverter capacitance loads.

Its main intrinsic problem is the high phase noise due to the continuous switching of the inverters. So, its application for RFIC is not feasible (Backer, 2001), however it is indicated for many applications as, for example, the clock generation for digital or mixed-signal circuits.

Another topology is the relaxation oscillator, which works charging and discharging a capacitor with constant current. In the same way that the ring oscillator, its tuning is made by the modification of the current. Its easy integration and compact size become this topology attractive for integrated circuits, even though the high current consumption necessary to reduce the phase noise limits its RFIC applications.

The third usually integrated topology is the tuned oscillator, which contains a resonator LC tank or a tuned crystal. The resonator generates the oscillation and an active circuit supplies the energy necessary to compensate the resistive losses of the resonator. A difficulty that exists to integrate this type of oscillator is due to the low quality that still exists in the integrated passive devices, however the main problem of this type of oscillator is the large area of spiral inductors. But, there are lots of advantages in this topology, as steady-state oscillation, great spectral pureness, and low power dissipation. Because of these advantages, nowadays this type of oscillator is more frequently used in RFIC applications (Hajimiri & Lee, 2001). The tuned oscillator can be implemented in different topologies. For RFIC applications with differential design, normally is chosen the CMOS or NMOS LC due to its easy design. For single-end design, the Colpitts oscillator is more interesting than the Hartley oscillator due to the larger number of the spiral inductors used in the Hartley topology. The VCO shown in Fig. 9 is a NMOS LC with the frequency control performed through the variation of the capacitance (varactor) of the LC tank.
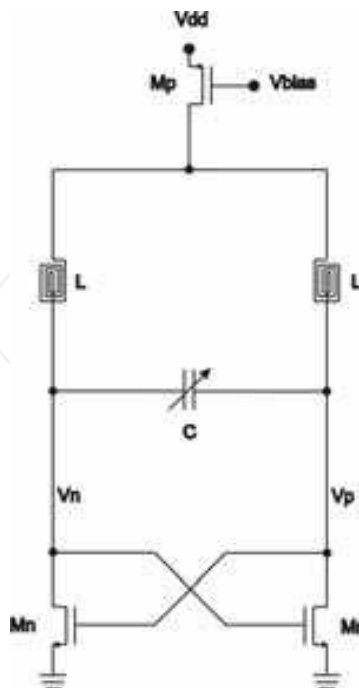
Fig. 9.– LC NMOS schematic.

This differential output is widely used in CMOS oscillators to make a direct connection with double-balanced mixers. If necessary to drive low impedance loads, the VCO output (Vp - Vn) must be buffered (not shown in the figure). An example of implemented oscillator in 0.35μm CMOS technology is shown in Fig. 8. This prototype has an overall area of 1.8mm^2.
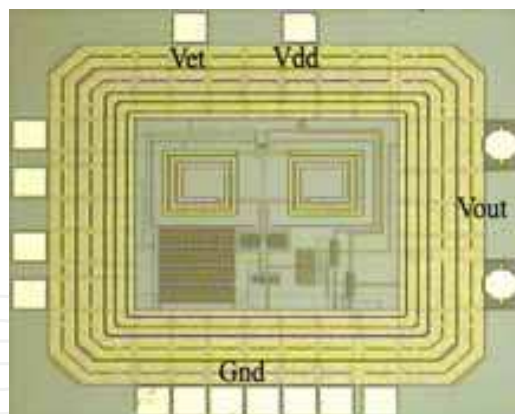

Fig. 10. – LC NMOS die (1400 x 1280μm).

4. Implementation of an integrated SMILE receiver in CMOS technology

The use of antenna array in a smart system requires independent RF channels (LNA, mixer, etc) for each array element. This increases hardware costs and power consumption, which are proportional to the number of array elements. Another problem is that the multiple-feedline arrays and complex multiple RF circuits result in difficulties for optimized circuit integration. Also, more noise arises inside the system with the growing of electronic devices.

As the SMILE scheme is a front-end receiver architecture which uses only one RF channel, carrying multiplexed information from multiple antennas, in this section is shown, as an example of implementation for SMILE applications, a single RF channel using a fully integrated multiplexed LNA with four input channels, a double-balanced mixer, and a VCO as local oscillator. All circuits were fabricated in 0.35µm CMOS technology. The circuits are designed to operate at 2.5GHz band with an IF of 750kHz. If compared to a single channel system, it has the same performance with the addition of switching functionality. The proposed system presents power consumption four times less and an overall area reduction around 70% when compared to a conventional smart antenna architecture using four separate RF channels.

4.1 Multiplexed low noise amplifier

The smart antenna systems, generally, are composed of separate LNAs, and, in this case, the LNAs are always polarized, what generates high power consumption with poor power efficiency, due to only one channel to be used in each time slot. This problem grows, becoming critical, with the increase of the channels number. As an interesting hardware solution, the SMILE technique is implemented with the use of a novel type of LNA, which compared to a single LNA, has the same performance with the addition of switching functionality (Capovilla et al., 2007).
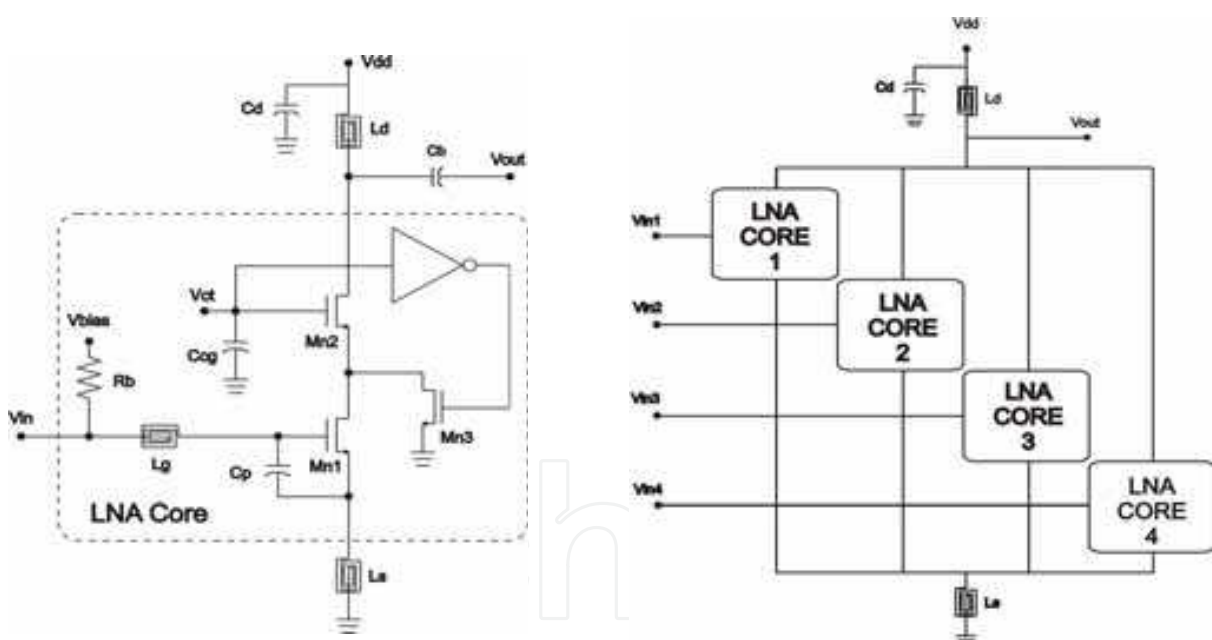

Fig. 11. – Multiplexed LNA with four input channels.

Analyzing this circuit shown in Fig. 11, the proposed structure is composed by four LNA-Core in parallel sharing the same L_d and L_s spiral inductors. Internally, the LNA has a capacitance of 1pF (C_d) from V_{dd} to ground for RF decoupling of the DC supply line.

The common-gate stage works like an NMOS switch and the shunt transistor Mn3 is used to improve the isolation of the LNA-Core. This shunt transistor is activated by a signal generated in the inverter cell that is activated with the same control signal that activates the

Mn2. When it is turned "ON", any residual RF signal existing in the LNA cascode pair is grounding (Huang & O, 2001).

A prototype of the LNA was designed to operate at 2.5GHz band (American WCDMA and WiMAX applications). A select pin controls which input is active by steering the current through the selected input stage and cutting off from the others.

This provides the optional switching functionality in front of the LNA, but without the insertion loss and noise figure penalty from the switch. In each channel, a control circuit is connected directly to the gate of the transistor Mn2.

When the control signal indicates an operation of a specific channel, the Mn2 of this channel is switched "ON" and the Mn3 "OFF". Conversely, for the other channels, the Mn1 is switched "OFF" and the Mn3 "ON". Therefore, only a desired channel is conducted to the output.
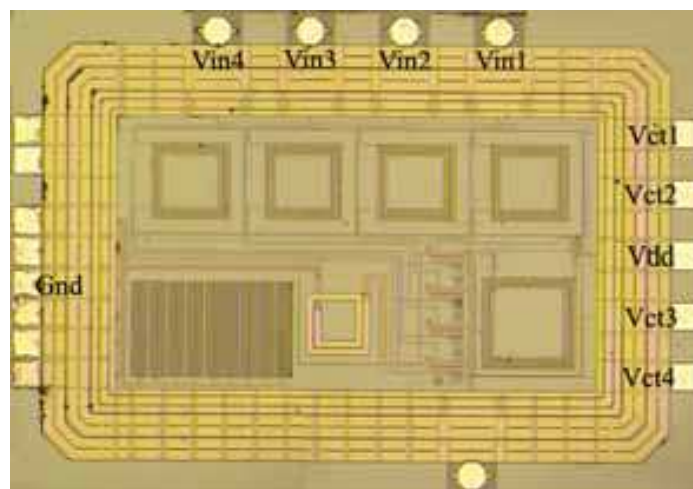

Fig. 12. – Multiplexed LNA with four channels die (2230 x 1580µm).

A photograph of the multiplexed LNA die is shown in Fig. 12 and was fabricated with an overall area of 3.52mm2. The six spiral inductors are clearly visible. The input spiral inductors (L_g) and the input pads are at the upper side of the die. The spiral at the lower left is Ls and the one at the lower right is L_d, which tunes the output of the LNA.

For comparison purposes a separate LNA, like a LNA-Core, has been fabricated having an area of 2.2mm2. The proposed LNA presents an area reduction of about 60% and power consumption four times less than a conventional system using four separate amplifiers.

4.2 Integrated single RF channel receiver

The RF channel of this smart receiver is composed by the fully integrated multiplexed LNA and a double-balanced mixer. As local oscillator is used an integrated LC NMOS VCO. The implemented system design in a SMILE scheme is shown in Fig. 13.
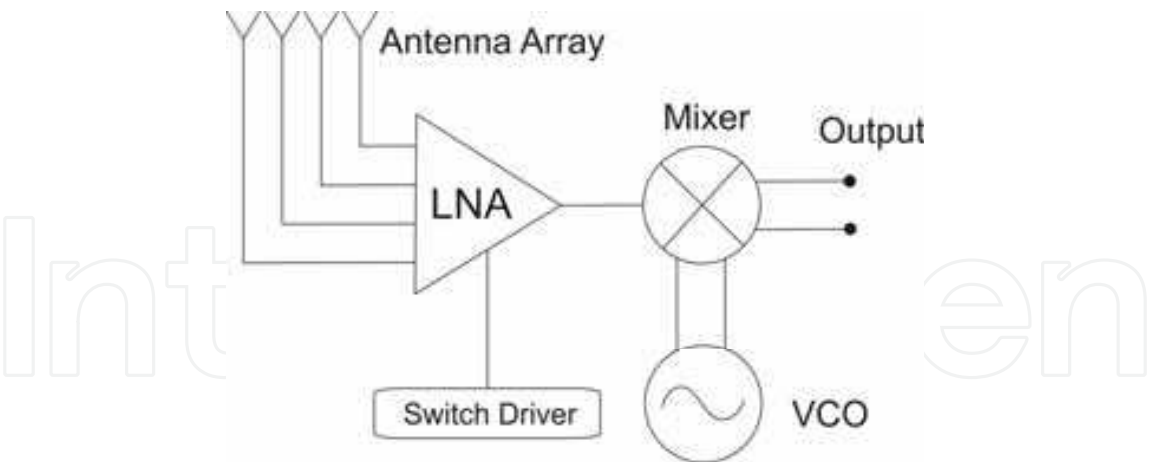
Fig. 13. – SMILE receiver scheme.

The proposed solution also reduces the overall noise figure of the system, since no RF switches are used. To test the circuits, it is used COB (Chip-on-Board) packaging technique, in which the bare die is directly bonded to the PCB (Printed Circuit Board). The board is fabricated using FR-4 material (ε_r=4.4 and thickness 1.6mm). It was prepared for characterization by using a microstrip test fixture.

All measurements are made with a 3.3V supply voltage and the current consumptions, under nominal conditions, are 6.5, 12, and 8mA for the LNA, mixer, and VCO, respectively. The total consumption is four times less than a normal smart antenna receiver with the same characteristics.
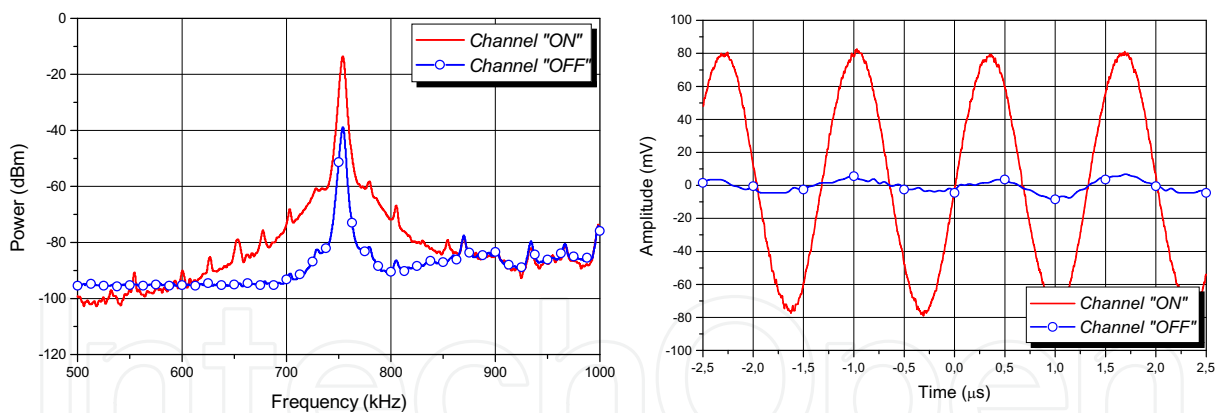

Fig. 14. - Switching characteristics of the channel one.

For these measurements, the RF power is -22dBm (2.6GHz) with a LO power of -2dBm (2.599250GHz). In Fig. 14 is shown the IF spectrum and IF waveform output in two situations: when the control signal 1 is switched "ON" and the other controls are switched "OFF" (channel one "ON"); and when the control signal 2 is switched "ON" and the other controls are switched "OFF" (channel one "OFF"). The total gain from channel 1 to IF output is above 9dB with an "ON-OFF" ratio of more than 25dB, sufficient for modern wireless applications.

The measured parameters of the circuits are summarized in Table 1. The measured SSB NF (Single-Side Band Noise Figure) of the mixer is 9.3dB and the LNA NF is 2.4dB, which results in a total NF of 3.9dB. The presented NF values are due to the measured gains to be lower than the design ones. This lower gain is due to the process variation to present a thicker gate-oxide in these fabricated prototypes. The total third-order nonlinearity is mainly limited by the transconductance stage of the mixer, with a total value of -2.8dB.

	S_{11}	Gain	Isolation	IIP3
	(dB)	(dB)	(dB)	(dBm)
LNA	-10	5	-17	4.5
Mixer	-34	4	-	3
Total	-12	9	-17	-2.8

Table 1. - Measured parameters of the circuits.

The SMILE scheme can also be used in quadrature system and, for this kind of application, a quadrature oscillator is needed. A QVCO generates two components in quadrature that feed the switching transistors of two mixers. One for the signal in phase and the other for the signal in quadrature. The design of the receiver is approximately equal to the same impedance and bias matching of the single design. The only difference is that the LNA output normally drives one mixer, and in this case, it drives two mixers in parallel. A simple impedance matching is enough to the design in quadrature works perfectly.

5. Conclusion

The application of CMOS RFIC has been shown as a trend for the implementation of modern wireless communications. The use of smart antennas to these systems together with the optimization of the receiver can result in many novel mobile applications. In scope of this chapter, the reconfigurable terminals using the smart antennas are considered as interesting environments to apply the RFIC CMOS. However, with the increase of the number of channels to improve the efficiency of the system, the RF devices have increased at same rate. For an array with N antennas, the total number of RF channels required is N. In this way, the power consumption and the devices expense is approximately N times those in a single antenna.

Another problem is about the hardware interconnectivity that becomes more and more complex with the increase of the channels. The SMILE technique appears as a new solution that must be able to solve this problem. The objective of this technique is to reduce the number of needed RF channels to only one, without loss of signal fidelity. This is obtained by independently switching the array elements at a rate above the Nyquist frequency, according to the sampling theory. After processing the RF channel, the spatially sampled signals are multiplexed to form only one output. Therefore, the aim of this chapter was to provide a simple guide to the building blocks of communication receivers in accordance with the present state of the art for this smart receiver application. It was shown the conception of several RFICs, for example, LNAs, mixer, and VCO implemented for the use in the stage of frequency conversion. All the circuits shown in this chapter, besides their

research characteristics, can be easily and quickly implement on commercial systems. As a final circuit example, an integrated single RF channel of the SMILE receiver prototype was shown. This receiver uses four multiplexed channels coming from four antennas. The multiplexation is made by a multiplexed LNA exclusively developed for this project. The characterization of the multiplexed amplifier, according to the "ON/OFF" functionality, confirms the good performance of the design operating at 2.5GHz band.

An early attempt at designing RFIC in the semiconductor foundry technologies using 0.13µm or nanometer process has revealed a new paradigm for the designers. A successful design approach for highly integrated RFIC in this environment will grow a lot, and in Brazil, the contact with TSMC (Taiwan Semiconductor Manufacturing Company) for migration of the circuits showed here to nanometer technologies are occurring at this moment. With all these attractive and perspective characteristics, the SMILE technique and the CMOS RFIC circuits, which have been separately or jointly developed for this application, must find great applications in modern wireless communications systems.

6. Acknowledgments

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Mobile and Wireless Communications Network Layer and Circuit Level Design

Edited by Salma Ait Fares and Fumiyuki Adachi

ISBN 978-953-307-042-1

Hard cover, 404 pages

Publisher InTech

Published online 01, January, 2010

Published in print edition January, 2010

Mobile and wireless communications applications have a clear impact on improving the humanity wellbeing. From cell phones to wireless internet to home and office devices, most of the applications are converted from wired into wireless communication. Smart and advanced wireless communication environments represent the future technology and evolutionary development step in homes, hospitals, industrial, vehicular and transportation systems. A very appealing research area in these environments has been the wireless ad hoc, sensor and mesh networks. These networks rely on ultra low powered processing nodes that sense surrounding environment temperature, pressure, humidity, motion or chemical hazards, etc. Moreover, the radio frequency (RF) transceiver nodes of such networks require the design of transmitter and receiver equipped with high performance building blocks including antennas, power and low noise amplifiers, mixers and voltage controlled oscillators. Nowadays, the researchers are facing several challenges to design such building blocks while complying with ultra low power consumption, small area and high performance constraints. CMOS technology represents an excellent candidate to facilitate the integration of the whole transceiver on a single chip. However, several challenges have to be tackled while designing and using nanoscale CMOS technologies and require innovative idea from researchers and circuits designers. While major researchers and applications have been focusing on RF wireless communication, optical wireless communication based system has started to draw some attention from researchers for a terrestrial system as well as for aerial and satellite terminals. This renewed interested in optical wireless communications is driven by several advantages such as no licensing requirements policy, no RF radiation hazards, and no need to dig up roads besides its large bandwidth and low power consumption. This second part of the book, Mobile and Wireless Communications: Key Technologies and Future Applications, covers the recent development in ad hoc and sensor networks, the implementation of state of the art of wireless transceivers building blocks and recent development on optical wireless communication systems. We hope that this book will be useful for students, researchers and practitioners in their research studies.

How to reference

In order to correctly reference this scholarly work, feel free to copy and paste the following:

C. E. Capovilla and L. C. Kretly (2010). Current Trends of CMOS Integrated Receiver Design, Mobile and Wireless Communications Network Layer and Circuit Level Design, Salma Ait Fares and Fumiyuki Adachi (Ed.), ISBN: 978-953-307-042-1, InTech, Available from: http://www.intechopen.com/books/mobile-and-wireless-communications-network-layer-and-circuit-level-design/current-trends-of-cmos-integrated-receiver-design

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