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Modeling and Performance Analysis of III-V Nanowire Field-Effect Transistors

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1. Introduction

A semiconductor nanowire (NW) is a solid rod with a diameter less than 100-200 nm composed of one or several semiconductor materials. The emergence of bottom-up chemical methods to fabricate one-dimensional semiconductor structures has enabled the synthesis of nanoscale wires that can serve as both devices and interconnects in nanoelectronic circuits.

During the last half century, a dramatic downscaling of electronics has taken place. The miniaturization of the devices found in integrated circuits is predicted by the semiconductor industry roadmap to reach atomic dimensions in few years. The narrowest feature of silicon devices - the gate oxide - should then reach its fundamental physical limit of four to five atoms thickness. At a thickness of less than four layers of silicon atoms, current will penetrate through the gate oxide causing the chip to fail. Intel's innovation of high-k/metal gate (Intel, 2003) has apparently solved the problem, however, to continue the aggressive downscaling of CMOS devices in order to sustain Moore's law beyond 22 nm technology node will require introduction of new materials and device architectures. Intel has been focusing on InSb materials for next generation high-speed, low-power logic applications (Chau et al., 2005).

Efforts have been given to use the self-assembly of one-dimensional semiconductor nanostructures in order to bring new, high-performance logic devices as an add-on to mainstream Si technology. Semiconductor NWs and carbon nanotubes (CNTs) can be the realistic additions.

NWs based on III-V and II-VI compound semiconductor materials have become the most attractive candidates for the next generation field effect transistors (FETs) because of the unique possibilities they offer for the rational control of fundamental properties such as dimension, composition, and doping during growth (Xia et al., 2003). They can be considered promising candidates for future high-speed, low-power electronic devices because of their narrow bandgap (E_g = 0.35 eV for InAs, for example) implying a small electron effective mass, which yields a very high mobility. For undoped InAs, the mobility can be as high as $\mu_n = 33000 cm^2/Vs$, compared with $\mu_n = 1500 cm^2/Vs$ for Si (Lind et al., 2006). Furthermore, the large intravalley separation energy of InAs allows for a high saturated velocity, $v_{sat} = 4 \times 10^7 cm/s$.

Nanowire field effect transistors (NWFETs) have been of particular interest recently, both as vehicles for the investigation of basic carrier-transport behavior and as potential future high-performance electronic devices.

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2. Background and motivation

Nanowires can be synthesized using many techniques, such as molecular/chemical beam epitaxy, vapor phase epitaxy/chemical vapor deposition, and laser ablation. The particular method used influences the potential material compositions, doping and crystal quality, and growth rate.

Most efforts on nanowire devices have focused on making NWFETs. Researchers have typically either studied individual NWs (Xiang et al., 2006) randomly placed on a substrate or have tried to fabricate transistors from arrays of vertical NWs including wrap-gated Si (Schmidt et al., 2006) and InAs NWs (Dayeh, Aplin, Zhou, Yu, Yu & Wang, 2007), even incorporating first attempts at bandgap engineering into the channel of the device. The carrier mobilities of such NWFETs have been shown to match or exceed those of planar silicon, and the devices can achieve gain. Furthermore, p- and n-type nanowires can be assembled into crisscross arrays where the junctions of the crossed wires serve as on-off switches.

A wide range of NW-based devices and systems, including transistors and circuits (Duan et al., 2001; Huang, Duan, Cui, Lauhon, Kim & Lieber, 2001; Zhong et al., 2003), light emitters (Gudiksen et al., 2002; Wang et al., 2001; Huang, Mao, Feick, Yan, Wu, Kind, Weber, Russo & Yang, 2001; Duan et al., 2003), and sensors (Cui et al., 2001) have been explored. NWFETs based on III-V (Dayeh, Soci, Yu, Yu & Wang, 2007; Dayeh, Aplin, Zhou, Yu, Yu & Wang, 2007; Bryllert et al., 2006; Lind et al., 2006; Thelander et al., 2004; Huang et al., 2005; Duan et al., 2001) and II-VI (Goldberger et al., 2005; Ng et al., 2004) compound semiconductor materials have demonstrated promising FET characteristics in various gate geometries, namely, top-gate (Wang et al., 2004; 2003), back-gate (Huang et al., 2005; Duan et al., 2001), wrap-around-gate(Ng et al., 2004; Bryllert et al., 2006), and core-shell (Lauhon et al., 2002) structures.

InSb and InAs NWs, in particular, are attractive candidates for NWFETs due to their high electron mobility at room temperature (Sze, 1981) and low contact resistance (Woodall et al., 1981). The low contact resistance is particularly important in nanoscale systems. Contacts often define performance at the nanoscale. Reports by Intel and Qinetiq on fabricated both *n*- and *p*-type InSb quantum well FETs show that InSb-based quantum well FETs can achieve equivalent high performance with lower dynamic power dissipation (Datta et al., 2005; Ashley et al., 1997; Chau et al., 2005; Radosavljevic et al., 2008). Recent discovery of the observation of Quantum Spin Hall effect in III-V (Liu et al., 2008) and II-VI (König et al., 2007) materials have also motivated the field of spintronics largly due to the fact that there is the possibility of low power logic devices design using the spin degree of freedom of the electron (Wolf et al., 2001; Murakami et al., 2003). Furthermore, III-V materials also have the potential to be used in NW band-to-band tunneling field effect transistors for high-speed, low-power (Khayer & Lake, 2009, in press; Luisier & Klimeck, 2009) and high-speed, high-power (Khayer & Lake, 2009a) applications.

III-V and II-VI NWs tend to be larger (20 - 50 nm diameters) making atomistic modeling difficult or sometimes impossible. However, full band (FB) models are necessary to understand on-off current ratios and radio frequency (RF) power. Although there are series of reports on the experimental realizations of InSb and InAs NWFETs (Datta et al., 2005; Ashley et al., 1997; Chau et al., 2005; Radosavljevic et al., 2008; Lind et al., 2006; Dayeh, Aplin, Zhou, Yu, Yu &Wang, 2007; Bryllert et al., 2006; Thelander et al., 2004; Ng et al., 2004), we find very few attempts to theoretically model them.

To accurately model charge density, spin density. effective mass, and interband tunneling, we have developed a full three dimensional (3D) discretized 8-band $\mathbf{k} \cdot \mathbf{p}$ model (Khayer & Lake, 2008a). We applied it to modeling InSb / InP and InAs / InP core-shell NWs. In the following sections, we will present the theory and performance of *n*- and *p*-type InSb and InAs NWFETs.

3. Theory and models

3.1 The InAs / InP and InSb / InP material systems

The choice of InAs and InSb as the base material for the NW devices is motivated by their physical properties: first of all, the bandgap is small, only 0.35 eV for InAs and 0.23 eV for InSb, and problems with electrical contacting of wires should be minimal. Secondly, the low electron effective mass, $m^* = 0.023m_0$ for InAs and $m^* = 0.013m_0$ for InSb, provides strong quantum confinement effects and a large energy level separation in the wires. The mobility is also high due to the low effective mass, which is of interest for high-speed device application. Another feature which is distinctive for these semiconductor materials (InAs) (Noguchi et al., 1991) is that the Fermi level is known to pin in the conduction band at the surface, at least for bulk material. Because of this, there is an accumulation of carriers at the surface. This behavior is in contrast to GaAs, which has a surface depletion that limits the minimum feasible diameter of a wire unless the surface is passivated. In principle, any metal should thus result in a good, Ohmic contact to InAs. However, a disadvantage with the strong pinning in the conduction band might be that it prevents realization of p-type InAs NWs. Most recently, experimental techniques have been developed to unpinning the Fermi level for the design of III-V FET source/drain contacts (Hu et al., 2009). Moreover, the InAs / InP and InSb / InP material systems are also relatively unexplored since the two materials are impossible to combine in bulk growth due to the large lattice mismatch.
The material parameters of these binary semiconductors are listed in Table 1 (Vurgaftman et al., 2001). These binary materials possess a zinc-blende crystal structure.

3.2 Electronic bandstructure calculation

Electronic bandstructure calculation can be performed in various ways (Yu & Cardona, 1999). The *ab initio* methods, such as Hartree-Fock or Density Functional Theory (DFT), calculate the electronic structure from first principles, i.e., without the need for empirical fitting parameters. These methods use a variational approach to calculate the ground state energy of a many-body system where the system is defined at atomic level.
In contrast to *ab initio* method, the empirical methods, such as tight-binding (Chadi & Cohen, 1974) and the $\mathbf{k} \cdot \mathbf{p}$ method (Luttinger & Kohn, 1955) involve empirical parameters to fit experimental data. Of them, the $\mathbf{k} \cdot \mathbf{p}$ method is widely used for direct bandgap semiconductors due to its simplicity and capability to capture essential physics of the materials in the band extrema. $\mathbf{k} \cdot \mathbf{p}$ method is based upon perturbation theory (Kane, 1956; 1957). In this method, the energy is calculated near a band maximum or minimum by considering the wavevector as a perturbation. In our work, we will use an 8-band $\mathbf{k} \cdot \mathbf{p}$ method to calculate the electronic bandstructure of InSb and InAs NWs.

3.3 Multiband k · p method

The multiband effective mass equation (Luttinger & Kohn, 1955) is widely used to describe the bandstructure of the low-dimensional structures. It can be expressed as,

$$i\hbar\frac{\partial}{\partial t}\Psi_\nu(\mathbf{r},t)=\sum_{\nu'}H_{\nu\nu'}(-i\nabla)\Psi_{\nu'}(\mathbf{r},t)+U(\mathbf{r},t)\Psi_\nu(\mathbf{r},t), \tag{1}$$

where ν represents band index and $H_{\nu\nu'}(\mathbf{k})$ is defined as

$$H_{\nu,\nu'}(\mathbf{k})=\begin{cases}\dfrac{\hbar^2k^2}{2m_0}+E_{\nu 0}, & \nu'=\nu\\ \dfrac{\hbar\mathbf{P}_{\nu\nu'}\cdot\mathbf{k}}{m_0}, & \nu'\neq\nu.\end{cases} \tag{2}$$

$P_{\nu\nu'}$ is called the momentum matrix element between bands ν and ν' and is defined as

$$P_{\nu\nu'}=-i\hbar\langle\overline{u}_{\nu,0}\,|\,\nabla\overline{u}_{\nu',0}\rangle. \tag{3}$$

Here $u_{\nu,0}$ represents the zone center Bloch functions for the νth band. The relation between the actual wavefunction and the multiband envelope functions follows readily from,

$$\Psi_0(\mathbf{r},t)=\sum_\nu u_{\nu,0}(\mathbf{r},t)\Psi_\nu(\mathbf{r},t). \tag{4}$$

Eq. (1) can be solved for the perfect spatially uniform semiconductor using a variety of well known techniques, but in a quantum confined structure, the crystal composition and/or strain varies from region to region and approximations are needed in order to solve Eq. (1). Many such approximate methods are now well known and are extensively used (Sercel & Vahalla, 1990). The choice of how many bands will be needed depends on the details of the problem to be solved.

3.4 Numerical calculations

Fig. 2a shows the schematic diagram of the simulated NWFETs. Square [100] InSb/InP and InAs/InP core-shell NWs with core cross-section of 2 - 60 nm are considered.

The 8-band $\mathbf{k}\cdot\mathbf{p}$ method as described by Gershoni et al. (Gershoni et al., 1993) is used to calculate the electronic bandstructures of the NWs. We include eight basis functions in the set, namely, the spin-up and spin-down s and p atomic orbital-like states. These are arranged in the following order: $|S\uparrow\rangle$, $|X\uparrow\rangle$, $|Y\uparrow\rangle$, $|Z\uparrow\rangle$, $|S\downarrow\rangle$, $|X\downarrow\rangle$, $|Y\downarrow\rangle$ and $|Z\downarrow\rangle$. As a result, the multiband effective mass equation is transformed into eight coupled differential equations for the envelope function F_n

$$\sum_{n'=1}^{8}H_{nn'}(\mathbf{r},\nabla)F_{n'}(\mathbf{r})=EF_n(\mathbf{r}). \tag{5}$$

H is the multiband Hamiltonian matrix and E is the eigenenergy. We use a finite difference method (Mamaluy et al., 2005) with a constant grid spacing of 1 nm to discretize the Hamiltonian. Spurious solutions of the $\mathbf{k}\cdot\mathbf{p}$ equations are eliminated by methods described in Refs. (Foreman, 1997; Kolokolov & Ning, 2003).

To make the discretized $\mathbf{k}\cdot\mathbf{p}$ Hamiltonian look like a nearest neighbor tight-binding Hamiltonian for a layered structure, the NW should be discretized as shown in Fig 1. It should be discretized in planes of sites. The indices of the first plane should run from 1 to N,

the indices of the second plane should run from N+1 to 2N, etc. The matrix $[D_1]$ in Fig. 1 is the block of the Hamiltonian matrix of the isolated 1st plane of sites. The matrix $[t_{1,2}]$ is the block of the Hamiltonian matrix that couples plane 1 to plane 2. If the NW consisted only of the 4 planes shown in Fig. 1, then the total Hamiltonian matrix would have the form

$$H = \begin{bmatrix} [D_1] & [t_{1,2}] & 0 & 0 \\ [t_{1,2}]^\dagger & [D_2] & [t_{2,3}] & 0 \\ 0 & [t_{2,3}]^\dagger & [D_3] & [t_{3,4}] \\ 0 & 0 & [t_{3,4}]^\dagger & [D_4] \end{bmatrix} \tag{6}$$

Considering the components of the **k** vector in Eq. (5) to be numbers and diagonalizing the matrix for a bulk crystal for $k = 0$, one can obtain the dispersion relationships, namely, the **k** dependent eigenvalues $E_n(\mathbf{k})$.

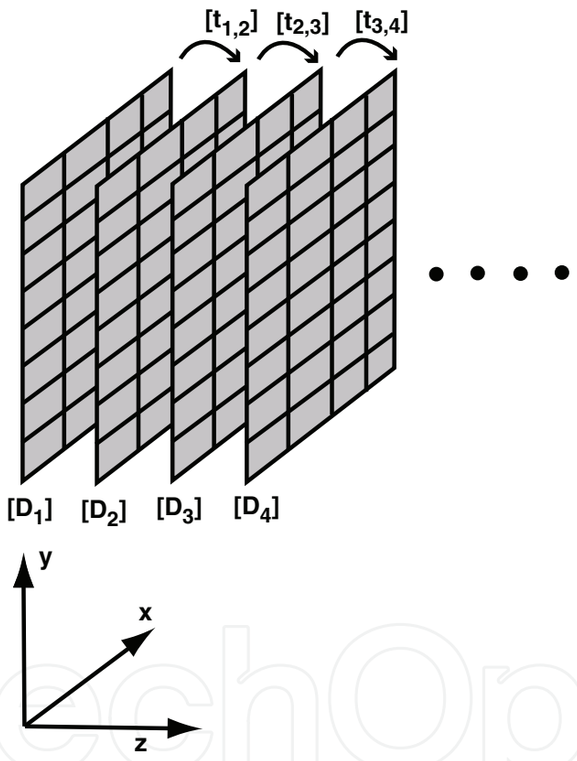

Fig. 1. Discretization scheme for NW.

The *I-V* characteristics of *n*-type InSb and InAs NWFETs are evaluated by using a semiclassical ballistic FET model as described in (Rahman et al., 2003) for ballistic planar MOSFETs and extended by J.Wang (Wang & Lundstrom, 2003) for ballistic high electron mobility transistors. The model is illustrated in Fig. 2(b). It consists of three capacitors, C_G, C_S, and C_D, which describe the electrostatic coupling between the top of the barrier and the gate, the source, and the drain, respectively. The potential at the top of the barrier is calculated as (Rahman et al., 2003)

$$U_{scf} = \left[C_G V_G + C_D V_D + C_S V_S + Q_{top} \right] / C_\Sigma , \tag{7}$$

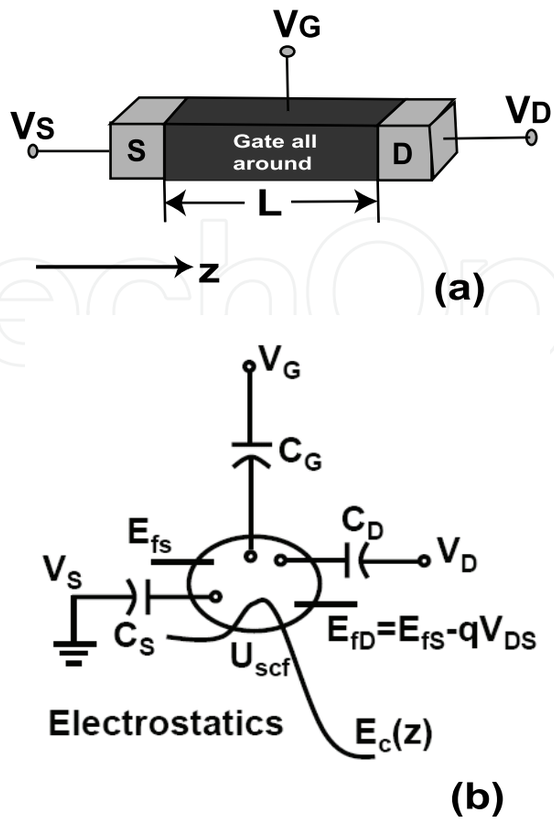

Fig. 2. (a) Schematic diagram of the simulated gate-all-around NW transistor, (b) The electrostatics of the semiclassical ballistic FET model used in the calculation. The diagrams are not to scale.

where V_G, V_D, and V_S are the applied biases at the gate, drain, and source terminals, respectively, $C_\Sigma = C_G + C_D + C_S$, and Q_{top} is the mobile charge at the top of the barrier. Q_{top} is governed by U_{scf}, the source and the drain Fermi levels, E_{FS}, E_{FD}, and the *E-k* dispersion for the channel material. In terms of energy, Eq. (7) becomes

$$E_{CG} = -q\left[\alpha_G V_{GS} + \alpha_D V_{DS} + Q_{top} / C_\Sigma\right], \tag{8}$$

where E_{CG} is the conduction band-edge under the gate, q is the magnitude of the electron charge, $\alpha_G = \frac{C_G}{C_\Sigma}$, $\alpha_D = \frac{C_D}{C_\Sigma}$, and the source is at ground. α_G and α_D are referred to as the gate and drain control parameters, respectively. They are calculated numerically from $\alpha_G = \frac{C_G}{C_\Sigma} = \left|\frac{\Delta E_{CG}}{\Delta q V_{GS}}\right|_{\Delta V_{DS}=0,\Delta N=0}$ and $\alpha_D = \frac{C_D}{C_\Sigma} = \left|\frac{\Delta E_{CG}}{\Delta q V_{DS}}\right|_{\Delta V_{GS}=0,\Delta N=0}$, with ΔN being the induced charge in the channel, using a three dimensional Laplace solver (Adams, 1989).

The charge under the gate, Q_{top}, for electrons, is calculated from

$$Q_{top} = -(q/2)\int_{\varepsilon_1(0)}^{\infty} dE N_{1D}(E-\varepsilon_1(0))\left[f(E-\eta) + f(E-\eta+U_D)\right], \tag{9}$$

where $U_D = qV_{DS}$, $\eta = E_{FS} - \varepsilon_1(0) + qU_{scf}$, E_{FS} is the source Fermi level, and $\varepsilon_1(0)$ is the 1st subband level at the top of the barrier at zero gate and drain bias. The factor of '1/2'' comes from the fact that under the gate in the ballistic limit, the left contact only fills the right moving states under the gate, and the right contact only fills the left moving states under the gate. The density-of-states corresponding to the left or right moving states is one half the full density of states. We use the Green's function method to calculate N_{1D},

$$N_{1D}(E) = \frac{1}{a}\mathrm{tr}\left[\frac{-1}{\pi}\mathrm{Im}\{G(E)\}\right], \tag{10}$$

where a is the discretization length and tr{...} is the trace over all states within a single discretized layer along the transport direction (including spin).
The exact Green's function G of the device is calculated as

$$G(E) = \left[EI - H_D - \Sigma_L - \Sigma_R\right]^{-1}, \tag{11}$$

where H_D is the device Hamiltonian, and $\Sigma_L = t_{1,0}g^L_{0,0}t_{0,1}$, and $\Sigma_R = t_{0,1}g^R_{N,N}t_{1,0}$ are the self-energies to the left and the right contact, respectively. $t_{1,0}$ and $t_{0,1}$ are the coupling matrices between the device and the left and the right contact, respectively. The g's are the surface Green's functions calculated using a decimation technique (Galperin et al., 2002; Sancho et al., 1985).
To evaluate the number of modes contributing to the drive current for the devices, we calculate transmission at each energy point E (Fisher & Lee, 1981),

$$T(E) = \mathrm{tr}\left\{\Gamma_L G \Gamma_R G^\dagger\right\}, \tag{12}$$

where $\Gamma_L = i(\Sigma_L - \Sigma_L^\dagger)$ and $\Gamma_R = i(\Sigma_R - \Sigma_R^\dagger)$, and tr... is the trace over all states within a layer including spin.
After self-consistency between U_{scf} and Q_{top} is achieved, the drain current for the devices is calculated as (Lake et al., 1997)

$$I = \frac{q}{h}\int_0^\infty dE T(E)\left[f(E-\eta) - f(E-\eta+U_D)\right]. \tag{13}$$

To compare the performance of different NWFETs, we set the maximum gate bias voltages such that the gate overdrive (V_{OD}) for each device is fixed at 0.2 V, i.e., $(V_{GS} - V_T)_{\max}$=0.2 V, where V_T is the threshold voltage for each device. V_T is determined as follows. For each single-moded n-type device, V_T is taken as the V_{GS} when the conduction band-edge under the gate (E_{CG}) reaches the energy $E_{FS} + kT$. At this V_{GS}, the single-moded n-type devices have the same threshold current, I_{th}. For the p-type devices, V_T is the gate voltage that produces this I_{th}. Thus, by definition, all of our NWFETs have the same current when V_{GS}=V_T

3.5 Analytical calculations

To understand the performance metrics of NWFETs, analytical expressions are derived for the current, the charge, the power-delay product, the energy-delay product, the gate delay time, and the cut-off frequency for a single-moded device operating in the quantum capacitance limit (QCL), ignoring thermal broadening, and assuming parabolic dispersion.

Devices are said to operate in QCL when the their quantum capacitance (QC) is lower than their geometric gate capacitance. The expressions for the power-delay product, the energy-delay product, the gate delay time, and the cut-off frequency are fundamental limits for these devices.

In equilibrium, the QC per unit length is defined as $C_Q = \frac{q^2 \partial n}{\partial E_F}$, and under the gate with large $V_{DS} >> k_B T$ applied

$$C_Q = \frac{q^2 \partial n}{\partial (E_{FS} - \varepsilon_1)}, \tag{14}$$

where ε_1 is the energy level of the fundamental mode including the effect of the self-consistent potential, i.e., $\varepsilon_1 = \varepsilon_1(V_{GS} = 0) - qU_{scf}$. The gate capacitance to ground, C_{GS}, is the series combination of the geometric (C_G) and quantum (C_Q) gate capacitance (Burke, 2004). Thus, when $C_Q << C_G$, $C_{GS} \approx C_Q$ and the device is said to be in the QCL. Physically, the QC is the energy broadened density-of-states evaluated at the Fermi level.

The QC affects how the band-edge under the gate responds to the gate bias. Taking the derivative of Eq. (8), we obtain

$$\left| \frac{\partial E_{CG}}{\partial q V_{GS}} \right| = \frac{\alpha_G}{1 + \frac{C_Q}{C_\Sigma}}, \tag{15}$$

where we used the fact that the QC defined in Eq. (14) is also equal to $C_Q = q \frac{\partial Q_{top}}{\partial E_{CG}}$. Eq. (15) shows that in the QCL ($C_Q << C_G$), the gate control of the band-edge under the gate is unaffected by charge in the channel, i.e., there is no screening. E_{CG} moves linearly with gate voltage in proportion to the gate control parameter α_G. However, for $C_Q >> C_G$, the gate voltage has little effect on the band-edge under the gate, i.e., screening is significant.

Under the gate, in the ballistic limit, ignoring thermal broadening, the QC per unit length is given by $C_Q = q^2 \partial n / \partial (E_{FS} - \varepsilon_1) = q^2 N_{1D}^+(E_{FS})$ where N_{1D}^+ is the one dimensional (1D) density-of-states with positive velocity which is just the standard 1D density-of-states divided by 2. N_{1D}^+ can be written in several ways, two of which will be useful later,

$$N_{1D}^+(E_{FS}) = \frac{2}{h v_{FS}} = \frac{1}{h} \sqrt{\frac{2m^*}{(E_{FS} - \varepsilon_1)}}. \tag{16}$$

In Eq. (16), v_{FS} is the velocity of an electron under the gate injected at the source Fermi level, E_{FS}. Therefore, the QC under the gate is,

$$C_Q = \frac{2q^2 L_G}{h v_{FS}} = \frac{q^2 L_G}{h} \sqrt{\frac{2m^*}{(E_{FS} - \varepsilon_1)}}. \tag{17}$$

The maximum drain current occurs when V_{DS} is biased to its maximum value of V_{DD}, and the energy of the fundamental mode under the gate is well below the Fermi level of the

source. Under these conditions, for a single-moded, spin-degenerate wire, the second term in Eq. (31) is negligible, and Eq. (31) becomes,

$$I = \frac{2qk_BT}{h}\ln\left(1+e^{(E_{FS}-\varepsilon_1)/k_BT}\right). \tag{18}$$

When the energy of the fundamental mode, ε_1, is pulled several k_BT below the Fermi level of the source, Eq. (18) reduces to

$$I_D \approx \frac{2q}{h}(E_{FS}-\varepsilon_1). \tag{19}$$

Thus, the current is proportional to the energy difference between the source Fermi level and the fundamental mode, and it is independent of any material parameters such as the effective mass or density-of-states. To calculate other quantities such as the power-delay and energy-delay products, quantities such as the current will be needed as a function of voltage rather than energy. The energy scale is converted to a gate voltage using Eq. (15) to write

$$E_{FS}-\varepsilon_1 = q(V_{GS}-V_T)\frac{\alpha_G}{1+\langle C_Q/C_\Sigma\rangle} = q\tilde{\alpha}_G(V_{GS}-V_T), \tag{20}$$

where we define the reduced gate control parameter $\tilde{\alpha}_G \doteq \frac{\alpha_G}{1+\langle C_Q/C_\Sigma\rangle}$ where $\langle C_Q/C_\Sigma\rangle$ is an average value. We will see that for the structures that we consider, the value of $\langle C_Q/C_\Sigma\rangle$ is approximately 0.1. Thus, the current as a function of voltage is

$$I_D \approx \frac{2q^2}{h}\tilde{\alpha}_G(V_{GS}-V_T), \tag{21}$$

with the understanding that $V_{GS} \geq V_T$. The transconductance is defined as $g_m = dI_D/dV_{GS}$ which from Eq. (21) is

$$g_m = \frac{\tilde{\alpha}_G 2q^2}{h}, \tag{22}$$

i.e., g_m is the quantum of conductance times the reduced gate control parameter.
The charge under the gate, Q_{top} is

$$\begin{aligned} Q_{top} = \int_{\varepsilon_1}^{E_{FS}} dE\, N_{1D}^{+}(E) &= \frac{2q\sqrt{2m^*}L_G}{h}\sqrt{E_{FS}-\varepsilon_1} \\ &= \frac{2q\sqrt{2m^*}L_G}{h}\sqrt{q\tilde{\alpha}_G(V_{GS}-V_T)}. \end{aligned} \tag{23}$$

The power-delay product corresponds to the energy required to charge the gate. If one assumes that all of the charge on the gate is imaged by the charge in the channel, one obtains a lower limit for this quantity given by (Knoch et al., 2008)

$$P\cdot\tau_D = \int_0^{V_T+V_{OD}} dV_{GS}Q_{top}. \tag{24}$$

Substituting Eq. (23) into (24) and integrating gives

$$P \cdot \tau_D = \frac{4L_G\sqrt{2m^*}}{3h\tilde{\alpha}_G}\left(q\tilde{\alpha}_G V_{OD}\right)^{3/2}. \tag{25}$$

The gate delay time, t_D is defined as (Knoch et al., 2008)

$$\tau_D = \frac{P \cdot \tau_D}{V_{DD} I_D}. \tag{26}$$

Substituting Eqs. (25) and (21) into (26), τ_D is evaluated as,

$$\tau_D = \frac{2L_G\sqrt{2m^*}}{3q\tilde{\alpha}_G V_{DD}}\sqrt{q\tilde{\alpha}_G V_{OD}}. \tag{27}$$

Since we are using a lower limit for $P \cdot \tau_D$, Eq. (27) provides a lower limit for τ_D.
The energy-delay is the product of the power-delay and the delay time. Multiplying Eqs. (25) and (27), $E \cdot \tau_D$ is

$$E \cdot \tau_D = \frac{16qm^* L_G^2}{9hV_{DD}} V_{OD}^2. \tag{28}$$

Again, this expression should be viewed as a lower limit for the energy-delay product.
The intrinsic cut-off frequency is calculated as $f_T = g_m/(2\pi C_{GS})$, where C_{GS} is the series combination of the geometric (C_G) and quantum (C_Q) gate capacitance (Burke, 2004). Assuming that $C_Q << C_G$ so that $C_{GS} \approx C_Q$, one obtains the upper limit of the intrinsic cut-off frequency,

$$f_T \approx \tilde{\alpha}_G \frac{v_{FS}}{2\pi L_G} = \frac{\tilde{\alpha}_G}{2\pi\tau_G} = \frac{\tilde{\alpha}_G}{2\pi L_G}\sqrt{\frac{2(E_{FS}-\varepsilon_1)}{m^*}} = \frac{\tilde{\alpha}_G}{2\pi L_G}\sqrt{\frac{2q\tilde{\alpha}_G V_{OD}}{m^*}}. \tag{29}$$

In Eq. (29), $\tau_G = L_G/v_{FS}$ is the gate transit time. The cut-off frequency has the form of one over the transit time divided by 2π.
The key concept to understanding the high intrinsic performance of single-moded NWFETs is the 'decoupling of the charge and the current.' This is apparent from Eqs. (21) and (23). The current is material independent. It does not depend on the density-of-states or the charge in the channel. The charge in the channel depends on the density-of-states through the effective mass. For a given current, the charge could be anything depending on the value of the effective mass. To optimize performance, one wants maximum current with minimum charge. This is obtained by minimizing the effective mass. Minimizing the effective mass serves two purposes. (i) It minimizes the charge in the channel according to Eq. (23), and (ii) it allows one to achieve a higher Fermi level in the source for a given doping. This maximizes the current by maximizing the source Fermi level, E_{FS} according to Eq. (19).

4. Results and discussion

4.1 The quantum and classical capacitance limit

In each case, the core material contains InSb or InAs surrounded by a cladding layer (shell material) of InP with a thickness of 6 nm (equivalent to an SiO_2 thickness of 2 nm) which is

treated as the gate insulator. We first show the effect of confinement on the electronic properties, mode spacing, and quantum capacitance, and then we present calculations of the current, power-delay product, delay times, energy-delay product, and cut-off frequencies. All numerical calculations are performed with T = 300K.

The bandgap vs. NW diameters and the electron effective mass of the lowest conduction band mode vs. NW diameters are found in (Khayer & Lake, 2008a). Fig. 3 shows the NW diameter dependence of (a) the bandgap and (b) the lowest conduction mode electron effective mass at the zone center. The bandgap for the InSb NW is 1.17 eV with the 2 nm wire diameter, and it falls to 0.37 eV with the 12 nm wire diameter. For InAs, the bandgap is 1.23 eV for the 2 nm wire diameter, and it falls to 0.54 eV for the 12 nm wire diameter. The electron effective mass at the zone center for the InSb NW with core cross section of 2 nm is $0.042m_0$, and that with core cross section of 12 nm in $0.023m_0$. For InAs, the mass is $0.052m_0$ with 2 nm core cross section and $0.028m_0$ with core cross section of 12 nm.

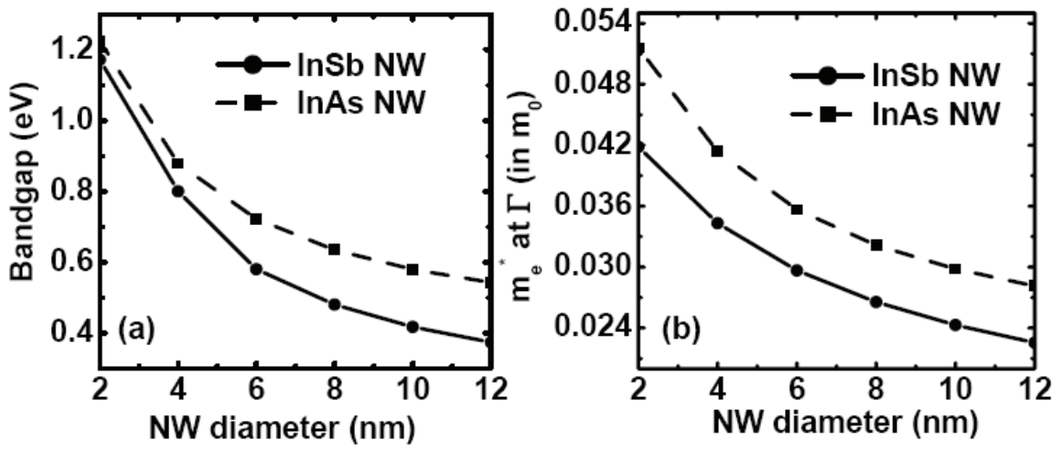

Fig. 3. (a) Bandgap as a function of NW diameter for the simulated InSb and InAs NWs, and (b) theNWdiameter dependence of the lowest conduction band electron effective mass as the zone center. [Reproduced with permission from (Khayer & Lake, 2008a); © 2008 IEEE]

Luryi Luryi (1987). QC in NWFET devices accounts for the fact that the gate field penetrates through the wire since it is not completely screened on the wire surface as is the case in an ideal macroscopic conductor. Devices are said to operate in the quantum capacitance limit (QCL) when their QC is less than their classical capacitance (CC). In highly scaled nanotransistors based on NWs or nanotubes exhibiting 1-D transport, the QCL limit can be reached Rahman et al. (2003); Knoch et al. (2008); Khayer & Lake (2008b). Significant performance improvement in terms of the power-delay product has been predicted in devices operating in the QCL Knoch et al. (2008); Khayer & Lake (2008b;a).

The *n*-type NWFETs operate in the QCL and the *p*-type NWFETs operate in the classical capacitance limit (CCL) as shown in Fig. 4(e, f). It is shown that the drive currents at a fixed gate overdrive are well matched for *n*- and *p*-type NWFETs (Khayer & Lake, 2009b). This is surprising since the density-of-states of the *p*-type FET is much larger than the density-of-states of the *n*-type FET. However, this effect has been observed both theoretically and experimentally by others Rahman et al. (2005); Li et al. (2008). Despite the matched current drive, the *p*-type devices operating in the CCL have twice the delay times, twice the power-delay products, and 4-5 times the energy-delay products of the *n*-type devices operating in

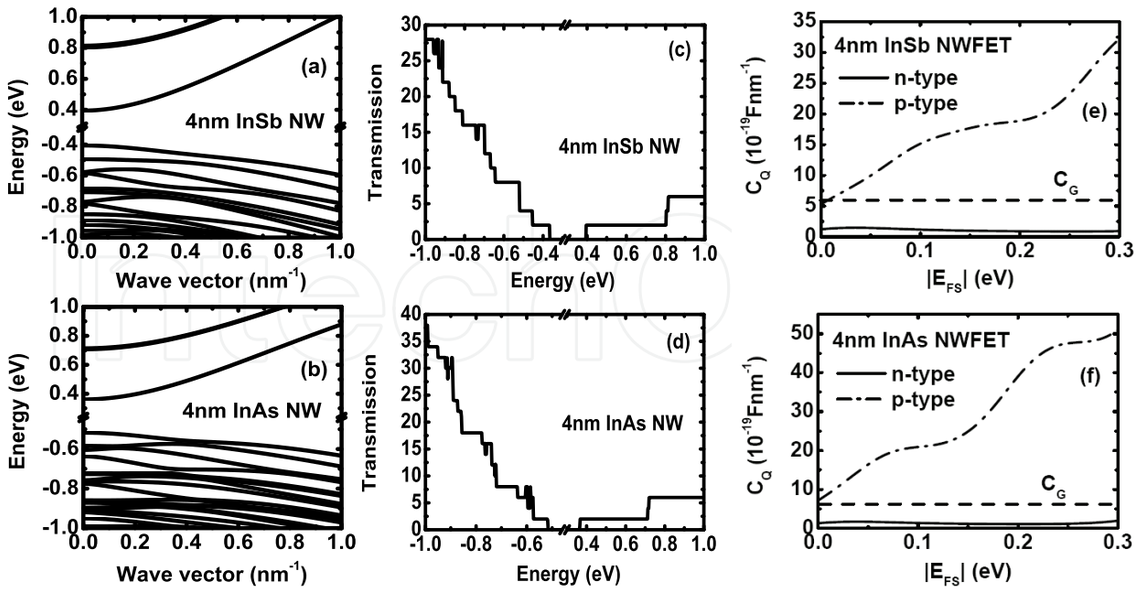

Fig. 4. $E - k$ dispersion relationship and the transmission plots for (a, c) InSb NWs and (b, d) InAs NWs. E=0 corresponds to the lowest conduction band energy of the *bulk* InSb or InAs materials. (e-f) Quantum capacitance under the gate as a function of source energy for the corresponding NWs. Figures are presented for both *n*- and *p*-type devices. Corresponding gate capacitances are also shown. [Reproduced with permission from (Khayer & Lake, 2009b); © 2009 IEEE]

the QCL. These effects have nothing to do with mobility since all transport is assumed ballistic. The effects arise solely from the density-of-states and electrostatics.

Fig. 4(a, b) shows the *E-k* dispersion relations calculated using the 3-D discretized 8-band $\mathbf{k} \cdot \mathbf{p}$ model for the two different materials. In each case, E = 0 corresponds to the lowest conduction band energy of the corresponding *bulk* InSb or InAs materials. It is apparent from the $E - k$ plots that the dispersion for the electrons quickly deviates from parabolic becoming significantly more linear above the energy of the mode minimum. Considerable band mixing in the excited hole subbands takes place for both the NWs.

Fig. 4(c, d) shows the transmission plots as a function of energy for the electrons and for the holes calculated from Eq. (12). There are two details worth commenting on for clarification. First, the initial turn-on of the transmission is 2 since the 8-band k·p model explicitly includes spin in the basis. The trace in Eq. (12) traces over all of the basis orbitals which include spin. Second, the non-monotonic behavior of the transmission for the p-type NWs is the result of the finite bandwidth and non-monotonic nature of the energy versus wavevector relations of the hole modes as seen in Fig. 4(a, b). Some modes have multiple regions of positive velocity, and as the energy moves down below a local extremum, a mode can turn off. The same effect has been observed in Si NWs (Zheng et al., 2005). Fig. 4(c, d) gives insight into the number of modes contributing to the drive current. For the n-type InSb and InAs NWs, the second set of modes occur at 0.35 eV and 0.4 eV above the fundamental mode, respectively. In all cases for the *n*-type devices, with a maximum gate overdrive of 0.2 V, the NWFETs are single-moded (2 spins) as shown in Fig. 4(c, d). For the *p*-type InSb and InAs NWs, the second set of modes occur at 57 meV and 89 meV below the fundamental

mode, respectively. Thus, the p-type devices are not single-moded, and there is a contribution from the higher modes to the current, charge and, in particular, to the quantum capacitance that we discuss next.

Fig. 4(e, f) shows the quantum capacitance under the gate as a function of the source Fermi level for both *n*- and *p*-type devices. The quantum capacitance is calculated from Eq. (14) with the charge, $-qn = Q_{top}$ calculated from Eq. (9). The geometrical gate capacitance, C_G, for the corresponding NWFET is also shown in each figure. C_G is calculated from $C_G = (2\pi\epsilon_r\epsilon_0)/(ln((2T_{ox} + T_{NW})/T_{NW}))$ assuming a coaxial gate geometry (Ramo et al., 1994), where T_{NW} is the diameter of the NW core and T_{ox} is the thickness of the shell. The effect of discrete, well-spaced modes on the quantum capacitance is clearly depicted in Fig. 4(e, f). For all *n*-type devices, $C_Q << C_G$ for the entire energy range considered and the devices are operating in the QCL. For all *p*-type devices, however, C_Q is comparable to or larger than C_G and the devices are operating in the CCL.

Fig. 5(a, b) shows the $\log(I_{DS})$ vs. V_{GS} transfer characteristics of both the *n*- and *p*-type InSb and InAs NWFETs calculated from Eq. (31). For the *p*-type devices, the polarity of $V_{GS} - V_T$ has been reversed. For all devices, V_{DS} is chosen to be large enough so that there is no back injection from the drain. The currents are balanced for the *n*- and *p*-type devices. The *n*- and *p*-type device currents are well-matched. This is surprising since the *n*- and *p*-type devices have very different densities-of-states and they fall into different capacitance regimes. Naively, one would expect that, in the ballistic limit, the device with the larger density-of-states and more closely spaced modes would carry more current.

Fig. 5(c, d) shows the carrier density, Q_{top} vs. V_{GS} for the InSb and InAs NWFETs. The carrier density is higher for the *p*-type devices. The *p*-type devices not only have more occupied modes, but the dispersion of each mode is considerably flatter than those in the conduction band (see Fig. 4(a, b)). This results in a larger density-of-states associated with each valence band mode. The net result is more charge in the channel for the *p*-type devices for a given gate overdrive and current.

Fig. 5(e, f) shows how the band-edges under the gate change with applied gate bias. These curves are explained by Eq. (15). Initially, the channel in both the *n*- and *p*-type devices is empty, there is a significant source-channel barrier to electron or hole flow, and, thus, the quantum capacitance, $|\partial Q_{top}/\partial(E_{FS} - \varepsilon_1)|$, is exponentially reduced. Therefore, initially, the band-edges for both *n*- and *p*-type devices move identically with gate voltage with a slope whose magnitude is given by the gate control parameter α_G. When the first set of excited modes under the gate are shifted by the gate bias such that they start to become populated by the source Fermi level at $V_{GS} = V_T$, the quantum capacitance turns on and is as shown in Fig. (4(e, f)). The single-moded, *n*-type devices remain in the QCL for the entire range of gate bias. At threshold, for the *n*-type devices, the magnitude of the slope $\left|\frac{\Delta E_{CG}}{\Delta q V_{GS}}\right|$ reduces slightly from $\alpha_G = 0.8$ to $\tilde{\alpha}_G \approx 0.7$. When the first set of excited modes of the *p*-type devices are shifted by the gate bias such that they start to become populated by the source Fermi level, the quantum capacitance becomes larger than the classical capacitance and the *p*-type devices move into the CCL with $C_Q > C_\Sigma$ as shown in Fig. 4(e, f). When this happens, the denominator of Eq. (8) increases, and the magnitude of the slope $|\partial E_{CG}/\partial q V_{GS}|$ decreases as shown in Fig. 5(e, f). In the ideal classical limit with an infinite density-of-states, C_Q becomes infinite, the slope $|\partial E_{CG}/\partial q V_{GS}|$ goes to zero, and the band-edge under the gate becomes

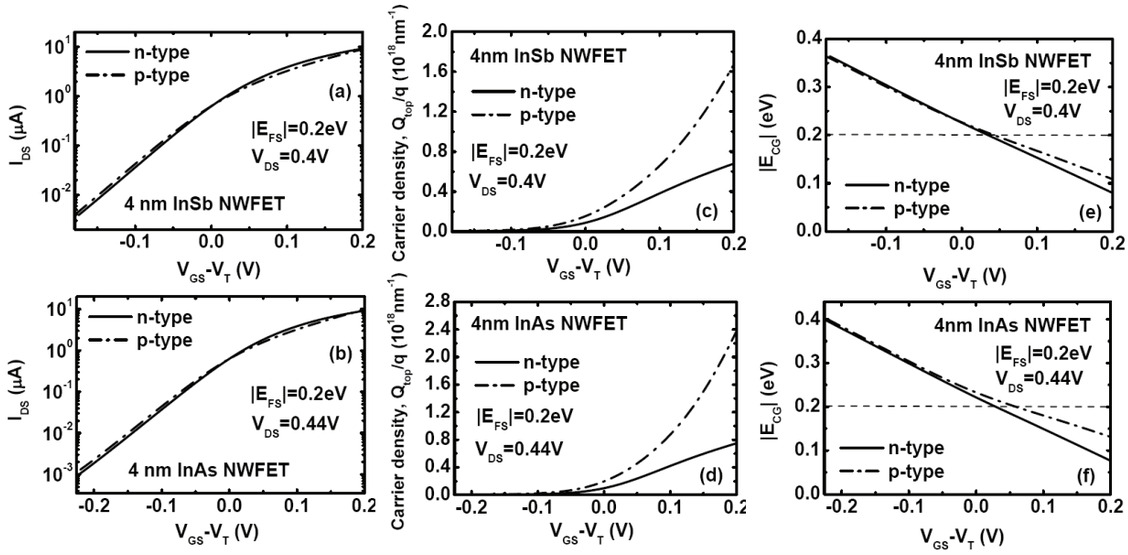

Fig. 5. log(I_{DS}) vs. V_{GS} transfer characteristics and the carrier density, Q_{top} vs. V_{GS} plots for (a, c) InSb NWs and (b, d) InAs NWs. The drain bias voltages are fixed at half of the energy bandgap for each NW as shown. For the *p*-type devices, the polarity of the voltage is reversed. (e, f) band-edges under the gate as a function of the gate bias for the devices. The source Fermi energy E_{FS} is at 0.2 eV for all devices and is shown by the horizontal dashed line. [Reproduced with permission from (Khayer & Lake, 2009b); © 2009 IEEE]

fixed, independent of the gate voltage. This decrease in $|\partial E_{CG}/\partial q V_{GS}|$ resulting from charging of the channel is the expected behavior of devices operating in the CCL.

For an *n*-type device, the positive gate bias lowers the band-edge in the channel which results in charging of the channel. The charge results in a self-consistent potential, U_{scf}, which works against the gate bias to raise the band-edge. The larger the density-of-states, the larger the negative feedback will be. This negative feedback is absent, or much reduced, in the QCL. Therefore, the gate bias moves the band-edge less in the *p*-type devices than in the *n*-type devices, and the band-edge in the channel presents a larger barrier to the source in the *p*-type devices than in the *n*-type devices for the same gate overdrive. Therefore, even though the density-of-states and carrier density is higher in the *p*-type channel than in the *n*-type channel, the barrier to source injection is also higher. For a NW in the ballistic limit, ignoring thermal broadening, the current resulting from a single mode *m* is $\frac{2q}{h}$ (E_{FS} – ε_m) where ε_m is the mode energy in the channel. For a *p*-type channel, a larger U_{scf} results in smaller energy differences $|(E_{FS} - \varepsilon_m)|$. Thus, although there are more modes carrying current, each mode is carrying less current than the single mode in the *n*-type device. As a result, the currents of the *n*-type and *p*-type devices tend to be similar for the same gate overdrive.

The negative feedback due to charging affects how far the bands move under the gate, which, in turn, determines how large the source Fermi level must be to avoid source injection saturation. At the maximum gate overdrive of 0.2V, the conduction band edge under the gate is pushed 0.12 eV below the Fermi level of the source for both the InAs and InSb NWFETs. For the p-type devices with greater charging, the band edges move less. At the maximum gate overdrive, the InSb and InAs bandedges under the gate are pushed 91

meV and 69 meV above the Fermi level of the source, respectively. Therefore to ensure that the current is not limited by source injection saturation, the source Fermi level should be at least ~ 0.15 eV above the conduction band edge of the source for the 4nm n-type NWFETs and at least ~ 0.1 eV below the valence band edge of the source for the 4nm p-type NWFETs. Finally, we compare to the numbers predicted or projected for other materials and dimensionalities. For *n*-type InSb and InAs NWFETs with 4 nm NW diameter, the values of $P \cdot \tau_D$ are half the value of 5×10^{-20} J, and the values of $P \cdot \tau_D$ with 10 nm NW diameter are close to the value of 5×10^{-20} J predicted in Ref. (Knoch et al., 2008) for a 3 nm diameter Si NWFET with a 10 nm gate length. The corresponding gate delay times for the *n*-type devices with 4 nm NW diameter are close to the value of 8 fs and the gate delay times with 10 nm NW diameter are twice the value of 8 fs predicted in Ref. (Knoch et al., 2008) for a 3 nm diameter Si NWFET with 10 nm long gate. The energy-delay product for *n*-type devices with 4 nm NW diameter is found to be 10 - 100 times lower than the projected experimental curve for a III-V planar *n*-channel MOSFET with a 10 nm channel width (Chau et al., 2005). For *n*-type devices with 10 nm NW diameter, however, the energy-delay product falls on the projected experimental curve for a III-V planar *n*-channel MOSFET with a 10 nm channel width (Chau et al., 2005). For *p*-type devices with 4 nm NW diameter, $E \cdot \tau_D$ is found to be 10 - 100 times lower than the projected experimental curve and with 10 nm NW diameter, $E \cdot \tau_D$ falls on the projected experimental curve for *p*-channel CNTFET and Si NWFET with 10 nm channel width (Chau et al., 2005).

4.2 The diameter dependent performance

To investigate diameter dependent performance, we choose the *n*-type NWFETs composed of InSb or InAs as core and InP as shell materials. The diameters are varied from 10 nm to 60 nm. To calculate the mode energies and $E - k$ dispersions for various diameter NWs, we use an analytical 2-band dispersion relation,

$$E(1+\alpha E) = \frac{\hbar^2 k^2}{2m^*}, \tag{30}$$

where $\alpha = \frac{1}{E_G}(1 - \frac{m^*}{m_0})^2$. E_G = 0.23 eV is the bulk bandgap, $m^* = 0.013m_0$ is the bulk electron effective mass, and m_0 is the bare electron mass.

The semiclassical ballistic model as described in sec. 3.4 is used to obtain the charge density, the self consistent potential and the current. After self consistency between the potential and the charge is achieved, the drain current for the *n*-type InSb NWFETs is calculated as,

$$I = \sum_m M \frac{qk_BT}{2\pi\hbar}\left[\Im_0(\eta_m) - \Im_0(\eta_m - U_D)\right], \tag{31}$$

where M stands for spin degeneracy, m is the mode index, k_B is the Boltzmann constant, T is the temperature. $U_D = V_{DS}/(k_BT/q)$ and $\eta_m = (E_{FS} - \varepsilon_m(0) + qU_{scf})/k_BT$, where E_{FS} is the source Fermi level and $\varepsilon_m(0)$ is the m-th subband level at the top of the barrier. The function $\Im_i(x)$ is the Fermi-Dirac integral.

The drain bias voltage is fixed at 0.5 V for all devices. To compare the effect of different cross-sections and doping, we fix the gate overdrive to 0.2 V for all devices. The threshold

voltages are determined from the linear I_D-V_{GS} curves. For all diameters, two different Fermi levels in the source are modeled, $E_F - E_c = 0.1$ eV and 0.2 eV.

It is shown that relatively larger diameter (≤60 nm) InSb NWFETs (Khayer & Lake, 2008b) operate in the QCL. This is a result of the small effective mass, and hence the smaller density of states of these material. Both the energy-delay and power-delay products are reduced as the diameter is reduced, and optimum designs are obtained for diameters in the range of 10 - 40 nm (Khayer & Lake, 2008b).

Fig. 6(a-c) presents the number of spin degenerate modes as a function of mode energy for 10nm, 30nm, and 60nm diameter InSb NWs, and Fig. 6(d-f) shows the corresponding quantum capacitances vs. the source Fermi energy. We consider InSb NWFETs with Fermi levels of up to 0.2eV in the source. In all cases, the NWFETs contain multiple modes as shown in Fig. 6(a-c). The relationship between the number of populated modes and the quantum capacitance is obvious from Figs. 6. Figs. 6(a) and 6(b) show the effect of discrete, well-spaced modes on the quantum capacitance, C_Q. The dashed lines in Figs. 6(e-f) show the geometrical gate capacitance, C_G. For source Fermi energy such that $E_F - E_C$=0.1eV, all of the InSb NWs with diameters ≤60nm have $C_Q < C_G$, and thus operate in the QCL.

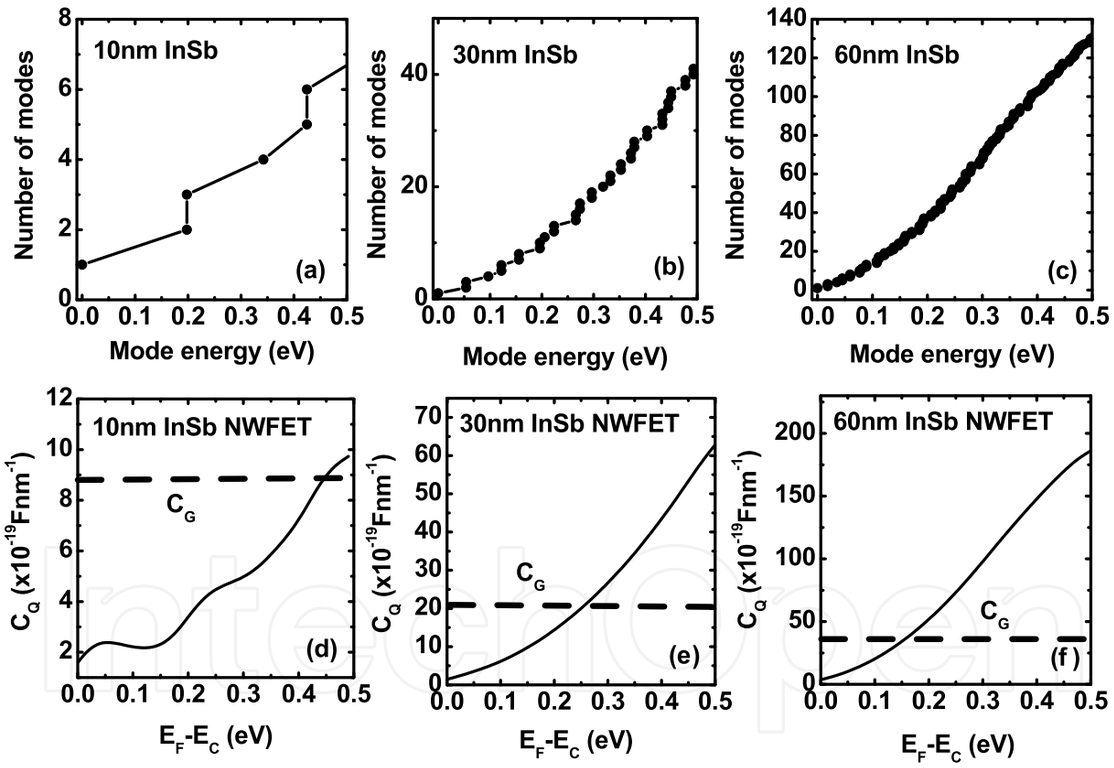

Fig. 6. (a-c) Number of conduction modes (without spin) as a function of the mode energy for the simulated InSb NWFETs with 10 nm, 30 nm, and 60 nm NW diameters. All the devices contain multiple modes within the energy range considered. (e-f) Quantum capacitance as a function of the source Fermi level for the corresponding NWFETs. The geometrical capacitance, C_G is also shown. C_G is calculated from $C_G = (2\pi\epsilon_r\epsilon_0)/(ln((2d_{ox} + d_{NW})/d_{NW}))$ assuming a coaxial gate geometry. All the devices are operating in the quantum capacitance limit within source Fermi level ($E_F - E_c = E_{FS}$) range of 0.1-0.2 eV. [Reproduced with permission from (Khayer & Lake, 2008b); © 2008 IEEE]

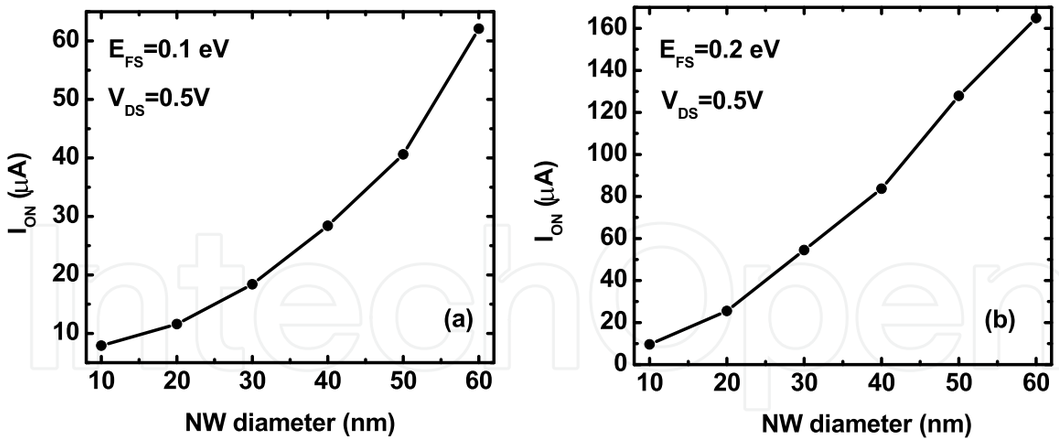

Fig. 7. ON-current as a function of NW diameter with source Fermi level ($E_{FS} = E_F - E_c$) of 0.1 eV (a), and 0.2 eV (b). The drain bias voltage is fixed at 0.5 V as shown. The gate voltage is fixed at a gate overdrive of 0.2V, i.e., $V_{GS} - V_T = 0.2$ where V_T is the threshold voltage for each device. [Reproduced with permission from (Khayer & Lake, 2008b); © 2008 IEEE]

within a particular Fermi energy, larger number of conduction modes become populated as the NW diameter increases (Fig. 6(a-c)), and the drain current increases. Fig. 7 shows the ON-current as a function of the NW diameter for two source Fermi energies, 0.1 eV (a), and 0.2 eV (b). The drain bias voltage is fixed at 0.5 V for each device, and the gate bias voltage is fixed at a gate overdrive of 0.2 V, $V_{GS} - V_T$=0.2 V, where V_T is the threshold voltage and has been calculated from the linear I_{DS}-V_{GS} characteristics for each device. The ON-current for all devices varies from 7 - 165 μA within a source Fermi energy variation of 0.1 - 0.2 eV.

With an increase of the NW diameter, as shown in Fig. 8(a, b), the power-delay product increases and the gate delay decreases . The power-delay product, $P \cdot \tau$, is calculated from $\int QdV_{GS}$, where Q is the magnitude of the charge in the channel. The gate delay is obtained from $\tau = \int QdV_{GS}/(V_{DD}\, I_{ON})$. The gate delay time τ for all devices varies from 4 – 16 fs within a source Fermi level range of 0.1-0.2 eV and decreases as the NW diameter increases (Figs. 8(a, b)). This is due to the higher ON-current for the larger diameter NWs (Figs. 7). $P \cdot \tau$ varies from 2×10^{-20} J to 68×10^{-20} J for all devices with a source Fermi level range of 0.1 - 0.2 eV. For $E_F - E_c = 0.1$ eV, the values of $P \cdot \tau$ for diameters 10 - 50 nm all match closely the value of 5×10^{-20} J predicted in Ref. (Knoch et al., 2008) for a 3 nm diameter Si NW FET with a 10 nm gate.

Fig. 8(c, d) presents the energy-delay product as a function of NW diameter. As diameter and Fermi energy increase, the energy-delay product also increases. The energy-delay is the product of the power-delay and the delay time shown in Fig. 8(a, b). It is interesting that the 1.4×10^{-33} Js energy-delay product of the 10 nm NW FET with $E_F - E_c = 0.2$ eV falls on the projected experimental curve for a III-V planar HEMT with a 10 nm channel width shown in Fig. 7 of (Chau et al., 2005).

Both the energy-delay and power-delay products are optimal for diameters in the range of 10 - 40 nm with source Fermi levels of 0.1 eV. Increasing the source Fermi level increases C_Q which causes a rapid degradation of the energy-delay product. Approximating τ as $\frac{C_Q V_{DD}}{I_D}$, the energy-delay product is proportional to $\frac{C_Q^2}{I_D}$. In this case, the increase in C_Q overrides the increase in I_D.

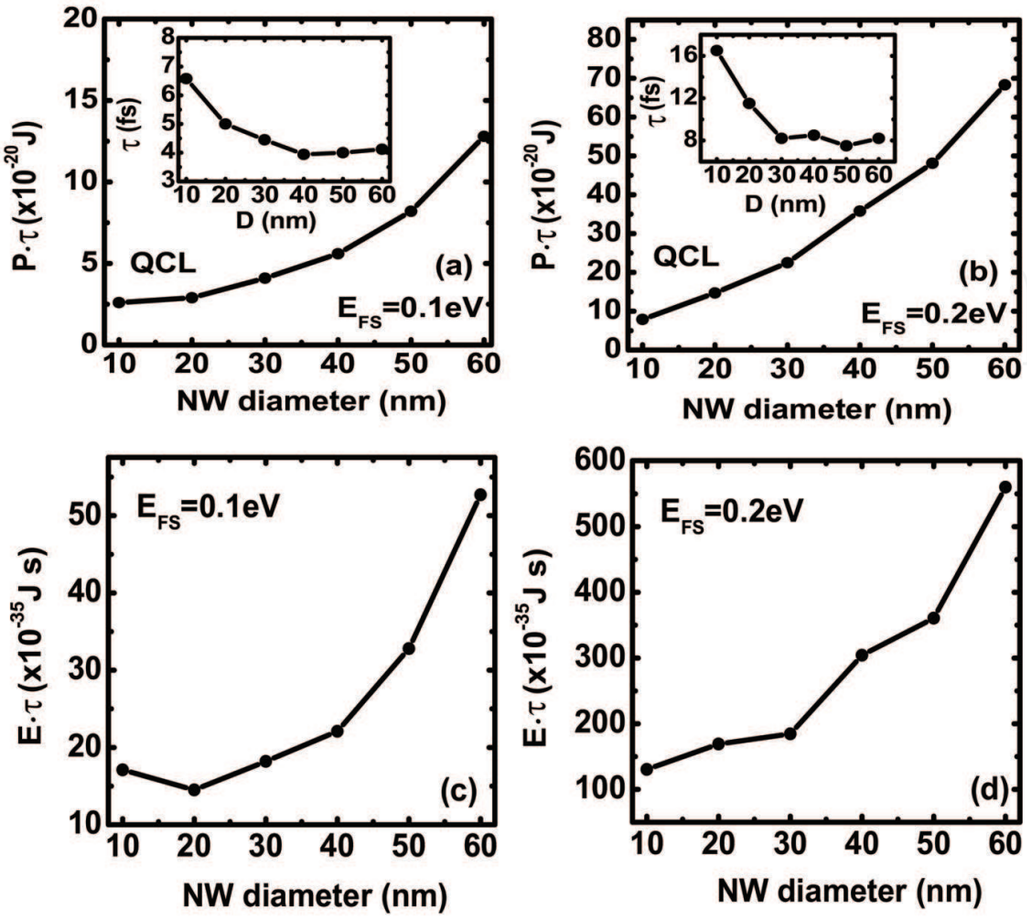

Fig. 8. Simulated $P \cdot \tau$ (power-delay product) (a, b) and $E \cdot \tau$ (energy-delay product) (c, d) as a function of NW diameter with source Fermi level ($E_{FS} = E_F$-E_C) of 0.1 eV , and 0.2 eV. $P \cdot \tau$ is calculated as $\int QdV_{GS}$, where Q is the total channel charge extracted from the simulations. Accordingly the gate delay time $\tau = \int QdV_{GS}/(V_{DD}I_{ON})$. $E \cdot \tau$ is the product of the $P \cdot \tau$ and the gate delay τ. Device operating regime, quantum capacitance limit (QCL), is indicated in the plots. These curves show a significant performance improvement in terms of the power-delay product and energy-delay product for the devices scaled towards the quantum capacitance limit with E_{FS} =0.1 eV. Inset in Figs. (a, b) shows the gate delay time as a function of NW diameter extracted from the simulations. A gate length of 10 nm was considered to calculate these values. [Reproduced with permission from (Khayer & Lake, 2008b); © 2008 IEEE]

5. Conclusion

In conclusion, we have presented a full 3-D discretized 8-band $\mathbf{k} \cdot \mathbf{p}$ model to calculate the electronic bandstructures of III-V and II-VI compound semiconductor materials in quantum confined structures. In particular, we have investigated high speed, low power InSb and InAs NWFETs in two operating regimes, the quantum capacitance limit and the classical capacitance limit. These materials are believed to be strong candidates for extending high performance logic beyond the 22 nm technology node.

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Nanowires Science and Technology

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This book describes nanowires fabrication and their potential applications, both as standing alone or complementing carbon nanotubes and polymers. Understanding the design and working principles of nanowires described here, requires a multidisciplinary background of physics, chemistry, materials science, electrical and optoelectronics engineering, bioengineering, etc. This book is organized in eighteen chapters. In the first chapters, some considerations concerning the preparation of metallic and semiconductor nanowires are presented. Then, combinations of nanowires and carbon nanotubes are described and their properties connected with possible applications. After that, some polymer nanowires single or complementing metallic nanowires are reported. A new family of nanowires, the photoferroelectric ones, is presented in connection with their possible applications in non-volatile memory devices. Finally, some applications of nanowires in Magnetic Resonance Imaging, photoluminescence, light sensing and field-effect transistors are described. The book offers new insights, solutions and ideas for the design of efficient nanowires and applications. While not pretending to be comprehensive, its wide coverage might be appropriate not only for researchers but also for experienced technical professionals.

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