Chapter

Noise Analysis in Nanostructured Tunnel Field Devices

Sweta Chander and Sanjeet Kumar Sinha

Abstract

Tunnel Field Effect Transistors (TFETs) have appeared as an alternative candidate of "beyond CMOS" due to their advantages like very low leakage current and steep sub-threshold slope i.e. <60 mV/dec., etc. From past decades, researchers explored TFETs in terms of high ON current and steep subthreshold slope at low supply voltage i.e. < V_{DD} = 0.5 V. The reliability issues of the device have profound impact on the circuit level design for practical perspectives. Noise is one of the important parameters in terms of reliability and very few research papers addressed this problem in comparison to other parameter study. Therefore, in this chapter, we discussed the impact of noise on Tunnel FET devices and circuits. The detail discussion has been done for the random telegraph noise, thermal noise, flicker noise, and shot noise for Si/Ge TFET and III-V TFETs. Recent research work for both low frequencies as well high frequency noise for different TFET device design has been discussed in details.

Keywords: Band-to-Band Tunneling, Flicker noise, Shot noise, Thermal noise, Random Telegraph Noise

1. Introduction

The semiconductor industry has been on a continuous run to search for miniaturized devices without compromising the electrical parameters [1]. Scaling down the device dimensions of *metal–oxide–semiconductor field-effect transistor* (MOSFET) has been very challenging due to the short channel effects like high subthreshold slope, high leakage current, and threshold voltage roll-off, etc. [2]. Tunneling-field-effect-transistor (TFET) has appeared as a potential substitute to replace already existing MOSFET because of small leakage current and steep Subthreshold Swing (SS) [3, 4]. The basic difference between the MOSFET and TFET is the working principle. In MOSFET the current through the channel is set by an energy barrier and the height of the barrier determines the amount carriers injected into the channel thermionically. But in TFET, the charge carriers tunnel through the barrier to reach the channel [5]. TFET is gated reverse-biased pin diodes that operate on Band to Band (BTBT) tunneling principle [6, 7]. In the miniaturized devices operating on low voltages, the electrical noise has a serious effect on the device performance [8, 9]. The non-white noises like flicker noise and burst noise become more vigorous as we scale down the device dimensions, which degrades the performance of semiconductor memories [10] and analog circuits [11]. Also, high-frequency white noise sources like shot noise and thermal noise are desirable in

analog/Radio-frequency (RF) applications [12]. In the literature, the effect of electrical noise on the performance of TFETs has not been reported much and still under exploration. In the presence of noise, it is quite difficult to comprehend the behavior of TFETs. In the literature, very few works related to the modeling of the impact of high-frequency noise and low-frequency noise on the performance of TFETs have been reported [13, 14]. This paper provides a detail study of types of electrical noise in TFET structures and the modeling of electrical noise in various TFET structures. This paper also elaborates on the basic working principle of TFET along with the device operation.

2. Tunnel field effect transistors

TFET is gated reverse-biased pin diodes that operate on BTBT) tunneling principle [15]. **Figure 1** shows the cross-sectional view of double gate TFET and energy band diagram of TFET for ON and OFF state, in which p-type silicon substrate of length L_{ch} is taken. The source and drain regions have lengths of L_s and L_d with heavily doped p-type and n-type materials. Also, gate oxide of thickness T_{ox} is deposited over a p-type silicon substrate.

When no voltage is applied at the gate terminal, no current flows through the channel. In TFETs, the off-current/leakage current is very small that makes it an energy-efficient device. When a positive bias is applied at the gate terminal, it pushes the conduction band down in the channel region. Thus, a tunneling path is formed between the source band and channel conduction bands.

In heterojunction TFET (HTFET), high ON current and low leakage current can be achieved. The source and channel may have large band gaps in the case of HTFET but at the source-channel interface, the tunneling barrier reduces significantly [16]. The energy band diagram of homojunction and heterojunction TFET is shown in **Figure 2**. In homojunction TFET, the same material is used for the source,

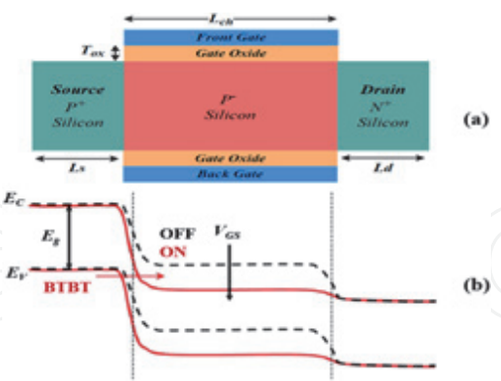

Figure 1.
(a) Cross-sectional view of double gate TFET (b) energy band diagram of TFET for ON and OFF state.

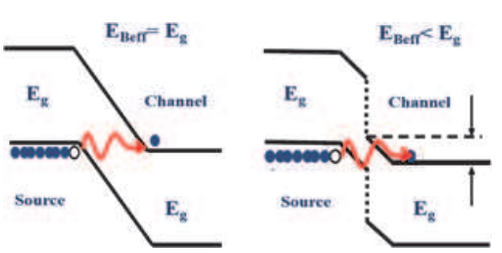

Figure 2.
Energy band diagram of homojunction and heterojunction TFETs [16].

channel, and drain. The barrier height and the bandgap of material are the same. In heterojunction TFET, at the source-channel junction, the barrier height reduces significantly.

3. Noise in MOS devices

It is very significant to study the sources of noise as noise degrades the quality of the desired signal. In MOSFET, the various noise sources are: (a) thermal noise introduced by the channel/polysilicon gate resistance/source-drain resistance/distributed substrate resistance, (b) flicker noise from the channel. In MOSFET device thermal noise dominates at high frequency and in the channel, it further gives rise to both drain channel noise and induced gate noise. In the nMOS structure, excess thermal noise exhibits in the channel. As drain to source voltage is increased, the noise in the channel increases [17].

D.P. Triantis et al. presented a systematic formulation of the high frequency noise in short-channel MOSFET. The reported MOSFET structure was operating in the saturation region [18]. The small-signal behavior and noise analysis of nanoscale MOSFET at RF was reported by M.A. Chalkiadaki and C.C. Enz [19]. A.G. Mahmutoglu and A. Demir presented an idealized trap model to encounter the behavior of traps present in the gate oxide [20]. H. Tian and A. EL. Gamal proposed a nonstationary extension noise model to analyze flicker noise in MOSFET circuits more accurately [21]. C. Hu et al. studied the low-frequency noise characteristics of MOSFET to investigate the effect of noise by changing metal interconnect perimeter length, device W/L ratio, and gate-biasing voltage [22].

Renuka Jindal developed noise mechanisms in MOSFET for both intrinsic and extrinsic noise. The study of intrinsic noise mechanisms is essential to study the effect of channel thermal noise, induced gate noise, and induced substrate noise on device operation [23].

4. Noises in tunnel FETs

In Tunnel FETs, different types of noise from low-frequency to high-frequency must be considered. Low-frequency noise can be further classified into random telegraph noise (RTN)/burst noise and flicker noise, while high-frequency noise can be further classified into shot noise and thermal noise.

4.1 Low frequency noise sources

4.1.1 Random telegraph noise

Random telegraph noise (RTN) is a non-white noise that mainly occurs due to the presence of impurities in semiconductors and thin gate-oxide films. The trapping and de-trapping of carriers in the channel are the source of RTN [24]. If the trap is located on the source-channel interface, RTN is more pronounced because the trapped charge can change the junction electric field which in turn affects BTBT [25]. It is a function of temperature, radiation, and induced mechanical stress. In audio amplifiers, the burst noise sounds as random shots, which are similar to the sound associated with making popcorn. The noise spectral density is given by RTN is given by Eq. (1) [26]:

$$S_{RTN}(f) = C\frac{4(\Delta I)^2}{1+\left(\frac{2nf}{f_{RTN}}\right)^2} \tag{1}$$

f_{RTN} is RTN noise corner frequency. The intensity of RTN noise depends upon the site at which the trap center is located concerning the Fermi level and the center area of the Fermi level is responsible for the generation of RTN noise.

4.1.2 Flicker noise

Flicker noise is a low-frequency noise that arises from the trapping and de-trapping of charge carriers in the trap states in the gate oxide around the quasi-fermi level. It is mostly generated at the interface of Si-substrate and gate oxide. At the interface of Si substrate, there exist dangling bonds. These dangling bonds give rise to extra energy states. The charge carriers that move across these energy states, get trapped in these sites. The noise spectral density is given by surface model is given by Eq. (2) [26]:

$$S_{\frac{1}{f}}\alpha\left(\overline{\Delta N}\right)^2\int_{\tau_1}^{\tau_1}\frac{1}{\tau}\,\frac{4\tau}{1+\omega\tau^2}d\tau = \left(\overline{\Delta N}\right)^2\frac{1}{f} \tag{2}$$

where, $\frac{1}{\tau_2} \ll \omega \ll \frac{1}{\tau_1}$ and the noise spectral density for surface model remains constant up to$f_2 = \frac{1}{2\pi\tau_2}$.

4.2 High frequency noise sources

Thermal noise and shot noise are the two types of noise sources that degrade the device's performance operating at high frequency. For the analysis of thermal noise effect on TFET structure, the thermal noise model of MOSFET in ON-state is used, when the applied drain-source voltage is zero [27]. Though, shot noise is the dominant form of high-frequency noise/white noise in heterojunction TFET. The modeling of shot noise can be done in the same way as it is done in tunnel diodes [28].

4.2.1 Shot noise

In electronic devices, the noise that arises due to the unavoidable random fluctuations of electric current when the charge carriers travel a gap is known as shot noise [29]. Shot noise exhibits since the current is not a continuous flow but it is the sum of discrete pulses in time where each pulse corresponds to the transfer of electron through a conductor. Shot noise is caused by the thermal motion of electrons and occurs in any conductor having resistance R. The most dominant white noise is shot noise and in TFET, it can be modeled similarly as it is modeled in tunnel diode.

$$i_{shot}^2 = 2qI_D\Gamma \tag{3}$$

where, Γ is Fano factor that indicates the deviation in the magnitude of shot noise from the nominal value I_D. Fano factor value depends upon applied voltage and it is frequency independent [30].

4.2.2 Thermal noise

In electronic devices, the noise generated inside a conductor at equilibrium due to the thermal agitation of charge carriers is known as thermal noise. In 1928, Johnson experimentally verified the theory of the fluctuating movement of charges in thermal equilibrium that was initially proposed by Einstein in 1905 [31]. The magnitude of random motion of free electrons and resistance of elements increases with an increase in temperature. Due to this thermal motion of charge carriers, a fluctuating voltage is created at the terminals of the conductor [12].

5. Recent study of noises in tunnel FETs

The electrical noise analysis especially the low-frequency noise analysis of TFET structure has been done by many researchers from universities and electronic companies. But the high-frequency analysis of TFET is yet to be explored a lot. In the past a few years, the research of various TFET structures has been accelerated. The brief review of impact of noise on various TFET structure is presented in this section.

The impact of single acceptor-type and donor-type interface trap induced RTN on TFET was reported in [32]. Using a charge-based approach, an analytical model for thermal noise and induced gate noise was proposed in junctionless FETs, whereas the power spectral density of noise was the same for the same drain voltage [33]. Neves et al. reported the effect of low-frequency noise on the behavior of vertical tunnel FETs (TFETs) experimentally and compared with MOSFET [34]. Chen et al. reported the amplitude of RTN on the characteristics of TFET experimentally and reveals that nonuniform distribution of BTBT generation rate along device width direction is responsible for high-amplitude of RTN. It also shows the high source doping concentration fluctuates the BTBT generation rate and reduces the RTN amplitudes [35]. High-frequency noise shows different behavior for the devices having different gate lengths. The scaling of gate length of the High-electron-mobility-transistor (HEMT) was performed in [36]. **Figure 3** shows the change in the value of the noise suppression factor by changing length.

Ghosh et al. presented analysis of flicker noise of TFET structure. A selective buried oxide (SELBOX) SiGe layer has been used at the source channel junction in the presence of trap concentrations as shown in **Figure 4a**. In **Figure 4b**, the presence of trap degrades both ON–OFF current ratio and SS has been studied. Thus, it degrades the overall performance of the device [37].

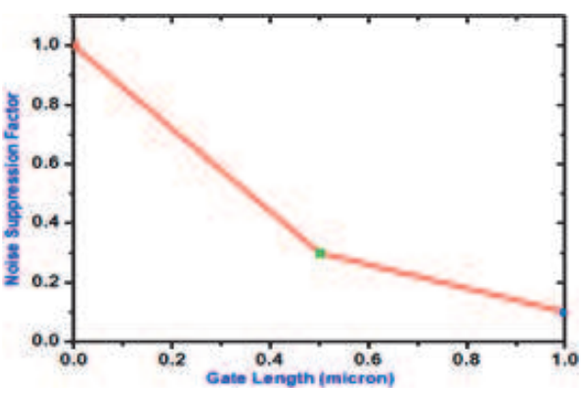

Figure 3.
Gate length vs. noise suppression factor [36].

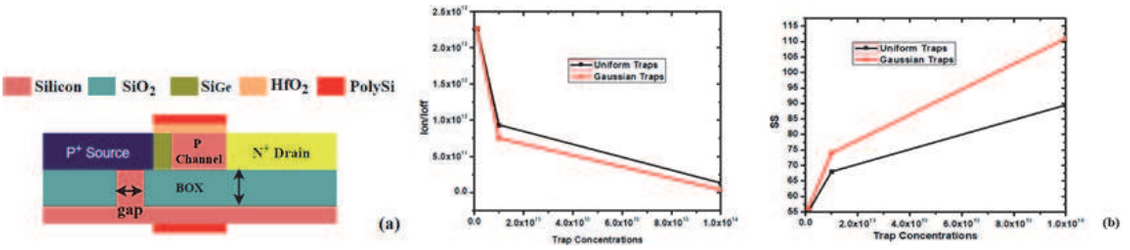

Figure 4.
(a) Proposed SELBOX structure, (b) effect of change in trap concentrations on ON–OFF current ratio and SS [37].

S.Y. Kim et al. reported the dependency of low frequency noise on the applied gate voltage of TFET device. At low gate voltage, the noise in TFET is high and for high gate voltage, electrons directly tunnel from source to drain and noise in TFET is low [38].

Another noise analysis of Ferroelectric Dopant Segregated Schottky Barrier TFET has been done for different types of materials in the dopant segregated layer and concluded that flicker noise affects the low frequency and mid-frequency range [39].

6. Noise in Si/Ge tunnel FETs

The conventional Si-based TFET exhibits SS of less than 60 mV/decade and a very small leakage current but practically implementation is still questionable because of low ON current. Thus, to improve the ON current, a thin layer of SiGe can be used on top of the Si source. It is found from, study that the proposed device is free from short channel effects. Using the strained SiGe layer improves on current while leakage current was still very low (fA) [40]. In **Figure 5**, the proposed TFET structure with a strained SiGe layer is shown.

The features like VLSI compatibility, mature synthesis techniques, and tunable bandgap makes SiGe compatible with the TFET structure. Li et al. experimentally demonstrated a TFET structure in which a thin layer of SiGe is inserted between source and channel. By using the SiGe layer, it has been found that the ON current increases and SS reduces. The barrier height of tunneling reduces and the lateral electric field increases that further increases the transport of carriers across tunneling junction. The performance of the proposed TFET device has been improved by using SiGe [41].

Vandooren et al. presented the electrical performance of vertical Si homo-junction and SiGe source hetero-junction TFETs. The analysis of trap-assisted tunneling through simulations and characterization has been performed. The trap-assisted tunneling worsens the onset characteristics and SS of the TFET. The simulation results of Ge TFET are in agreement with experimental data up to some

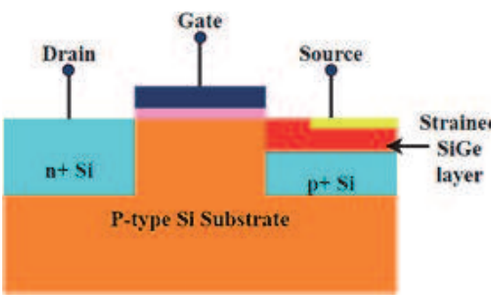

Figure 5.
TFET structure with strained SiGe layer [40].

extent. The results demonstrated that SiGe TFET exhibits improved performance than Si TFET because of the lower bandgap [42].

For HTFET and FinFET, an electrical noise model for thermal noise, flicker noise, and shot noise was realized in a differential amplifier with a capacitive load circuit. The circuit shown in **Figure 6** was studied for subthreshold HTFET design to obtain the same range of gain. From the analysis, it evident that the HTFET structure offers to gain twice the gain of FinFET structure. Also, the cut-off frequency is higher in TFET. Also, small-signal amplitudes can be detected by HTFET design. Based on the overall design analysis, it has been found that the proposed device design is more suitable for the applications operating in low-voltage/low-power [26].

Apart from noise, ambipolar behavior also affects the performance of the device. The comparison of different structures of TFET has been reported by Sathish et al. In TFET structures, heterojunctions have been used to form a source/body junction. By doing so, the tunneling distance can be lowered and the ON current can be increased. It can also be used to control the ambipolar behavior of TFET. Heterojunction TFET characteristics can be determined by using different materials structures [43].

For the fabricated devices at the nanoscale, flicker noise becomes very problematic because flicker noise increases the reducing the device dimensions. The measure of device quality and reliability is done by checking the level of flicker noise. Das et al. presented the analysis of low-frequency flicker noise on dual dielectric pocket HTFET as shown in **Figure 7**. Three different gate-source underlap lengths and different thicknesses were considered. This proposed device exhibits a super steep slope and high current ratio. In the analysis, two different trap distributions (uniform and gaussian) were considered. The study specifies that the ON current of

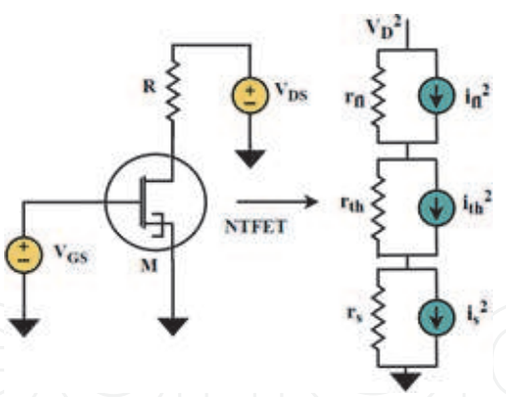

Figure 6.
Representation of noise model implemented at transistor level [26].

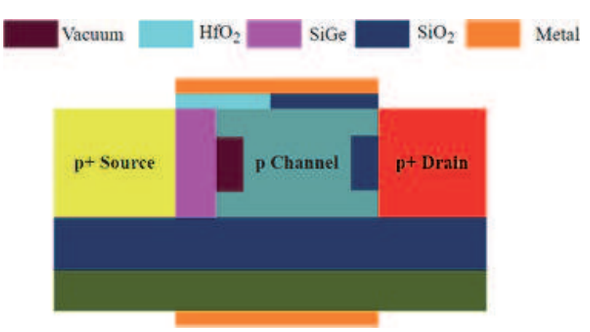

Figure 7.
2-D structure of dual dielectric pocket HTEFT [44].

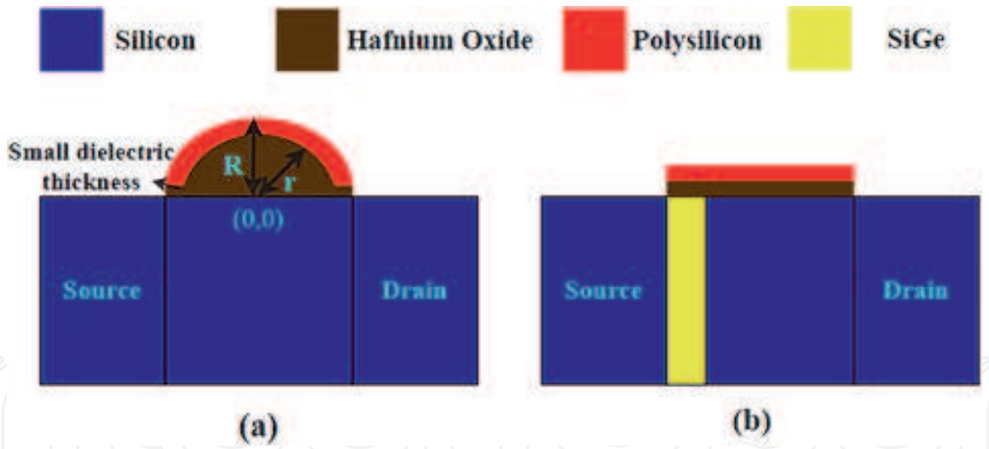

Figure 8.
(a) 2-D structure of novel circular gate TFET (b) and hetero-junction TFET [44].

the reported HTFET structure is not affected by presence of interface traps as compared to the OFF current [44].

Goswami et al. proposed a new architecture of TFET with a circular gate. The electrical noise analysis was performed for both structures; (a) proposed structure (circular gate), (b) HTFET as shown in **Figure 8** [45]. A comparative analysis for both the structures was done also. The uniform and gaussian trap distributions were simulated and based on the simulation results it can be concluded that structure 'a' shows the lesser impact of noise than structure 'b'. Flicker noise shows an intense effect at low frequency and mid-frequency range. While at high-frequency, diffusion noise effects. Nonetheless, the drain current in structure 'a' is more prone to traps than the drain current in structure 'b'. The cut-off frequency of structure can be improved by using gate-drain underlap and it is well-suited for digital applications.

7. Noise in III-V tunnel FETs

In the TFET device, during ON state, very low drive current/ON current flows from source to drain. The drive current can be improved by using low bandgap materials like SiGe, InGaAs, InAs. The use of SiGe has been already discussed in the previous section. **Figure 9** shows the schematic diagram of homojunction and heterojunction TFET using III-V materials.

Pandey et al. reported RTN study analysis of HTFET using III-V materials with 20 nm long and 40 nm wide channels. RTN due to the presence of a single charge trap has been modeled by placing the trap charges to pre-defined coordinated mesh. When the electron got captured in a trap, it causes a reduction in the drain current. Also, the analysis of the relative amplitude dependence of RTN on trap location has been performed. Different locations of the trap were considered for the analysis. Firstly, when the trap is present in the channel, from the source towards drain region. Secondly, three different cases can be considered by changing the depth of

Figure 9.
Homojunction and heterojunction TFET using III-V materials.

the trap like when the trap is (a) present in oxide (b) present in the oxide-channel interface (c) present inside the channel. From the analysis, it has been observed that the relative amplitude of RTNnoise is maximum for case c followed by case b. But the relative RTN amplitude is minimum when the trap is present in gate oxide [13].

Bijesh et al. presented GaAsSb/InGaAs heterojunction TFET using III-V materials. In this work, a high ON current has been achieved at the low drain to source voltage. Also, in the case of InGaAs homojunction, the ON current increases to double the value in heterojunction. Because in heterojunction TFET, reduction in the effective tunneling barrier has been observed. Flicker noise analysis for both homo and heterojunction TFET structure has been performed. The effect of flicker noise on drive current is lower in the case of heterojunction TFET than in homojunction TFET structure. An analytical model to analyze the flicker noise characteristics for both the TFET structure has been developed [46].

Bu et al. developed an analytical model to determine the variation of the electrostatic potential because of the presence of charged trap in the gate oxide of the TFET device. A noise model based on the flow of current through tunneling of carriers in the channel has been proposed. The power spectral density of the TFET device is presented that shows dependency on the frequency and applied gate voltage. It is evident from the analysis that the noise power spectral density of because of the tunneling is more affected by voltage applied at gate terminal than the movement of traps through the channel. The noise observed in the channel is due to the variation in the mobility of traps [47].

8. Impact of noise in TFET based circuit and memory design

In the processors, SRAM memory cell have been broadly used as data caches and these memory cells are the most significant digital building blocks. Fan et al. widely reviewed the effect of single-trap-induced RTN on TFET, and FinFET. The effect of noise on BTBT dominated current conduction in TFET and thermionic based current conduction has been presented in both device and circuit level. The trap location has an intensive effect and that effect varies with applied bias variation and type of trap. The worst-case analysis of different parameters for RTN noise has been investigated for TFET based 6 T/8 T SRAM cells [48]. For different trap locations A, B, C, A', B′ the analysis of TFET device has been performed. **Figure 10** demonstrates the diagram of reverse-biased TFET with a single charge trap and having asymmetric source and drain dopant concentrations.

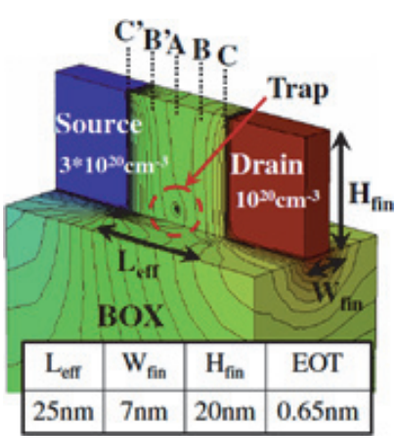

Figure 10.
Potential contour by charge trap [48].

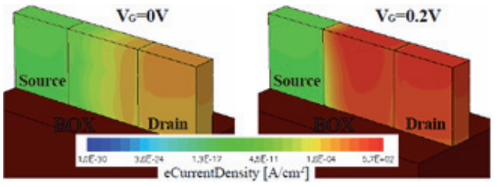

Figure 11.
TFET electron density profile for two different voltages [50].

S.H. Fani et al. presented a new low-power TFET 8 T-SRAM cell with an improved noise margin. The stability of the 8 T-SRAM cell was improved by using supply feedback. The proposed structure exhibits 33% in reading noise margin and 26% in write margin as compared to conventional 6 T SRAM cell for the supply voltage of 0.3 V. The area of the proposed SRAM is larger than the existing one but the features like stability and high performance at very low voltage supply make it useful. The use of the TFET device has limited the working of SRAM cells as it is a unidirectional device but this issue has been resolved by using transistors (n-type and p-type) placed parallelly and the use of one bit-line [49].

The investigation of the effect of RTN noise present in TFET-based 8 T SRAM cell was done by Fan et al. To account the effect of negatively charged trap, the atomistic 3D TCAD simulations were performed for the analysis of TFET-based SRAM. From the analysis, it has been observed that if the trap is present near the tunneling junction, fluctuation in drain current has been observed. The RTN causes 16% additional variation for 8 T SRAM circuit configuration [50]. The electron current density profile for gate voltage values of 0 V and 0.2 V has been shown in **Figure 11**. An increase in gate voltage increases the electron current density.

Luong et al. fabricated half SRAM (HSRAM) cells to examine the capability of TFETs for 6 T-SRAM for the first time. This reported structure has been strained with Si nanowire. The proposed TFET structure does not work up to the mark even when the ambipolar behavior has not been included. Also, analysis of the proposed structure has restricted the static figure of merit [51].

Pandey et al. investigated the effect of a single charge trap RTN in HTFET-based SRAM. This study focused on the analysis of Schmitt trigger mechanism-based variation tolerant 10 T SRAM. A comparison of Si-FinFET and HTFET in terms of iso-area SRAM cell configurations has been done. It has been clear from the analysis that HTFET based SRAM cells show very good performance even in the presence of RTN. For the applied voltage of 0.2 V, the proposed structure offers 15% more improvement as compared to Si-FinFET. Also, the HTFET ST SRAM structure shows less delay in a read operation and consumes less power [52].

The performance of MOSFET devices degrades on scaling down the dimensions. All the issues can be solved using TFET structures as TFET devices offer low leakage current and steeper SS. Nonetheless, TFETs are ambipolar and produce low ON current. However, this behavior can be overcome by using increasing the doping concentration. The main challenges in TFETs are to achieve high ON current, low OFF current, and low average SS. By choosing an accurate predictive model, proper choice of materials, and dimensions of the device, these challenges can be overcome.

9. Conclusion

Noise is one of the important parameters in terms of reliability. This review reported the impact of noise in Tunnel FET devices to understand the reliability issues. The detail discussion has been done for the random telegraph noise, thermal

noise, flicker noise, and shot noise for Si/Ge TFET and III-V TFETs. Recent research work for both low frequency as well high frequency noise for different TFET device design has been discussed in details. The effect of noise for memory and circuit based on Tunnel FET devices as also been discussed. The effect of noise on BTBT dominated current conduction in TFET and thermionic based current conduction has been presented in both device and circuit level. The analytical models for noise analysis of different TFETs structures has also been reported which is required for circuit implementation and memory design.

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References

[1] R. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester and T. Mudge, "Near-threshold computing: reclaiming Moore's law through energy efficient integrated circuits", Proc. IEEE, vol. 98, no. 2, pp. 253–266, 2010.

[2] S. Chander, P. Singh and S. Baishya, "Optimization of direct tunneling gate leakage current in ultrathin gate oxide FET with High-K dielectrics", International Journal of Recent Development in Engineering and Technology, vol. 1, no. 1, pp. 24-30, 2013.

[3] S. O. Koswatta, M. S. Lundstrom and D. E. Nikonov, "Performance comparison between p–i–n tunneling transistors and conventional MOSFETs", IEEE Trans. Electron Devices, vol. 56, pp. 456–465, 2009.

[4] W. Y. Choi, B. G. Park, J. D. Lee and T. J. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec", IEEE Electron Device Lett, vol. 28, pp. 743–745, 2007.

[5] S. Banerjee, W. Richardson, J. Coleman and A. Chatterjee, "A new three-terminal tunnel device", *IEEE Electron Device Lett*er, vol. 8, pp. 347–349, 1987.

[6] K. K. Bhuwalka, J. Schulze and I. Eisele, "Scaling the vertical tunnel FET with tunnel bandgap modulation and gate workfunction engineering", IEEE Trans. Electron Devices, vol. 52, pp. 909–917, 2005.

[7] S. Chander, B. Bhowmick and S. Baishya, "Heterojunction fully depleted SOI-TFET with oxide/source overlap", Superlattices and Microstructures, vol. 86, pp. 43-50, 2015.

[8] G. Ghibaudo and T. Boutchacha, "Electrical noise and RTS fluctuations in advanced CMOS devices", Microelectron. Rel., vol. 42, no. 4, pp. 573–582, 2002.

[9] M. J. Knitel, P. H. Woerlee, A. J. Scholten and A. Zegers-Van Duijnhoven, "Impact of process scaling on 1/f noise in advanced CMOS technologies", IEDM Tech. Dig., pp. 463–466, 2000.

[10] M. Agostinelli, J. Hicks, J. Xu, B. Woolery, K. Mistry, K. Zhang, *et al.*, "Erratic fluctuations of SRAM cache Vmin at the 90 nm process technology node", IEDM Tech. Dig., pp. 655–658, 2005.

[11] K. K. Hung, P. K. Ko, C. Hu and Y. C. Cheng, "A physics-based MOSFET noise model for circuit simulators", IEEE Trans. Electron Devices, vol. 37, no. 5, pp. 1323–1333, 1990.

[12] H. F. Teng, S. L. Jang and M. H. Juang, "A unified model for highfrequency current noise of MOSFETs", Solid-State Electron., vol. 47, no. 11, pp. 2043–2048, 2003.

[13] R. Pandey, B. Rajamohanan, H. Liu, V. Narayanan and S. Datta, "Electrical noise in heterojunction interband tunnel FETs", IEEE Trans. Electron Devices, vol. 61, pp. 52–560, 2014.

[14] R. Bijesh, D. K. Mohata, H. Liu and S. Datta, "Flicker noise characterization and analytical modeling of homo and hetero-junction III–V tunnel FETs", Device Res. Conf. Dig., pp. 203–204, 2012.

[15] L. Zhang and M. Chan, "SPICE modeling of double-gate tunnel-FETs including channel transports", IEEE Transactions on Electron Devices, vol. 61, no. 2, pp. 300-307, 2014.

[16] M. R. Tripathy, A. K. Singh, A. Samad, S. Chander, K. Baral, P. K. Singh and S. Jit, "Device and circuit-level

assessment of GaSb/Si Heterojunction vertical tunnel-FET for low-power applications", IEEE Transactions on Electron Devices, vol. 67, no. 3, pp. 1285-1292, 2020.

[17] R. P. Jindal, "Hot-electron effects on channel thermal noise in fine-line NMOS field-effect transistors. IEEE Transactions on Electron Devices, vol. 33, no. 9, pp. 1395-1397, 1986.

[18] D. P. Triantis, A. N. Birbas and D. Kondis, "Thermal noise modeling for short-channel MOSFETs", IEEE Transactions on Electron Devices, vol. 43, no. 11, pp. 1950-1955, 1996.

[19] M. A. Chalkiadaki and C. C. Enz, "RF small-signal and noise modeling including parameter extraction of nanoscale MOSFET from weak to strong inversion", IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 7, pp. 2173-2184, 2015.

[20] A. G. Mahmutoglu and A. Demir, "Analysis of low-frequency noise in switched MOSFET circuits: Revisited and clarified", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 62, no. 4, pp. 929-937, 2015.

[21] H. Tian and E. L. Gamal, "Analysis of 1/f noise in switched MOSFET circuits", IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 48, no. 2, pp. 151-157, 2001

[22] C. Hu, G. P. Li, E. Worley, and J. White, "Consideration of low-frequency noise in MOSFETs for analog performance", IEEE Electron Device Letters, vol. 17, no. 12, pp. 552-554, 1996.

[23] R. P. Jindal, "Compact noise models for MOSFETs", IEEE Transactions on Electron Devices, vol. 53, no. 9, pp. 2051-2061, 2006.

[24] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "Random telegraph noise of deep-submicrometer MOSFETs," IEEE Electron Device Lett., vol. 11, no. 2, pp. 90–92, 1990.

[25] T. G. M. Kleinpenning, "1/f noise and random telegraph noise in very small electronic devices", Physica B, vol. 164, pp. 331–334, 1990.

[26] A. Konczakowska and B. M. Wilamowski, "Noise in semiconductor devices", Fundamentals of Industrial ElectronicsCRC Press, pp. 11-11, 2018.

[27] R. P. Jindal, "Gigahertz-band high-gain low-noise AGC amplifiers in fine-line NMOS", IEEE Journal of Solid-State Circuits, vol. 22, no. 4, pp. 512-521, 1987.

[28] J. Tiemann, "Shot noise in tunnel diode amplifiers," Proc. IRE, vol. 48, no. 8, pp. 1418–1423, 1960.

[29] B. E. Turner, "Noise in the tunnel diode," Ph.D. dissertation, Dept. Electr. Current Rectifiers, Diodes, Electron., Univ. British Columbia, Vancouver, BC, Canada, 1962.

[30] F. Wu, T. Tsuneta, R. Tarkiainen, D. Gunnarsson, T. H. Wang, P. J. Hakonen, "Shot noise of a multiwalled carbon nanotube field effect transistor", *Physical Review B*, vol. 75, no. 12, pp. 125419, 2007.

[31] N. E. Flowers-Jacobs, A. Pollarolo, K. J. Coakley, A. E. Fox, H. Rogalla, W. L. Tew and S. P. Bez, "A Boltzmann constant determination based on Johnson noise thermometry," *Metrologia*, vol. 54, no. 5, pp. 730, 2017.

[32] M. L. Fan, V. P. H. Hu, Y. N. Chen, P. Su and C. T. Chuang, "Analysis of single-trap-induced random telegraph noise and its interaction with work function variation for tunnel FET", IEEE transactions on electron devices, vol. 60, no. 6, pp. 2038-2044, 2013.

[33] F. Jazaeri and J. M. Sallese, "Modeling channel thermal noise and

induced gate noise in junctionless FETs", IEEE Transactions on Electron Devices, vol. 62, no. 8, pp. 2593-2597, 2015.

[34] F. S. Neves, P. G. Agopian, J. A. Martino, B. Cretu, R. Rooyackers, A. Vandooren, E. Simoen, A.V.Y. Thean and C. Claeys, "Low-frequency noise analysis and modeling in vertical tunnel FETs with Ge source", IEEE Transactions on Electron Devices, vol. 63, no. 4, pp. 1658-1665, 2016.

[35] C. Chen, Q. Huang, J. Zhu, Y. Zhao, L. Guo and R. Huang, "New understanding of random telegraph noise amplitude in tunnel FETs", IEEE Transactions on Electron Devices, vol. 64, no. 8, pp. 3324-3330, 2017.

[36] M. W. Pospieszalski, "On the limits of noise performance of field effect transistors", International Microwave Symposium IEEE, pp. 1953-1956, 2017.

[37] P. Ghosh and B. Bhowmick, "Low-frequency noise analysis of heterojunction SELBOX TFET", Applied Physics A, vol. 124, no. 12, pp. 1-9, 2018.

[38] S. Y. Kim, H. S. Song, S. K. Kwon, D. H. Lim, C. H. Choi, G. W. Lee and H. D. Lee, "Gate Voltage Dependence of Low Frequency Noise in Tunneling Field Effect Transistors", Journal of nanoscience and nanotechnology, vol. 19, no. 10, pp.6083-6086, 2019.

[39] P. Ghosh and B. Bhowmick, "Deep insight into material-dependent DC performance of Fe DS-SBTFET and its noise analysis in the presence of interface traps", AEU-International Journal of Electronics and Communications, vol. 117, pp. 153124, 2020.

[40] N. Patel, A. Ramesha and S. Mahapatra, "Drive current boosting of n-type tunnel FET with strained SiGe layer at source", Microelectronics Journal, vol. 39, no. 12, pp. 1671-1677, 2008.

[41] W. Li and J. C. Woo, "Vertical P-TFET with a P-type SiGe pocket", IEEE Transactions on Electron Devices, vol. 67, no. 4, pp. 1480-1484, 2020.

[42] A. Vandooren, D. Leonelli, R. Rooyackers, A. Hikavyy, K. Devriendt, M. Demand, R. Loo, G. Groeseneken and C. Huyghebaert, "Analysis of trap-assisted tunneling in vertical Si homo-junction and SiGe hetero-junction tunnel-FETs", Solid-State Electronics, vol. 83, pp. 50-55, 2013.

[43] M. Sathishkumar, T. A. Samuel and P. Vimala, "A Detailed Review on Heterojunction Tunnel Field Effect Transistors", International Conference on Emerging Trends in Information Technology and Engineering IEEE, pp. 1-5, 2020.

[44] D. Das and U. Chakraborty, "A Study on Dual Dielectric Pocket Heterojunction SOI Tunnel FET Performance and Flicker Noise Analysis in Presence of Interface Traps", Silicon, vol. 13, no. 3, pp. 1-12, 2021.

[45] R. Goswami, B. Bhowmick and S. Baishya, "Electrical noise in circular gate tunnel FET in presence of interface traps", Superlattices and Microstructures, vol. 86, pp. 342-354, 2015.

[46] R. Bijesh, D. K. Mohata, H. Liu and S. Datta, "Flicker noise characterization and analytical modeling of homo and hetero-junction III–V tunnel FETs", Device Research Conference IEEE, pp. 203-204, 2012.

[47] S. T. Bu, D. M. Huang, G. F. Jiao, H. Y. Yu and M. F. Li, "Low frequency noise in tunneling field effect transistors". Solid-State Electronics, vol. 137, pp. 95-101, 2017.

[48] M. L. Fan, S. Y. Yang, V. P. H. Hu, Y. N. Chen, P. Su and C. T. Chuang, "Single-trap-induced random telegraph noise for FinFET, Si/Ge Nanowire FET,

Tunnel FET, SRAM and logic circuits", Microelectronics Reliability, vol. 54, no. 4, pp. 698-711, 2014.

[49] S. H. Fani, A. Peiravi, H. Farkhani and F. Moradi, "A novel TFET 8T-SRAM cell with improved noise margin and stability", *IEEE 21st International Symposium on Design and Diagnostics of Electronic Circuits & Systems,* pp. 39-44, 2018.

[50] M. L. Fan, V. P. H. Hu, Y. N. Chen, P. Su and C. T. Chuang, "Investigation of single-trap-induced random telegraph noise for tunnel FET based devices, 8T SRAM cell, and sense amplifiers", *IEEE International Reliability Physics Symposium,* pp. CR-1, 2013.

[51] G.V. Luong, S. Strangio, A. T. Tiedemann, P. Bernardy, S. Trellenkamp, P. Palestri, S. Mantl and Q. T. Zhao, "Experimental characterization of the static noise margins of strained silicon complementary tunnel-FET SRAM", European Solid-State Device Research Conference IEEE*,* pp. 42-45, 2017.

[52] R. Pandey, V. Saripalli, J. P. Kulkarni, V. Narayanan, S. Datta, "Impact of single trap random telegraph noise on heterojunction TFET SRAM stability", IEEE Electron Device Letters, vol. 35, no. 3, pp. 393-395, 2014.