Chapter

Managing Heat Transfer Issues in Thermoelectric Microgenerators

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Abstract

This chapter deals with heat transfer challenges in the microdomain. It focuses on practical issues regarding this matter when attempting the fabrication of small footprint thermoelectric generators (μTEGs). Thermoelectric devices are designed to bridge a heat source (e.g. hot surface) and a heat sink (e.g. ambient) assuring that a significant fraction of the available temperature difference is captured across the active thermoelectric materials. Coexistence of those contrasted temperatures in small devices is challenging. It requires careful decisions about the geometry and the intrinsic thermal properties of the materials involved. The geometrical challenges lead to micromachined architectures, which silicon technologies provide in a controlled way, but leading to fragile structures, too. In addition, extracting heat from small systems is problematic because of the high thermal resistance associated to heat exchanged by natural convection between the surrounding air and small bare surfaces. Forced convection or the application of a cold finger clearly shows the usefulness of assembling a heat exchanger in a way that is effective and compliant with the mechanical constraints of micromachined devices. Simulations and characterization of fabricated structures illustrate the effectiveness of this element integration and its impact on the trade-off between electrical and thermal behavior of the active materials in device performance.

Keywords: thermoelectricity, silicon technology, micromachining, silicon nanowires, heat exchangers

1. Introduction

It is quite evident that extending or improving human senses has enabled human societies to prosper by acquiring information from their surroundings and gaining knowledge from it. Internet of Things (IoT) embody this trend today combining distributed sensing with high connectivity so that wise decisions and actions follow information gathering and analysis [1, 2]. Trillion Sensors is another paradigm onto which IoT is further exploited on the basis that the more extensive or intensive the deployment of sensor networks is, the more fruitful the knowledge that can be derived from them would be [3, 4].

Small dimensions (nanometers to micrometers) are appropriate in the sensitive part of sensors when they need to interact with phenomena or entities equally characterized by such small dimensions (light, molecules, living cells ...). An overall small size for the sensors themselves is not devoid of interest either. The smaller they are, the more sustainable their fabrication is in terms of materials and energy, and the more cost-effective they become. Small size is also enabling in itself, e.g. medical implants, as well as convenient, e.g. payloads.

Sensing requires energy. A certain provision of energy autonomy is needed for sensors to be deployed in remote locations, harsh environments, or where they need to remain temporary unattended. Batteries is a common way to provide such autonomy, but their charge is finite impeding long-term autonomy scenarios. Moreover, their recharge, replacement and disposal imply a logistic and environmental burden that will not be affordable when IoT gets to its full extent mobilizing tens of billions of devices and an even larger number of sensors.

Secondary batteries can be kept recharged by coupling them with energy harvesters able to draw energy present in the environment [5]. Heat is abundant in natural scenarios, and waste heat is also abundant in human-made scenarios due to laws of thermodynamics and our profuse use of thermal machines. When such heat gives rise to temperature gradients (a situation as simple as a hot surface exposed to air), thermoelectricity is a convenient way to extract electric energy from them [6, 7].

For that extraction to be optimum, the external thermal gradient needs to be fully transposed into the thermoelectric generator itself. Physical interaction of small devices with their environment may exploit profitably some scale factors when going down in dimensions, but, sometimes, small sizes pose a handicap or challenge for such interaction, too. This is the case when trying to cool down locally a part of a small device by exchanging heat with the surrounding air. This chapter tries to illustrate this point by sharing the issues and strategies the authors have dealt, and are dealing with, in their quest for silicon-based miniaturized thermoelectric generators.

2. Silicon-based thermoelectric generators

Silicon technology has been developed around an enabling and highly abundant semiconductor material. It is a mature technology apt to mass-production of devices with economy of scale and it is the champion technology of miniaturization. Not surprisingly, it boosted microelectronics in the XX century and nanoelectronics in the XXI century. In addition to the set of techniques that allow the fabrication of integrated circuits by depositing and patterning thin films on a silicon wafer, silicon technologies also developed micromachining techniques that allow carving and shaping the silicon wafers into structures that are able to interact with the environment. Sensors and actuators belong to the latter category. Since energy harvesters are environmental interacting devices and, application-wise, they should not be much larger than the sensors they will feed, it is only logical that their fabrication will similarly benefit from the silicon technologies toolbox. These technologies do not only excel in miniaturization but also in *integration* capabilities. This is an important aspect as well. Traditional thermoelectric generators are *assembled* from couples of semiconductor pellets, various millimeters in side, that are arranged electrically in series and thermally in parallel together with additional connecting strips and appropriate thermal elements. When going down in dimensions, assembly becomes harder and offers much less latitude for process automation. In this way, resourcing to technologies that inherently offer integration capabilities is convenient, if not a must.

2.1 Micro thermal device architecture

The traditional thermoelectric generators mentioned above feature a π-architecture, where the π symbol gives a visual clue about how each thermocouple is built assembling vertically two semiconductor pellets (*aka* legs) of different polarity (to add-up the contribution of both electrons and holes) and connecting them electrically with a horizontal conductive strip. Several of those thermocouples are then connected in 1D or 2D arrangements [8]. Such disposition is well adapted to exploit vertically occurring gradients: the bottom part is placed in contact with the heat source while the top part contacts the heat sink and the thermoelectric material in between translates the heat flowing through it (or the temperature difference spanning across it) into magnitudes of electrical relevance, V and I, and therefore power ($V{\cdot}I$).

Silicon technologies are of planar nature. They enable massive parallelism at x and y directions for shaping *laterally* devices made from the superposition of several active thin films. Such shaping also involves patterning in the z direction, but the accumulated depth of the films is much lower than the lateral dimensions at play, leading to aspect ratios that are opposite to those that characterize π –shape thermocouples.

The main objective when defining the architecture and the technological route for a *micro* thermoelectric device is to obtain two areas of contrasted temperature in the *surface* of the chip since the thermoelectric materials will be arranged *laterally*. An architecture that translates an external vertical gradient into an internal lateral one is called *transversal,* and to make it possible a *thermal isolated platform* is defined.

The platform consists of a thin silicon area fabricated by eliminating the silicon beneath it. In order to preserve its thermal isolation from the surrounding bulk silicon, the physical connections between them should be minimized. Such connections are the mechanical supports that keep the platform in place (e.g. ancillary silicon bridges) and the thermoelectric materials themselves (and whatever supports they may need). In order to minimize the thermal conduction of these elements, they must be produced with *low thermal conductance either* by resourcing to low thermal *conductivity* materials, when available and technologically feasible, or by acting on their *geometrical dimensions* making them long and thin.

Figure 1 shows the schematics for such a device. Any hot surface in which this device is placed will act as a heat source. The top surface will be exposed to air acting as heat sink and will exchange heat with it. Due to their different thermal mass, the bulk rim area will hardly cool down, thus being the hot part of the device, while the platform will experience a larger decrease of temperature becoming the cold(er) part of it.

With respect to the thermoelectric material, the depicted device follows a uni-leg approach. Two thermoelectric materials are still at play, but a metal one replaces one of the semiconductor legs in order to close the circuit. Some thermoelectric performance is sacrificed because metals behave poorly thermoelectrically (they have higher thermal conductivities and close to zero Seebeck coefficients), but for the architecture presented and to keep processing simple, the use of a metal leg is technologically convenient.

Regarding the semiconductor thermoelectric material, one distinct feature of our approach is resourcing to silicon materials, namely arrays of silicon nanowires (Si NWs). The rationale behind this option is to attempt the fabrication of *all-silicon* microgenerators, thus leveraging the full potential of silicon technologies. Thermoelectric performance of bulk silicon at ambient or moderate temperatures is bad because of its high thermal conductivity. Incidentally, this is the reason why it is

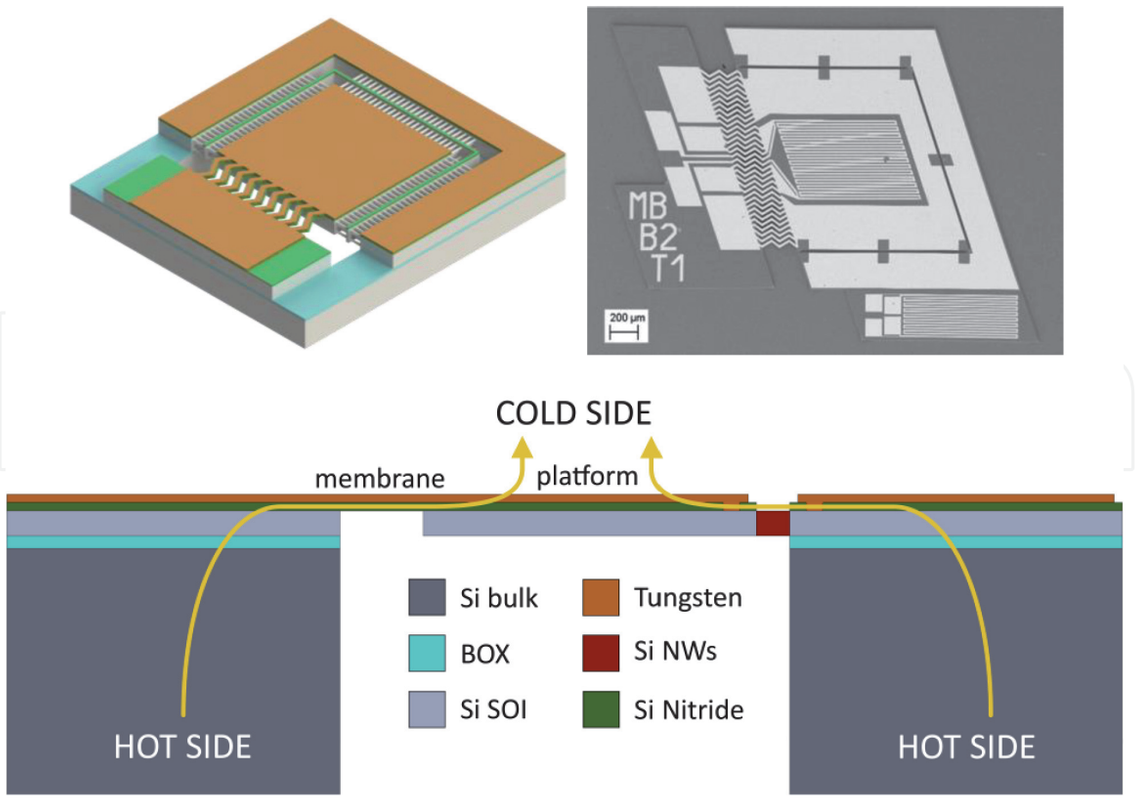

Figure 1.
From left to right and top to bottom: 3D sketch of an integrated planar micro-thermocouple; SEM image of a fabricated device; schematic cross-section of the device identifying the thermally isolated platform and other relevant elements, and the expected heat flow from hot to cold areas in a transversal architecture. The typical area for the platform of the devices discussed is 1 mm².

removed under the platform in the first place. However, nanostructuration of silicon in at least one dimension was shown to significantly lower its thermal conductivity when such spatial constraint is in the order or lower than the mean free paths of heat carriers (phonons) [9, 10].

Moreover, arrays of Si NWs can be conveniently grown as a post-process using a *bottom-up* method, known as CVD-VLS, which is mediated by previously deposited catalytic gold nanoparticles [11]. Following this procedure, this material can spontaneously fill the lateral void between the platform and the surrounding bulk silicon rim. Moreover, the NWs are attached quasi-epitaxially to the giving and receiving silicon walls minimizing any thermal and electrical contact resistance that could appear at those connection points [12]. Such minimization of parasitic resistances is an advantage of micro-*integration* when compared to macro-*assembly*. Further details on how Si NWs are grown and integrated in the proposed architecture can be found in our earlier published work [13–16].

The metal leg cannot be integrated in the same self-standing way. It is deposited as a thin film, so it needs a physical support. These ancillary supports need to be thermally optimized since they bridge the hot and cold areas. The nature of these supports has evolved across the different generations of our devices: from long and thin silicon bridges (400 µm x 100 µm x 15 µm) to wide and very thin Si_3N_4 membranes (100 µm x 1000 µm x 0.3 µm). Since thermal conductivity of Si_3N_4 is two orders of magnitude lower than the one of silicon, there is a net gain in thermal conductance, while enabling a shorter and wider (and less electrically resistive) metal leg.

The thermal impact on platform isolation of the *active* thermoelectric material, Si NWs, can be modulated by the nanowire length. The longer the nanowires are, the

higher their thermal resistance is. This leads to a platform better isolated from the bulk silicon rim and a larger resulting temperature difference (ΔT). Growing longer nanowires requires longer processing times, so a clever way of obtaining arbitrarily long nanowires in a reasonable time is to divide the span to be bridged by them into a number of consecutive trenches (see **Figure 1**). We usually cover lateral voids of several tens of microns by dividing them into 10 or 15 μm wide trenches (as shown in the sketch of **Figure 1**). It must be noted that increasing the length of the NWs has a linear impact on their thermal conduction, but a sublinear impact on the overall thermal conductance of the device. NWs are just one of the several concurring heat leak paths across the platform and rim (metal legs, metal leg supports, platform mechanical supports, air itself), so increasing their length beyond the point where their thermal conductance starts competing with those of others makes no sense. Of course, another way to affect the thermal conduction of the thermoelectric material is choosing materials with lower thermal conductivity. In our case, and without moving beyond silicon compatible materials, SiGe NWs, which can be grown in a similar way, but exhibit better thermal properties, have been successfully integrated producing ΔTs significantly larger than Si NWs, specially under natural convection and the absence of heat exchangers [17].

As said, longer NWs generally imply larger ΔT and, thus, a larger thermovoltage. However, a resulting larger voltage is not necessarily associated to a larger power. Power (P) goes as V^2/R, and since increasing the length of the NWs will also increase the electrical resistance of the device, a trade-off is established. Beyond certain NW length, V may still increase but P will decrease. The value at which this happens will not only depend on the balance of the thermal and electrical properties of the thermoelectric material, but also on the thermal relevance of the thermoelectric material in the thermal design of the overall device. This is of particular significance for this chapter as the way the platform exchanges heat with the ambient is an important element of the thermal resistance of the whole device and determines the corresponding internal ΔT distribution. As commented, the goal of the thermal design of the device is to transpose most of the *external* gradient available to the active *internal* hot and cold areas. For that, the thermal resistance across platform and bulk silicon rim should be larger than the other two thermal resistances in series: the one of the hot part with the heat sink and the one of the cold part with the surrounding air. Being a solid–solid interface in usual application scenarios, keeping the former small poses no great problem; however, reducing the latter is much more challenging. As will be shown, the degree to which that reduction can be achieved would affect the tipping point of the thermal and electrical trade-off and impact also on materials and dimensional choices.

It must be noted that the heat transfer issues discussed in this chapter revolve about the challenge of exchanging heat in planar micromachined structures exhibiting very small exchange surfaces [18–22], while the particular nature of the thermoelectric material employed (e.g. NWs) is of no significance: the same conclusions will apply if silicon membranes, silicon-based thin films, or any other thermoelectric films of interest were considered instead.

2.2 Optimization considerations (load matching)

When considering the optimum design for a thermoelectric microgenerator (μTEG) the generated power is the parameter which needs to be maximized. It is well known that for a given μTEG with its own internal resistance, the power that is transferred to the load is maximized when the internal resistance and the load resistance are equal. This case is usually known as load matching condition [23].

Considering the electrical circuit diagram shown in **Figure 2**, which represents a μTEG, formed by a voltage source (V_{OC}) and its internal electrical resistance (R_{TEG}), connected to a load resistance (R_L), it is straightforward to evaluate the total dissipated power at the load as:

$$P_L = V_L \cdot I_L = I_L^2 \cdot R_L = \left(\frac{V_{oc}}{R_{TEG} + R_L}\right)^2 \cdot R_L \tag{1}$$

Finding the value of R_L which maximizes P_L implies after a few calculations the load matching condition, $R_{TEG} = R_L$. It is important to notice that the only parameter allowed to change in this optimization is the load resistance. Therefore, one can write the maximum power as:

$$P_{L,max} = \frac{V_{oc}^2}{4R_L} = \frac{V_{oc}^2}{4R_{TEG}} \tag{2}$$

As can be seen in **Figure 3**, where the output power of a μTEG is plotted versus load resistance for three different internal resistances, each curve has a maximum for the load matching condition. But now the influence of the internal resistance is highlighted, where the lower its value, the greater the power output. In **Figure 3**, for example, halving the internal resistance can double the power output at the load matching condition. This highlights the importance of reducing the internal resistance when designing a μTEG.

Some publications discussing load matching focus on the need to modify the internal resistance, increasing it, in order to match the load resistance [22]. According to **Figure 3**, this is in fact an error. It is always a better approach to minimize the internal resistance in order to increase the power output even further. Once the internal resistance is the minimum possible, then the load matching condition can be applied to maximize the power output. Actually, many integrated circuits exist which efficiently implement maximum power point tracking (MPPT) algorithms to extract the maximum power from a power source by modifying its load resistance.

This load matching approach can be analogously applied to the temperatures involved in the μTEG and is known as thermal matching. A simplified conductance network describing the μTEG (K_{TEG}) in parallel with K_{LK} accounting for parasitic thermal leakages and in series with K_S representing the conductance to ambient (to both heat source and heat sink) is shown in **Figure 4**.

To explore which is the K_{TEG} value that maximizes P_{max}, as was done in the electrical case, Eq. (2) can be rewritten as:

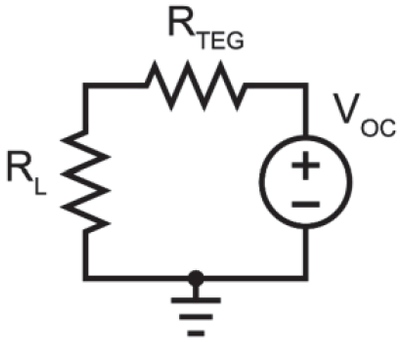

Figure 2.
Equivalent circuit of a μTEG, formed by a voltage source (V_{OC}) and its internal resistance (R_{TEG}), connected in series with a load resistance (R_L).

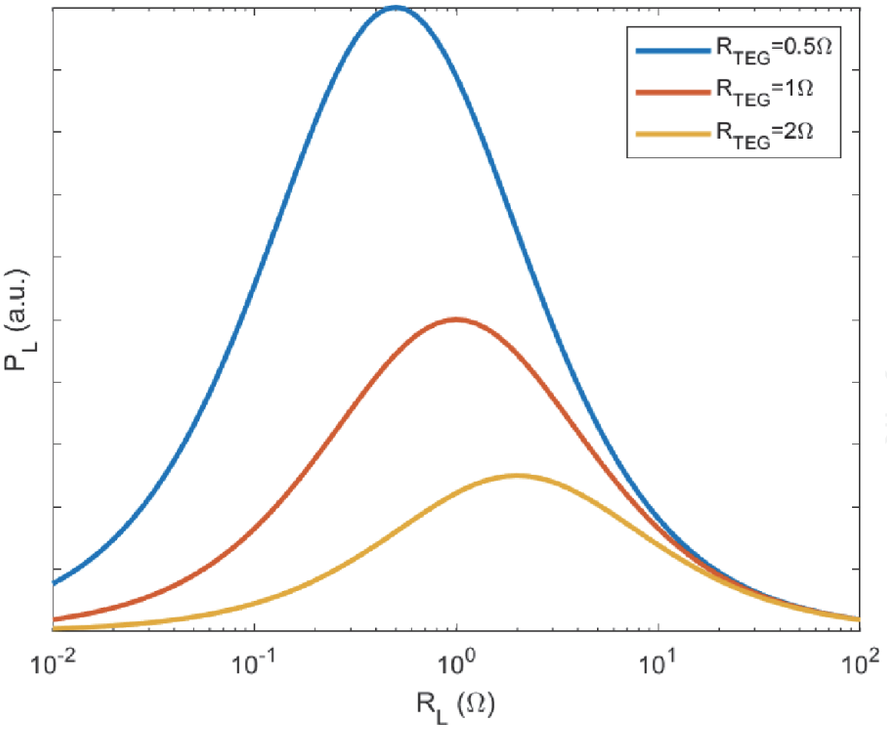

Figure 3.
Power output of a μTEG versus load resistance for different R_{TEG} values.

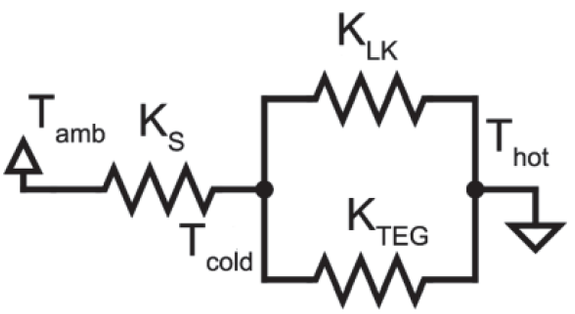

Figure 4.
Simplified thermal conductance network describing the μTEG with parallel and series thermal conductances.

$$P_{L,max} = \frac{V_{oc}^2}{4R_{TEG}} = \frac{(S \cdot \Delta T)^2}{4R_{TEG}} \tag{3}$$

Where S is the Seebeck coefficient and ΔT is the temperature difference across the μTEG, or T_{hot}-T_{cold} from **Figure 4**. Therefore:

$$\Delta T = \Delta T_A \frac{K_S}{(K_{TEG} + K_{LK} + K_S)} \tag{4}$$

Where ΔT_A is the total available temperature difference, T_{amb}-T_{hot}. K_{TEG} is the internal thermal conductance of the μTEG and K_S represents the thermal conductance to the ambient.

When decreasing R_{TEG}, as deemed appropriated in the previous paragraphs, it is important to keep in mind that K_{TEG} is bound to increase, as they are inversely proportional. This is because of the implicit assumption that changing K_{TEG} implies a geometry modification, not a material property change and the geometry change affects both electrical resistance and thermal conductance of the μTEG. Ignoring any leakage contribution (K_{LK} = 0 W/K) in Eq. (4), the power output (solid) and ΔT

(dotted) versus K_{TEG} can be seen in **Figure 5**. Three different K_S cases have been considered to highlight the fact that, the larger K_S, the larger the power output, even for a constant K_{TEG}. It can be seen that when $K_{TEG} = K_S$, the maximum power condition when $K_{LK} = 0$, then the temperature drop across the μTEG is 50% of the available temperature difference.

Similar to the electrical case, many papers discussing thermal matching focus on reaching a temperature drop in the μTEG equal to the temperature drop across K_S [5, 24, 25]. When this K_S represents a heat exchanger, some authors suggest a low K_S heat exchanger to match K_{TEG} and therefore maximize the power output according. While this approach assures operation at the mathematical local maximum for a given K_S, it is a bad practice because it ignores the absolute maximum, which takes place at larger K_S values for a given K_{TEG}.

Looking at **Figure 5**, if $K_{TEG} = 1$ W/K, this reasoning would imply that $K_S = 1$ W/K would be necessary, and 50% of the total available temperature difference would drop across the μTEG. However, with a better heat exchanger, $K_S = 10$ W/K or even $K_S = 100$ W/K, then ΔT will asymptotically approach ΔT_A, and the power output will asymptotically reach:

$$P_{L,max} = \frac{(S \cdot \Delta T_A)^2}{4R_{TEG}} \tag{5}$$

In conclusion, both load matching and thermal matching are conditions that are mathematically true, but from a practical point of view, care must be taken when designing a μTEG to maximize its power output. First of all, its electrical internal resistance (R_{TEG}) must be minimized, and after that, power output can be maximized by connecting a load which matches that of the μTEG, or simply an IC implementing an MPPT algorithm. On the thermal side, as R_{TEG} is minimized, the thermal conductance (K_{TEG}) is consequently maximized. Then, as the μTEG is already optimized, and it is not possible to further increase K_{TEG}, the only option is to act on the external components, which in this case is the heat exchanger, and to choose one with an as large as possible K_S, so that almost all of the available ΔT will be internally transferred to the μTEG.

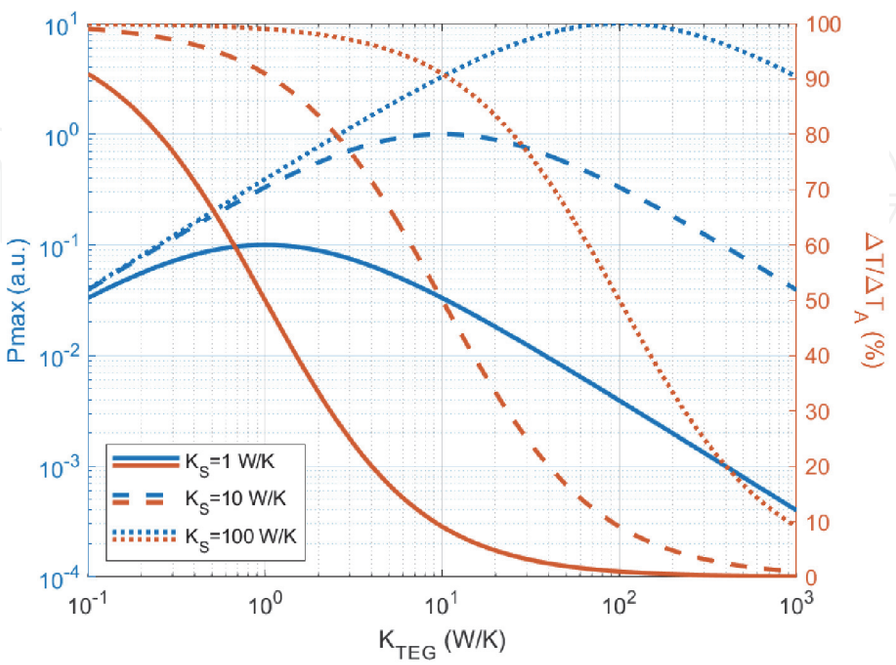

Figure 5.
P_{max} (left, blue curves) and $\Delta T/\Delta T_A$ (right, red curves) versus K_{TEG} for different K_S values. For $K_{TEG} = 1$, thermal matching conditions would call for $K_S = 1$, but larger P_{max} values are possible for larger values of K_S.

3. Decreasing the platform thermal resistance

As mentioned before, the performance of μTEG devices depends on the temperature difference 'seen' by the thermocouples. Therefore, minimizing thermal resistances in series with those elements would improve the performance of the device. In this section, such improvement is demonstrated by decreasing the thermal resistance between the suspended platform and the ambient, usually the cold part, by favoring the heat flow locally. Two methods have been used to increase such heat exchange: (i) by forcing heat convection onto the platform and (ii) by contacting it with a cold mass. The promising results obtained from the experiments described in the next two subsections call for optimizing this effect through the development of a procedure to integrate a heat exchanging structure, which will be shown in section 4.

3.1 Forced convection experiments

As the working scenario for the μTEG devices is dominated by a temperature difference between the hot and the cold parts, heat convection could play also an important role on how these temperatures are established. Convection is a mechanism of heat flux originated from the movement of the surrounding fluid, which will be typically air for the usual applications of the presented devices. Depending on how this movement is induced, convection can be classified as natural or forced.

Natural convection is based on the warming up of the air that is close to a heat source that, due to the lowering of its density, tends to move upwards, giving its place to colder air and so promoting the heat exchange. In forced convection, air is forced to move and then renew by an external force.

In order to demonstrate the improvement in the performance of the device, three different sets of experimental measurements have been performed on a device at three different convection conditions. The first one corresponds to natural convection, which occurs when the device is operated by letting it rest on top of a hot surface exposed to ambient at room conditions. The second and third sets of measurements correspond to forced convection regimes. In the second case, this is accomplished by the use of a standard CPU fan (see **Figure 6**) placed over the device, while in the third, an air jet, obtained through a syringe connected to the compressed air line in the laboratory, is directed towards the device. More details are available at [26].

Such experimental measurements have been performed on two different devices, featuring 30 and 60 μm long silicon NWs (by filling 3 and 6 trenches as described in section 2.1). Consequently, each one of the devices has different electrical and thermal resistances.

The obtained experimental results are shown in **Figure 7**. The devices have been measured at different temperatures of the hot plate (from 50 to 200 °C in 25 °C steps).

The measurement results show a very clear improvement in the performance as a result of forced convection. The maximum output power obtained when the device is mounted under the fan is multiplied by 3 when compared with the natural convection regime, while when under the more directed and higher flow air jet, the performance increases nearly three orders of magnitude: from a few nW to almost 0.7 μW. Moreover, the more performant air convection is, the less relevant become the thermal properties of the thermoelectric material. In natural and air forced convection cases, the larger output power corresponds to the longest nanowires, whereas in the air jet forced convection the opposite is true. This happens because the longer nanowires also have a larger electrical resistance, and its larger thermal

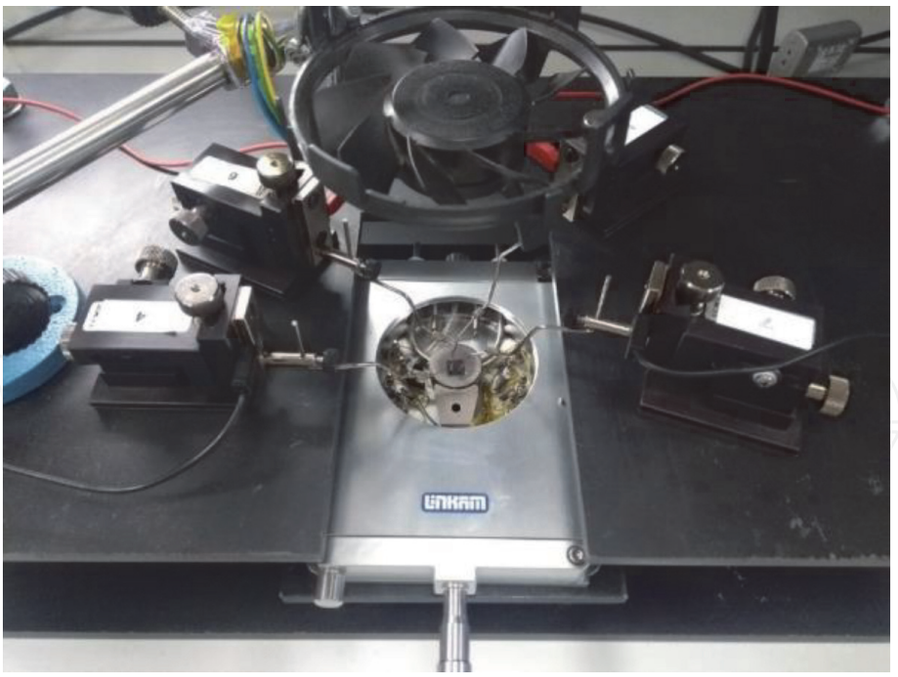

Figure 6.
Experimental setup used for the thermoelectrical characterization of μTEG devices under a forced convection regime induced by a CPU fan located on the top. The device is mounted on the thermal chuck of a Linkam station.

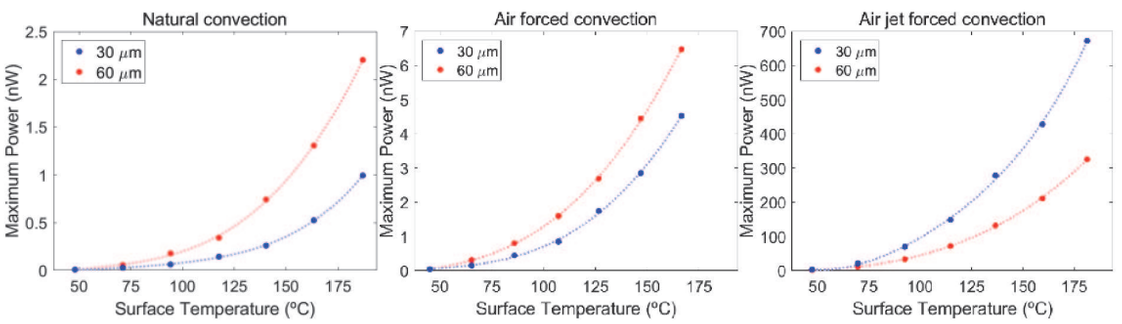

Figure 7.
Maximum power versus chip surface temperature for three different heat convection regimes and on two different devices (adapted from [26]).

resistance is not significant in this case where the platform to ambient thermal resistance is enough to assure a large ΔT.

3.2 Cold finger approach

In the previous subsection, it has been experimentally demonstrated how important a good thermal connection with the surrounding ambient is in order to improve the overall performance of μTEG devices. Nevertheless, forced convection scenarios are not always available and artificially forcing them needs additional energy consuming devices. Therefore, in order to explore a passive strategy to diminish the thermal resistance to the surrounding ambient, the effect of contacting the microplatform with a metallic probe has been assessed. With this experiment, the feasibility of the addition of a heat exchanging structure as a general strategy for the reduction of the thermal resistance to the ambient will be demonstrated.

The experimental setup consists of a metallic probe dipped in thermally conducting paste, which is carefully positioned on the micro-platform by the use of a micro-manipulator.

The performance improvement obtained by means of this approach can be observed in **Figure 8**, which shows a plot of the Seebeck voltage output of the device placed on a hot plate at 150 °C when the cold finger is being attached. It can be observed that the voltage increases rapidly after contact, and it rises even more when the applied force to the cold finger is increased slightly, so demonstrating the reduction of the thermal resistance when the physical contact is improved.

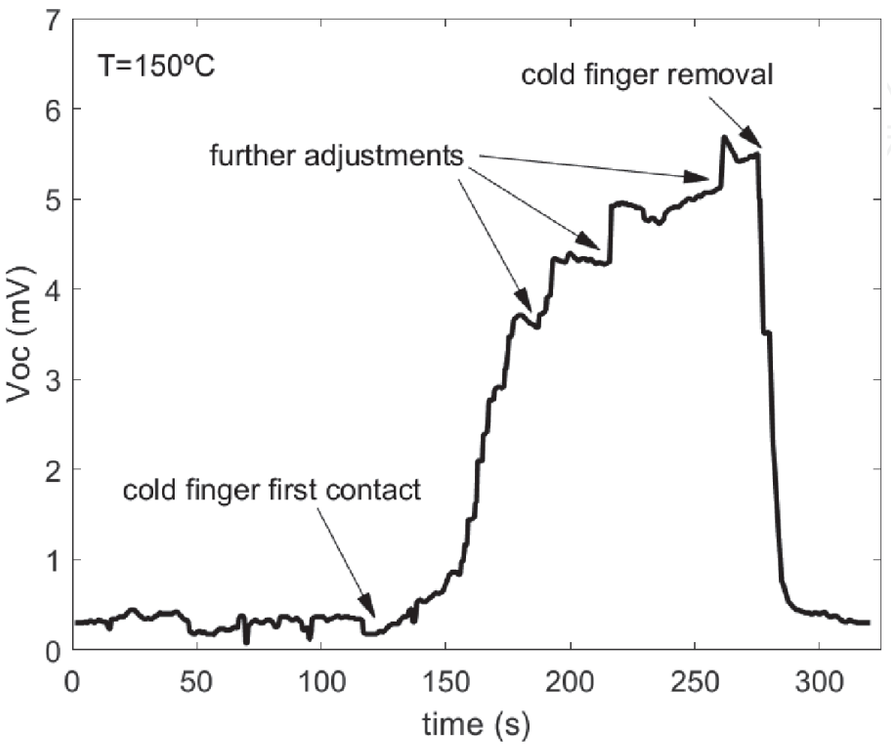

Figure 8.
Voltage evolution while the cold finger is being attached and detached.

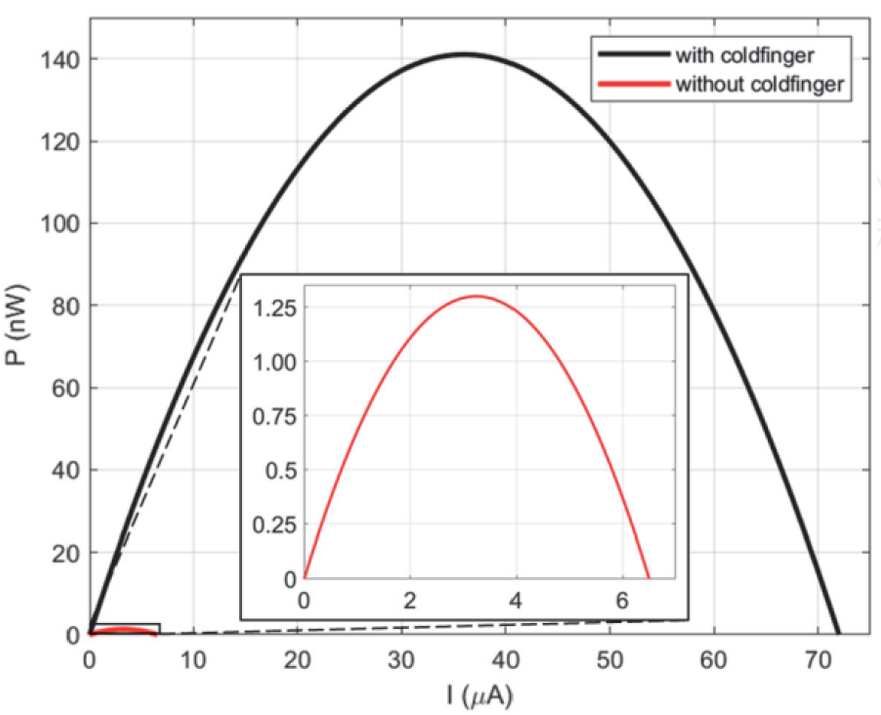

Figure 9.
Power curves for a device, with and without the cold finger, on a hot plate at 250 °C.

In **Figure 9** the power curves obtained from the same device at a hot plate temperature of 250 °C with and without the cold finger are shown. It can be seen an important improvement in the performance of two orders of magnitude, from 1.3 to 142 nW, so proving the effectiveness of the cold finger approach as a proof of concept validating the further development of more effective heat exchanging structures.

4. Heat exchanger

The previous section highlights the importance of physically contacting the platform in order to improve heat extraction, and thus cooling it more efficiently. According to section 2.2 and the results shown in section 3.2, the need for a heat exchanger has been proven. In this section, we study the implementation of such component on the μTEG. This poses several problems from the technological point of view, especially considering the starting device architecture used to expose the thermoelectric material to a thermal gradient. The thermally isolated platform is a fragile structure and physically contacting it without caution might break it. A proper methodology with auxiliary components needs to be developed components to provide such contact safely.

The approach implies to have a thermally conductive piece contacting the platform and interfacing this part of the device with a heat exchanger of appropriate size. For this reason, such piece will be dubbed as 'adapter'. The contact needs to be compliant to absorb any excess vertical displacement with deformation. The compliant part of this contact will be a certain amount of silver paste. A rigid spacer (PMMA), sitting both on the silicon bulk rim and the platform, will also be necessary to limit the maximum excursion of the adapter over the platform so that pressure between the heat exchanger on top and the platform below can be applied in a safe way. Finally, the heat exchanger itself, a commercial one of similar footprint is assembled onto our chip. In this case, our chip is 7x7 mm^2 and the smallest commercial heat exchanger found is 8x8 mm^2. A PCB with a through-hole, to insert a copper plate improving the thermal conductance from the hot surface to the bulk silicon rim, and a slightly larger partial etch to fit the chip and facilitate the wire bonding to auxiliary copper traces, are included in the assembly as shown in **Figure 10**.

4.1 Modeling results

The feasibility of the approach has been first tested building a physical model and solving finite element simulations (COMSOL) to evaluate the expected

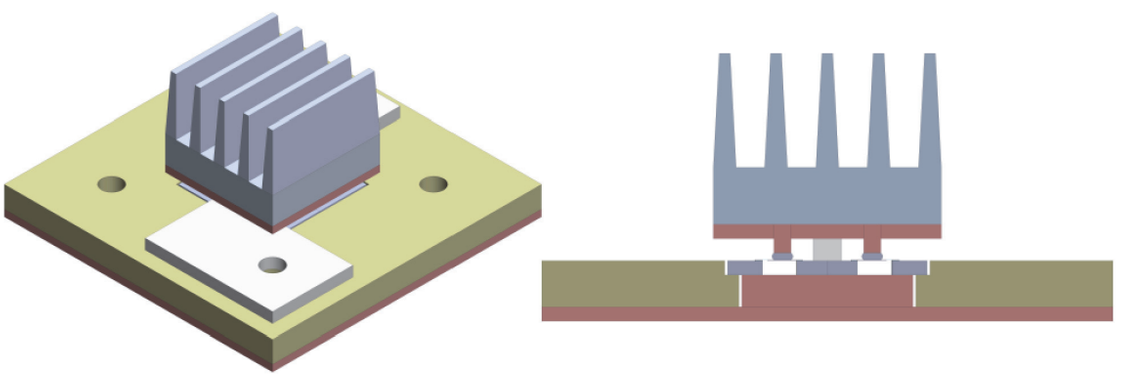

Figure 10.
Isometric, cross section and detailed view of the proposed approach to safely contact the thin silicon platforms.

improvement on performance. The thermal and electrical properties of the materials used in the model are listed in **Table 1**.

The model boundary conditions include a constant hot temperature at the bottom (T_{hot} = 100 °C) and natural convection on the vertical and horizontal walls of the heat exchanger through a heat exchange coefficient directly calculated in COMSOL for an air ambient temperature of 27 °C. When such element is not present, the heat exchange coefficient is applied directly on the platforms surface. **Figure 11** shows the temperature distribution for the whole model under such conditions. As it can be seen, even with a heat exchanger, the lowest temperature reached in the cold part is slightly below 70 °C although the ambient temperature is 27 °C. This is because the thermal resistance from the heat exchanger to the ambient is approximately one third of the total thermal resistance while the thermal resistance from the bottom of the PCB (actually most of this is from the silicon chip) to the heat exchanger is approximately two thirds of it.

	κ ($W \cdot m^{-1} \cdot K^{-1}$)	σ ($S \cdot m^{-1}$)	S ($V \cdot K^{-1}$)
Silicon	150	$12 \cdot 10^3$	
Silicon oxide	1.4	—	
Silicon nitride	30	—	
Silicon NWs	25 (1)	$12 \cdot 10^3$ (1)	$250 \cdot 10^{-6}$
Tungsten	174	$7.76 \cdot 10^6$ (2)	
Thermal paste	5	—	
Copper	401	—	
FR4 (PCB)	0.3	—	
Spacer (PMMA)	0.2	—	

(1) Silicon NWs are modeled as a block, not individual nanowires, and the block material properties assume an occupation of only 5% of the total area with nanowires, while the remaining 95% has air material properties.
(2) Tungsten electrical conductivity is different from the bulk literature values. The sheet resistance on a real device has been measured to obtain this value.

Table 1.
Thermal and electrical properties of the materials used in the model.

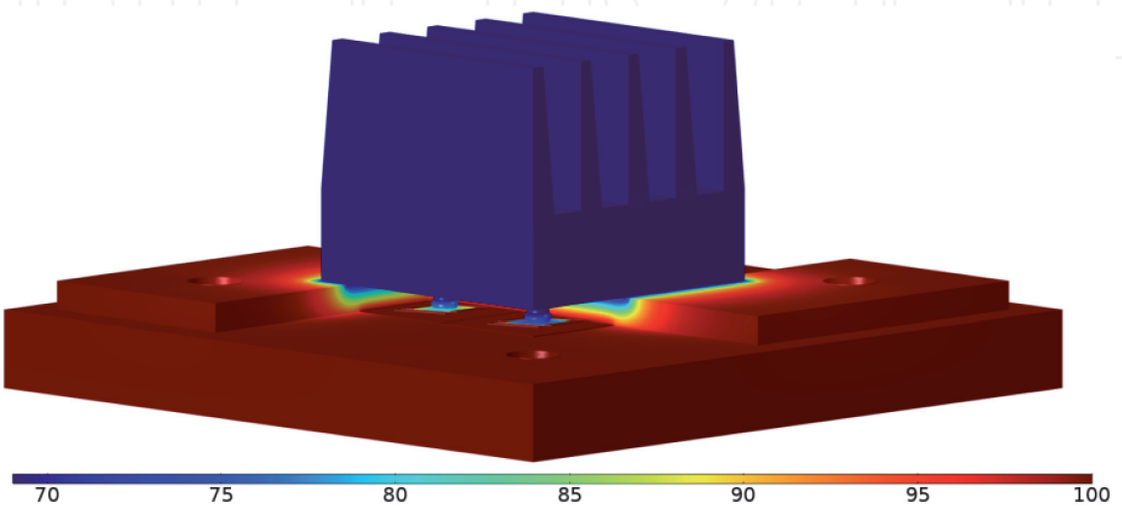

Figure 11.
Temperature distribution for the whole model with T_{hot} = 100 °C.

The internal temperature distribution for chips with four platforms with NW lengths of 10, 20, 30 and 40 μm (T1 to T4) has been analyzed for the cases with or without heat exchanger. The difference is significant as shown in **Figure 12**. The temperature difference across the NWs in the best case reaches about 25 °C of the total 73 °C externally available, when the heat exchanger is in place (right). This means the thermal resistance of the nanowires is approximately twice the thermal resistance from the platform to the ambient through the heat exchanger.

On the other hand, for the case without heat exchanger (left), the temperature differences across the nanowires do not reach beyond 2 °C. In this case, the thermal resistance to the ambient is much larger than the nanowires thermal resistance, and a very small temperature drop develops across the active thermoelectric material.

If the temperature solution from the finite element model is coupled to an electrical model through the Seebeck coefficient of the nanowires, the I-V curves and power output for each platform considering both scenarios can be obtained.

These results are shown in **Figure 13**, where the power output has been plotted as power density considering a device area of 2 mm^2, large enough to contain the whole platform (approximately 1 mm^2) and space for additional contacts.

Clearly, a much larger power is obtained when the heat exchanger is in place due to the much higher ΔT perceived by the NWs. In addition, the behavior of the four platforms evolve differently. Without the heat exchanger, voltage and power scale with the length of nanowires since their thermal resistance is the dominant part of the total device thermal resistance and such length is directly determining the

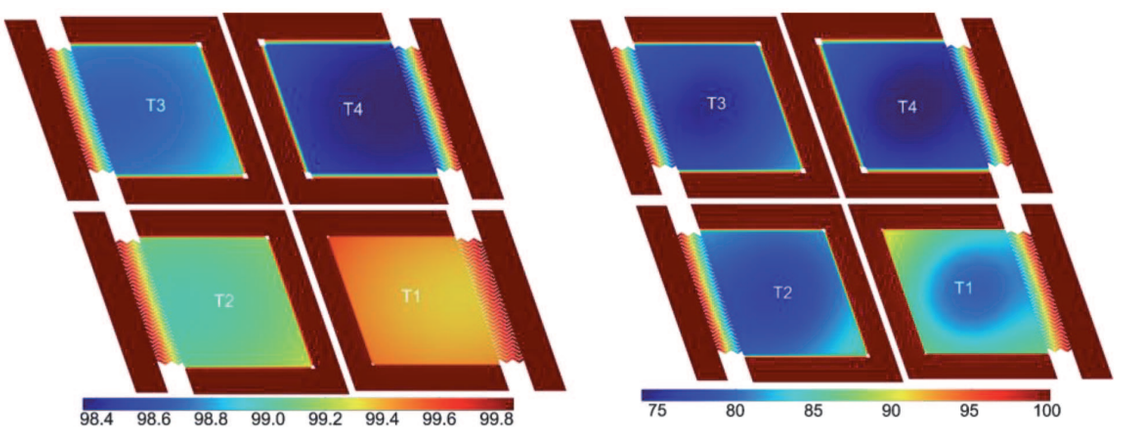

Figure 12.
Temperature distribution for each platform (from T1 to T4) without heat exchanger (left) and with heat exchanger (right).

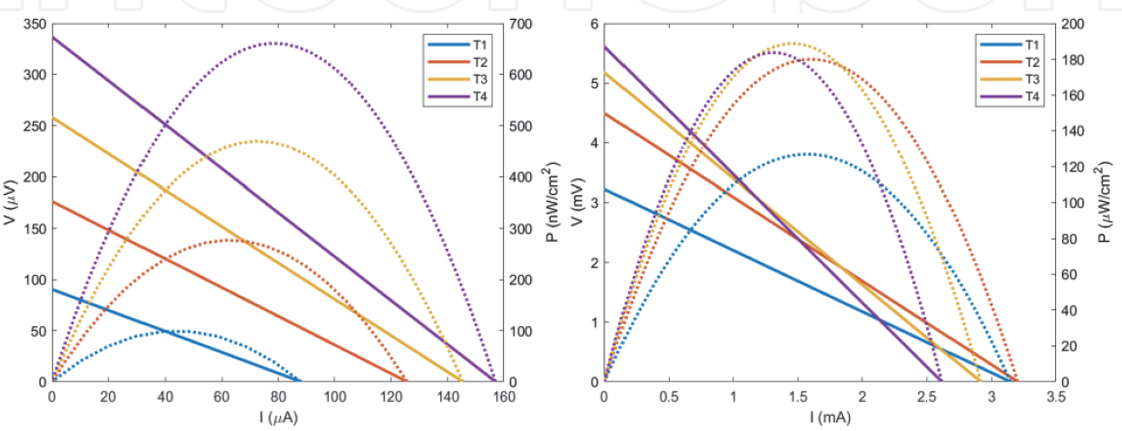

Figure 13.
I-V curves (solid lines), and power output (dotted lines), versus current for T1-T4 devices, without (left) and with heat exchanger (right).

attained ΔT. However, when the presence of the heat exchanger secures most of ΔT, the positive effect of the lower thermal conductance of longer nanowires, which is still there, rapidly saturates and even reverse (see T4 vs. T3) because the detrimental impact of the increasing electrical resistance becomes dominant.

4.2 Manual assembly and impact on measurements

The significant increase in the generated power when applying a forced convection or a cold finger and the results from the simulations including a heat exchanger directed our efforts to the construction of the previously described heat exchanger assembly on our μTEGs (see **Figure 10**).

The preparation sequence of the required components is given in **Figure 14a**. A heat exchanger adapter is made from four Cu wires (one per on-chip a device), with diameter similar to the size of the suspended platform (which they will contact after the assembly) inserted in a square brass piece and machined to the appropriate length. The tips of the wires are dipped with thermal paste (**Figure 14b**) to fill the gap between the Cu wires and the suspended platforms to guarantee good thermal contact (**Figure 14c**). A PMMA spacer with a thickness appropriately matching the length of the protruding Cu wires is then assembled between the heat exchanger adapter and the μTEG, and finally, the aluminum heat exchanger is placed on top of adapter using a thermal paste (**Figure 14d**). Further details can be found in [27] from which **Figures 14–17** have been adapted.

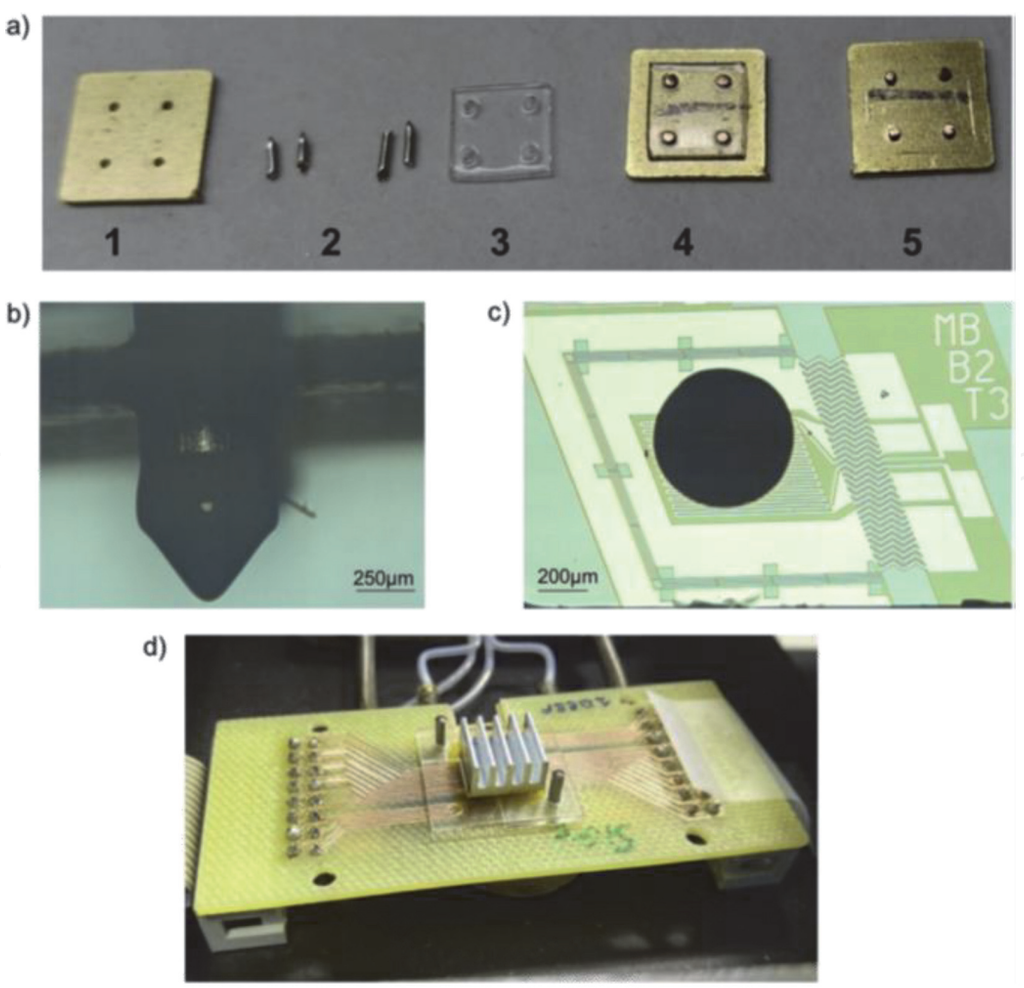

Figure 14.
(a) Steps of the construction of the heat sink adapter. Optical microscope images of (b) the Cu wire dipped in thermal paste and (c) the footprint left on the platform of the test device. (d) An image of the final assembly.

Through the described integration scheme, a first evaluation of the performance improvement brought by a heat exchanger to the μTEG is enabled. In this study harvesting measurements with and without heat exchanger were performed by placing the assembled devices on a Linkam THMS 350 V heating stage at various temperatures in a natural convection environment. Three different cases were measured: without heat sink, with heat sink and with heat sink + pressing, where for the latter a force is applied on top of the assembly to reduce the thermal resistance of the thermal paste. Chips with different thermoelectric materials were measured: Si NWs, Si-Ge NWs and Si microbeams. At the current stage of technology maturity, a rather low number of devices has been measured, but the results shown in the next subsections correspond to significant devices of each category. In terms of measurement uncertainties, the most important source are thermal fluctuations that due to the thermoelectric nature of the device introduce variations in the measured V and I, which have been estimated to be below 10 μV and 1 μA, respectively.

4.2.1 Measurements with Si NWs

The Seebeck voltage vs. hotplate temperature curves for the Si NWs-based μTEGs with different number of trenches are shown in **Figure 15**. As anticipated, all the devices presented output voltages that scaled with the number of trenches (i.e. length of NWs). However, the reduction of the thermal resistance between the cold side (suspended platform) and the ambient when a heat exchanger is integrated resulted in a large increase of ΔT across the NWs and hence higher overall voltages.

In terms of power, the maximum power densities obtained at hot plate temperatures of 100 °C without the heat exchanger were in the range of 0.05–0.1 μWcm^{-2}.

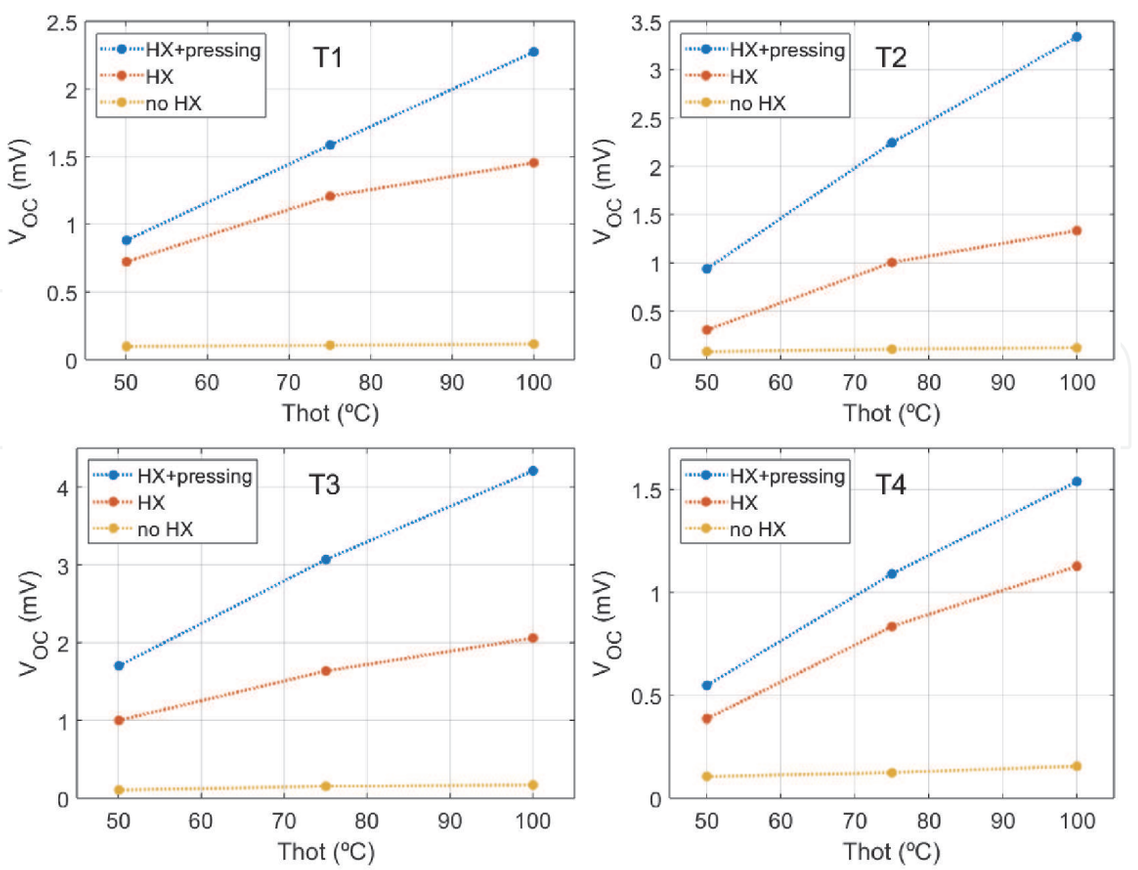

Figure 15.
Seebeck voltage vs. hot plate temperature for Si NWs-based μTEGs with different number of trenches (T1-T4) with and without heat exchanger.

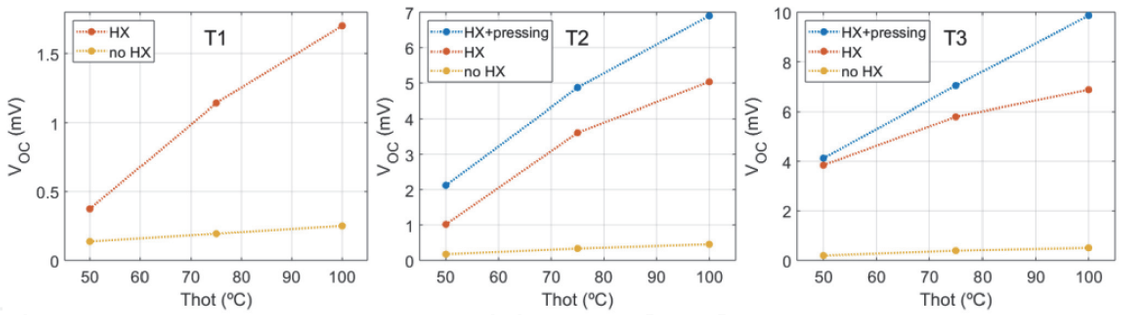

Figure 16.
Seebeck voltage vs. hot plate temperature for SiGe NWs-based μTEGs with different number of trenches (T1-T3) with and without heat exchanger.

As expected, a tremendous increase in power density was observed after the integration of the heat exchanger + pressing, and values in the range 7–42 μWcm^{-2} were observed. No clear trends were observed with the number of trenches.

4.2.2 Measurements with SiGe NWs

For devices with SiGe NWs, considerable higher Seebeck voltages were observed when compared to Si NWs (**Figure 16**), due to the higher thermal resistance resulting from the lower intrinsic thermal conductivity of the former. With and without heat exchanger, the devices performed better with increasing number of trenches. Also, power densities rose considerably with the integration of the heat exchanger. As already observed for the Si NWs, the voltage and generated power improved further when a slight pressure was applied to the heat exchanger, It is worth noticing that the maximum power thus obtained does not differ much for Si and SiGe NWs: 41.6 μWcm^{-2} vs. 45.2 μWcm^{-2}, respectively, considering a T3 device on a hotplate at 100 °C. This points to the dilution of the effect of better starting thermal properties when the heat exchanger is present.

4.2.3 Measurements with Si microbeams

Si microbeams devices were fabricated to compare the performance of bulk Si with Si NWs. After the integration of the heat exchanger + pressing, the results presented in **Figure 17** show a remarkable three orders of magnitude increase in the generated power from ~650 pW to ~690 nW for a T1 device, i.e. from 32.5 nWcm^{-2} to 34.5 μWcm^{-2}. This result evidences again that once the heat exchanger

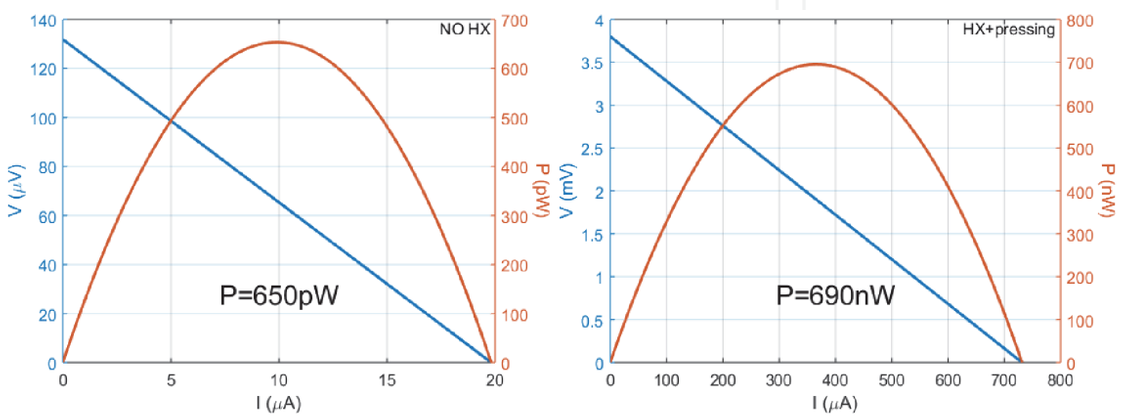

Figure 17.
I-V and power curves for the Si microbeams based μTEGs without heat exchanger (left) and with heat exchanger and pressing (right) for a hot plate temperature of 100 °C.

is in place, the thermal properties of the thermoelectric material become second order. Hence, by optimizing their electrical properties and ensuring a good ΔT with the aid of a heat exchanger, it is possible to obtain high power densities even with high thermal conductivity thermoelectric materials such as Si microbeams.

4.3 Semiautomatic assembly with integration density

In order to translate the promising power densities of a single structure into useful absolute power levels, a certain number of thermocouples needs to be integrated and connected. The μTEGs design was modified to attain a higher integration density by reducing the number of active sides. The new thermocouple has a rectangular shape with one side featuring the membrane providing mechanical support and metallic connection, and the opposite side composed of the trenches to be filled with NWs. In **Figure 18**, a 3D schematic of the new unitary thermocouple is shown. The same cross-section profile of **Figure 1** still applies. With this new design, many elements can be integrated in the same chip: up to fifty thermocouples (each with an approximate size of 5 x 0.6 mm^2) fit in series or series–parallel configuration in a 49 mm^2 chip, as shown in **Figure 19**. Both configurations would lead to the same harvested power, but the series one will scale up voltage while the parallel one will scale up current.

This compact design requires new components and a novel and more efficient approach for the integration of the heat exchanger in order to boost their thermal performance. A micromachined Si adapter (substituting the Cu wires, brass plate and PMMA spacer of the previous section) is necessary for the distribution of the force exerted on the platform by the heat exchanger, and different designs featuring the corresponding serial or parallel arrangements were fabricated. **Figure 20** (left) depicts the Si adapter designs where the central columns contact the platform of each thermocouple in the chip and the ones at the corners act as force distributers. Similar to the previous section, a commercial Al mini heat exchanger will be placed on top of the Si adapter to help the circulation of heat from the Si rim of the μTEG (warm side) through the thermoelectric material to the platform (cold side) to achieve the desired larger ΔT. The heat flux representation through the assembly is shown in **Figure 20** (right).

To achieve a good thermal contact, which is key for a maximum generated power, a thermal interface material (TIM) needs to be placed between the thermocouple and the adapter. To this aim, an inkjet printer (Dimatix) was chosen to deposit a controlled amount of TIM only on the columns of the adapter.

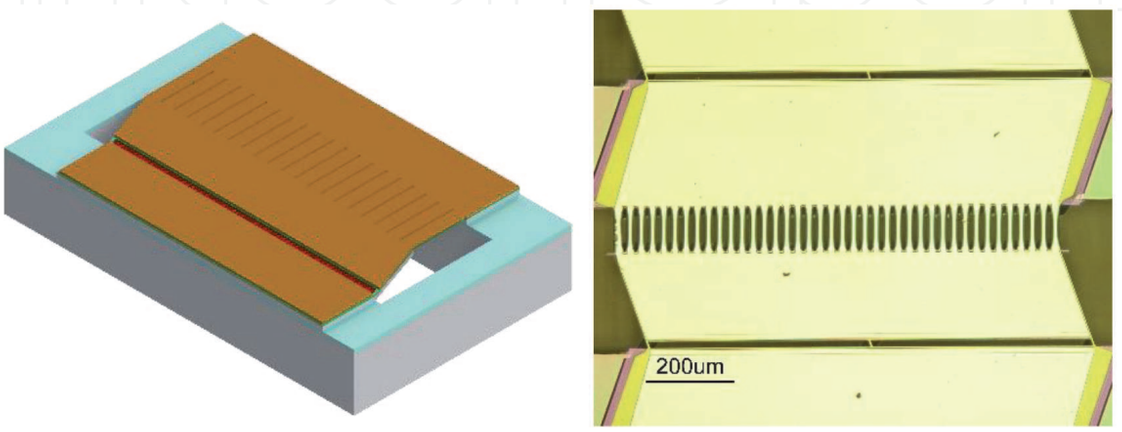

Figure 18.
3D schematic of the new thermocouple design (left) and an optical microscope image of the fabricated micromachined platform.

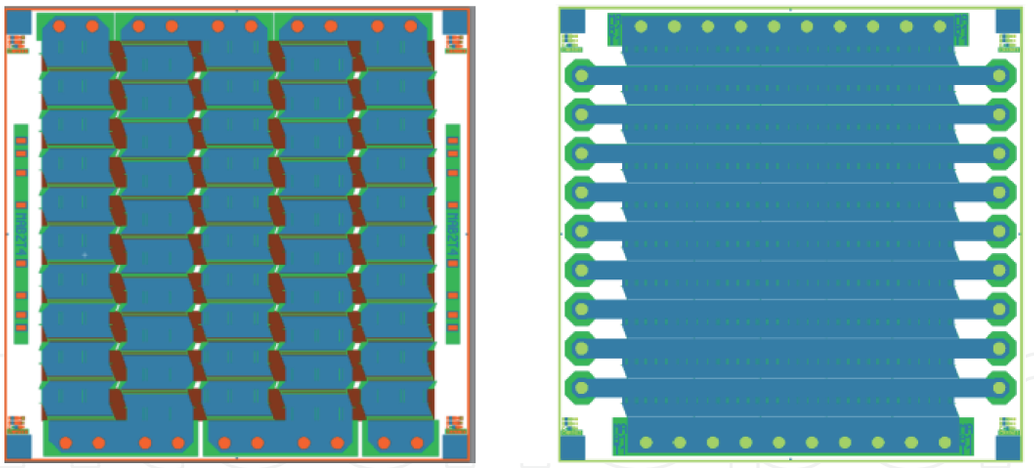

Figure 19.
Layout of the new compact design featuring 50 thermocouples in serial connection (left) and serial connection of 10 arrangements of 5 thermocouples in parallel configuration (right).

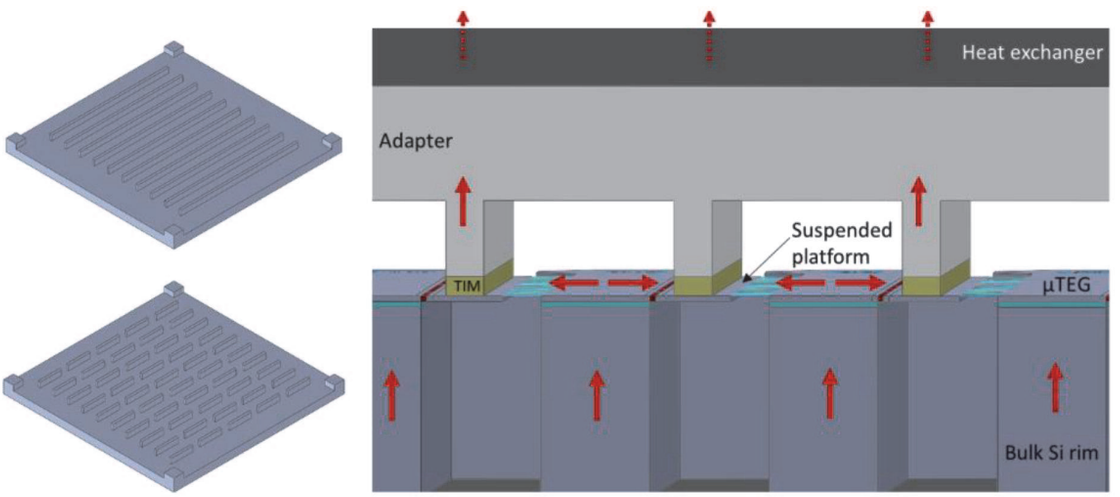

Figure 20.
Schematic of the different designs of the micromachined Si adapter (left). Heat flux through a parallel type μTEG, the adapter and the heat exchanger (right).

After dispensing the TIM, the adapter is placed face-down onto the thermocouple chip already wirebonded on a PCB. This is done with the help of a pick & place machine (Finetech) that enables proper chip alignment and attachment with a controlled gentle force (0.1 N). A holder with a removable lid for the adequate handling of the Si adapter during the process has been designed and 3D-printed. It allows accessing the corresponding side of the adapter, first to the inkjet printer, and then to the pick & place machine. The whole assembly process is depicted in **Figure 21**.

This is a still ongoing process. Two different inks are being tested to act as TIM between the adapter and the suspended platforms: a conductive silver nanoparticle ink (Agfa Orgacon SI-J20X) and a SU8 based polymeric ink (Micro Chem Prielex). The tests involve the assessment of the adequacy of the viscosity and adhesion of the TIM and the evaluation of the endurance of the μTEGs platforms during the assembly. Other TIM materials already used for the mainstream attachment of heat exchangers onto microprocessors can be also evaluated, as well as other ways of locally dispensing them, such as stamping. In any case, the goal is to obtain an integration route for the heat exchanger, without which no workable ΔT would be possible in such miniaturized devices, that is prone to the automatic handling of the

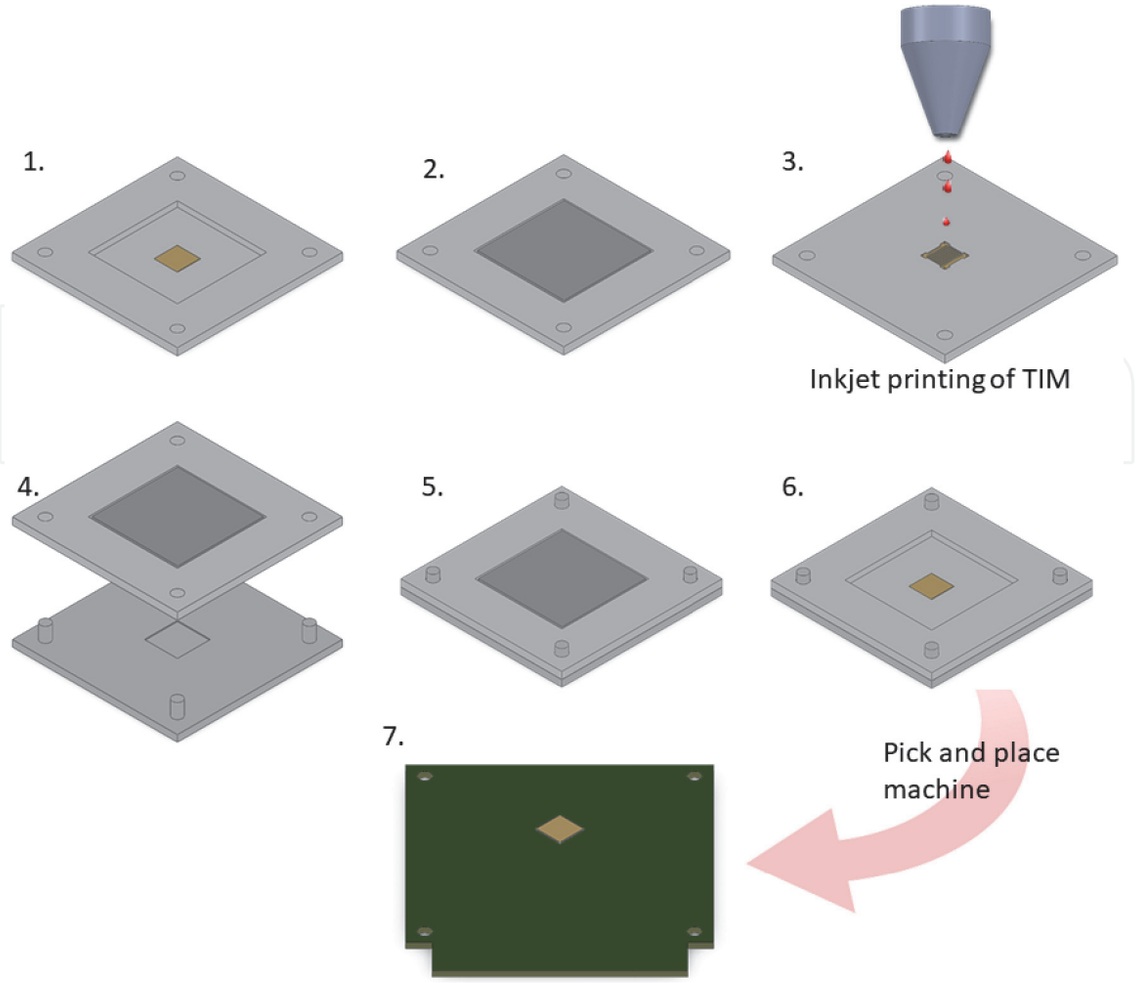

Figure 21.
New assembly route of the heat exchanger Si adapter onto the encapsulated μTEGs chip.

involved chips and it is compatible with their dimensional and mechanical endurance constraints.

5. Conclusions

With this chapter, the authors have tried to show the challenges to sort out when fabricating microgenerators (μTEGs) with planar silicon technologies. Such technologies offer a cost effective way of mass-production of miniaturized devices. However, the very nature of such technologies, the high thermal conductivity of bulk silicon and the typical thickness of the layers involved advises using silicon micromachining to enable areas of lateral thermal contrast. Such transversal architectures helps to translate naturally occurring vertical thermal gradients into internal lateral ones. In this way, a temperature difference will develop across a horizontally and self-standing laid thermoelectric material whose length is a design parameter. A material properties trade-off ensues: the longer the material, the higher its thermal resistance, increasing the attainable ΔT and the obtained Seebeck voltage, but the larger will be its electrical resistance, reducing the power obtainable from that voltage. In addition, it has been shown that the overall attainable ΔT is heavily influenced by the very poor heat exchange capabilities with the environment of small bare surfaces. Simulations and experiments show that the presence of a heat exchanger largely increase the effective ΔT, but brings into play interesting heterogeneous integration challenges still to be fully solved in terms of an effective

but gentle attachment of an intermediate adapter that needs to be designed ad hoc for proper heat flow handling. The presence of the heat exchanger also affects the tilting point of the previously mentioned thermal/electrical trade-off, and thus on the final choice of materials. In the examples given, silicon-based materials have been used (silicon microbeams, silicon and silicon germanium nanowires), but similar structures could be devised for instance for any thermoelectric material in thin film form.

Acknowledgements

This manuscript contains work supported by projects FP7-NMP-2013-SMALL-7 (Contract n. 604169) SiNERGY, TEC2016-78284-C3-1-R (AEI/FEDER, EU) MINAUTO and TEC2016-78284-C3-2-R (AEI/FEDER, EU) SIGGNAL. This research has made use of the infrastructure of the Spanish ICTS Network MICRONANOFABS (CNM site) partially supported by MINECO. I. Donmez-Noyan thanks the 'Programa de Doctorat en Ciència de Materials de la UAB' for the support in her formative activities.

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