Chapter

GaAs Compounds Heteroepitaxy on Silicon for Opto and Nano Electronic Applications

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Abstract

III-V semiconductors present interesting properties and are already used in electronics, lightening and photonic devices. Integration of III-V devices onto a Si CMOS platform is already in production using III-V devices transfer. A promising way consists in using hetero-epitaxy processes to grow the III-V materials directly on Si and at the right place. To reach this objective, some challenges still needed to be overcome. In this contribution, we will show how to overcome the different challenges associated to the heteroepitaxy and integration of III-As onto a silicon platform. We present solutions to get rid of antiphase domains for GaAs grown on exact Si(100). To reduce the threading dislocations density, efficient ways based on either insertion of InGaAs/GaAs multilayers defect filter layers or selective epitaxy in cavities are implemented. All these solutions allows fabricating electrically pumped laser structures based on InAs quantum dots active region, required for photonic and sensing applications.

Keywords: GaAs, heteroepitaxy, photonics, Si, integration

1. Part 1: GaAs growth on Si(001)

The growth of polar zinc-blende GaAs on a non-polar Si(001) substrate can lead to planar defects named antiphase boundary (APB). The APB planes are made of III-III or/and V-V bonds that can propagate in the layer through the {110}, {111} or higher index planes (**Figure 1**) [2, 3].

The elastic strain field due to APB changes atomic distances and hence electronic states, acts as a carrier diffusion and/or non-radiative recombination centers. APBs nucleate at the edges of the single-layer steps present at nominal (001) silicon surfaces. Until now, the APBs formation was mainly inhibited by using (i) off-axis Si(001) substrates tilted by 4–6° towards [110] direction [4, 5] or (ii) Si(211) substrates [6] where Si double-layer steps could be formed easily. However, these wafers are not compatible with industrial Si CMOS standards which uses nominal Si (001) wafers, i.e. with a miscut angle equal or lower than 0.5°. The best option to prevent the APBs nucleation is to promote double layer step formation on nominal Si(001) substrate as it is the case for off-axis wafers.

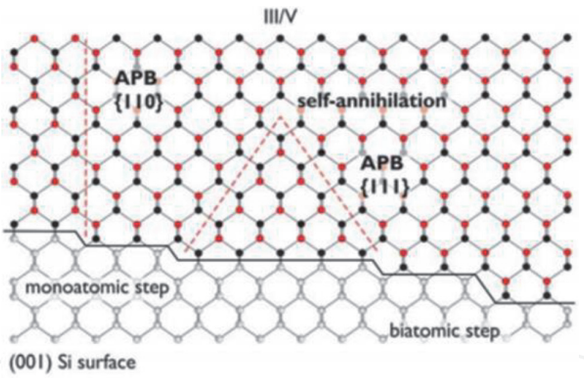

Figure 1.
Ball-and-stick model of III-V-on-Si with {110} and {111}-APBs. The single-layer step edges initiate the formation of the APBs while the surface with double-layer steps allows a single-domain III-V cristal. From reference [1].

1.1 Silicon surface preparation under H_2 ambient

Considering the thermodynamical models, the double-layer steps formation on nominal Si(001) is predicted as highly unfavorable in ultra-high Vacuum (UHV) or in inert gas ambient. The stress relaxation induced by dimerization of the (2 × 1)-Si (001) reconstruction promotes single step formation until a miscut angle lying in a range between 1 and 3° [7–10]. Thus, the (001) surface of nominal wafers is made of alternating (2 × 1) and (1 × 2)-reconstructed terraces (named A-type and B-type terraces respectively) separated by S_A and S_B single steps according to the Chadi's nomenclature (**Figure 2**) [8]. For A-type terraces the Si-dimer rows are parallel to the step edges while they are perpendicular for B-type terraces.

However, computational modeling highlights a possible mechanism to get a nearly single-domain Si(001) surface by selective etching of S_B steps (i.e. by removing the B-type terraces) **under very specific H_2 annealing process conditions** [11]. The energy needed for this process to occur has been calculated by using DFT and the most favorable mechanism has been highlighted. For calculation simplification, a Si(001) 2 × 2 reconstructed surface has been considered, but the conclusions will be transferable to the real case ie. Si(001) 2 × 1 reconstruction.

The removal of two neighboring silicon atoms from the considered Si(001) surface (**Figure 2**) creates the so-called single-dimer vacancy (SDV) [12]. Line defects on the surface can appear by aligning SDV together, either in lines, creating dimer-vacancy lines (DVL) or in rows creating dimer-vacancy rows (DVR) [13] as shown respectively in green and pink areas of **Figure 3a**.

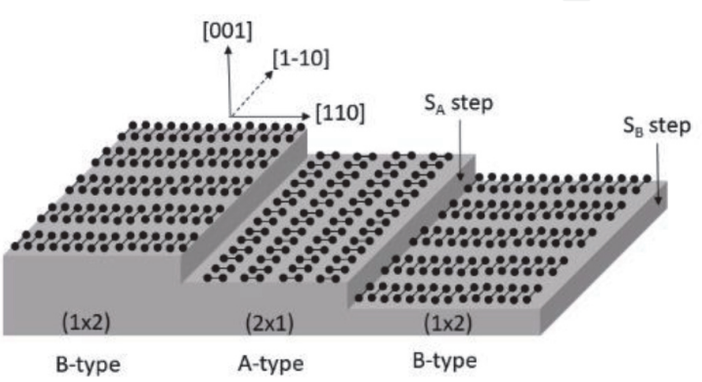

Figure 2.
Dimerization of the Si(001) surface with alternating (2 × 1) and (1 × 2)-reconstructed terraces (named A-type and B-type terraces respectively) separated by S_A and S_B single steps.

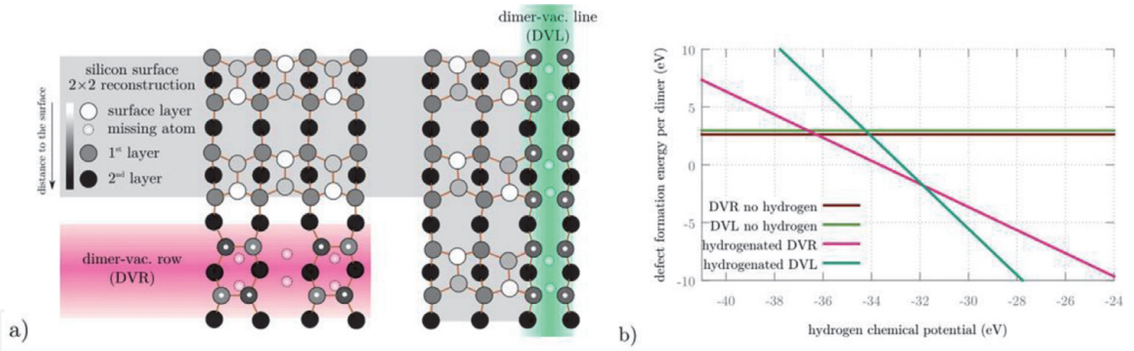

Figure 3.
(a) Schematic view of the DVR and DVL line defects on the 2 × 2 reconstructed silicon surface. Only two silicon bulk layers are represented (black and dark grey) in addition to the surface layer which is reconstructed. The distance from the surface is coded in gray-scale. Silicon atoms marked with a small white disk are hydrogenated in the case of hydrogenated DVR and DVL. (b) The variation of the formation energy of both DVR and DVL defects, bare or hydrogenated with respect to the chemical potential of the hydrogen. From [11].

The formation energy of the bare line defects DVR and DVL (i.e. with dangling bonds, labelled DVR and DVL no hydrogen), are represented on the **Figure 3b**. In order to take into account the hydrogen of the chamber in CVD ambient, the bare line defects are modified by placing a single hydrogen atom on each silicon of the first bulk layer with a dangling bond (**Figure 3a**), changing their geometry and their formation energies. Indeed, the DFT calculations show that for both defects and whatever the surface states, the geometry distortions of the bare defects are considerably reduced when the defect is hydrogenated. In the DVR case, for instance, the dimers in the line adopt a flat position instead of a tilted one. This reduction in elastic stress is key in the formation energy lowering of the line defects. As shown on **Figure 3b**, for hydrogen rich conditions (right handside of the graph **Figure 3b**), the formation energies of both hydrogenated DVR (H-DVR) and DVL (H-DVL) are lower than for the bare defects. Moreover, two regimes can be observed whatever the surface state is. One range for superhigh H chemical potentials where the H-DVL is favored, and a medium range of H chemical potentials where the H-DVR takes prominence. It is worth to note that the gain in energy per dimer can be quite important (several eVs) when comparing the different ranges, showing that the selectivity with respect to H chemical potential is quite strong.

The role of hydrogen is thus twofold. It first induces a large increase of dimer-vacancy concentration due to the lowering of their formation energy. The second effect of hydrogen is to select DVR with respect to DVL when using suitable hydrogen annealing conditions. This latter point is the key to obtain a single domain Si(001) surface. Indeed, the DVRs cross the B-type terraces in a direction perpendicular to the step edges. This can generates a nearly complete etching of the S_B steps if the terraces are not too large. This assumption was tested with a 600 Torr/900°C/10 min H_2 annealing of different on-axis Si(001) wafers. Prior to the H_2 annealing, the native oxide is removed by SICONI™ process [14]. Atomic force microscopy (AFM) images of **Figure 4a**. shows the result obtained from a wafer with a very slight 0.05° misorientation near the [110] direction. The DVRs that run across the B-type terraces can be clearly distinguished. They lead to comb-like shaped B-type terraces. Nevertheless, the terrace width is too large (the miscut angle too small) to obtain a complete removal of B-type terraces. On the contrary, when using a wafer with an higher misorientation (0.15°) in the [110] direction, the B-type terraces can be selectively etched as shown in **Figure 4b**. The AFM line profile confirms the formation of double steps (~2.7 Å in height)). However, there is still a few small islands remaining at the step edges (not clearly visible from the AFM image). This behavior was also observed by other authors working on

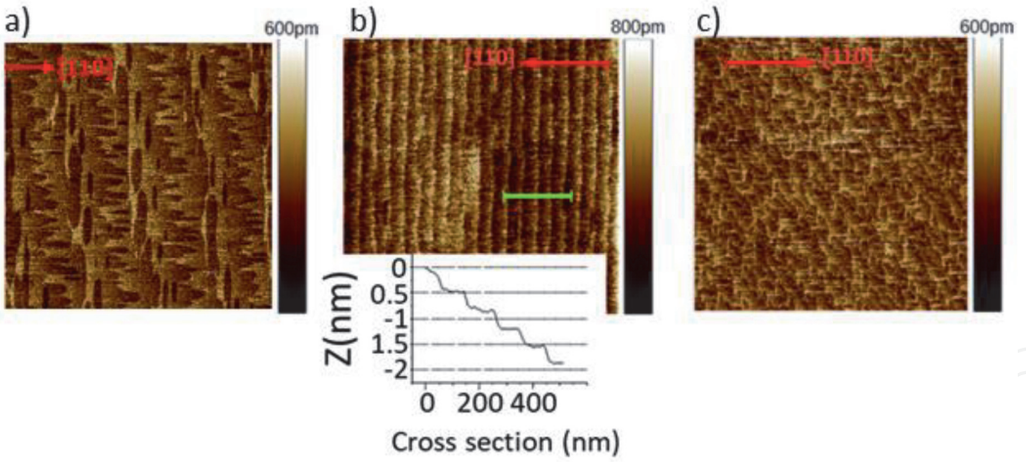

Figure 4.
2 × 2 μm² AFM image of nominal Si(001) surfaces after 600 Torr/900°C/10 min H_2 annealing (a) substrate 0.05° misoriented near [110]. DVRs crosse the B-type (A-type) terraces in a direction perpendicular (parallel) to the single-step edges (b) substrate 0.15° misoriented in [110]. The surface is double-stepped with terraces width of ~100 nm and step height of ~2.7 Å (line profile in inset). (c) substrate 0.12° misoriented near [100]. H-DVRs lead to dendritic single-steps oriented in <110> directions. Images partially reproduced from [11].

GaP-on-Si growth [15, 16]. H_2 annealing of a Si(001) substrate with a 0.12° miscut near the [100] direction was also tested. When the miscut direction slightly differs from the <110> azimuthal directions, each terrace boundary is made of two types of step edge (with both S_A and S_B steps). The selective etching of the S_B-segments leads to a dendritic shape of the terraces (**Figure 4c**). Thus, it is not possible to achieve double-layer steps formation on wafers having a miscut direction different from <110>. It should also be noted that the S_B step etching only occurs for hydrogen conditions near the atmospheric pressure and for a temperature > 850°C [11]. Otherwise, the generation of dimer-vacancies agglomeration is energetically not favorable for such hydrogen chemical potential (**Figure 3b**).

1.2 APBs-free GaAs growth on Si(001)

The effectiveness of the Si surface preparation for APBs removal was proven from GaAs growth on different types of nominal wafers. MOCVD growth of GaAs-on-Si can be achieved using a two-step process [4, 5]: few nanometers of a high-density nucleation layer is first deposited at low temperature (350–450°C) followed by the coalescence of the nuclei during temperature ramp up to 550–700°C. Then at this temperature, a thicker GaAs layer is epitaxially grown to improve the material quality. Classical group-III precursors are TMGa or TEGa while group-V precursors are often TBAs or AsH_3 for the high temperature step. The precursors are injected in the MOCVD chamber using purified H_2 as carrier gas. **Figure 5a** shows the morphology of the GaAs surface grown on Si wafer with miscut angle <0,1° (the type of Si surface presented in **Figure 4a**). Thanks to their V groove shapes, randomly oriented APBs can be observed by AFM with a linear density of several μm^{-1}. This APB density is equivalent to the one obtain for a GaAs growth on a silicon substrate without any surface preparation. It results in a large surface roughness with a root mean square (RMS) value of about 1.5–2 nm. As mentioned before, the APBs originate at the single-step edges between the very large (2 × 1)/(1 × 2)-Si(001) terraces of **Figure 4a**. Thus, the self-annihilation of the APBs is not possible in the GaAs layer (with a typical thickness around 400 nm) due to the large inter-APB distance.

As the Si wafer miscut angle is increased above 0.1° exactly in the [110] direction, the APBs can be easily removed. The AFM image of a 150 nm thick GaAs layer

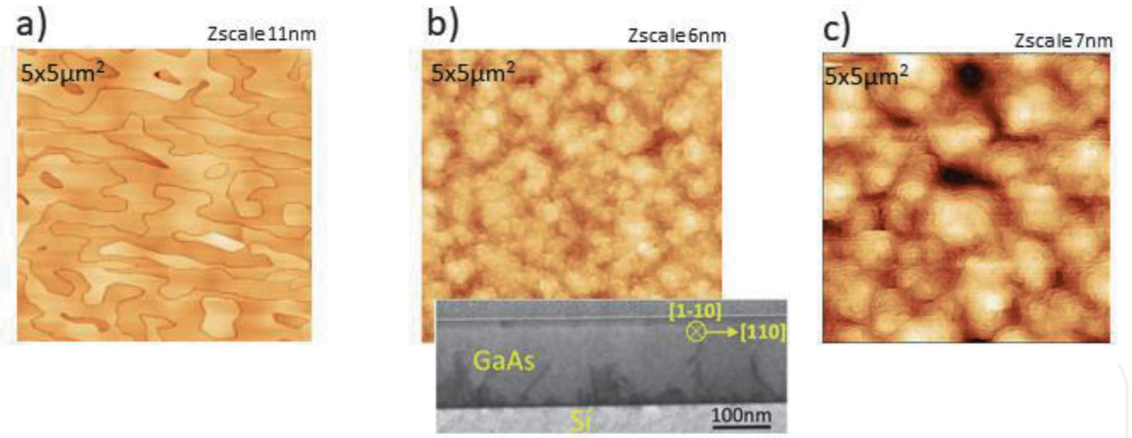

Figure 5.
5 × 5 µm² AFM images of (a) 400 nm-thick GaAs epitaxially grown on 0.05°-miscut angle Si(001) wafer: High density of randomly oriented APBs. RMS roughness = 1.7 nm. (b) 150 nm-thick epitaxially grown APBs-free GaAs on Si(001) wafer with a 0.15°-miscut angle toward the [110]. The (110)-STEM cross section in inset shows a layer free of APBs beyond about 70 nm of thickness. (c) APBs-free GaAs film grown on Si wafer with a > 0.1°-misorientation toward a random direction. In this case, 300-400 nm of thickness is necessary to get rid of APBs. Images partially reproduced from [11, 17].

is shown in **Figure 5b**. The surface roughness is improved and the RMS value drop to 0.8 nm. This roughness is similar to the one reported for 1 µm thick GaAs grown on 4°-6° offcut Si(001) substrate [18–20], despite the fact that only 150 nm of GaAs were grown. No V-groove feature is observed indicating that a APBs-free surface is formed. The absence of APBs on top of the GaAs layer is confirmed by the STEM cross section image (inset of **Figure 5b**.). The (110)-STEM cross-section shows a dark zone at the bottom of the GaAs layer due to the highly defective Si/GaAs heterointerface. The defective area is a combination of multiple crystalline defects such as dislocations, stacking faults and APBs due to the remaining small monoatomic silicon islands mentioned before. However, for a thickness beyond about 70 nm, no more APB planes propagate toward the surface. Indeed, the APB planes that nucleate at these monoatomic step edges have intersected pairwise during the high temperature growth and thus self-annihilated. The kinking of APBs in the III-V layers followed by their self-annihilation is often explained by kinetic phenomena [21, 22]. In such mechanisms, the adatoms incorporation rate is anisotropic along the two azimuthal <110> directions. In GaAs, several groups have indeed already shown a diffusion constant of Ga atoms 4 times larger along the As dimer lines regarding to the one along the dimer rows [23–25]. It results in a bias between the growth rate of the domains in antiphase responsible for the kinking of the APBs.

Interestingly, a GaAs film grown on Si wafer with a misorientation above 0.1° and toward a random direction (different from the <110>) is also APBs-free beyond a thickness of about 300-400 nm (**Figure 5c**). This can be achieved even though the Si surface is only made of single-layer steps. Actually, this silicon surface, described in the previous section and in **Figure 4c**, is made of very narrow dendritic terraces. Thus, the (2 × 1)/(1 × 2)-Si domains size are small enough to enable the self-annihilation of the APBs. However, when the misorientation is not in the <110>, a 100 nm-thick GaAs layer is not sufficient to get rid of the APBs and a thicker buffer layer is required.

In an industrial point of view, this is particularly important to relax the constraint on the wafer miscut specifications. Any substrate with a miscut-angle >0.1° can be used whatever the in-plane direction of the wafer slicing. Therefore, contrary to the GaP-on-Si system, the double-layer steps on nominal silicon wafers is not mandatory to achieve a APBs-free GaAs layer.

In the same fashion, the GaAs layer can be epitaxially grown by using a lattice-matched Germanium buffer layer [26]. Beyond the APBs issue, using a relaxed Ge buffer layer is also an interesting strategy to decrease the threading dislocation density in the GaAs layer, as we will see in the next paragraph. Due to the fact that GaAs will be quasi-lattice matched to the Ge strain relaxed buffer and thanks to a reuse of the existing threading dislocations to create new misfit sements if needed, the GaAs/Ge interface should exhibit no such high density of defects as when growing directly GaAs on Si. This will permit a clearer view of the GaAs/Ge interface to precisely observe the defects present when growing polar material on Ge, which is not possible when growing GaAs directly on Si.

$5 \times 5\ \mu m^2$ AFM images (**Figure 6**) show the surface of 300 nm thick GaAs layers grown on 1 μm-thick Ge/Si(001) substrates with three different offcut angles in the <110> direction: (a) 0.1°, (b) 0.3°, and(c) 0.5°. The APBs density decrease as function of the miscut angle. With a silicon wafer having a miscut angle of 0.5° the 300 nm-thick GaAs layer is completely free of APBs.

Contrary to the direct growth of GaAs on Si, we still observe APBs with a 0.3° offcut Si substrate.

In order to have insight on the defects at the interface in this case, cross-sectional TEM images of a GaAs layer grown on Ge-buffered Si substrate with a 0.5° offcut in the <110> direction are shown in **Figure 7**. The left hand image shows the overall stack, with (from bottom to top) the 0.5° offcut silicon substrate, the 800 nm thick Ge strain relaxed buffer and the 280 nm thick GaAs layer. The interface between GaAs and Ge is highlighted by a thin white line superimposed in the left hand part of the image. No APBs nucleating at this interface are observed, but some dark dots are nevertheless present. The image in the right hand part of **Figure 5** is a magnified view of this interface, showing randomly distributed, different size dark dots which are small (<50 nm), and not at the origin of any extended defects.

Higher resolution images of two of these interface defects have shown that dark spots at the interface are voids, not APBs. Therefore, we observe no APB when using a 0.5° offcut Si substrate for growing GaAs with an intermediate Ge strain relaxed buffer. This hints that bi-atomic steps are achieved at the surface of the Ge strain relaxed buffer using the appropriate hydrogen bake (T > 750°C at 80 Torr H_2), and we observe no APB annihilation such a seen previously when growing GaAs directly on Si.

The progressive improvement of the GaAs layer quality as function of the Si-miscut angle can also be observed from the FWHM of the (004) diffraction line in XRD ω-scan (**Figure 8**).

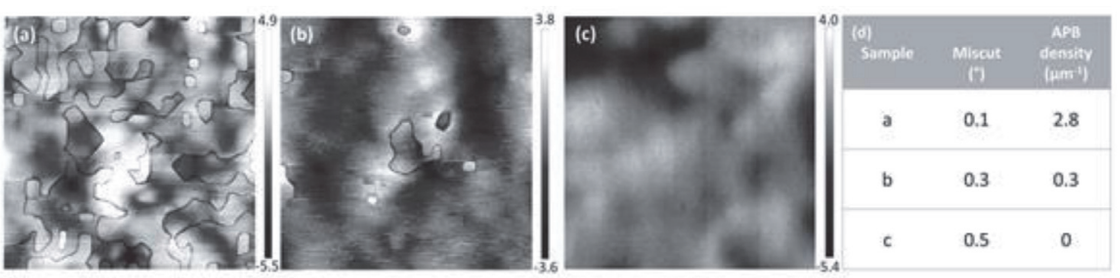

Figure 6.
$5 \times 5\ \mu m^2$ AFM images of the surface of GaAs layers grown on Ge-buffered silicon(001) substrates with three different offcut angles: (a) 0.1°-offcut angle, (b) 0.3°-offcut angle, and (c) 0.5°- offcut angle. All the offcut angles are in the <110> direction. The scale on the right hand side of each image is labeled in nm. The table (d) presents the APB density measured for each sample. AFM image sides are along the <100> directions. From [26].

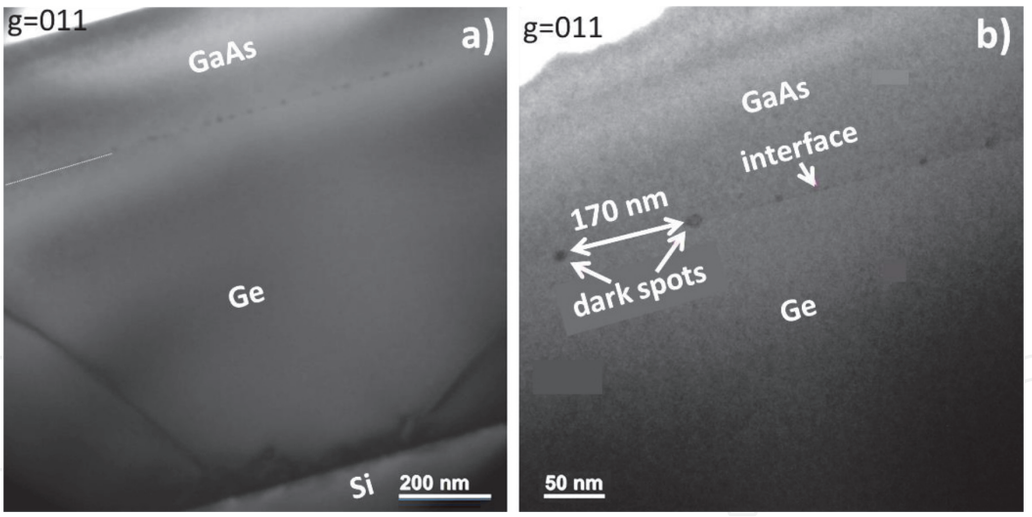

Figure 7.
Cross-sectional TEM images of a GaAs layer on a Ge-buffered Si substrate. The left hand image is an overview of the overall stack, with the 0.5° offcut Si substrate at the bottom. The right hand image is a zoom of the GaAs/Ge interface.

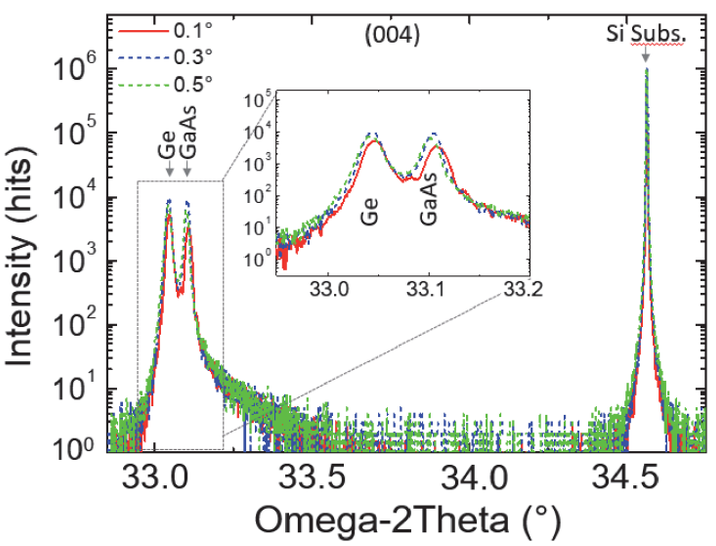

Figure 8.
High resolution, X-ray diffraction profiles around the (004) order (in the triple axis configuration) for a GaAs layer grown on a Ge-buffered silicon substrate with a 0.1° (solid line), 0.3° (dashed line), and 0.5° (dotted line) offcut. From [26].

Detrimental influence of APBs on the optical properties is highlighted from photoluminescence (PL) measurements at 300 K [17]. PL spectra of **Figure 9** compares the near band edge luminescence (1,42 eV) of GaAs-on-Si layers with and without APBs. Both layers are n-doped at 7.10^{17} cm^{-3}. The PL intensity of the APBs-free GaAs film is three times higher than the one of the GaAs layer with APBs. Furthermore, the PL peak of the APBs-free is 40% narrower. These results are directly correlated to the role of APBs acting as non-radiative recombination centers.

In the same way, the influence of APBs on the electrical properties is highlighted from the Hall effect measurements on a 250 nm-thick GaAs active layer n-doped at 7.10^{17} cm^{-3}. This n-doped active layer is grown on intrinsic GaAs-on-Si buffer layers with/without APBs. Hall effect measurements, in the Van der Pauw configuration, are performed by taking 5 points across the whole 300 mm wafer. The mean electron mobilities are reported in **Table 1**. The electron mobility (μ_e) of the GaAs active layer grown on the APBs-free buffer layer is one decade higher than the one

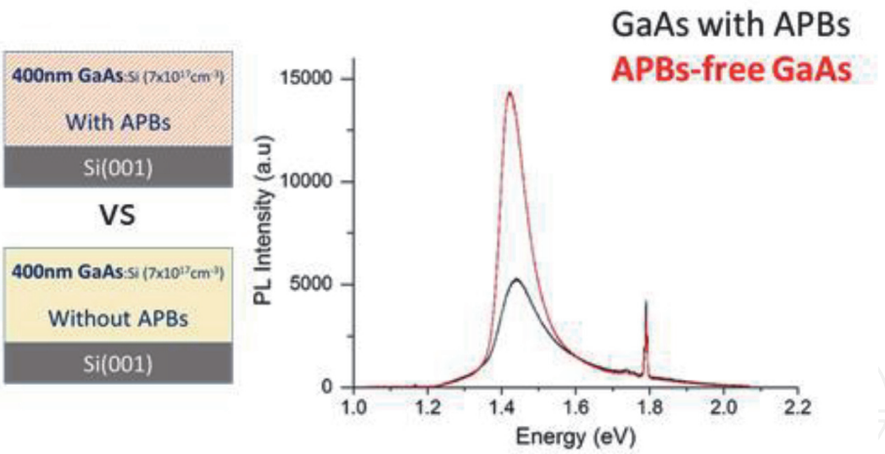

Figure 9.
PL spectra at 300 K for GaAs-on-Si layers with and without APBs. The PL intensity is 3 times higher for the layer without APBs. The FWHM of the peak is 40% lower [17].

250 nm GaAs:Si (7×10^{12} cm^{-3}) Active layer without APBs	**VS**		**250 nm GaAs:Si(7×10^{12} cm^{-3}) Active layer without APBs**
400 nm GaAs buffer With APBs			**400 nm GaAs buffer Without APBs**
Si(001)		Si(001)	
Sample	Doping level (cm^{-3})	Electron mobility (cm^2/V.s)	Resistivity (W/cm)
GaAs-on-Si with APB	7×10^{17}	200	2×10^{-2}
GaAs-on-Si without APB	7×10^{17}	2000	4×10^{-3}
GaAs-on-GaAs	7×10^{17}	2500	3×10^{-3}

Table 1.
Hall effect measurements at 300 K for GaAs-on-Si layers with/without APBs. The electron mobility is 10 times higher for the layer without APBs [17].

obtained on the buffer with APBs. The μ_e = 2000 cm^2V^{-1} s^{-1} value of the APBs-free layer is nearly equivalent to the mobility measured from an homoepitaxy n:GaAs-on-GaAs in the same reactor.

1.3 Summary

APBs formation during the heteroepitaxy of GaAs on nominal Si(100) substrates has hindered for a long time the development of GaAs devices on a Si CMOS platform. With new technologies and processes established by researchers and tools suppliers to control the atmosphere in growth chambers and prepare the Si surface before the epitaxy, one can get rid of APBs easily on GaAs/Si(100).

2. Part 2: reduction of threading dislocations density

The strategies to reduce the threading dislocation density (TDD) in the III-V layer can be classified according to two major tendencies: 1) engineering of thick buffer layer (strained layer superlattices, germanium buffer layer, ...) to annihilate

the defects before growth of the III-V active layer. 2) Selective area epitaxy in dielectric cavities (SiO_2,SiN, ...) formed by standard technological steps (deposition, lithography, etching, ...). In this last approach, the threading dislocation (TD) propagation is geometrically limited in one direction by the sidewalls of the patterns. These two majors will be described more deeply in the following paragraphs.

2.1 Insertion of dislocation filters

2.1.1 Introduction to dislocations

The technology of monolithic integration of III-V on Si is of great interest due to combining the superior optical properties of III-V materials and the advantages of Si substrates such as low cost and high scalability [27]. However, as most III-V semiconductor materials have a relative large difference in lattice constant to Si, high density of crystal defects are generated during the epitaxial growth. This leads to the failure of the technique of direct deposition of III/V on Si become commercially viable in 1980s, despite intensive studies have been demonstrated in that era [28]. The lattice mismatch property creates a substantial stress accumulation in the first few pseudomorphic layers of deposited material, as shown in **Figure 10a**. As the stress is accumulated above a critical value of growth thickness, the strain-relaxation process leads the generation of misfit dislocations (MDs). The MDs are associated with missing or dangling bonds along the mismatched interface which are shown in **Figure 10b** [30], thus MDs lie entirely on the growth plane. Since the dislocations cannot be eliminated within a crystal due to energetic reasons, the MDs must either reach the edge of crystal or turn upward through the deposited layers to form TDs. As a result, from the transmission electron microscopy (TEM) shown in **Figure 10c**, TDs seem to extend from the interface of III-V and Si, and go through the epilayer. TDs are likely to be transferred from MDs when the distance to the sample edge is much longer than the distance to the epi-layer surface. Meanwhile, TDs could also transfer to MDs either through dislocation glides, extending the misfit segment beneath it, or in active region during the electron–hole recombination through the phenomenon known as recombination-enhanced dislocations

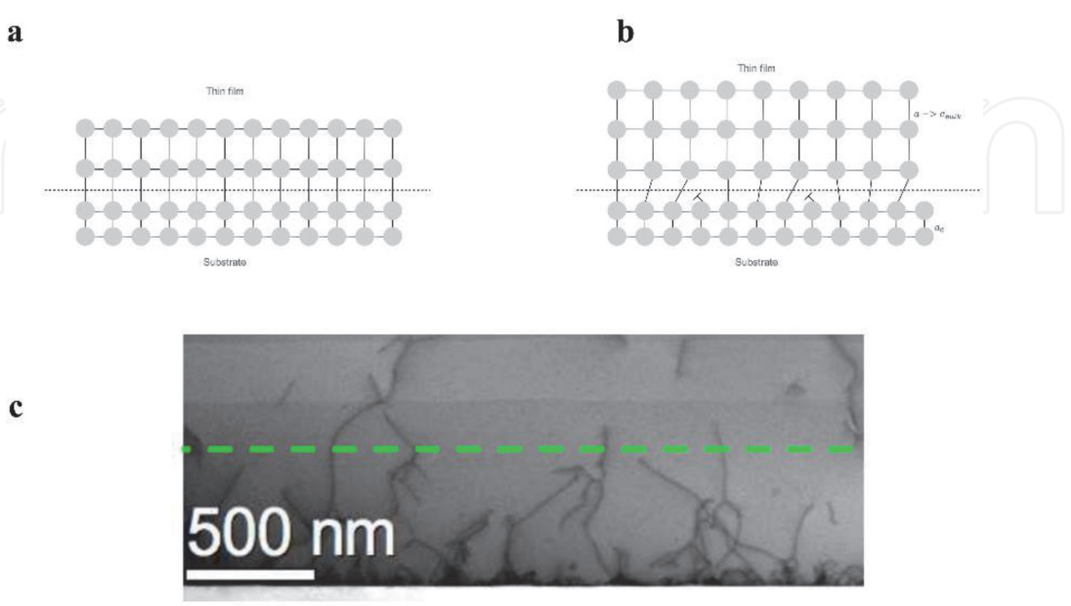

Figure 10.
Schematic change in lattices of thin film on substrates and bright field scanning TEM image of TDs. (a) denoting the initial pseudomorphic layers of deposited materials. (b) denoting MD as spinning "T". (c) a bright-field STEM image showing the TDs. (adapted from Ref. [29]).

motion [31]. Typically, in the growth of GaAs on Si, the TDD is around 10^{10} cm^{-2} at the growth interface [32]. Unfortunately, the viable TDD in active region for practical optoelectronic devices should be below 10^{6} cm^{-2} [32], which held back the development of many III-V on Si material systems for some time. Those dislocations have associated trap states serving as nonradiative recombination centers to reduce the photon emission efficiency and/or minority carrier lifetime [32], resulting in a degradation of devices performance. In addition, those states in the band could also increase the leakage current of the devices [3].

Efforts have been made to control the TDD in GaAs grown on Si substrates. As the thickness of deposited layer increases, TDs will glide, move and react with other TDs depending on their Burger vectors, resulting in a repulsion or annihilation as **Figure 11** shows. As TDs keep propagating in the overlayers, they are likely to meet other dislocations to be self-annihilated as shown in **Figure 11**. If there is a strain induced by the lattice mismatched between the underlayer and overlayer, generated TDs are expected to experience lateral forces which drive TDs into edge as **Figure 11** deflection to edge shows.

The deflection process relives the strain induced by lattice mismatch and makes TDs to react with other TDs more likely and/or convert TDs into MDs to decrease the TDD. As demonstrated by Masami and Masafumi in 1990, the dislocation density n in a thick GaAs layer grown on Si can be estimated through the following Equation [34]:

$$n(x) = \frac{1}{\left(1/D_0 + b/a\right)\exp\left(ax\right) - b/a}$$

where x is the thickness of the GaAs layer, D_0 is the dislocation density at the interface, a and b are two constants related to the density of etch pit defects (EPD) and coalescence of dislocations respectively. According to their characterization, $D_0 = 10^{12}$ cm^{-2}, $a = 2 \times 10$ cm^{-1}, and $b = 1.8 \times 10^{-5}$ cm. For the dislocation density in a thin GaAs film on Si, it can be estimated through $n(x) = D_0 h^m$, where D_0 is the dislocation density at the interface and m is the empirical value with minus symbol [28, 35, 36]. In order to reduce the TDD to the level of 10^{6} cm^{-2}, the thickness of GaAs is estimated to be as thick as 100 μm [34].

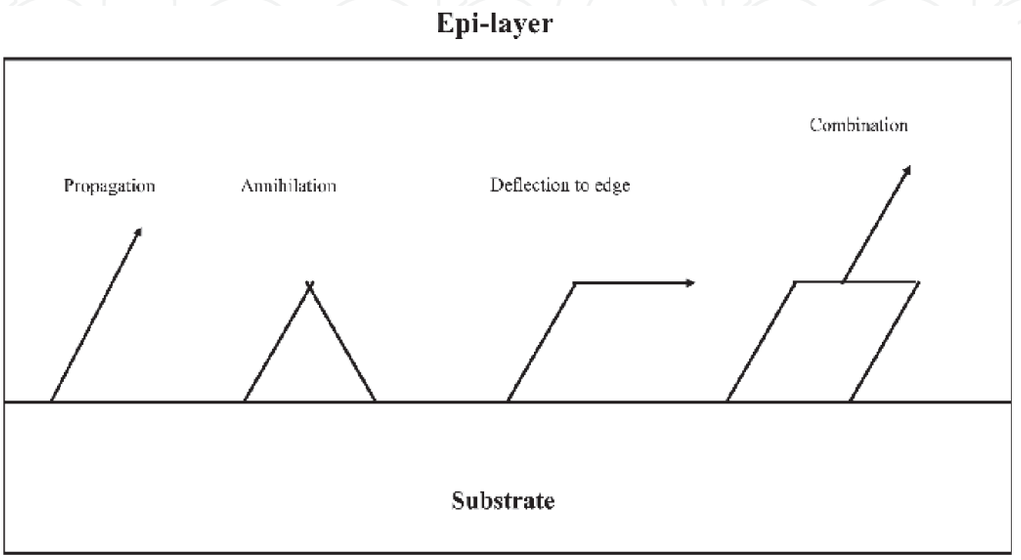

Figure 11.
Mechanisms of dislocation motion in GaAs/Si. (Reproduced from Ref. [33]).

However, due to the difference in thermal expansion coefficients of GaAs and Si, a GaAs layer which is thicker than 7 μm will induce micro cracks on GaAs thin films [37]. In addition, a thick GaAs buffer on Si will bend the wafer [34]. Thus, a more effective method known as dislocation filtering has been put forward to induce designed strain to bend the TDs and to encourage TDs to move, interact and annihilate [28]. The most common dislocation filter layer (DFL) system includes strained layer superlattice (SLSs) and quantum-dot (QD) DFL, while different SLS structure including InGaN/GaN [38], InGaAs/GaAs, InAlAs/GaAs [32] and GaAsP/GaAs [39], have been studied. A typical cross-sectional TEM measurement for InGaAs/GaAs SLSs DFLs is shown in **Figure 12(a)**, indicating how the TDs are eliminated within DFLs. Taking InGaAs/GaAs DFL for example, a layer structure of InGaAs/GaAs is shown in **Figure 12(b)**. The strain direction, induced by the lattice mismatch, inside the DFL is shown in **Figure 12(c)**.

The appropriate choice of composition and thickness for SLS is dependent on the material and the prior dislocation density. Since the purpose of DFL structure is to introduce strain to promote the TD motions, forming dislocations should be avoided within DFL, which means the thickness for each layer should below the critical thickness. For most SLSs, the thickness of each layer should below 20 nm [28, 29, 32]. By using SLS DFL technique, researchers from University College London have successfully reduced the TD density down to the 10^6 cm^{-2} [27].

Although SLSs have been proved to remove more than 90% of TDs [28], the induced strain which bends TDs is still within 2 dimensions. QD is a 0-dimensional nanostructure with much larger strain field compared to SLS. As a result, it is believed that QD can also sever as the DFL, which might be even superior than SLSs [40]. Researchers from University of Michigan have proved that InAs QDs were the most suitable QD. A fabricated laser structure with InAs QD DFL was demonstrated with a threshold current density of 900 Acm^{-2} [40].

2.1.2 Validation of SLS DFL

$In_xGa_{1-x}As$/GaAs SLSs have been recently studied on the GaAs/Si material platform due to its variable strain force. Since the bending efficiency to TDs depends on the strained induced by the lattice-mismatched, the indium composition, the

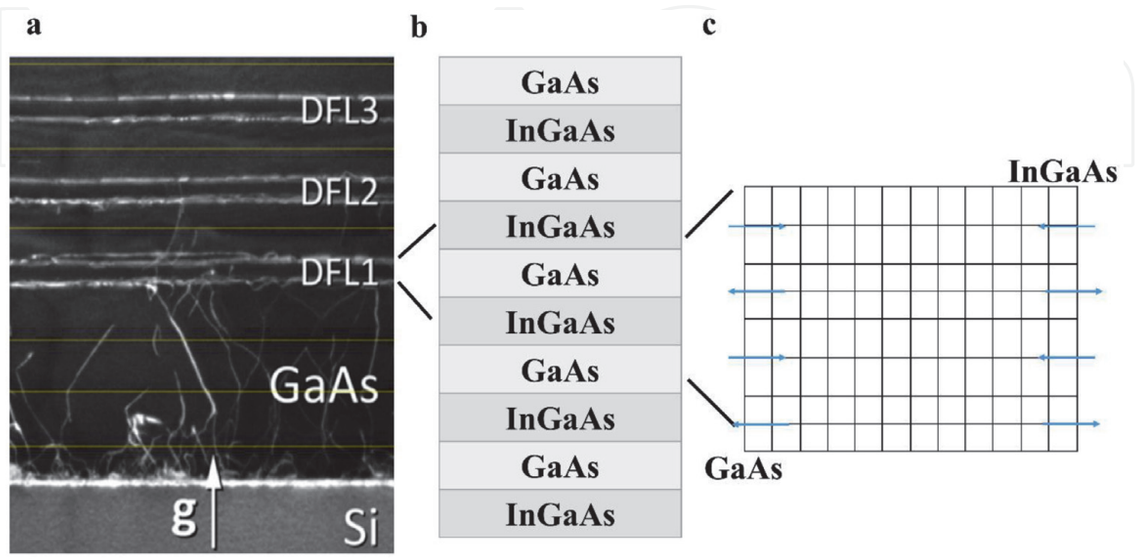

Figure 12.
An InGaAs/GaAs DFL schematic structure in different views. (a) The DFL sample structure in the cross-section TEM. (Reproduced from Ref. [28]). (b) The layer structure of 5 layers of SLSs. (c) The DFL structure in lattice view. The blue arrow denotes the direction of the strain.

thickness of strained layer, and the repetition of SLSs as well as the DFLs are of the greatest interest and need to be considered when optimizing the SLS.

Experiment Techniques

We have investigated the $In_xGa_{1-x}As/GaAs$ SLSs DFLs [32, 41]. As shown in **Figure 13a**, a 1 μm two-step grown GaAs were grown on n-doped Si substrate (001) with 4° offcut towards <011> by using Molecular Beam Epitaxy (MBE) system, while the Si substrate was performed at 900°C for 30 minutes to deoxidize. Then three sets of DFLs were grown, while each DFL structure was composed of five periods of $In_xGa_{1-x}As/GaAs$ SLSs. On the top of DFL, an optimized InAs dot-in-a-well (DWELL) structure was embedded between two 100 nm GaAs layers and 50 nm $Al_{0.4}Ga_{0.6}As$ layers [42, 43]. A final 300 nm GaAs was deposited on the whole structure.

Effectiveness of DFL composed of SLSs

PL measurement was applied through a 635-nm solid-state laser excitation at room temperature. The PL results of InAs QDs with different $In_xGa_{1-x}As/GaAs$ DFL parameters are summarized in **Table 2** and shown in **Figure 14**. In view of the PL intensity and the full width at half maximum (FWHM), it can be known that sample 1 (18% In composition) exhibits a higher PL intensity than sample 2(16% In composition) and sample 3(20% In composition). The PL intensity is highly related to the crystal quality, which corresponds to the TDD. Thus, 18% In composition is proved to contribute to the best crystal quality compared with the other indium compositions. When the thickness of GaAs layer was changed, sample 4 is similar to

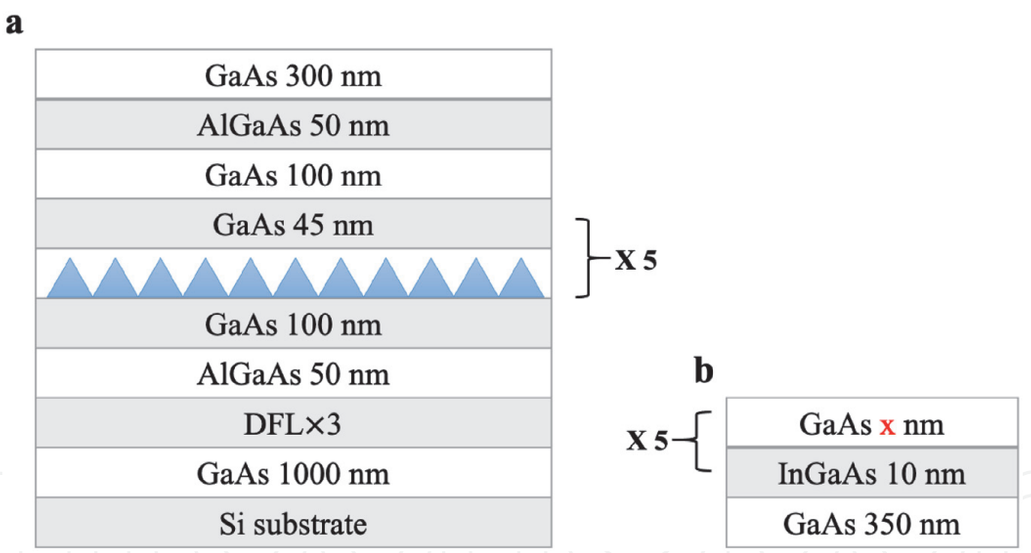

Figure 13.
Schematic diagram of InAs/GaAs DWELL structure monolithically grown on Si substrates with different DFL structures. (a) Schematic diagram of the whole structure. (b) Schematic diagram of the InGaAs/GaAs SLSs as DFL.

Sample	$In_xGa_{1-x}As$	GaAs Thickness (nm)	PL intensity (a.u)	FWHM (nm)
1	$x = 0.18$	10	4	40.3
2	$x = 0.16$	10	2.6	39.8
3	$x = 0.20$	10	2.2	42
4	$x = 0.18$	9	3.9	40.4
5	$x = 0.18$	8	2	46.1

Table 2.
Details parameters for $In_xGa_{1-x}As/GaAs$ SLSs in each sample.

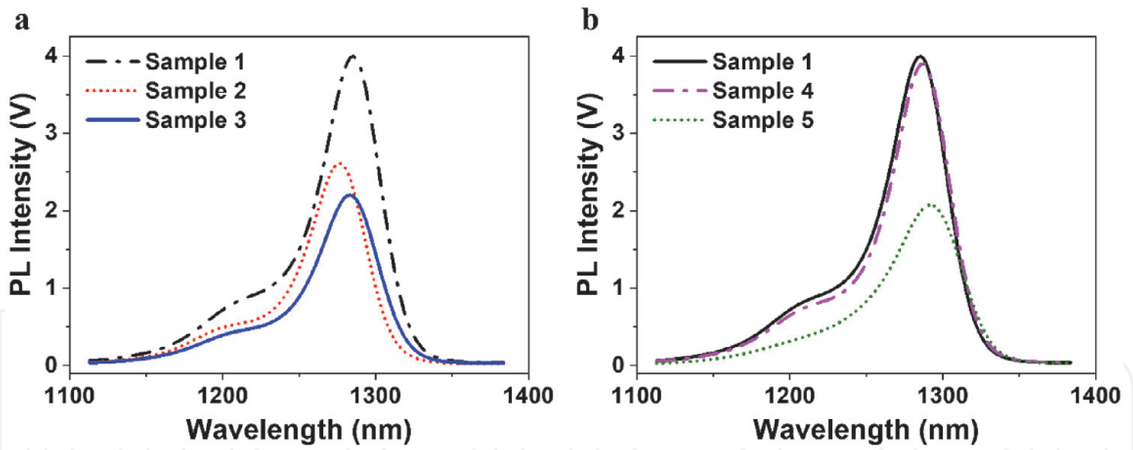

Figure 14.
PL spectra of different samples at room temperature. (a) Sample 1, 2, and 3 with indium composition of 18%, 16%, 20% respectively. (b) Sample 1, 4, and 5 with GaAs spacer layer thickness of 10 nm, 9 nm and 8 nm respectively. (Reproduced from Ref. [32]).

sample 1 in view of the PL intensity, while sample 5 has a significant reduce. In addition, the FWHM of sample 5 is much wider than other 2. This phenomenon is explained through an 8 nm thin GaAs layer cannot release the strain completely so that the accumulated strain degrades the material quality [32].

To further investigate the effectiveness of DFL, Cross-sectional TEM measurements were applied to examine the crystal quality and the effectiveness of DFL. The dark-field TEM image and the bright-field TEM image are shown in **Figure 15**. As shown in **Figure 15a**, high number of TDs appear at the GaAs/Si interface propagating towards the epilayers, as most of them annihilate with others in the first 200 nm. However, there are still a great number of TDs propagating towards the upper layer. After the DFL, only a few TDs puncture the DFL and keep propagating upwards, while most TDs are blocked by the DFL.

In order to further investigate the DFL performance, DFL efficiency (η) is defined as the fraction of TDs it removes, which can be described as [28, 44].

$$\eta = 1 - \frac{n(\text{experiment})}{n(\text{predict})}$$

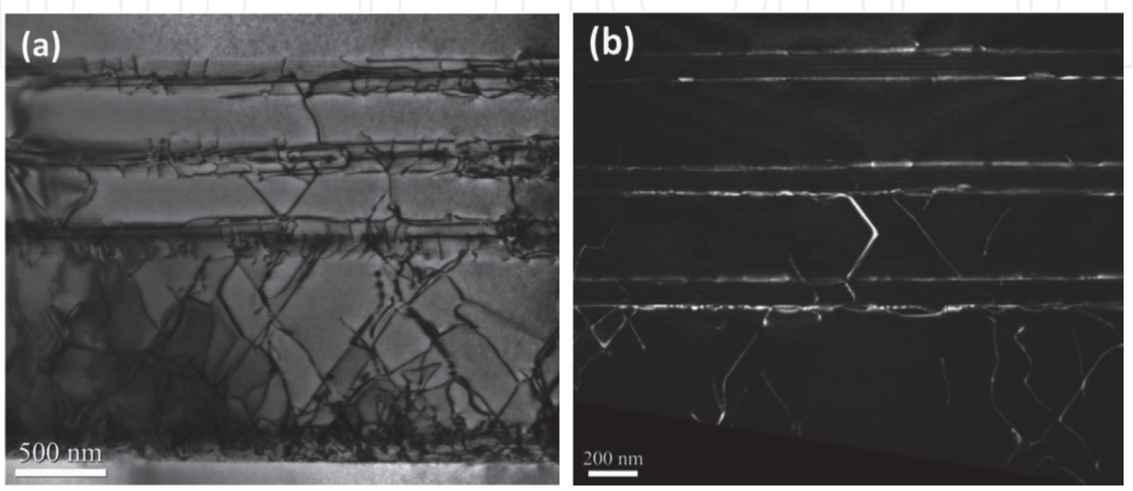

Figure 15.
The cross-sectional TEM image for TDs around DFL structure. (a) Dark-field TEM image (b) Bright-field TEM image (Reproduced from Ref. [32]).

Where n(experiment) denotes the number of dislocations just above the DFL, and n(predict) denotes the dislocations predicted by the equation $n(x) = D_0 h^m$, where $m = -0.5$. The efficiencies of different types of DFL are shown in **Figure 16**. From the figure, it can be known that almost half of TDs propagate through the first set of DFL regardless of indium composition of $In_xGa_{1-x}As$ layer. However, the sample with $In_{0.18}Ga_{0.82}As$/GaAs SLSs shows a superior ability in filtering efficiency compared to others, which achieves over 80%. The demonstrated highest efficiency presents a good balance between TD generation and strain induced to annihilate TDs.

Apart from the InGaAs/GaAs SLSs, InAlAs/GaAs SLSs is also another great option severing as DFL [45–47]. Due to the larger shear modulus of InAlAs, it is expected that the critical misfit for generating new TDs is much larger than that of InGaAs. We compared $In_{0.15}Ga_{0.85}As$/GaAs DFL and $In_{0.15}Al_{0.85}As$/GaAs DFL by growing InAs/GaAs QD samples on Si (100) substrates [41]. The $In_{0.15}Ga_{0.85}As$/GaAs DFL composed three repeats of 5 period of 10-nm $In_{0.15}Al_{0.85}As$ and 10-nm GaAs SLS separated by 400 nm GaAs spacer layer, while the $In_{0.15}Al_{0.85}As$/GaAs DFL had almost same structure except replacing the $In_{0.15}Ga_{0.85}As$ to $In_{0.15}Al_{0.85}As$. EPD were counted for both samples. After three sets of SLSs, the defects density of the sample with InAlAs/GaAs DFL was around 2×10^6 cm^{-2}, while the other one with InGaAs/GaAs DFL was round 5×10^6 cm^{-2} [41]. In addition, the sample with InAlAs/GaAs DFL had a higher PL peak intensity as well as thermal activation energy compared to the sample with InGaAs/GaAs [41].

2.1.3 Self-assembled QD as DFL

Since it is the Peach-Koehler force in strained layer to bend the TDs to encourage annihilation, self-organized QDs possess an even stronger Peach-Koehler forces, which means QDs are expected to bent TDs more efficiently [48]. Meanwhile, the strain field surrounding QD is 3 dimensions which is superior than 2 dimensions in SLSs.

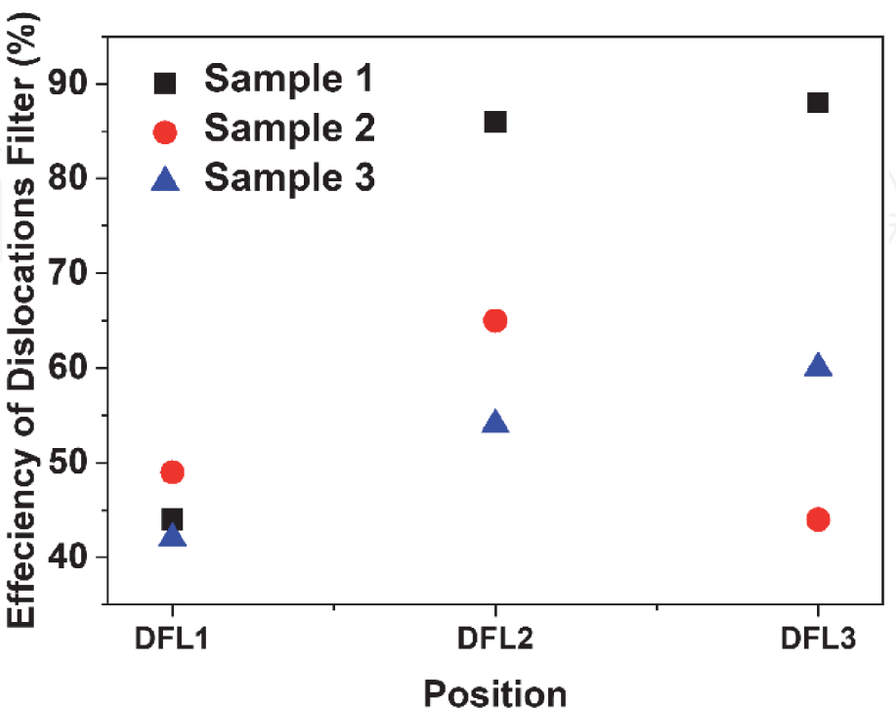

Figure 16.
Summary of the efficiency of dislocation filter for Sample 1, 2 and 3 respectively (Reproduced from Ref. [28]).

Theoretical models.

Several parameters need to be considered when using self-organized QDs as DFLs including QD composition, size, areal density, and the number of dots. The theoretical simulation of the effectiveness of dislocation bending is developed by J. Yang et al. [48], which assuming QD islands are coherently strained with pyramidal in shape. The energy ΔE_{rel} releases when the MD formed to bend the TDs can be calculated through

$$\frac{\Delta E_{rel}}{L} = \frac{2G_{dot}(1+\nu)}{(1-\nu)} f_{eff} b_{eff} h$$

While the dislocation self-energy ΔE_{dis} can be described as

$$\frac{\Delta E_{dis}}{L} = \frac{1}{2\pi} \frac{G_{buff} G_{dot}}{G_{buff} + G_{dot}} b^2 \left(\frac{1-\nu \cos^2\beta}{1-\nu}\right) \left[\ln\left(\frac{2r}{b}\right) + 1\right]$$

The bending will occur when the $\Delta E_{rel} \geq \Delta E_{dis}$. Here, L is the length of the MD, G_{dot} (G_{buff}) is the shear module of dot (buffer layer), ν is the Poisson ration,b is the Burger's vector, b_{eff} is the project of Burger's vector on the buffer layer, f_{eff} is the effective lattice mismatch between the QD and the underlying buffer layer, h is the height of QD, β is the angle between the Burger's vector and the dislocation line, r denotes an outer cutoff radius of the dislocation strain field.

According to the simulations, the bending area ratio, which denotes the bending area divided by the area of QD bases, is shown in **Table 3**. InAs QDs are proved to be the most suitable self-organized QD serving as dislocation filters with the largest bending area and largest critical layer numbers for QD multilayers [48].

Experiment Techniques

Considering the theory and results above, InAs QDs DFL has the highest efficiency compared with other QD DFLs for GaAs monolithically grown on Si. In order to investigate the TD behavior in QD DFL region, a buffer structure shown in **Figure 17** is grown with N-type doped InAs QD dislocation filter on Si (001) substrate with 4° misorientation towards [111]. A thin (<2 μm) GaAs layer is first grown by MOVPE with free of antiphase domain. The TDD at its surface is estimated to be (2–5) $\times 10^7$ cm^{-2}. The dislocation filter consists of 10 layers of InAs QD separated by 50 nm GaAs layers. On the top of QD dislocation filter, a 800 nm GaAs is grown.

Effectiveness of DFL composed of QDs

Cross-sectional TEM measurements were applied to investigate the propagation of dislocations in the QD DFLs. Images were obtained with various g, including [2,$\bar{2}$,0], [1,$\bar{1}$,1], and [0,0,4] as shown in **Figure 18a, b** and **c**, respectively. Two different types of TDs can be observed: pure edge dislocation labeled as C and 60° mixed TDs labeled as A and B. It is obvious from the cross-sectional TEM images

Quantum Dots	Dot Density	QD base area	Bending area ratio of a single QD	Bending area ratio of a single layer
Unit	(cm^{-2})	(nm^2)		
$In_{0.6}Al_{0.4}As$	2×10^{11}	27–56	~0	~0
$In_{0.5}Ga_{0.5}As$	5×10^{10}	80–132	<1%	~0
InAs	2×10^{10}	120–210	80%	10%

Table 3.
Bending area ratios for different QDs (Reproduced from Ref. [48]).

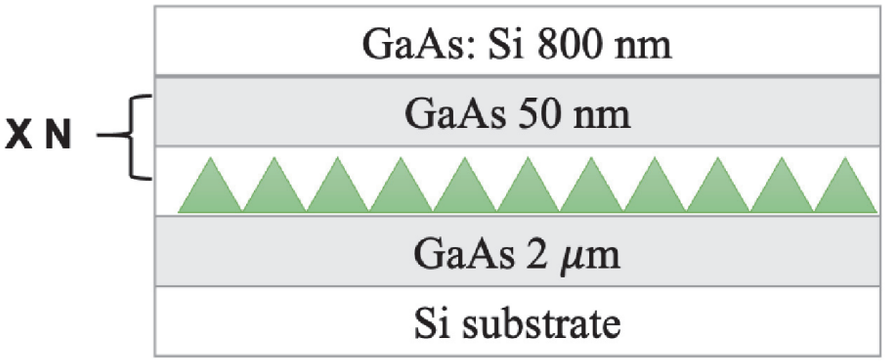

Figure 17.
GaAs grown on Si with 10 InAs QD layer as dislocation filter. (reproduced from Ref. [48]).

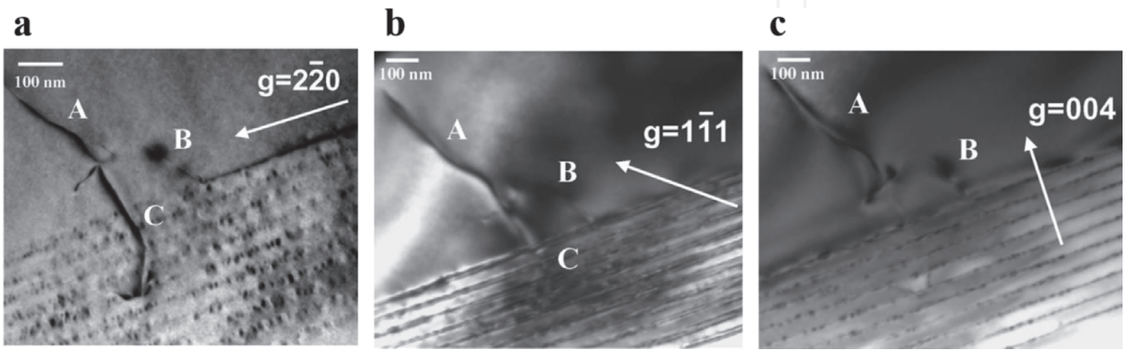

Figure 18.
Cross-section TEM images of dislocation propagation in the ten-layers InAs QD with various diffraction conditions: (a) g = [2,$\bar{2}$,0], (b) g = [1,$\bar{1}$,1], (c) g = [0,0,4]. (Reproduced from Ref. [48]).

that the QD DFL can bend 60° mixed TDs effectively. In addition, pure edge TDs, which cannot be blocked by the 2-D SLS [49], can be terminated within the QD DFL. Although the detail of this termination is not fully understood, it is believed that the formation of a dislocation loop or the annihilation with a dislocation with reverse Burger's vector result in the termination [48]. Recently, with the help InAs QD DFL, J. Wang et al. demonstrated a low dislocation density of 2×10^6 cm^{-2} [50], with a high efficiency of 96% calculated.

Conclusion

In the past 30 years, efforts have been made to decrease the TDs induced by the lattice mismatch between GaAs and Si. Many researchers have successfully adopted DFL method to decrease the density of TD to 2×10^6 cm^{-2} [45, 50]. However, a 9-μm thick GaAs buffer is indispensable if no other technique applied to achieve that density. Thus, the DFL technique is much more effective in reducing TDs comparing to grow GaAs buffer, which is summarized in **Table 4**.

With the DFL technique, researchers make it possible to reduce the vast number of TDs to a level which is commercially viable in a thin film around 2.5 μm. This

Technique	Thickness
Thick GaAs buffer layer	9 μm
InAlAs/GaAs SLSs as DFL	2.35 μm
InAs QD as DFL	2.205 μm

Table 4.
Summary of the requisite thickness with different methods to reduce the density of TD to 2×10^6 cm^{-2}.

technique has promoted the implement of III-V materials directly grown on Si such as growth of III-V lasers on Si substrates [27, 50].

2.2 GaAs growth on Germanium strain relaxed buffer

As germanium material has lattice parameter and thermal expansion coefficient close to those of the GaAs, a common strategy is to benefit from all the Ge heteroepitaxy on silicon developments to reduce the structural defects in the GaAs layer [31, 41, 51–53]. This way, we avoid additional threading dislocation nucleation. Currently, the TDD in a 1.5 μm thick Ge-buffer on Si(100) is in the 10^7 cm^{-2} range by using [54, 55] a thermal cycle annealing (TCA). The **Figure 19a**, extract from the works of Bogumilowicz et al. [56], shows the TDD evolution in function of the Ge buffer and GaAs total thickness, with a GaAs layer fixed at 270 nm thick. The GaAs layer is smooth (<1 nm RMS) and free of APBs thanks to the process described in the previous section. The TDD was estimated by using three methods: (i) from the XRD rocking curve width, the value is extracted with the Ayer's model [57] (ii) by counting the dark spots on the cathodoluminescence (CL) image of the GaAs surface, (iii) by counting the pits on the AFM image of the GaAs surface. Whatever the method, the authors show that the TDD tends to reach a plateau at a value around 3×10^7 cm^{-2}. Nevertheless, the downside of the Ge virtual substrate method is the wafer bowing due to the difference between the thermal expansion coefficients (around 120% for Ge and Si). The **Figure 19b** is a plot of the 300 mm wafer bow versus the film thickness. For the thickest Ge buffer layer (1.38 μm) the bow is measured at −240 μm. Such a value is still a hurdle for the wafer handling and processing with the 200/300 mm foundry tools.

2.3 TDD reduction by selective area growth

Selective growth method is often used in heteroepitaxy of semiconductors where cavities are used to block geometrically the propagation of structural defects that generate at the interface of lattice mismatch semiconductors. Different techniques could be implemented such as Epitaxial Lateral Overgrowth (ELOG) and Aspect Ratio Trapping (ART). We will describe more in details the last one.

ART allows to block inside the cavities some of the threading dislocations and planar defects propagating perpendicularly to the trench direction. Still, a few structural defects propagate through the film. **Figure 20a** summarizes the principle

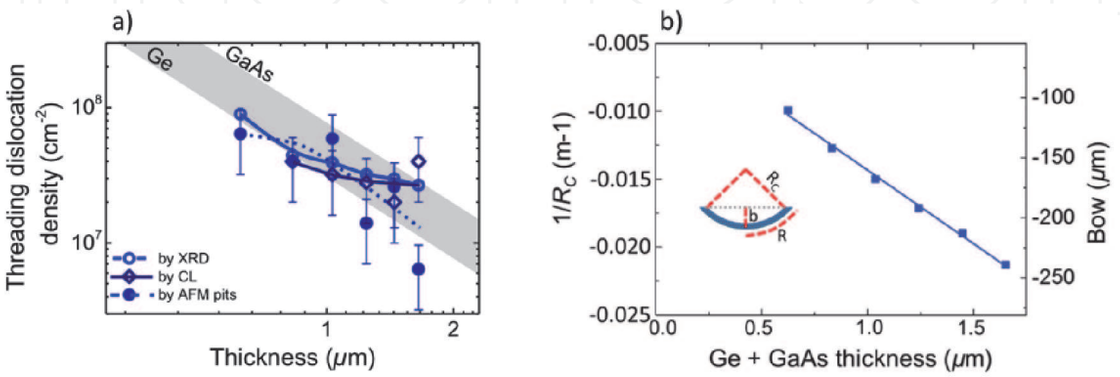

Figure 19.
(a) Plot of the TDD in the GaAs overlayers as a function of the total Ge + GaAs thickness. The light gray area corresponds to the expected TDD values in Ge or GaAs single layers as a function of thickness. Estimated error bars are shown for the TDD extracted from AFM and CL. The TDD error bar for the XRD data is $\pm 10^7 cm^{-2}$. (b) Plot of the substrate bow versus the total Ge + GaAs thickness.

of the method. In fact, the TDs propagating through the dense {111}-planes can be blocked by the geometry of the patterns. In this case the aspect ratio (height on width h/l) of the pattern must be such that $h/l \geq tan\,\theta_{(111)} = \tan(54.7°) = 1.4$. Therefore, for example, with a 150-thick dielectric, the cavity must be no wider than ~100 nm. Nevertheless, as we can see on the figure, the planar defects which lie parallel to the trenches can be more difficult (or impossible) to trap.

In the example of ART from the works of Lau et al. [58], they use about 100 nm-width oxide trenches on Si(001) etched by a wet solution of KOH to form a "V-groove" (**Figure 20b** and **c**). Indeed, with this type of wet etching the {111}-Si planes are revealed at the bottom of the trenches. This approach has the advantage to free the III-V layer from the APBs which doesn't form on Si(111) surface. The GaAs is then epitaxialy grown to obtain a nanoribbons array in the trenches. The growth process is achieved in a classical way with two steps: one low temperature nucleation (365°C) step followed by a fast growth at high temperature (570°C). The STEM images highlight some microtwins, at the Si/GaAs interface, which are trapped by the V-groove structure (**Figure 20c**). However, outside that thin area the GaAs layer is single-domain with a good crystalline quality. The XRD rocking curve from the (004) peak was measured in both configuration parallel and perpendicular to the line. For a 200 nm-thick GaAs the FWHM of each peaks are measured at 400 arcsec and 550 arcsec for the perpendicular and parallel configuration respectively. That difference is attributed to the defects not trapped by the trenches in the parallel direction. Some of these defects can be seen on the STEM cross-section, parallel to the trench, of **Figure 20d**. The Moiré fringes are formed by the interferences between the Si et GaAs crystal at the V-groove level. Besides the defects trapping by the cavity, the low defectivity is ascribed to the stress relaxation by the partial dislocations associated to the stacking faults and microtwins at the interface. This phenomenon has already been reported with the InP growth in other works [60, 61].

More recently, Kunert et al. [62] used a SAE approach to achieve some GaAs and GaSb nano-ridges (NRs) which come out from the cavities with tunable shapes and facets as function of the process conditions (**Figure 21a**). These type of NRs can serve as laser diodes structure as well as planar photodetectors. The nano-ridges growth is achieved in trenches where the silicon has been etched in wet solution to form a v-groove of Si-{111} planes. The defect density on the top surface of NRs was assessed in the direct space from electron channeling contrast imaging (ECCI). This latter method can be implemented more easily and with a better statistic than TEM. The graph of **Figure 21b** summarizes the TDD and planar defect density (PDD) in

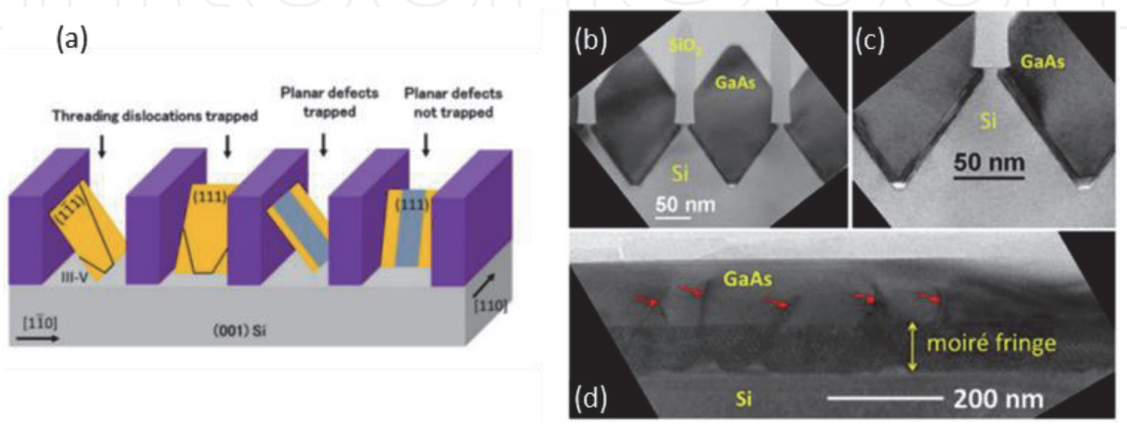

Figure 20.
(a) Principle of ART. (b) GaAs growth in V-groove shaped Si/SiO_2 trenches. (c) SFs and microtwins at Si/GaAs interface. (d) STEM cross-section along the trench. The TDs are indicated by the red arrows. The Moiré fringes are formed by the interferences between the Si et GaAs crystal at the V-groove level. From [58, 59].

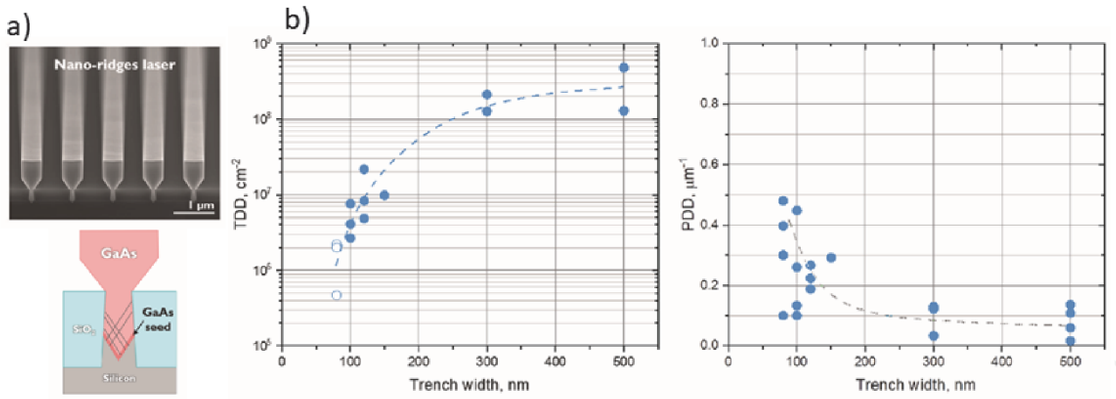

Figure 21.
(a) GaAs nano-ridges in SAE. (b) TDD and PDD as function of the trench-width. From [62].

surface of the GaAs as function of the trenches width. A remarkable achievement is the low TDD which decrease below 4.5×10^5 cm^{-2} for the very narrow trenches of 80 nm (AR 3.75). Therefore such TDD is therefore very closed to the one of a bulk GaAs substrate ($\sim10^5$ cm^{-2}). This result was observed on both GaAs and GaSb NRs. The planar defect density (essentially stacking faults) shows, however, an inverted relationship with the trench width. The PDD is indeed significantly higher in the narrow cavities. It rises from a value below 0.2 µm^{-1} in the >300 nm-wide trenches to 0.5 µm^{-1} for trenches below 100 nm-wide. The authors assume that the Shockley partial dislocation at the SF-planes ends may help to release the stress in the narrow trenches.

Furthermore, Baron et al. [63] highlighted the efficiency of the ART method for the optical emission of AlAs/InGaAs/AlAs QWs. The QWs are grown on top of a 150 nm-thick GaAs buffer layer in SiO_2 trenches with differents aspect ratio ranging from 0.2 to 1.3 (**Figure 22a**). In this work a 1.3 AR is necessary to free the GaAs buffer layer from APBs and to obtain a PL at 300 K. This way the **Figure 22b** shows the normalized µPL spectra for InGaAs QWs with different Indium content. The PL peak position measurement combined with the InGaAs layer thickness measurement by STEM (**Figure 22c**) allows for the calculation of an Indium content of 7%, 16%, 35%, 42% in the 4 samples. These values are very close to the targeted concentrations. Besides, to observe the influence of defects at the local scale, CL measurements at 15 K were performed on top of the nanoribbon arrays (**Figure 22d**). Since the layer is free of APBs, the dark zone, corresponding to non-luminescent areas, are attributed to the dislocations that are not trapped by the structure and propagating through the QWs.

This explanation of the TDs acting as luminescence quenchers was pushed further in another work [64] combining FIB-STEM, CL and strain measurement of the III-V nanoribbons by precession electron diffraction (PED) [65, 66]. The **Figure 23a**. shows a STEM cross-section of the nanoribbons with their AlAs/InGaAs QWs. The structural defects crossing the QWs are labeled from d_1 to d_5. Prior to the STEM lamella preparation CL intensity imaging (**Figure 23b**) was performed at the same location of the nanoribbon (the area is located thanks to platinum marker deposited on top of the NRs array). The authors highlighted that the luminescence is not homogenous along the NRs and the dark and bright area are bounded by two TDs indexed as d_3 and d_4 on the image. In addition, the CL peak position of the brighter area shift of about 10 nm toward the higher wavelength (**Figure 23c**). Both the intensity and the peak shifting can be spatially correlated to the 0.5% $\varepsilon_{[110]}$ strain variation starting from the d_3 dislocation and measured thanks to the PED method (**Figure 23d**).

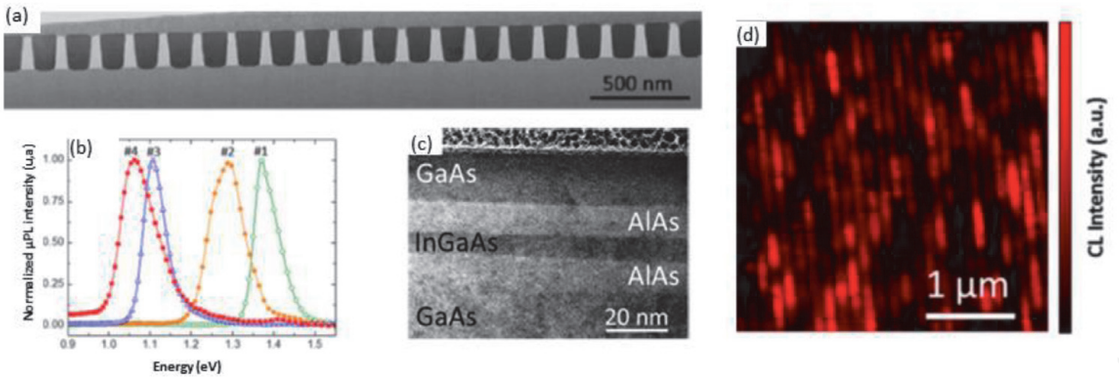

Figure 22.
(a) low magnification cross-sectional STEM image of a GaAs layer grown in 140 nm wide SiO2 trenches on (001)-oriented Si substrate showing a good uniformity of the selective growth. The trenches are oriented along the [1–10] direction and are 180 nm deep. (b) Normalized room temperature lPL spectra of different InGaAs. QWs having different composition of Indium of (#1) 10%, (#2) 20%, (#3) 30%, and (#4) 40%. (c) Cross-sectional TEM image of the top layers showing the stack of GaAs/AlAs/InGaAs/AlAs/GaAs layers with no crystalline defects. (d) 5 K panchromatic CL mapping of the nanoribbons array. From [64].

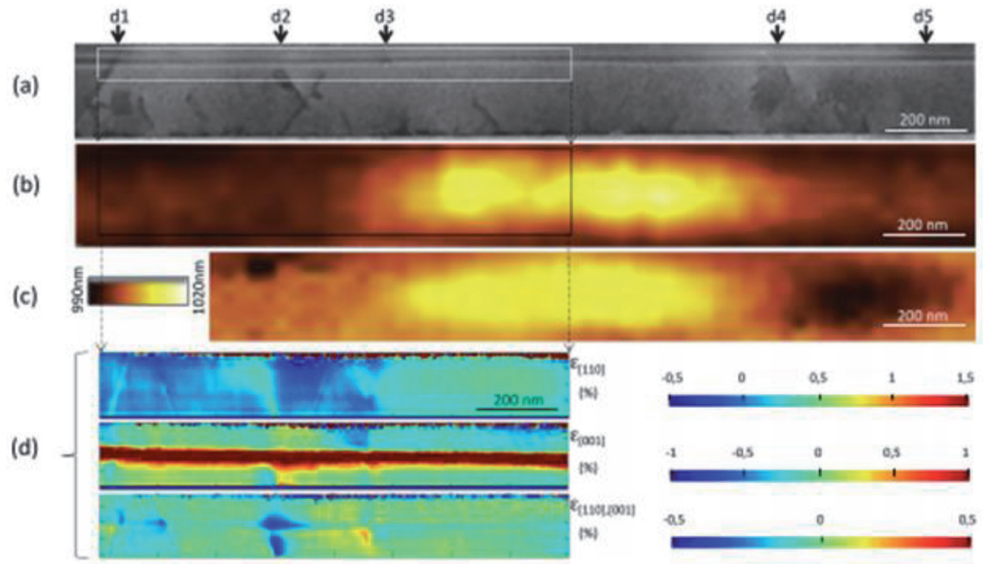

Figure 23.
Spatial correlation between mappings: (a) cross section STEM, (b) top-view CL intensity, (c) CL peak positions, and (d) cross section ε [110], ε[001], and ε [110, 001] strain distortions realized on a single III-V QWF. The high luminescent area is bounded by dislocations d3 and d4 and associated with a peak position shift toward higher wavelength. ε [110] shows a 0.5% distortion along this III-V QWF, and no significant distortion for ε[001] and ε [110, 001]. From [64].

The SAE approach entails a large number of variants, including epitaxial lateral overgrowth ELO [67] and confined epitaxial lateral overgrowth (CELO) [68]. These alternatives often use a "3D" confinement of defects. However, if they are in certain cases, very efficient, they generally require a complex and cost consuming patterning of the substrates. For an overview of the latter methods one can refer to the references [59, 69].

2.4 Summary

In the past 30 years, efforts have been made to decrease the TDs induced by the lattice mismatch between GaAs and Si. Introduction of DFL method as well as the use of Aspect Ratio trapping method allow to decrease the threading dislocation density in the 10^5–10^6 cm^{-2} range, value required to obtain efficient devices.

3. Part 3: realization of InAs QDs/GaAs laser emitter on APB-free GaAs/Si platform

3.1 The Development of QD laser on Si

The advantages of high data rate, broad bandwidth, mature fabrication processes and low power consumption make Si photonics become a desirable approach, meeting the future demands of optical interconnections. To date, significant achievements have been made in Si photonics and most of key components have been well demonstrated, including low-loss waveguides, high-speed modulators and high-performance photodetectors [70–74]. However, the realization of high-performance Si-based on-chip light sources still remains challenging for the full integration of optoelectronics integrated circuits [75]. Among various of approaches, monolithically integrating high-performance III-V QD lasers on Si substrate has been considered as a promising method to develop an on-chip optical source for Si photonics [76–78]. The advanced properties of low threshold, high defects tolerance and high temperature stability contribute largely to the development of QD lasers [27, 79–81].

Before illustrating the recent progress of QD lasers grown on Si (001) substrates, it is worth to discuss briefly about some key milestones in the development of monolithic integration of III-V lasers on Si. Although some optimized heteroepitaxy techniques have reduced the TDD of III-V on Si from originally $\sim 10^9$ cm^{-2} to $\sim 10^6$ cm^{-2}, QW lasers directly grown on Si still suffered on their high threshold and limited lifetime due to the enhanced TD generation [82–85]. An early result presented a QW laser with InP buffer as thick as 15 μm with decent performance and lifetime [86]. However, due to the difference of thermal expansion coefficient between III-V epi-layer and Si substrate, the thick buffer is also vulnerable to the formation of micro-cracks, which destroys the yield of Si-based devices [87]. The research of III-V QD lasers on Si (001) comes out since early 2000s. After the early attempt by using droplet epitaxy to grow QD lasers, the successful address of Stranski-Krastanov growth mode on the growth of QDs presents significant advantages on emitting light with the presence of high TDD caused by mismatch in lattice constants and thermal expansion coefficients [88, 89]. By taking the benefits of ultra-high vacuum and precise control, MBE system has been widely considered as a suitable technique for the growth of high-performance QDs.

Recently, numerous achievements that pursuing high performance III-V QD lasers on Si have been demonstrated. The offcut Si substrate was addressed initially to prevent the formation of APB. In 2001, the first QD laser on Si emitting at 855 nm at room temperature under continuous-wave operation was presented by growing InGaAs QDs on Si substrate with MOCVD [90]. More importantly, the aging test illustrated the advantage of reliability for QD lasers on Si compared with QW counterparts. By further optimizing the active region and III-V buffer, such as utilizing DFLs and P-type modulation doped QD region, the performance of QD lasers on Si was highly improved, realizing a characteristic temperature (T_0) of 244 K between operation temperature of 25–95°C and a reduced threshold current density of 900A/cm^2 at that time [48, 91]. These results suggest the possibility of QD lasers directly grown on Si substrate as an efficient and reliable light source for Si photonics.

The aforementioned works of QD lasers were all operated under emission of 1.1 μm. However, the recent ever-growing demands on telecommunication and data-communication system, led to significant achievements on 1.3 μm InAs/GaAs QD lasers on Si substrate. The first room temperature 1.3 μm emission of QDs on Si grown by MOCVD was achieved by Li et al. at 2008, with the help of Sb [92].

However, due to the high TDD in the GaAs buffer, its PL intensity was eight times weaker than QDs grown on the native GaAs substrate, even with a high QD density obtained of 7×10^{10} cm^{-2}. This also suggested the importance of developing improved GaAs buffer on Si substrate associated with well-performed DFLs. The first electrically pumped 1.3 μm InAs/GaAs QD laser directly grown on Si substrate by MBE was successfully demonstrated by Wang et al. in 2011 [93]. The laser structure was grown on an offcut Si substrate with 4° miscut angle to [110] orientation. An improvement initialized from the growth of AlAs nucleation layer instead of GaAs nucleation layer, realizing a reduction of defects observed at the interface of AlAs/Si [94]. The threshold current density was reduced to 725A/cm^2 at room temperature under pulsed operation, with a single facet output power of ~26 mW achieved at room temperature. The highest operation temperature was 42°C with a T_0 of 44 K.

Extensive studies were devoted following the first demonstration of electrically pumped 1.3 μm QD laser on Si. In 2012, by utilizing Ge-on-Si virtual substrate, the first room-temperature continuous-wave electrically pumped InAs/GaAs QD laser monolithically grown on Si substrate with a Ge buffer layer was demonstrated by MBE [95]. A low threshold current density of 162 A/cm^2 was achieved at continuous-wave mode with a room temperature lasing emission of 1.28 μm. The operation temperature was as high as 84°C under pulsed mode. Although these results were outstanding, a 1.3 μm InAs/GaAs QD laser directly grown on Si substrate was still far from practice, until the successful demonstration by us in 2016. By applying unique epitaxial method and improved fabrication process, the first high-performance and long-lifetime 1.3 μm QD laser directly grown on Si was achieved [29]. As shown in **Figure 24a, 1** μm GaAs buffer was grown by three steps on a deoxidized Si substrate to improve the material quality, followed by four sets of DFLs consisted of five sets of InGaAs/GaAs SLSs and high temperature annealed

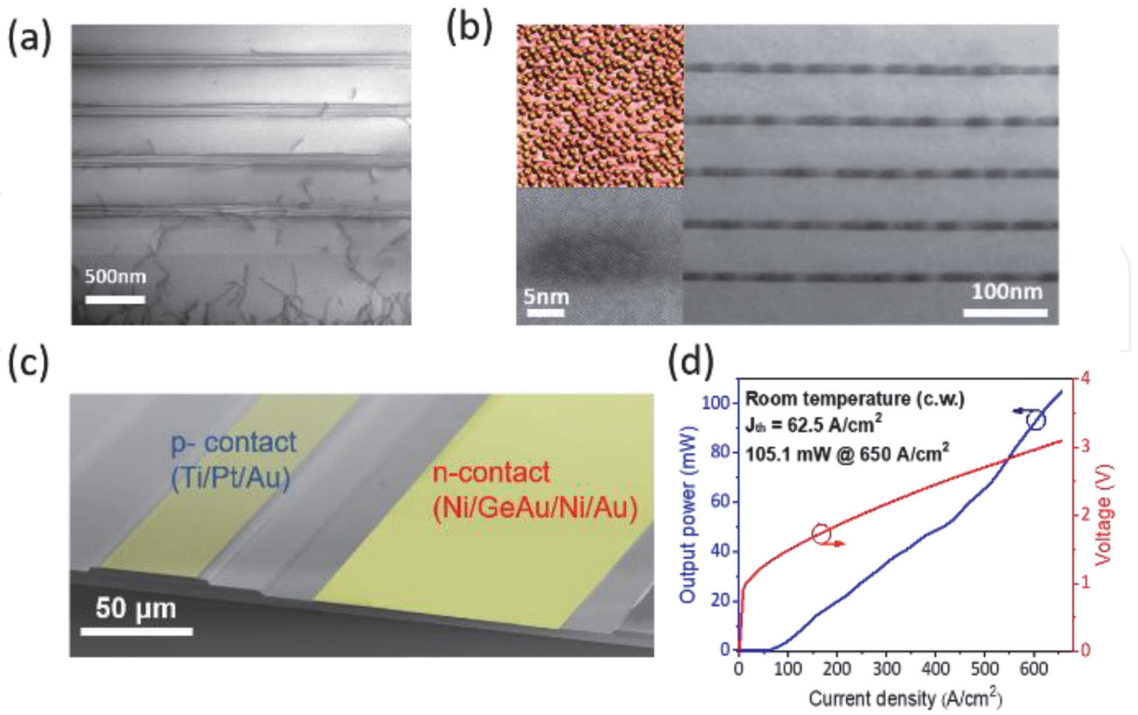

Figure 24.
(a) TEM image of GaAs buffer on Si including dislocation filter layers. (b) TEM image of active region, upper inset: 1 × 1 μm² AFM image of uncapped QDs, and bottom inset: TEM image of a single QD. (c) SEM image of fabricated broad-area laser. (d) Light-current–voltage curve of lasing characteristics under continuous-wave condition at room temperature. Reproduce from [29].

300 nm GaAs spacer layer. The TDD after DFLs was successfully reduced to the level of 10^5 cm^{-2}. High-performance laser structure with five stacks of InAs/GaAs DWELL active region was developed upon this platform. A TEM image of active region was shown in **Figure 24b** where QDs were coherently grown, without any visible defects. The two inset images presented a 1×1 μm^2 AFM image which show a good uniformity with 3×10^{10} cm^{-2} dot density and the typical shape of a single QD. Broad-area lasers were fabricated as shown schematically by a scanning electron microscope (SEM) image in **Figure 24c**. The light-current–voltage curve of the device was shown in **Figure 24d**. An ultra-low threshold current density of 62.5 A/cm^2 under continuous wave at room temperature was obtained, which was the lowest threshold current density value achieved for any kind of lasers on Si substrate at that time. The single facet output power measured under injection current density of 650 A/cm^2 was exceeded 105 mW. The highest operation can be achieved up to 75°C under continuous-wave mode and 120°C under pulsed mode. Moreover, negligible degradation was observed after 3100 h aging test, realizing an extraordinaire mean time to failure lifetime more than 100,158 h. After that, Si-based monolithically integrated narrow-ridge Fabry-Perot and distributed feedback QDs laser are fabricated based on these outstanding outcome [96, 97].

3.2 InAs/GaAs QD laser on on-axis Si (001) substrate

These previous discussions on QD lasers were all fabricated on offcut Si substrate, which are not fully compatible to the CMOS technique. The commercialized on-axis Si (001) platform demands an miscut angle less than 0.5°. As discussed in the first section of this chapter, the heteroepitaxy technique on on-axis Si (001) was satisfied by forming APB-free GaAs buffer. Beyond the successful demonstration of QD lasers on offcut Si platform, QD lasers grown on CMOS-compatible Si (001) substrate were successfully developed in recent years [98–105], owing to the demonstration of the APB-free GaAs and GaP templates on Si.

The first electrically pumped continuous-wave InAs/GaAs QD laser monolithically grown on-axis GaAs/Si (001) substrate was demonstrated in 2017 [98]. Following by a 400 nm APB-free on-axis GaAs/Si (001) platform grown by MOCVD, MBE system was employed to grow QD laser structure with four repeats of DFLs, which consist of five sets of InGaAs/GaAs SLSs. The five stacks of InAs/GaAs QD layers sandwiched by AlGaAs cladding layers were grown subsequently. A 1×1 μm^2 AFM image of uncapped InAs QD on Si (001) substrate was shown in **Figure 25a**, realizing a good uniformity and a dot density of $\sim 3.5 \times 10^{10}$ cm^{-2}. The sample was fabricated to broad-area laser devices with as-cleaved facets for laser characteristic measurements. A comparison of room-temperature continuous-wave light-current–voltage characteristics between QD laser on on-axis GaAs/Si (001) platform and native GaAs substrate was shown in **Figure 25b**. The GaAs-based QD laser presented a threshold current density of 210 A/cm^2, while that of on-axis Si-based QD laser was 425 A/cm^2. The calculated slope-efficiency and differential quantum efficiency of GaAs-based QD laser were $\sim$ 0.12 W/A and 12.7%, respectively. The QD laser on on-axis Si (001) also show decent results on corresponding characteristics, which the calculated slope-efficiency was 0.068 W/A and differential quantum efficiency was 7.2%. **Figure 25c** presents a temperature dependent light-current curve of Si-based QD laser operated under continuous-wave mode. The maximum operating temperature achieved was 36°C. As shown in **Figure 25d**, the pulsed results of light-current characteristic at various heatsink temperature presented a highest operation temperature of 102°C, which was the first demonstration of QD laser directly grown on on-axis Si (001) substrate that observed lasing over 100°C. The inset image of **Figure 25d** shows the characteristic

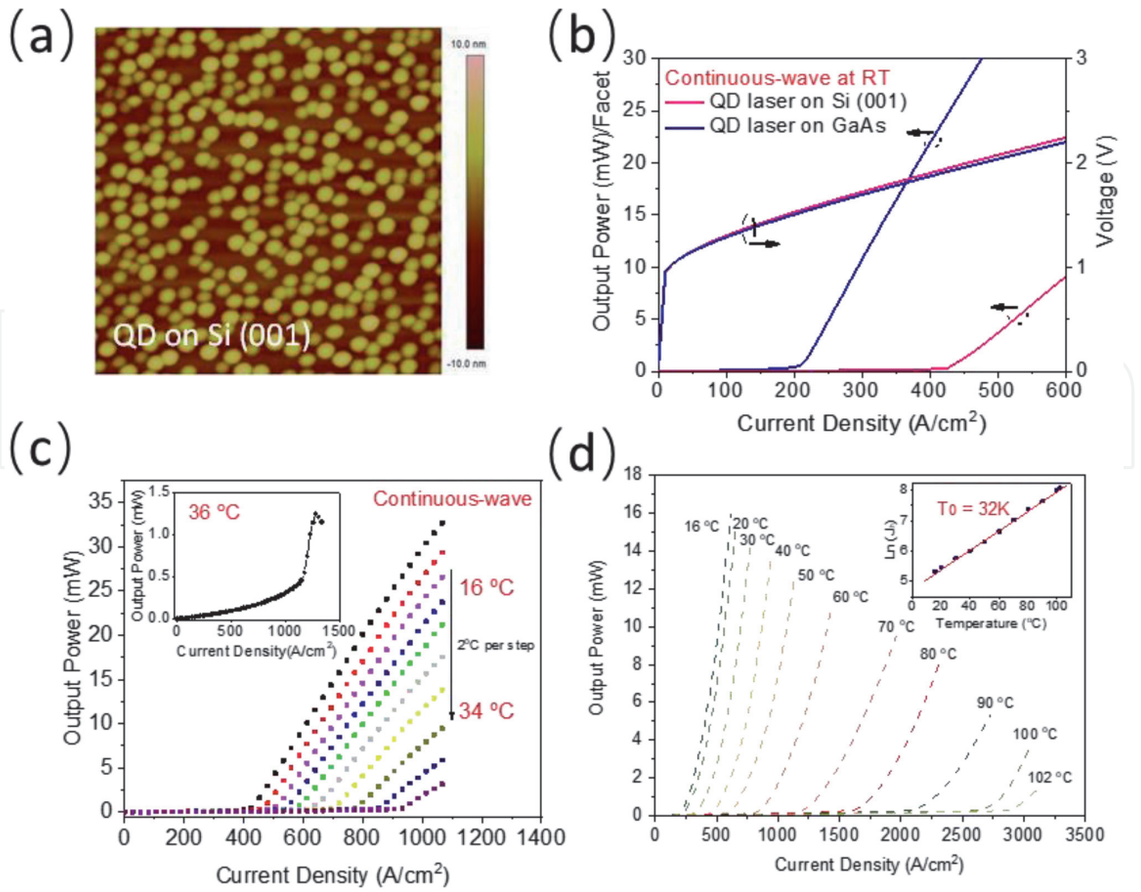

Figure 25.
(a) 1 × 1 μm² AFM image of uncapped InAs QDs grown on on-axis Si (001) substrate. (b) Light-current–voltage characteristic comparison of an InAs/GaAs QD laser grown on on-axis Si (001) and native GaAs substrate at room temperature under continuous-wave operation. (c) Single facet light-current curve for InAs/GaAs QD laser on on-axis Si (001) as a function of temperature under continuous-wave operation, inset: light-current curve at a heat sink temperature of 36°C. (d) Single facet light-current curve for InAs/GaAs QD laser grown on on-axis Si (001) substrate at different heat sink temperatures under pulsed condition, inset: natural logarithm of threshold current density against temperature in the ranges of 16–102°C. Reproduce from [98].

temperature T_0 of 32 K between 16–102°C. This result is further improved by K. Li et al. with an optimized DFLs and QDs [99].

As shown in **Figure 26a**, four repeats of $In_{0.18}Ga_{0.82}As$/GaAs SLSs DFLs were well performed to annihilate TDs with total buffer thickness of ~2 μm. The active region of laser was consisted of five repeats of InAs/GaAs DWELL structure, realizing a room temperature peak PL emission of ~1308 nm with a linewidth of ~32 meV. A comparison of room temperature PL results of InAs/GaAs QD on

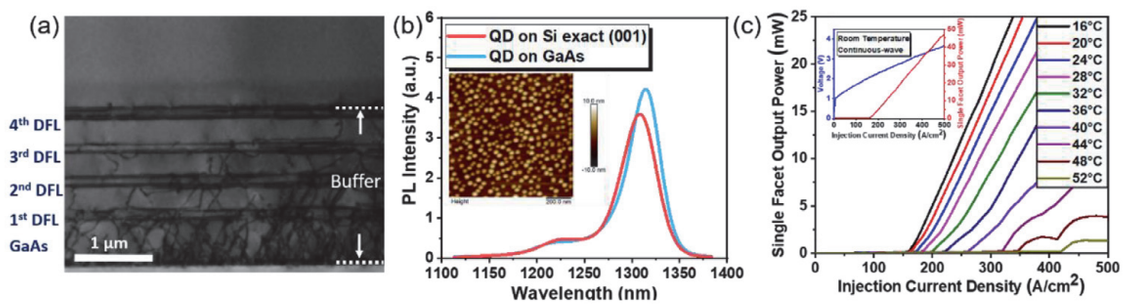

Figure 26.
(a) Cross-sectional TEM image for whole buffer; (b) A comparison of room temperature PL results, inset: an AFM image of uncapped InAs/GaAs QD layer; (c) Light-current characteristics of InAs/GaAs QD laser grown on Si exact (001) at various operation temperature, inset: light-current–voltage characteristic at room temperature. Reproduce from [99].

on-axis Si (001) and native GaAs substrates was shown in **Figure 26b**, the inset image shows an AFM image of uncapped InAs/GaAs QD layer with about $\sim 4 \times 10^{10}$ cm^{-2} dot density. The laser samples were fabricated into 50 μm × 3 mm broad-area laser devices. The characterization of laser devices was all measured under continuous wave. As shown in the inset image of **Figure 26c**, the threshold current density as low as ~160 A/cm^2 has been achieved at room temperature, which was improved compare to previous result. A single facet output power of 48 mW was obtained at an injection current density of 500 A/cm^2 without any thermal rollover. The threshold current density increased with the rising of operation temperature and laser operation was observed up to 52°C. The T_0 obtained was ~60.8 K between 16–36°C.

In order to investigate the defect tolerance of QD and QW structure, an InAs/GaAs QD laser directly grown on on-axis GaAs/Si (001) platform and an InGaAs QW laser in the same structure except active region were grown for comparison [100]. By further analyzing the performance of QD and QW laser and their thermal activation energy (E_a), the great characteristics of QD laser on dislocation tolerance and thermal reliability have been proved.

Temperature dependent PL measurements were performed for both QD and QW samples. As shown in **Figure 27a**, PL intensity of the QD sample at room-temperature was about six times lower than the PL intensity at 20 K. In contrast, the difference for the QW sample shown in **Figure 27b** was ~1000 times between 20 K and room temperature. Moreover, the integrated PL intensity for both samples was measured in order to estimate their E_a. The results were shown in **Figure 27c**, which were 240 meV and 35 meV for QD and QW lasers, respectively. The significantly higher E_a observed for the QD could contribute to its higher optical intensity at high temperatures. As shown in **Figure 28a, 25** μm × 3 mm broad-area lasers were fabricated for both QD and QW samples. The room-temperature characteristics of them under continuous-wave mode were illustrated in **Figure 28b**. The threshold current density of ~173 A/cm^2 for QD laser was achieved. In addition, over 100 mW single-facet output power was obtained under injection current density of 670 A/cm^2. In contrast, there was no lasing observed for the QW device at room-temperature even at higher injection levels. After comparing with modelling results, this study indicated that QW laser cannot work properly above 10^7 cm^{-2} of TDD [100, 101]. **Figure 28c** presented a temperature dependent light-current curve of QD laser on Si (001). The highest continuous-wave operation was observed over 65°C. These results quantitively suggested that QD laser had its natural advantages on defect tolerance and temperature insensitivity. It also demonstrated that QD laser monolithically integrated on on-axis Si (001) substrate can be a promising on-chip optical source for Si photonics.

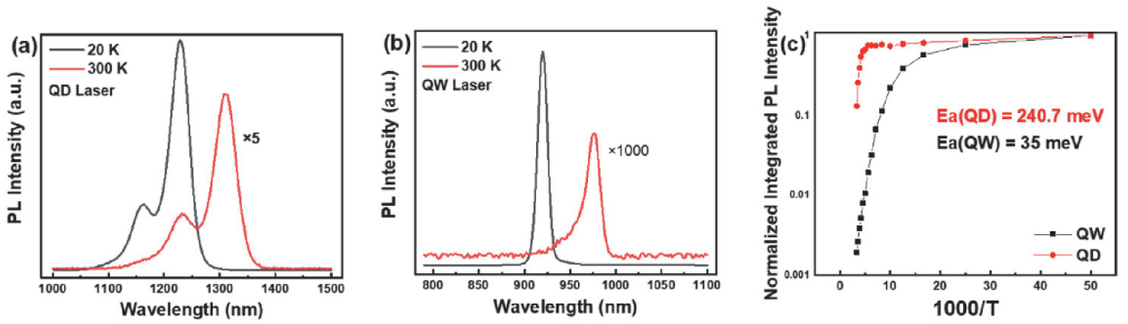

Figure 27.
Comparison of PL spectra at room-temperature (300 K) and 20 K for (a) the QD laser, and (b) the QW laser. (c) Temperature-dependent integrated PL intensities of the InAs QD and InGaAs QW lasers from the temperature region of 20 K to 300 K, showing Ea of both samples. Reproduce from [100].

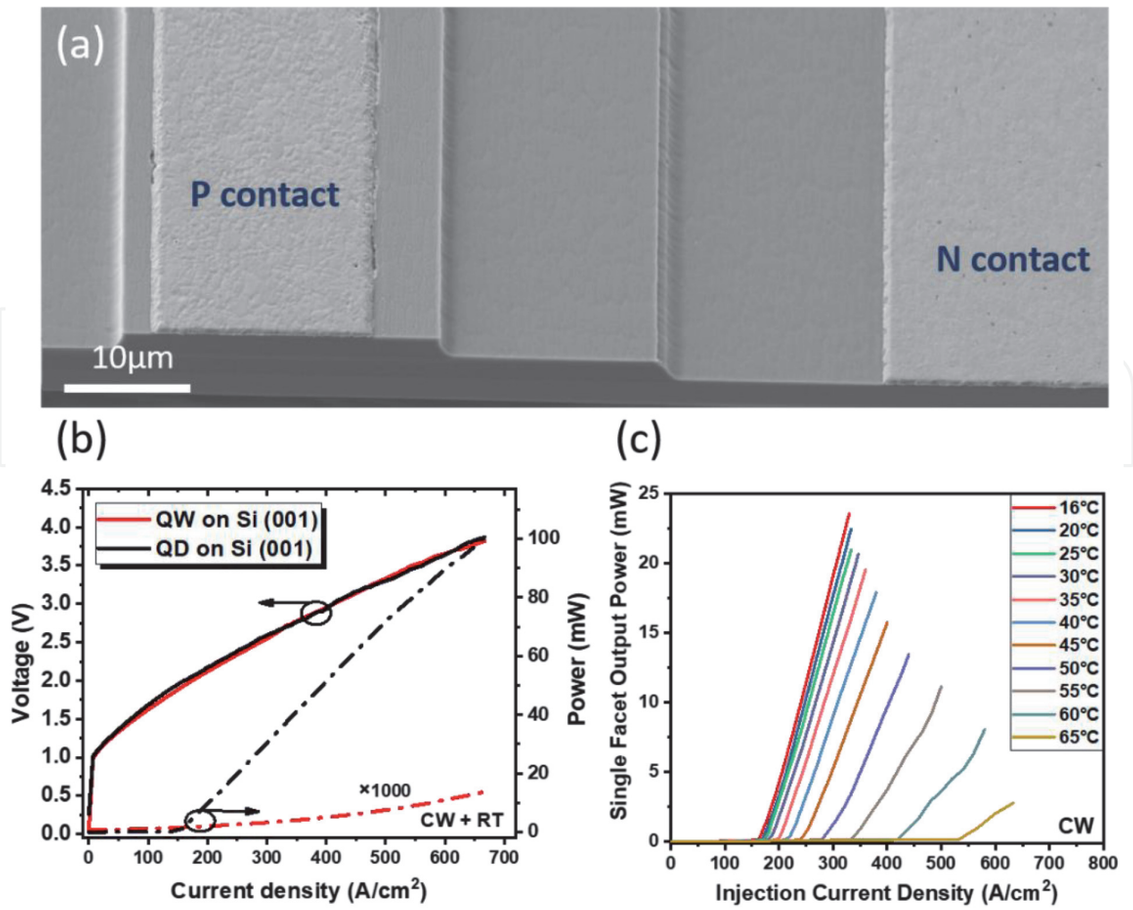

Figure 28.
(a) SEM image of an example of broad area laser fabricated by QD and QW samples with 25 μm ridge width and 3 mm cavity length. (b) Comparison of room-temperature light-current–voltage characteristics for QD and QW lasers directly grown on on-axis Si (001) substrate. (c) Temperature-dependent light-current measurement of the QD laser under continuous-wave mode. Reproduce from [100].

3.3 Microdisk QD laser grown on on-axis Si (001) substrate

Despite the outstanding progress has been made on edge-emitting QD lasers on on-axis GaAs/Si (001) substrate. For the dense integration with light source on Si that compatible to CMOS technique, microdisk lasers with small footprint has been considered as a promising approach for realizing nanophotonic integrated circuits. Additionally, compared with Fabry-Perot laser cavity, microdisk lasers also benefit from their advantages on low threshold and high quality factor which could bring less optical loss [106]. Recently, by applying the well-performed on-axis GaAs/Si (001) platform and optimized DFLs, a monolithically grown InAs/GaAs QD microdisk laser on on-axis Si (001) substrate with ultra-low threshold at room temperature was successfully demonstrated [107]. The device was optically pumped under continuous-wave mode. **Figure 29a** presented a schematic structure of this fabricated microdisk laser where the top of disk was the active region that consisted of three stacks of InAs/GaAs DWELL layers separated by 50 nm of GaAs space layer and 69 nm of AlGaAs cladding layer. A typical fabricated microdisk laser with disk diameter of 1.9 μm was shown in the SEM image of **Figure 29b**, which indicated a smooth etched surface with 73.5° sidewall tilt. The cross-sectional TEM image in **Figure 29c** shows the whole epilayer structure on on-axis GaAs/Si (001) substrate.

The collected lasing spectra for the microdisk laser with 1.9 μm diameter was illustrated in **Figure 30a**. The results presented a free spectral range of 76 nm –

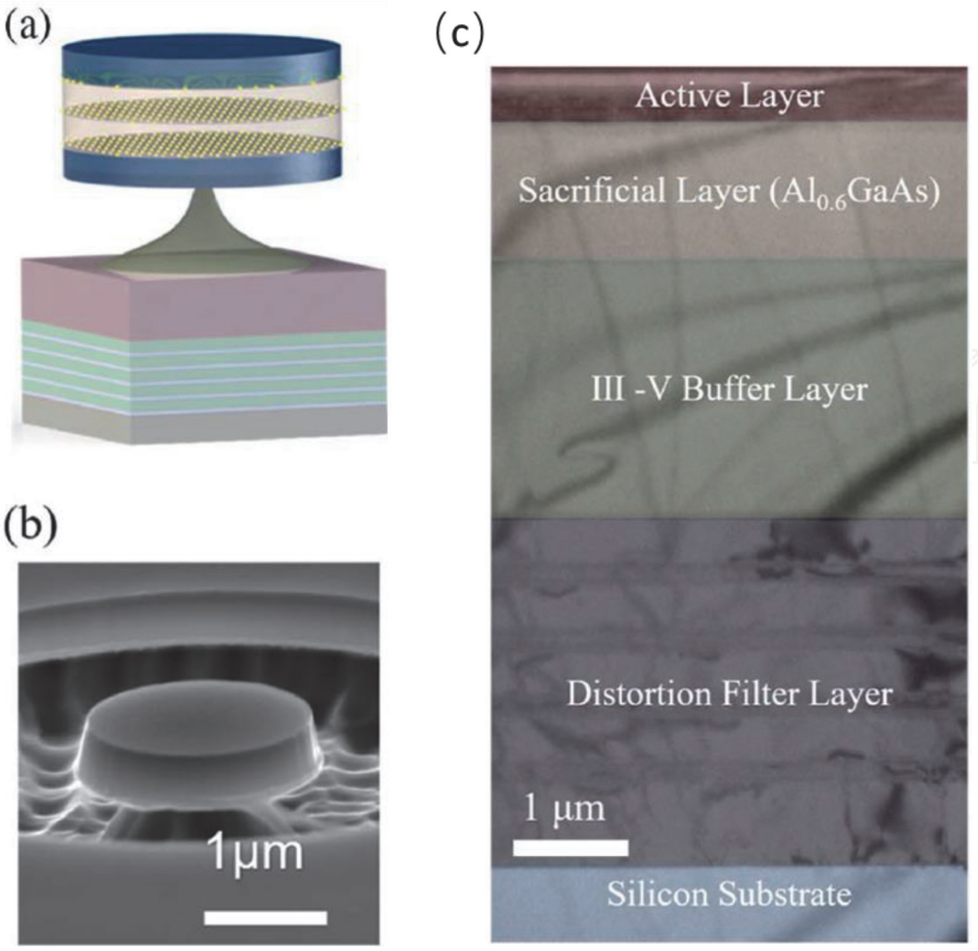

Figure 29.
(a) Schematic diagram of a QD microdisk laser fabricated on on-axis Si (001) substrate. (b) SEM image of a QD microdisk laser with 1.9 μm diameter. (c) Cross section TEM image of the epitaxial structure of QD microdisk laser on on-axis Si (001) substrate. Reproduce from [107].

89 nm between adjacent whispering gallery modes. Both ground state and excited state emission were observed. A main peak wavelength of 1263 nm was located at the first excited state. **Figure 30b** shows the collected intensity and linewidth as a function of input optical power for the corresponding peak emission at 1263 nm. An ultra-low threshold of 2.6 ± 0.4 μW and a clear narrowing trend of FWHM was obtained. The threshold of this result was even lower than the InAs QD microdisk lasers on native GaAs and InP substrates [109–111]. Additionally, the sample was fabricated into microdisk lasers with variable diameter from 1 μm to 2 μm. The corresponding threshold of main peak of microdisk lasers were presented as a function of diameter in **Figure 30c**. All the results of threshold were below 3.5 μW. The fluctuation of threshold versus the diameter of microdisk may result from the slight factor difference in fabrication process.

3.4 Continuous-wave QD photonic crystal lasers on on-axis Si (001)

As a promising ultra-compact on-chip light source, III-V photonic crystal lasers on Si benefits on their ultralow power consumption and small footprint. Most recently, Zhou et al. demonstrated an optically pumped InAs QD photonic crystal laser on on-axis GaAs/Si (001) substrate, which was the first monolithic integration of photonic crystal laser emitting at 1.3 μm on CMOS-compatible Si (001) substrate [108].
A single mode operation with ultra-low threshold down to ~0.6 μm and a large

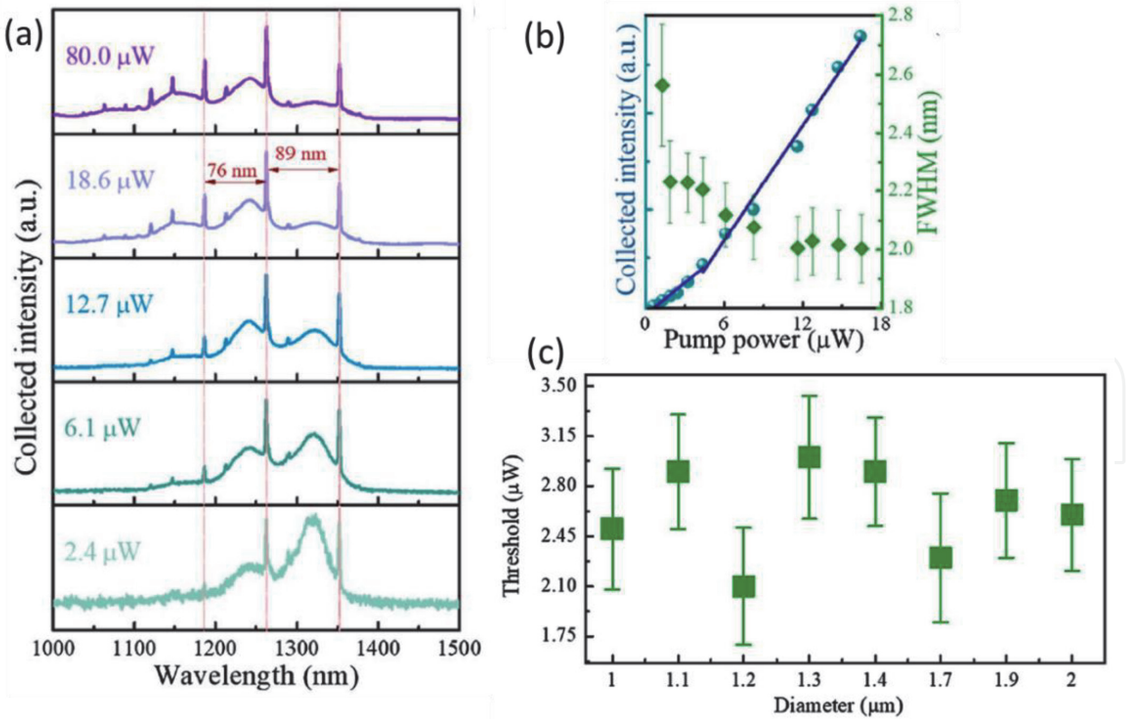

Figure 30.
(a) Collected intensity as a function of wavelength with different pumped power below and above the threshold of QD microdisk laser on on-axis Si (001). (b) The corresponding collected intensity and linewidth versus pumped power for the first excited state emission at 1263 nm. (c) Threshold of main lasing peak of QD microdisk laser as a function of various diameter. Reproduce from [108].

coupling efficiency for room temperature spontaneous emission under continuous-wave condition were achieved. 3D finite-difference time- domain (FDTD) simulation method was applied in order to obtain a high-quality factor for the resonance among QDs emission spectrum. **Figure 31a** shows a schematic structure of fabricated photonic crystal laser with 1 μm thickness of air slab underneath the cavity to enhance the vertical light confinement. The structure of active region that consists of four repeats of InAs/InGaAs/GaAs DWELL layers sandwiched by 50 nm GaAs space layers and 40 nm AlGaAs cladding layers was shown in **Figure 31b**. The collected intensity and linewidth of photonic crystal laser as a function of input power were shown in **Figure 31c**. The optically pumped QD photonic crystal lasers exhibited single-mode operation with an ultra-low threshold of ~0.6 μW. The inset image shows a peak wavelength at ~1306 nm with different pumped power. The Lorentzian fitting curve indicated a linewidth of ~0.68 nm and a calculated cavity quality factor of 2177. The soft turn on process shown in **Figure 31c** also presented a typical behavior of laser with high spontaneous emission coupling efficiency (β). The logarithmic plot of light–light curve with fitting results of this QD photonic crystal laser were shown in **Figure 31d**. It indicated the best fitting data obtained at $\beta = 0.18$, realizing a large spontaneous emission coupling efficiency under continuous-wave condition at room temperature.

3.5 Summary

QD laser on Si has attracted great research interests in recent years, which brings new approach for achieving efficient light source of Si-based photonics integration. These works discussed in this section with established epitaxy technique of APB-free on-axis GaAs/Si (001) platform, effective DFLs and optimized QD layers demonstrate that high-performance QD laser monolithically integrated on on-axis

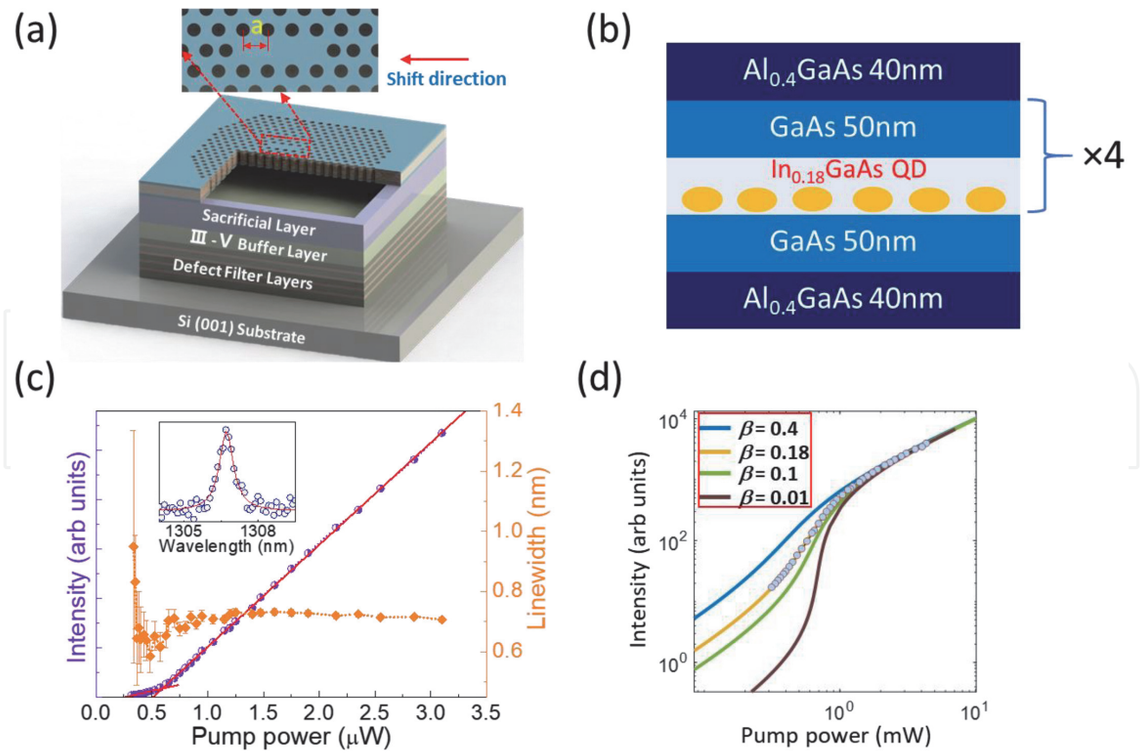

Figure 31.
(a) Schematic structure of QD photonic crystal laser on on-axis Si (001). (b) A diagram of active region in our photonic crystal laser. (c) Collected light–light curve and linewidth of the lasing peak at 1306 nm, inset: Lorentzian fitting of data below the threshold. (d) Logarithmic light–light plot of fitted and collected data. Reproduce from Ref. [108].

Si (001) substrate can be a promising on-chip optical source for Si photonics. Different approaches also provide new routes to form the basis of future monolithic light sources for the application of optical interconnects in large-scale silicon optoelectronics integrated circuits.

4. Conclusions

Heterogeneous integration of III–V compound semiconductors is promising to realize functionalities such as laser sources and photodetectors, and silicon based waveguides on Si platform. The direct heteroepitaxy of GaAs on nominal Si(100) wafers used by the microelectronics industry faces several issues to produce high quality material. In this chapter, we discussed the recent advances to tackle the formation of antiphase domains and to reduce the threading dislocation density. Currently, APB is no more an issue, as solutions have been proposed to obtain thin (<400 nm) GaAs film without APB, solutions based on dedicated cleaning and annealing processes of Si substrate before the GaAs epitaxy. The threading dislocations have hindered the development of GaAs devices on a Si CMOS platform and many solutions have been studied in th epast. We have reviewed the most efficient methods that used interchangeably the insertion of a Ge buffer between silicon and GaAs, the insertion of dislocation filter layers in the GaAs, or selective epitaxy in a cavity with a proper aspect ratio. All these progresses allowed reaching the range of 10^6–10^5 cm^{-2} TDD required to elaborate performant optoelectronics devices. Next we developed the fabrication of InAs QDs/GaAs laser emitters in the infrared region integrating GaAs buffer without APB grown on nominal Si(100) wafers and DFL to reduce the TDD. Different type of devices were fabricated such as broad area laser

electrically pumped and operating at room temperature and up to 65°C, microdisk QDs lasers and continuous-wave QD photonic crystal lasers.

This paves the way towards the monolithic integration of optoelectronics and microelectronics functionalities on the same silicon CMOS platform, promising tremendous evolution in the data treatment and computing fields.

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