Chapter

RF MEMS Switch Fabrication and Packaging

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Abstract

RF (Radio Frequency) MEMS (Micro Electro Mechanical Systems) technology is the application of micromachined mechanical structures, controlled by electrical signals and interacting with signals in the RF range. The applications of these devices range from switching networks for satellite communication systems to high performance resonators and tuners. RF MEMS switches are the first and foremost MEMS devices designed for RF technology. A specialized method for fabricating microsturctures called surface micromachining process is used for fabricating the RF MEMS switches. Die level packaging using available surface mount style RF packages. The packaging process involved the design of RF feed throughs on the Alumina substrates to the die attachment, wire bonding and hermetic sealing using low temperature processes.

Keywords: RF MEMS switches, surface micromachining, low temperature packaging

1. Introduction

Due to the reduced size, cost and low power consumption as well as very high precision, MEMS applications have extended from mere pressure and temperature sensors to vast array of applications viz., Aerospace, Automobile, Biotechnology, Consumer products, Defense and the most important and pertinent Telecommunications [1]. Hence RF MEMS devices have the advantage of increased functionality, substantial performance improvements, high agility, modularity and reconfigurability [2]. These devices are applicable to high performance communication systems such as satellite communication and m applications [3].

RF MEMS switches are the first and foremost MEMS devices designed for RF technology. RF MEMS switches compared to their semiconductor counterparts such as FET and PIN diodes show far superior performance. The current–voltage non-linearity that is the bane of semiconductor devices is non-existent in the case of RF MEMS switches. The power consumed by these switches is far less since most of the switches using electrostatic and piezoelectric actuation require negligible power requirements. They are also not plagued by issues of harmonics and intermodulation of signals. They exhibit very low insertion loss in the range − 0.05 to −0.2 dB at a frequency of 40 GHz. They also possess very high isolation in the range of −40 dB at 40 GHz [4, 5]. The only drawback is that their switching speed is far inferior compared to their semiconductor counterparts. However, there are several high performance communication circuits such as in defense and satellite systems where speed may not be the criteria whereas low power consumption and high RF

performance would be the key features required. Due to these features they improve the overall performance of the systems into which they are integrated. Hence, the focus of this work is on RF MEMS switches which are a superior alternative to existing semiconductor switches.

MEMS devices are fabricated by the use of special techniques called micromachining. Micro fabrication or micromachining or micro manufacturing is the use of a set of manufacturing tools based on thin and thick film fabrication techniques commonly used in the electronics industry. It is also a technology for creating small three dimensional structures with dimensions ranging from sub centimeters to sub micrometers. A vast majority of MEMS structures are fabricated using bulk micromachining process. This involves etching of bulk wafer leading to three dimensional structures such as beams, cantilevers and cavities. These processes can be realized on substrates such as Silicon, Glass and Gallium Arsenide etc. The thickness of the structures can range from a few micrometers to 200 mm. The resulting dimensions of microstructures are much larger compared to surface micromachining process. Surface micromachining is a process based on building up of material layers and then selectively retaining or etching by continued processing. The bulk of the substrate remains untouched. LIGA processes combine IC lithography and electroplating and molding to obtain depth. Patterns are created in a substrate and then electroplated to create 3D molds. These molds can be used as the final product, or various materials can be injected into them. This process has two advantages. Materials other than Silicon can be used e.g. metal, plastic and devices with very high aspect ratios can be built [6].

This chapter provides the complete details of the unit step processes used for the fabrication and packaging of RF MEMS switches. The focus is on fabrication of low actuation voltage RF MEMS switches [7–10]. There are several challenges involved in the fabrication of MEMS switches such as, structural deformation, residual stress, non-release of structural layer to name a few. These challenges are overcome and addressed throughout the fabrication process by optimization of several unit processes. The unit processes used is discussed in each section of this chapter.

1.1 Fabrication process steps

Surface micromachining process is used for fabricating the switches. In the present work, fabrication costs were brought down by

- low resistivity Silicon wafers as substrate
- Use of only four masks for fabrication [11]

The sections below give the detailed description of the fabrication steps followed for successful fabrication of RF MEMS shunt switches.

The test wafers used in this work is P-type {100} low resistivity 4″ wafers with resistance ranging from 1 to 100 Ω. Using low resistivity wafers to fabricate RF MEMS switches has the advantage that integration with CMOS circuits is easier. However, use of low resistivity Silicon wafer leads to higher insertion loss due to inherent parasitics.

The following are the process steps used for fabrication:

i. Cleaning of test wafer: Using RCA-1 and RCA-2 processes.

ii. Oxidation of the test wafer: Using wet oxide process

iii. CPW metal layer patterning: Using sputtering and lithography steps

iv. Dielectric deposition and layer patterning: Using PECVD for Silicon Nitride depostion followed by lithography steps.

v. Sacrificial layer deposition and patterning: Using Photoresists and lithography steps

vi. Top layer deposition and patterning: Using sputtering and lithography steps.

vii. Top layer release: Using Critical point dryer.

Figure 1 gives pictorial representation of the process steps followed for fabrication of the RF MEMS shunt switches.

1.1.1 Cleaning of test wafer

The cleaning of the Silicon wafer is the first process employed to removing any organic residue or films on the Silicon wafers. The cleaning process is performed in two parts [12]. The first part of the cleaning process is the famous RCA-1 named after the laboratory at which it was developed. In this process five parts of water is mixed with one part of Ammonium Hydroxide (NH_4OH) and one part of Hydrogen Peroxide (H_2O_2). This mixture is then heated to 75°C on a hot plate. Once the solution bubbles vigorously the Silicon wafer is soaked in this solution for 15 minutes. The wafer is then dipped in a solution made of one part of Hydrofluoric acid (HF) and 50 parts of water for 30 seconds. This solution serves the purpose of etching out the thin oxide layer developed on the wafer. The wafer is again washed with DI water. The next step also called RCA-2 involves the use of Hydrochloric (HCl) acid, Hydrogen Peroxide (H_2O_2) and DI water in the ratio of 1:1:6. This solution is then heated to a temperature of 75°C for 15 minutes after which the Silicon wafer is placed in this solution. RCA-2 completely removes the traced of ionic contaminants from the wafer surface.

1.1.2 Oxidation of test wafer

The oxidation of Silicon wafer leads to the formation of a layer of native oxide i.e., Silicon Dioxide on the wafer surface. It is seen that only Silicon material has the

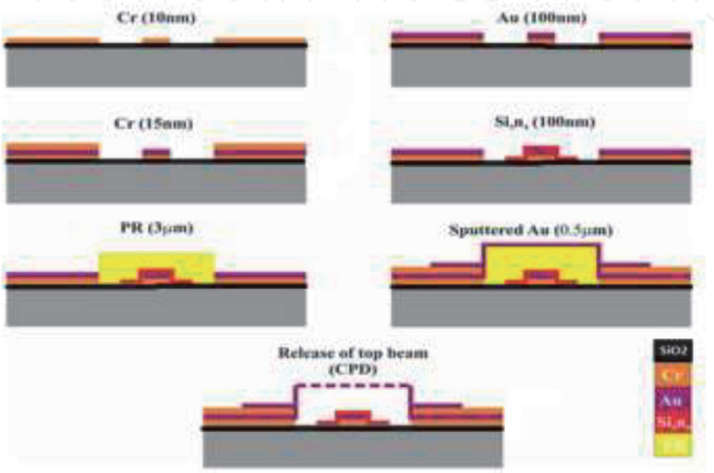


Figure 1.
Steps involved in fabrication of capacitive shunt switches.

ability to form a native oxide which has led to its wide usage in the IC industry. This layer serves a number of purposes. It acts as a surface passivation layer by protecting the surface from moisture and other atmospheric contaminants.

The main aim of using Silicon dioxide for RF MEMS switches is for the need for isolation and insulation from the low resistivity silicon wafer used as the substrate. By using Silicon Dioxide it is seen that the parasitics between the Co-Planar Waveguide (CPW) layer and the silicon substrate underneath are drastically reduced. This approach leads the application of silicon substrate for RF circuits and wireless communication systems [13–16]. The formation of oxide layer in this work is through the wet oxidation process since the requirement is only for passivation.

The wafer was placed in a Nano pyrogenic furnace as shown in **Figure 2** to obtain a Silicon Dioxide layer of 1 μm thickness. The following steps were followed to oxidize the wafers. The time required for the Silicon Dioxide thickness of 1 μm was calculated to be approximately 4 hours, 30 minutes.

1. The furnace temperature is ramped to 500°C with Nitrogen gas flow at 5 liters/min. The furnace temperature is then raised to a temperature of 1100°C. This process of heating up takes 1–2 hours.

2. Once the set point temperature is reached, the wafers are put into a Quartz boat and loaded into the tube utilizing a furnace loader.

3. During the heating up process, pure oxygen and hydrogen flows through the water bubbler for 4 hrs and 30 minutes resulting in gas saturation with water vapor.

4. The wafers were then annealed using Nitrogen gas with the gas allowed to flow at 5 litre/min for 10 minutes.

5. The wafers are then cooled for ten minutes and checked for oxide thickness.

The thickness of the oxide layer was measured using an ellipsometer and was found to be around 1.063 μm.

1.1.3 CPW metal layer patterning

The proposed RF MEMS capacitive shunt switches have been integrated with a CPW line. The fabrication of CPW lines is easily integratable with the fabrication

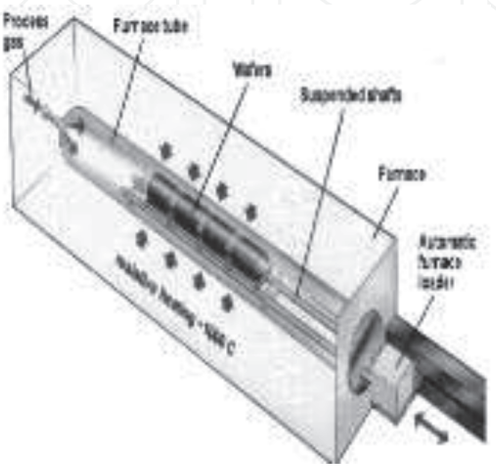


Figure 2.
Details of oxidation furnace at CeNSe, IISc.

steps required for the RF MEMS switch, which justifies the choosing of CPW lines over microstrip lines. This section gives fabrication steps for the CPW layer formation on the Silicon wafer.

a. **Sputtering of Gold layer**: The sputtering of gold layer depends on various parameters such as temperature, target distance, deposition pressure and Argon flow rate [17]. TECPORT sputter coater is used for obtaining the Chrome/Gold layer as shown in **Figure 3**. The process parameters of the sputter coater were set at a base pressure of $5x10^{-6}$ Torr, deposition pressure of $6.5x10^{-3}$ Torr, target to substrate distance set at 7.5 cm, with the Argon flow rate at 250 Scc/m. A seed layer of 10 nm is sputtered using a DC power of 100 W, a pre-sputtering time of 600 seconds and a deposition time of 22 seconds. For Gold DC Power was set at 25 W with a pre sputtering time of 30 seconds followed by a deposition time of 220 seconds with the deposition rate at 5 ^{0}A/sec. This was followed by Chrome sputtering to form a layer of 15 nm thickness. This process step would ensure good adhesion of the anchors of the top Gold beam with the bottom layer.

b. **Lithography for CPW layer**: The first photolithography step is used to pattern the CPW lines. A positive Photoresist (PR) AZ5214E is spin coated at speed of 4000 rpm using the spin coater for 40 seconds. It is then soft baked at 110°C for 1 minute. The wafer is then loaded into the EVG Mask aligner for PR exposure as shown in **Figure 4**. The proximity of the mask aligner is set at 30 μm and the energy for UV rays is set at 15 mJ. The mask used for this layer is as shown in **Figure 4**. The wafer is then post baked at 110°C for 1 minute and flood exposed using 75 mJ. The wafer is then immersed in the developer MF 26 A for around 20–30 seconds. The wafer is then subjected to a hard bake at 110°C for 3 minutes. The wafer is then inspected under the microscope to ascertain that the PR has developed.

c. **Gold/Chromium etch:** The etching of Gold (Au)/Chromium (Cr) is achieved by Potassium Iodide and Iodine (KI/I_2) solution in a ratio of KI: I_2: H_2O = 4 g: 1 g: 40 ml. At room temperature etch rate is approximately 1 μm/min for Chrome/Gold. For the Cr/Au/Cr thicknesses of 10 nm/100 nm/15 nm respectively the time is set to 10 to 20 sec for Cr etch, 60 to 120 sec for Au

Figure 3.
TECPORT sputter coater.

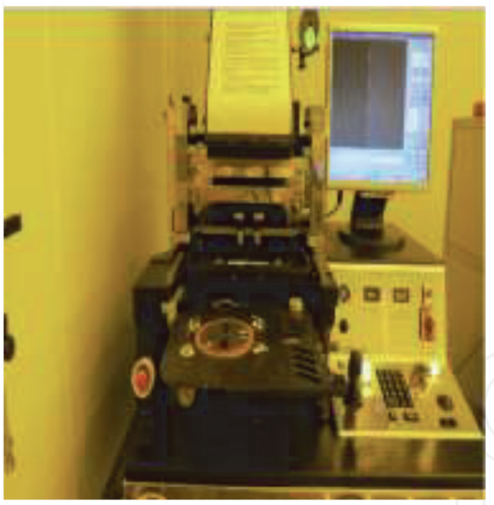


Figure 4.
EVG mask aligner at CeNSE, IISc.

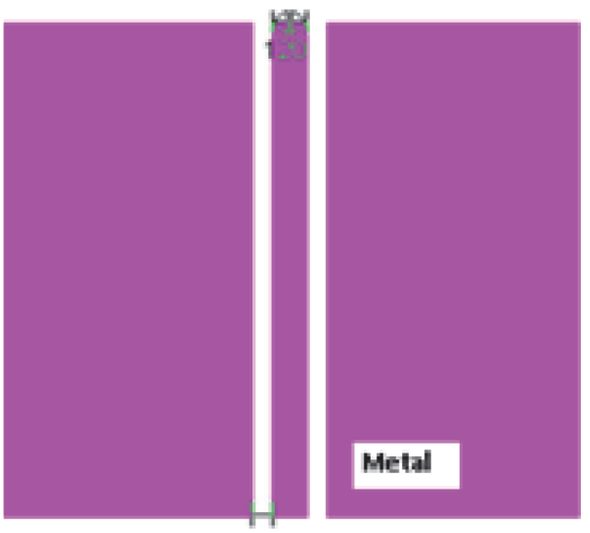


Figure 5.
Mask 1 for CPW layer patterning.

etch and 10 to 20 sec for Cr etch. **Figures 5** and **6** represent the mask for patterning and the resulting CPW layer respectively.

1.1.4 Dielectric layer deposition and patterning

The following process steps were followed for the deposition and patterning of dielectric Silicon Nitride (Si_3N_4) on the central signal line of the CPW layer.

a. **Deposition of Si_3N_4:** This layer provides the dc isolation between the signal line and the ground line when the switch is actuated to the down-state position. A thinner layer of Si_3N_4 will result in a higher capacitance in the downstate but would lead to pinhole problems which occur in thin dielectric layers. Also, the thin dielectric layer must be able to withstand the actuation voltage without breakdown.

Oxford Instruments Plasma technology Plasma Enhanced Chemical Vapor Deposition (PECVD) system is used for deposition of Si_3N_4 as shown in **Figure 7**. PECVD is a process by which thin films are deposited from the conversion of

Figure 6.
Optical microscope image.

Figure 7.
Oxford PECVD for Si_3N_4 deposition at CeNSE.

gaseous materials into solid state, due to a chemical reaction occurring in the presence of plasma. PECVD uses electrical energy to generate the plasma. Due to the presence of plasma, the gas mixture is transformed into highly reactive ions and molecules, which leads to low temperature requirements as compared to CVD processes. PECVD processes results in high quality films which have good adhesion, uniformity and good step coverage [18].

Silane (SiH_4) is usually supplied along with an inert gas like Nitrogen, Argon or Helium. Silane reacts with Ammonia (NH_3) to produce Si_3N_4 and a by-product Hydrogen. This reaction is as depicted by the chemical reaction as given below.

$$3SiH_4 + 4\,NH_3 \rightarrow Si_3N_4 + 12\,H_2$$

b. **Lithography for Si_3N_4:** The patterning of Si_3N_4 is achieved by first depositing a positive photoresist AZ4562 by placing it on a spin coater. The spin coater rotates at 4000 rpm for 40 sec. After soft baking at 110°C for 1 minute, the PR is exposed to UV rays through a mask aligner at proximity of

30 μm and energy of 110 mJ. The PR is then developed using the developer AZ 351B for 45–60 seconds. Next, the wafer is hard baked on an oven at 110°C for 3 minutes.

c. **Etching of Si_3N_4:** The etching of Si_3N_4 is performed using a dry etch process called Reactive Ion Etch (RIE). Reactive Ion etching is a process wherein the reactive species react with the material to be etched only when the surfaces of the material are activated by the collision of incident ions from the plasma. The etching characteristics like etch rate, etch profile, etch uniformity, etch selectivity can be controlled very precisely by selecting the right combination of recipes of chamber pressure, flow rate of gases, applied RF power and electrode bias. The etch rates are slow typically about 10 nm/ min up to 50 nm/min.

The RIE-F equipment used at CeNSe, IISc is as shown in **Figure 8**. For etching of Si_3N_4 the chamber pressure is set at 10 mTorr, RF power at 50 W with the main power at 2000 W. The flow rate of Sulfur Hexa Flouride (SF_6) is set at 45 scc/m with the temperature at 5°C. For etching out 100 nm of Si_3N_4 the required time was 12 seconds. The mask used for the patterning of the Si_3N_4 layer is as shown in **Figure 9**.

d. **Photoresist strip:** This is followed by the wet etching of the photoresist by dipping the wafer in acetone for 5 minutes followed by immediate cleaning

Figure 8.
RIE F CeNSe, IISc.

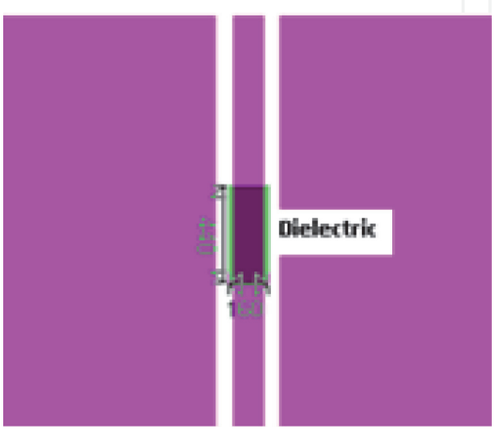


Figure 9.
Mask 2 for silicon nitride.

using Isopropyl Alchohol (IPA). This is to prevent the re-deposition of stripped photoresist on the substrate since Acetone has high vapor pressure. This is followed by cleaning with Ultrsonicate Acetone for 3 minutes. **Figure 10** shows the patterned silicon nitride layer.

1.1.5 Sacrificial layer deposition and patterning

The sacrificial layer is the layer which will be etched out to release the top metal layer. The topography and planarity of the top membrane is defined by the sacrificial layer planarity. Several materials like metals, dielectrics and photoresists have been used as the sacrificial layer. The choice of the sacrificial layer is based on the processing steps that follow the deposition of this layer, the temperature range, the required planarity and profile of surface. Here, a positive Photoresist (PR) S1813 is used as the sacrificial layer. This PR has to be deposited with utmost accuracy in order to define the gap between the top electrode and bottom electrode of the RF MEMS switch. The complete process of sacrificial layer deposition and patterning can be explained by the following steps:

Sacrificial layer Optimization: The PR S1813 is a positive photoresist which has excellent adhesion, excellent coating uniformity with effective broadband exposure. This PR is used for a wide variety of process flow requirements such as lift-off, dry etch, wet etch, the thickness of the PR to name a few. The plot in **Figure 11** gives the resist thickness versus spin for the Shipley family of PRs. Thick PR layers can be achieved in one step, however they have the disadvantage of being non-uniform over the wafer surface. In order to achieve uniform and thick PR coating, the coating process is performed in three steps. In the first step, the spin coater is run at low speeds of 500 rpm for 30 sec. This low spin speed and reduced spin time

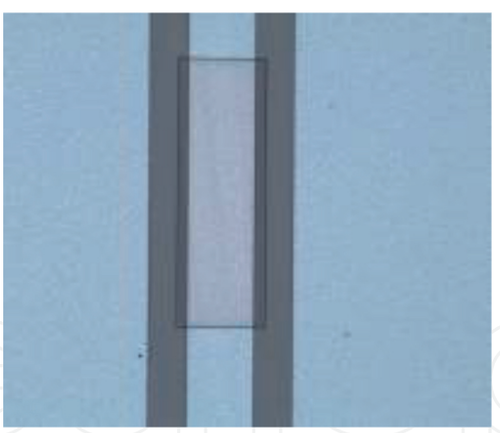


Figure 10.
Optical microscope image of silicon nitride layer formed.

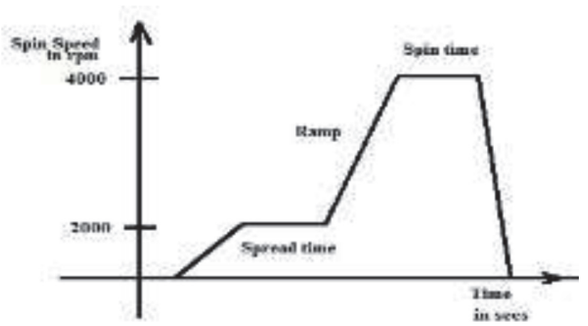


Figure 11.
PR deposition using multiple step method.

will result in uniform coating of thick resist on the wafer. In the second step the speed is ramped upto 1000 rpm within a time of 30 sec. A solid film of the photoresist is formed with the complete evaporation of the solvent. This step decides the thickness and uniformity of the photoresist. The third step consists of the spin coater speed set at 2000 rpm for 40 sec. This last step ensures that any leftover solvent is completely evaporated. The complete cycle of spin coating is as shown in **Figure 11**. Using a Dektak optical profiler the thickness of this layer was confirmed to be 3 μm.

Sacrificial layer patterning: The patterning of the sacrificial layer photoresist is processes by first depositing one more layer of positive PR S1813 on this layer. This was achieved by the spin coater speed set to 500 rpm for 30 seconds, followed by a ramp up of 1000 rpm for 30 sec and 200 rpm for 40 sec. After soft baking the PR is exposed to UV rays through a mask aligner at a proximity of 30 μm and energy of 75 mJ. The mask used for generating the pattern for this layer is as shown in **Figure 12**.

The PR is then developed using the developer AZ 351B for 30–60 seconds. Next, the wafer is hard baked on an oven at 90°C for 30 minutes. The PR layer thickness shrunk from 3 μm to 2.09 μm after development and baking.

1.1.6 Top layer deposition and patterning

The top layer or beam formation defines the performance of the RF MEMS switch. The top layer designs were simulated using Coventorware™. These designs have been chosen due to their lower pull-in voltages. Gold is the choice for the top layer due to its favorable characteristics such as, its high conductivity, non-tarnishing property, high Young's Modulus and compatibility with micromachining processes. The top metal layer deposition and patterning is described in the following sections.

a. **Gold layer deposition:** The deposition of this layer was carried out using the TECPORT sputtering equipment. It may be recalled that the bottom layer has the composition of Cr/Au/Cr. This composition would lead to excellent adhesion of the top layer anchors with the previously deposited Chrome layer. Several Iterations were carried out in order to sputter the top Gold layer without residual stress. Several parameters such as temperature, rate of deposition were optimized in order to arrive at top layers without buckling after release process.

Finally, with the optimized parameters setting temperature and rate of deposition a stress free top layer was arrived at. The stress free top layer is of critical importance for reduction in actuation voltage. The process parameters of the sputter coater were set at a base pressure of $5x10^{-6}$ Torr, deposition

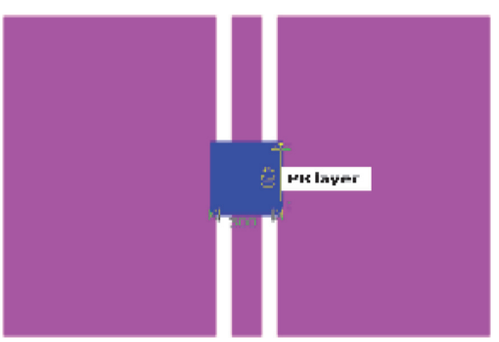


Figure 12.
Mask 3 for PR layer.

pressure of $6.5x10^{-3}$ Torr, target to substrate distance set at 7.5 cm, with the Argon flow rate at 250 sccm. The DC Power was set at 25 W with a pre sputtering time of 30 seconds followed by a deposition time of 1100 seconds with the deposition rate set at 5^0A/sec.

b. **Gold layer patterning:** The four switch designs chosen for the top Gold layer are shown as four respective masks in **Figure 13**. The lithography involved the use of AZ5412E positive PR. This was spin coated at 4000 rpm for 40 sec. The wafer was then soft baked aligner at a proximity of 10 μm and energy of 50 mJ The PR is then developed using the developer MF 26A with the wafer dipped in the developer of 20–140 sec. Next, the wafer is hard baked on an oven at 90°C for 30 minutes. For Gold etch, freshly made Potassium Iodide and Iodine (KI/I_2) solution in a ratio of $KI:I_2:H2O$ = 4 g:1 g:40 ml is used. The unwanted Chrome deposition on the bottom layer is also etched out using a Chrome etchant for 5 to 10 seconds.

1.1.7 Top layer release

The release of the top switch membrane is the most crucial step in the whole fabrication process. There are many methods to release the top layer without deformation and stiction. The first step in the top layer release is to etch the sacrificial layer. This could be achieved by using dry etching or wet etching. In wet etching, conventional liquid solvents are used to completely remove the sacrificial layer followed by drying. The drying could be through the process of air drying or through critical point drying.

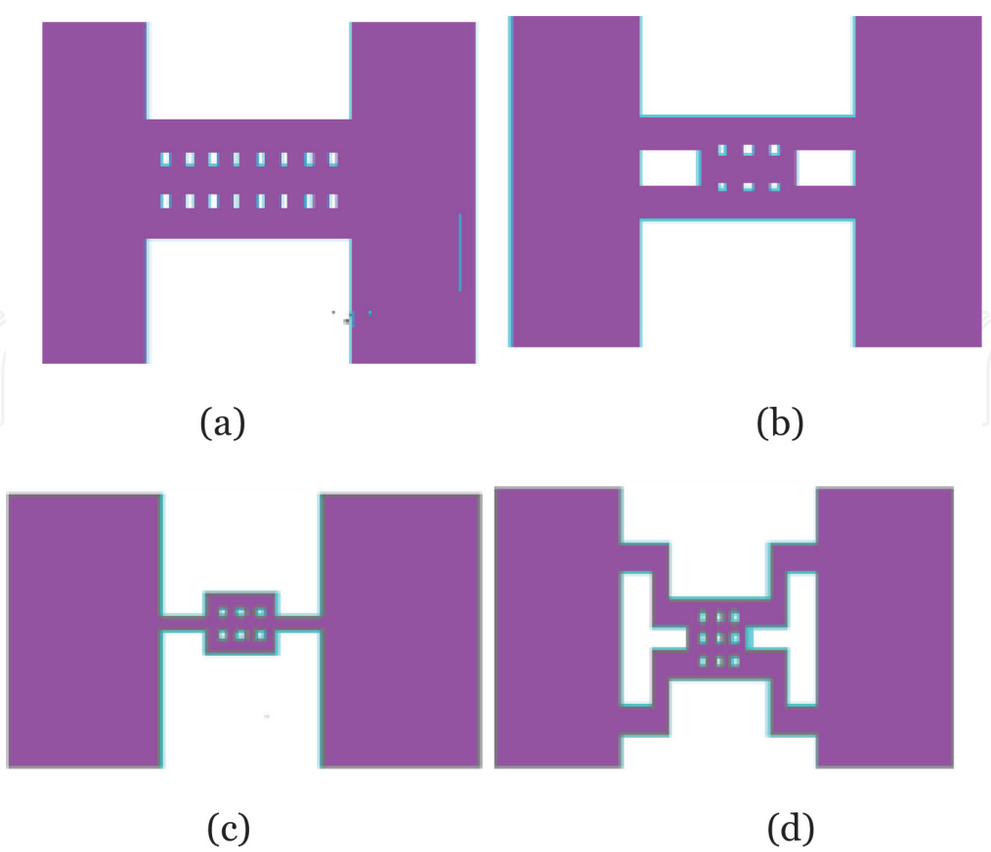


Figure 13.
Four top layer designs for RF MEMS switch. (a) Fixed-fixed beam switch. (b) Fixed-fixed Flexure switch. (c) Fixed-Fixed Single Flexure switch. (d) Crab leg Flexure switch.

Critical Point Drying (CPD) was found to be the best method for MEMS devices [19]. In this work the wet etch was followed by CPD to release the top layer. PR layer first stripped by using Piranha solution. The Piranha solution is prepared by mixing Sulfuric Acid and Hydrogen Peroxide in the ratio of 3:1. This is an extremely strong oxidizing agent which removes organic residues and especially PRs from the substrate.

Critical point drying.

There was the requirement of a drying technique wherein surface tension could be reduced to zero and a continuity of state of the liquid could be obtained. It was found that if the temperature of the liquefied gas is increased the resulting pattern of the meniscus is flat indicating a reduction in surface tension. This results a very low surface area of the liquid which in turns leads to the evaporation of the liquid. This is called the critical point of the liquid. The critical phenomena can be utilized as a drying technique as it achieves a phase change from liquid to dry gas without the effects of surface tension and is therefore suitable for delicate biological specimens. MEMS devices. Of all the gases that were tested for the critical point, Carbon Dioxide (CO_2) remains the most common medium for the CPD procedure and is termed the 'Transitional Fluid'. However, CO_2 is not miscible with water and therefore water has to be replaced in the specimen with another fluid which is miscible with CO2, this is termed the 'Intermediate Fluid'. IPA is solvable in CO_2 and hence most of the MEMS devices are place in this liquid for CPD process.

The critical point dryer used in this work was the Tousimis Samdri® line of Supercritical Point Drying machine as shown in **Figure 14**. The wafer after the Piranha dip was placed with great care in a petri dish containing IPA. This was then carefully transferred to the CPD equipment. Once the release cycle was finished, the Switches were inspected under a microscope and then using Scanning Electron Microscope (SEM) and were found to be free of residual stress on the top beam. Also, the gap between the top membrane and the bottom electrode was clearly visible without any PR residues.

1.2 Packaging of RF MEMS shunt capacitive switches

The main objectives of packaging of MEMS devices are to protect the actual functioning of the device from external environmental influences like chemicals, temperature, electromagnetic influences. The packaging forms a foundation on which the actual device is mounted thus giving much needed mechanical support. Packaging also helps in routing of interconnections of the chip with the outside world.

Figure 14.
Tousimis Samdri critical point dryer at CeNSE, IISc, Bangalore.

The most critical factor for the successful commercialization of micro level devices is packaging. With the maturity gained in IC (integrated circuits) fabrication over the past many years, the packaging of ICs also has gained great maturity and sophistication. The same cannot be said about MEMS packaging. Although some of the advancements of IC packaging can be applied to meet the requirements of MEMS devices, some specialized techniques are required for MEMS packaging. Packaging of MEMS devices is much more complex and expensive than conventional IC packaging. This is because MEMS devices usually consist of three dimensional structures with free movement. This leads to the requirement of encapsulated cavities. Microsystem packaging also involves, bonding, interconnecting, and assembly of micro scale component to form a microsystem product. Packaging is the last and crucial step in the lifecycle of MEMS devices and may cost anywhere between 20–90% of the total device cost. Important functions of packaging are listed below:

- Mechanical reinforcement and ruggedness
- Environment invulnerability against temperature, electromagnetic aberrations, chemical reactions
- Interfacing with outside world
- Hermetic sealing
- Assimilation of multiple chips to form a multifunctional system

In the case of MEMS devices the requirement of hermetic sealing may vary from device to device since some of the MEMS devices need an exposure to the environment in which they work and some other devices do not. It is also necessary to note that the packaging needs are special and case specific due to the micro mechanical structures. MEMS packaging involves key design and packaging considerations such as wafer thickness, wafer dicing, thermal issues, stress effects, isolation, protective coatings and hermetic sealing.

The packaging for RF MEMS devices has to meet more stringent specifications due to the high frequency range of interest. Also, the demand is for high performance, low cost strategies which is usually a challenge. Furthermore, apart from the general MEMS packaging issues, the packaging of RF-MEMS devices has the following concerns.

1. Hermiticity of the packages should be ensured to provide high reliability RF MEMS devices since their operation depends on the ambient conditions under which they perform.
2. Interconnects, package substrates and passivation layers through the package to the outside world should offer low loss and low intermodulation.
3. Footprint of the total packaged device must be small, keeping with the requirement of miniaturization and high component densities especially for satellite and wireless communication systems.

The packaging of RF MEMS devices can be classified into two broad categories, one, wafer level packaging and the other, die level packaging. This work focuses on die level packaging hence the following paragraphs will focus on this.

1.2.1 Die level packaging

This is a type of packaging used for low volume requirements. Die level packaging is also called 1-level of packaging. The 1-level package usually consists of a prefabricated metal can/ceramic/plastic package with leads for connecting to the outside circuits or systems. These packages come with the base as well as the lid. For both ceramic as well as metal packages the cavity formation in the base of the package is an established method. The MEMS chip is attached to the base package using low temperature solder based epoxies and baked for removal of gaseous by products of the solder or epoxy. The next step involves the placement of the top cover over the base package in a vacuum or nitrogen atmosphere. Next, hermetic sealing is done along the package rim which is performed using localized heating.

This method of packaging is expensive and is suitable for telecommunication base stations, satellites and defense systems but not for high volume applications like mobile phone handsets. Furthermore, the additional costs are mainly due to the great care with which the MEMS chips are to be handled after their release. Furthermore, standard scribing procedures cannot be used for dicing the wafer into chips since there is a high possibility of introduction of contaminants on wafer surface. These contaminants cannot be removed by mere cleaning. This cleaning will furthermore require a critical point drying for every chip which would further escalate the costs. A generic 1-level packaging is as shown in **Figure 15**.

In this thesis the focus is on die level packaging using available surface mount style RF packages. However, the whole packaging process is performed under low temperature in order to free the MEMS structures of thermally induced stress which otherwise would affect the performance of the switch. The details of the packaging process starting from the design of RF feed throughs on the Alumina substrates to the die attachment, wire bonding and hermetic sealing are discussed in details in the following sections.

1.2.2 Packaging of RF MEMS shunt capacitive switches

The packaging of RF MEMS switches involves the following steps:

- Dicing of wafer
- Design of RF feed throughs on Alumina substrate
- Attachment of the base package to Alumina substrate

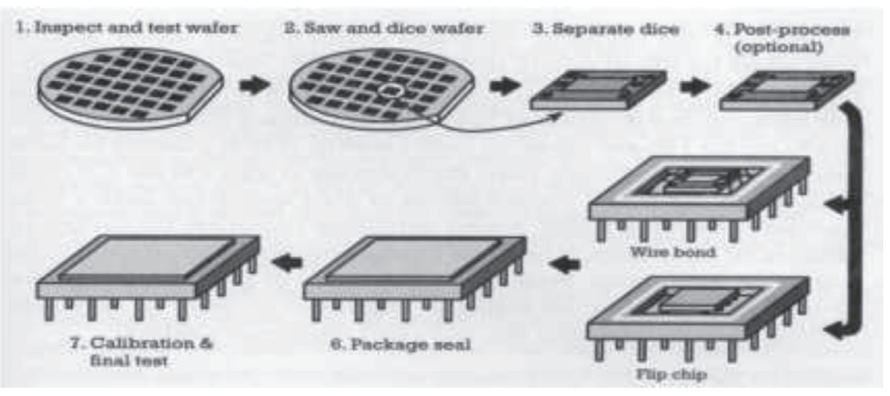


Figure 15.
Simplified one level RF MEMS packaging flow.

- Die bonding to package base
- Wire bonding
- Hermetic sealing

2. Dicing of wafer

Wafer dicing is the process by which the individual unit of dies are separated from the wafer. This process may be carried out by using mechanical sawing, scribing, breaking or laser cutting. Of the several issues and challenges of RF MEMS packaging, dicing is one of the foremost challenges. In the case of ICs, the resultant contaminants or debris due to the dicing process, on the surface of the die can be easily removed by a post-dicing cleaning process, however, in the case of MEMS devices the fragile mechanical structures on the die may get damaged by these contaminants. Dicing methods such as mechanical sawing, scribing and breaking lead to debris from the dicing process which may scatter on to the die leading to buckling or breaking of the delicate MEMS structures. Therefore, the choice of the dicing process is of utmost importance in the case of RF MEMS devices.

In order to obtain least residues from the dicing process, Chicago Laser System (CLS 960) Neodymium-doped Yttrium Aluminum Garnet (Nd:YAG) laser has been employed. This is shown in **Figure 16**. Nd:YAG lasers are one of the most common types of laser used in cutting and welding steel, semiconductors and various alloys. These lasers typically emit light with a wavelength of 1064 nm, in the infrared.

Figure 16.
Chicago laser system (CLS 960) laser dicer.

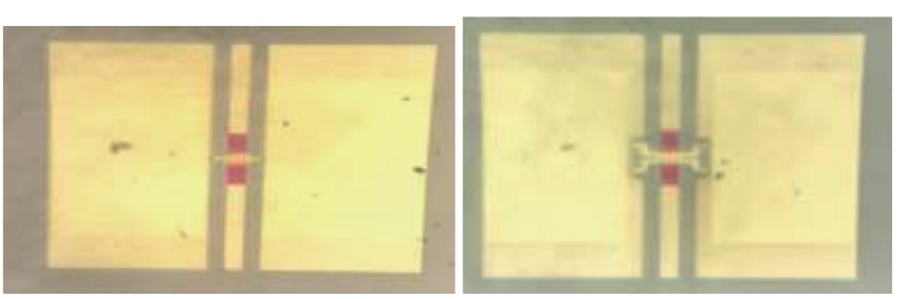


Figure 17.
Diced chips as seen under a microscope.

The wafer to be diced was mounted on the dicing platform with the alignment set. The wafer is then diced into unit chips or dies with high precision. The unit dies obtained were observed under a microscope. It was visually confirmed that the RF MEMS switches were undamaged. The samples of diced chip are as shown in **Figure 17**.

3. Design of RF feed throughs on Alumina substrate

There are several choices of substrates for packaging like Quartz, Silicon, Aluminum nitride (AlN) and Alumina (Al_2O_3) to name a few. Ceramic substrates such as Aluminum Nitride and Alumina are most commonly used packaging materials for MEMS. Alumina is the primary choice because it combines economic, physical and electrical advantages [20]. Also, Alumina is readily available in sizes that range from tiny chips to large ceramics in thicknesses from 0.25 mm to 1.5 mm and in a variety of shapes and designs. The finished substrate can be drilled or cut with diamond tools and lasers.

Some of the key properties of Alumina are as given below:

- Good thermal conductivity
- High strength and stiffness
- Resistance to strong acid and alkali attack at high temperatures
- Excellent size and shape capability
- Excellent dielectric properties from DC to GHz frequencies
- compatibility with thick film resistors and dielectrics
- Excellent adhesion with thick film conductors

Having chosen Alumina as the substrate material, the RF feedthroughs on the Alumina substrate had to be designed. The generic CPW line is as shown in **Figure 18**. The design of the CPW lines on the Alumina substrate was based on many parameters such as trace (S) and ground line (G) lengths, permittivity of Alumina (ϵ_r), material properties of conductor and the operating frequency. The designed layout for CPW lines on the Alumina substrate is as shown in **Figure 19**.

Silver Palladium paste (7474 Ag/Pd) is used to form the CPW conductors on the Alumina substrate. This paste is chosen for its excellent solderability and excellent

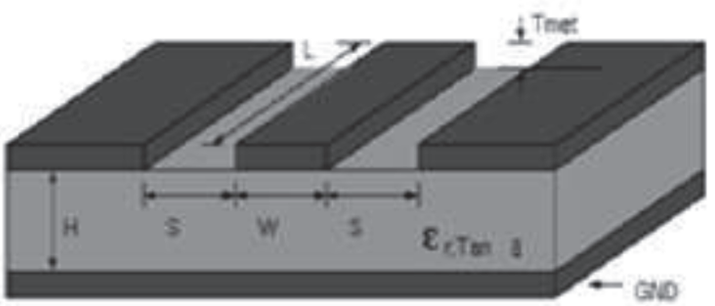


Figure 18.
Schematic of CPW line.

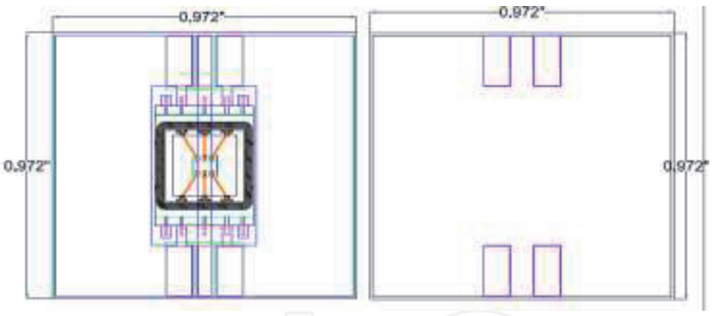


Figure 19.
CPW layout on alumina substrate. (1) Front view. (2) Back view.

aged adhesion on substrates like Alumina and it's comparatively low cost. The three steps involved in the formation of CPW lines on the Alumina substrate is as given below.

- Scribing
- Screen-Making
- Printing, Drying and Firing

i. **Scribing:** Scribing is basically designing on the substrate using laser. The blank substrate is first divided into a number of regions by scribing. The laser used in this process is a combination of Nitrogen, Carbon Dioxide (CO_2) and helium gases. At higher temperatures, the valence electrons combine to produce laser light.

The advantages of laser scribing are

1. High edging steepness
2. Small edge roughness
3. No micro cracks
4. Small thermal influence by optimized uv treatment
5. Contact free material processing
6. High precision and positional accuracy.

After the scribing process the plates are subjected to the de-burring process. De-burring is done to remove the ceramic particles that accumulate on the surface due to laser penetration. De-burring is done using another ceramic plate. The plates are cleaned in de-ionized water and then dried in an oven at 120°C.

ii. **Screen-Making:** This is the preliminary process for printing. Here, the stainless steel mesh is first stretched with hydraulic force. The frames are then attached to the mesh. The chromo difloro film, is first stuck on to the wet screen and dried in the oven after which they are exposed to UV light with the respective photo film layer. The film is developed using water. After screen making process is over, printing is performed on the Alumina substrate.

These are the following precautions to be observed in screening:

1. The screen should be free of foreign particles.

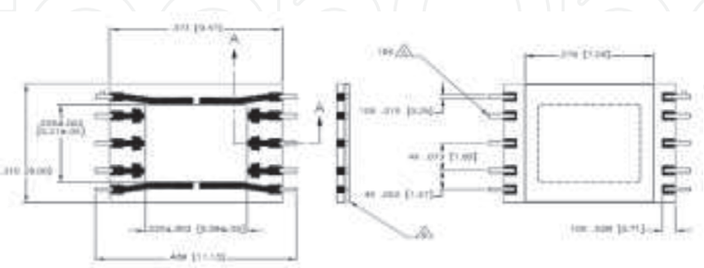
2. The screen tension should be within the specification of workmanship.

iii. **Printing:** In this process, the conductors are printed on the substrate. The conductor paste is (7474 –Palladium Silver) is screen printed. It is then dried at 150° C for 15–20 minutes in order to remove the solvents and then fired at 850° C in a fast firing furnace. At this temperature sintering takes place with a dwell time of 10 min and then ramp down takes place after which the paste starts behaving like a conductor. At the end of this process CPW lines on the Alumina substrate were formed.

4. Attachment of base package to alumina substrate

Surface mount packages are used for packaging the diced chips. The current packaging methodology proposes the use of surface mounted plastic packages supplied by Elecsys technologies, USA. These packages are suitable for DC to 18 GHz range which is also the frequency of interest of the RF MEMS switches. These packages also have their leads to be co-planar compatible. These packages have a conductive metal base attached to an Alumina ceramic ring frame with a cup shaped lid with a b-stage epoxy preform for sealing. **Figure 20** shows the layout details of the SMX series packgae used for packaging the RF MEMS shunt switches. **Figure 20(a)** shows the base of the package with leads made of Copper and Gold. **Figure 20(b)**shows the top view of the base package showing the jutting leads.

The attachment of Base Package to the substrate is achieved by using a non-conductive epoxy named 8700 K. This epoxy is a high thermal conductivity, low temperature curing, microelectronics grade adhesive. It is then cured at 150°C for 2 hours. In order to connect the base package pins to the CPW conductor lines, a conductive epoxy 84–1 LMINB1 is used. This conductive epoxy used, is a high purity silver filled die attach adhesive ideal for application by automatic dispenser.



(a) (b)

Figure 20.
Layout details of the SMX series package. (a) inside view (b) top view.

5. Die bonding

Die bonding or die attach is one of the most crucial steps in the packaging process especially in the case of MEMS devices. This requires careful handling of the

diced MEMS chip/die since the die contains fragile mechanical structures. The dies have to be picked from the wafer either using manual methods or by automatized grippers. They have to be then placed on the base package cavity. The choice of die bonding process depends upon package sealing strategy, operating conditions and environmental and reliability requirements. The die attach can be achieved through the following bonding methods:

1. eutectic bonding

2. solder attach

3. epoxies, silver filled glass or polymide

Eutectic bonding uses a die bonding technique with an intermediate metal layer (Au/Al) which would result in a eutectic system. The most important feature of this type of bonding is that the eutectic temperature can be much lower than the melting temperature of individual elements. Solder Attach is the most preferred type of die bonding since the solder provides for good thermal conductivity. But this type of die bond would lead to large amount of heat generation during the attachment process which may lead to a large thermal stress on the mechanical structure in the case of a MEMS device.

Epoxy bonding is achieved by attaching die to the substrate by using epoxy glue. A drop of the epoxy is first dispensed on the substrate and the die is placed on it. In order to cure the epoxy the substrate or package may need to be heated. Most commonly used adhesives are polyimide, epoxy and silver filled glass. Epoxy bonding has the following important features such as low curing temperature, used for wide range of die sizes and can be reworked easily [21, 22]. Epoxy is used for die attachment in this work.

The bare die is attached to the Base Package using non- conductive epoxy (H74 epoxy) and curing at room temperature of 25°C for 48 hours, keeping in mind the low temperature requirement for packaging in this work [23]. H74 epoxy is a thermally conductive epoxy designed for hybrid circuit assembly including die attach. The outstanding feature of this epoxy is that its curing process is fast even at low temperatures and also has a built in color change when the adhesive is cured. The adhesion of the dies is good and is confirmed by the non-destructive pull test (NDPT) and die shear test. It is passing the NDPT of greater than 16 grams and the die shear strength is greater than 6.55 kgs. The tested samples are as shown in the **Figure 21**.

Figure 21.
Die shear test.

6. Wire bonding

Wire bonding is a process by which interconnections are made between the die to the suitable location on the substrate or package. Wire bonding has the advantage of being low cost and flexible method of interconnection and is widely used to assemble majority of semiconductor packages. They also have the advantage that they can be used upto a frequency of 100 GHz if properly designed. Thus it is most suitable for RF MEMS switches.

Thermosonic bond is formed by the combination of three parameters, ultrasonic, thermal and mechanical force. A thermosonic bonding machine uses a piezoelectric transducer which converts the electrical energy to a vibratory/ultrasonic motion. This is in turn converted to an amplified oscillatory motion using a velocity transformer. This oscillatory motion is delivered to a heated bonding tip. The thermal energy and the ultrasonic motion together create a softening of the lead wire and hence its deformation leading to a required contact area using low temperature and low force.

Hence, in the proposed work thermosonic bonding has been chosen as the wire bonding technique due to its desirable properties of operation at low temperature and low force. A Kuilelle and Soffa thermosonic bonder is as shown in **Figure 22** which is used for the wire bonding process. Ball and wedge bonds of Gold wire of 2 mil are used for wire bonding between bare die to the package base pads as shown in **Figure 23(a)**. The NDPT test was also performed to ensure the strength of the wire bonds. The wire bonds were then covered with Epotek-301-2FL, a low stress adhesive especially used for glob top encapsulation over wire bonds. The curing for

Figure 22.
Kulicke and Soffa thermosonic ball bonder.

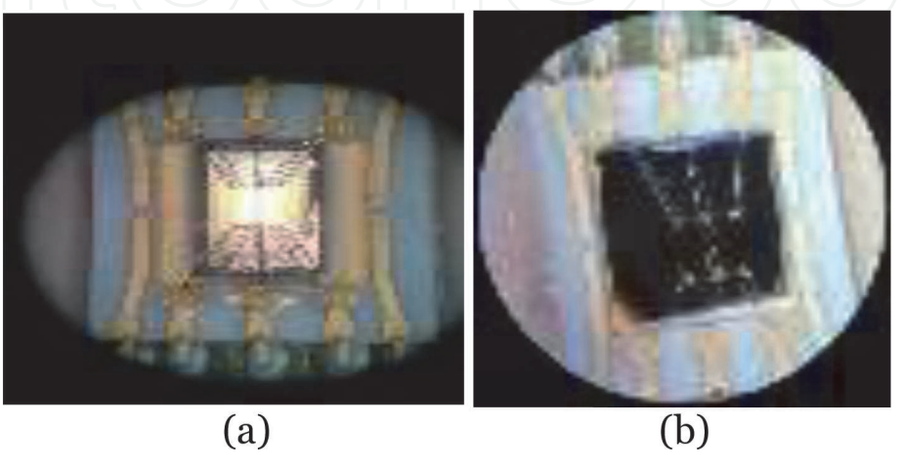


Figure 23.
Wire bonding. Hermetic sealing and soldering of SMA. (a) Gold wire bonding. (b) Gel dispensed on bonding Wedge.

this adhesive was done at room temperature of 25°C for 72 hours. **Figure 23(b)** shows the adhesive covered wire bonds.

Hermetic seals are airtight seals that prevent the invasion of oxygen, moisture, humidity, and any outside contaminant to enter a sealed environment. This kind of a sealing is of utmost importance in semiconductor devices and MEMS devices. In the case of MEMS devices this is a top priority since the performance of a MEMS sensor or actuator directly depends on the ambient conditions under which they operate.

This work proposes the use of epoxy resins to seal the package lid to the base package. The top can/case is attached to the base package using a non-conductive epoxy H74 and cured at a room temperature of 25°C for 48 hours. The package with the top case attached is as shown in **Figure 24**. This method of curing was tested on samples in order to ascertain the complete curing. The specification sheets states that this epoxy requires a temperature of 150°C for 5 minutes and a temperature of 100°C for 20 minutes, for curing. However, curing at room temperature of 48 hours has led to the complete sealing. This was ascertained by performing a leak test on the packed RF MEMS switch. There are several types of leak tests to confirm the hermiticity of sealed packages. The Helium leak test was performed following a procedure as explained below. The vacuum method is the most sensitive leak detection technique. It requires that part of the package be placed under hard vacuum and the other part to be pressurized with helium. The side which is placed under vacuum is connected to the leak detector. If there is a leak, the helium that penetrates this side will be detected by the leak detector. The package under test passed the standard leak test with a test value of 5.0×10^{-8} std. atm.cc/sec.

In order to characterize the packaged MEMS switches Sub Miniature version A (SMA) connectors have been used. These connectors are designed to be used between DC and 18 GHz. The SMA's chosen for this work with part number 1367–000-G91P-35 were procured from Delta Electronics Manufacturing Corporation.

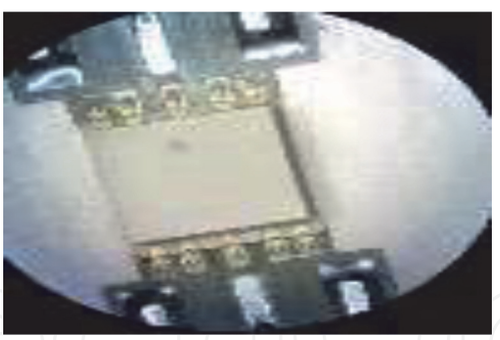


Figure 24.
Lid sealed package.

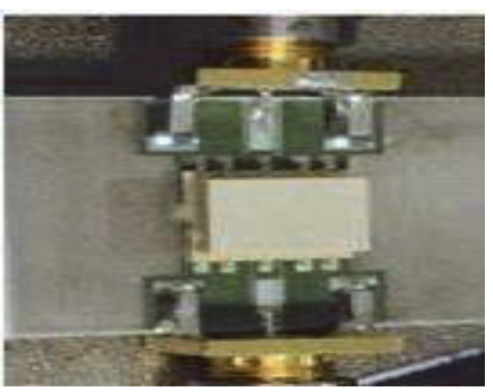


Figure 25.
Package with SMA connectors.

These connectors were soldered to the Alumina substrate using solder wire (Sn 63: Pb37) as shown in **Figure 25**.

7. Conclusions

The objective is to fabricate the simulated designs using low cost fabrication processes. Considering the ease of implementation and complications of the processes involved, it is focused to fabricate only the capacitive shunt switches using a low cost, low resistivity silicon wafer as the substrate and using only four masks for the whole process. Surface micromachining process was used to fabricate these switches. During the fabrication several challenges such as residual stress of top gold film, planarization of sacrificial layer, release of top beam were encountered and are overcome. Several rounds of optimization of unit process led to the successful fabrication of these switches. Packaging the fabricated switches, was done using low temperature methods to minimize the effect of packaging on the structure. The packaging of these switches used SMAs. The packaging involved several steps such as wafer dicing, conductor screen printing on substrate, die bonding, wire bonding and hermetic sealing. The switches are packaged and hermetically sealed by using a unique method of curing and sealing using room temperature methods, in order to avoid thermally induced stress in the fragile MEMS beams of the switches. The proposed packaging methodology has passed both the shear test and the hermeticity tests. By optimizing the fabrication process to cater to batch processing and also finding methods of CMOS compatible methods, this technology will help meet the ever growing demands of wired as well as wireless communication for low loss high performance RF switches.

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I think my research would have been only in the simulations stage if not for the project funded by National Program on Smart Materials and Structure (NPMASS) ADA, INDIA. This opportunity changed my perspective of my research since I was able to fabricate devices hands on in one of the best laboratories of the world.

The fabrication was carried out at the Centre for Nano Science and Engineering, IISc, Bangalore. I would like to express my deep sense of gratitude to Dr. K. N Bhat, Professor Emeritus, CeNSe, IISc, Bangalore for his time and valuable inputs during the fabrication of RF MEMS switches. With his repertoire of knowledge, he was able to guide us through difficult phases of fabrication. I also would like to thank the team at CeNSe for their co-operation throughout the project.

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References

[1] G. K. Ananthasuresh, K. J. Vinoy, S. Gopalakrishnan, K. N. Bhat, V. K. Aatre, “Micro and Smart Systems”, Wiley India, 2010.

[2] Vijay K. Varadan, K.J. Vinoy, K.A. Jose “RF MEMS and Their Applications”, John Wiley & Sons, 2003.

[3] Gabriel M. Rebiez “ RF MEMS: Theory, Design and Technology” , John Wiley and Sons, 2003.

[4] Hyman, Daniel, Juan Lam, Brett Warneke, Adele Schmitz, T. Y. Hsu, Julia Brown, James Schaffne, "Surface-micromachined RF MEMs switches on GaAs substrates", International Journal of RF and Microwave Computer-Aided Engineering, Vol. 9, no. 4, pp.348–361, 1999.

[5] Kim, Che-Heung. "Mechanically coupled low-voltage electrostatic resistive RF multithrow switch." IEEE Transactions on Industrial Electronics, Vol.59, no. 2, pp. 1114–1122, 2012.

[6] Marc J. Madou ,“Fundamentals of Microfabrication: The Science of Miniaturization”, Second Edition, CRC Press, 13-Mar-2002

[7] S. Pacheco, C. T. Nguyen, and L. P. B. Katehi, “ Micromechanical electrostatic K-band switches”, IEEE International Microwave Symposium Digest, MTT-S, Baltimore, USA, pp. 1569–1572, June 1998.

[8] Dimitrios Peroulis, S.P.Pacheco, K. Sarabandi,Linda P.B.Katehi.,” Electromechanical Considerations in developing Low Voltage RF MEMS switches”, IEEE Transactions on Microwave theory and techniques, Vol. 51 no.1, pp.259–70, Jan 2003.

[9] S. Pacheco, C. T. Nguyen, and L. P. B. Katehi,” Design of low actuation voltage RF MEMS switch”, International Microwave Symposium Digest, IEEE MTT-S, Boston, USA, Vol.1, pp. 165–168, 2000.

[10] D. Peroulis, S. Pacheco, and L. P. B. Katehi,” MEMS devices for high isolation switching and tunable filtering”, International Microwave Symposium Digest, Boston, MA, IEEE MTT-S, Vol.2, pp. 1217–1220, June 2000.

[11] Shekhar S, Vinoy KJ, Ananthasuresh GK,“Surface-Micromachined Capacitive RF Switches with Low Actuation Voltage and Steady Contact”, Journal of Microelectromechanical Systems. Apr. 2017.

[12] W.Kern, Ed, Handbook of Semiconductor cleaning Technology, Noyes Publishing; Park Ridge, NJ, 1993, Ch1

[13] Jasbir, Sharma, Krishanapura Nagendra, and Das Gupta Amitava. "Fabrication of low pull-in voltage RF MEMS switches on glass substrate in recessed CPW configuration for V-band application" , Journal of Micromechanics and Microengineering, Vol.22, no.2, pp. 025001, 2012.

[14] Philippine MA, Zareie H, Sigmund O, Rebeiz GM, Kenny TW,” Experimental validation of topology optimization for RF MEMS capacitive switch design”, Journal of Microelectromechanical Systems. Vol.22, no.6, pp. 1296–309, Dec 2013.

[15] Fernández-Bolaños, M., Perruisseau-Carrier, J., Dainesi, P. and Ionescu, A.M,” RF MEMS capacitive switch on semi-suspended CPW using low-loss high-resistivity silicon substrate”, Microelectronic Engineering, Vol.85, no.5, pp.1039–1042, 2008.

[16] Jiang, Hongrui, Zhihong Li, and Norman C. Tien. "Reducing silicon-

substrate parasitics of on-chip transformers." In Micro Electro Mechanical Systems, 2002. The Fifteenth IEEE International Conference on, pp. 649–652. IEEE, 2002.

[17] Yoshikiyo Hatakeyama, Kei Onishi and Keiko Nishikawa, "Effects of sputtering conditions on formation of gold nanoparticles in sputter deposition technique", **RSC Adv.,** 2011,**1**, 1815–1821

[18] Rahman, H.U., Johnson, B.C., Mccallum, J.C, " Fabrication and characterization of PECVD silicon nitride for RF MEMS applications", Microsyst Technol 19**,** 131–136 2013.

[19] Ijaz H. Jafri, Heinz Busta, Steven T. Walsh, "Critical point drying and cleaning for MEMS technology", Proceedings Volume 3880, MEMS Reliability for Critical and Space Applications; 1999

[20] Khatib, M-K. El, Arnaud Pothier, and Pierre Blondy. "Packaging of RF MEMS switching functions on alumina substrate", arXiv preprint, arXi*:* 0711.3297, 2007.

[21] Cheng Zhao, Jing Song, Lei Han, Qing-An Huang, "Effects of thermally induced packaging stress on a distributed RF MEMS phase shifter", Microsystem Technology, Vol. 21, pp. 869–87, 2015.

[22] Y K Kim, E K Kim, S W Kim, and B K Ju, "Low temperature epoxy bonding for wafer level MEMS packaging", Sensors and Actuators A, Vol. 143, no. 2, pp. 323–8, May 2008

[23] Y K Kim, E K Kim, S W Kim, and B K Ju, "Low temperature epoxy bonding for wafer level MEMS packaging", Sensors and Actuators A, Vol. 143, no. 2, pp. 323–8, May 2008.