Chapter

Introductory Chapter: Integrated Circuit Chip

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1. Introduction

The technological advancement of integrated circuit chips (or colloquially referred to as an IC, a chip, or a microchip) has progressed in leaps and bounds. In the span of less than half a century, the number of transistors that can be fabricated in a chip and the speed of which have increased close to 500 and 5000 times, respectively. Back in the old days, about five decades ago, the number of transistors found in a chip was, even at its highest count, less than 5000. Take, for example, the first and second commercial microprocessors developed in 1971 and 1972. Fabricated in the large-scale integration (LSI) era, the Intel 4004 4-bit microprocessor comprised merely 2300 transistors and operated with a maximum clock rate of 740 kHz. Similarly, the Intel 8008 8-bit microprocessor released immediately a year later after its 4-bit counterpart comprised merely 3500 transistors in it and operated with a 800 kHz maximum clock rate. Both these two microprocessors were developed using transistors with 10 μm feature size. Today, the number of transistors in a very large-scale integration (VLSI) (or some prefer to call it the giant large-scale integration [GLSI]) chip can possibly reach 10 billion, with a feature size less than 10 nm and a clock rate of about 5 GHz. In April 2019, two of the world's largest semiconductor foundries—Taiwan Semiconductor Manufacturing Company Limited (TSMC) and Samsung Foundry—announced their success in reaching the 5 nm technology node, propelling the miniaturization of transistors one step further to an all new bleeding edge [1]. According to the announcement made in the IEEE International Electron Devices Meeting in San Francisco, the TSMC's 5 nm chip would be produced in high volume in the first half of 2020 [2, 3]. TSMC has also started work on their 3 nm nodes [3].

There is little doubt that the electronics world has experienced a quantum leap in its technology for the past 50 years or so and this, to a large extent, is due to the rapid improvement in the performance, power, area, cost and "time to market" of an IC chip. This chapter provides a succinct illustration on the historical evolution of the IC chip, a general overview of the fundamental building block of the chip—the field-effect transistors, and a brief description of the IC design process.

2. A brief history

The thermionic triode was regarded as the predecessor of transistors that are prevalently used to build electronic devices today. Being invented in 1907, the triodes were made of vacuum tubes which were relatively large in size and were naturally cumbersome to be used. In December 1947, however, three physicists working in the AT&T Bell Laboratories— Dr. Walter Houser Brattain, Dr. John Bardeen and Dr. William Bradford Shockley, Jr.—achieved a remarkable scientific

breakthrough when they successfully constructed the solid-state equivalence of the thermionic triode, i.e. the first point-contact germanium transistor. As can be seen in **Figure 1**, the solid-state transistor that they developed consisted of an n-type germanium crystal block and two layers of gold foils placed in close proximity with each other. The foils acted as the contacts of the transistor. Together with the contact at the base, the transistor had a total of three contacts—which were named the emitter, collector and base contacts. When a small current was applied to the emitter contact, the output current at the emitter and base contacts would be amplified [4, 5].

In comparison with its predecessor, the solid-state transistor was diminutive in size. It also consumed much lower power, operated at relatively lower temperature and gave significantly faster response time. It is therefore apparent that the semiconductor transistor is more superior to its conventional vacuum tube brethren. Owing to its advantages and viability, the vacuum tubes were eventually replaced by the solid-state electronic devices. The inexorable widespread usage of the semiconductor transistors in electronic circuits has triggered a dramatic revolution in the electronic industries, kicking off the era of semiconductor. Because of this significant contribution, Bardeen, Brattain and Shockley were awarded the Nobel Prize in Physics in 1956 [4].

It is worthwhile noting that, when the solid-state device was first introduced, it was not coined the term "transistor." Instead, it was generally referred to as the "semiconductor triode." According to the "Memorandum for File" published by the Bell Telephone Laboratories (BTL) [6], six names had been proposed for the device—namely, "semiconductor triode," "surface states triode," "crystal triode," "solid triode," "iotatron" and "transistor." The word "transistor" (which originates from the abbreviated combinations of the words "transconductance" and "varistor") proposed by Dr. John Robinson Pierce of BTL had ultimately turned out to be the winner of the internal poll [6].

The first silicon transistor was developed by Dr. Morris Tanenbaum of BTL in January 1954, whereas the first batch of commercially available silicon transistors were manufactured by Dr. Gordon Kidd Teal of Texas Instruments (TI) in the same year. In 1955, the first diffused silicon transistor made its appearance. To reduce the resistivity of the collector, the transistor with an epitaxial layer

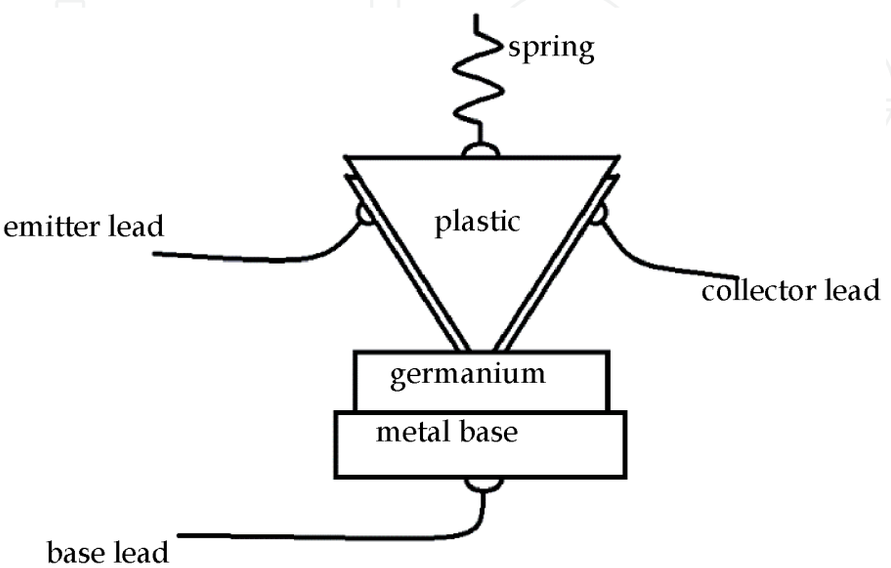

Figure 1.
An early model of the point-contact transistor.

deposited onto it was developed in 1960. In the same year, the planar transistor was proposed by Dr. Jean Amedee Hoerni [4, 7].

In 1958, Jack St. Clair Kilby, who was then an engineer in TI, successfully developed the first integrated circuit (IC). The device was just a simple 0.5 inch germanium bar, with a transistor, a capacitor and three resistors connected together using fine platinum wires. About half a year later in 1959, Dr. Robert Norton Noyce from Fairchild Camera (also one of the cofounders of Intel Corporation) invented independently his own IC chip. The interconnection in Noyce's 4 inch silicon wafer was realized by means of etching the aluminum film which was first deposited onto a layer of oxide [7]. Both Kilby and Noyce shared the patent right for the invention of the integrated circuit. In 2000, Kilby was awarded the Nobel Prize in Physics "for his part in the invention of the integrated circuit."

The first-generation computers were made of vacuum tubes. Conceived in 1937, the Atanasoff-Berry computer (ABC) (which was generally regarded as the first computer by many) and the Electronic Numerical Integrator and Computer (ENIAC) (which was credited as the first general purpose computer) built in late 1945 belong to the first-generation computers. The vacuum tube triode was swiftly replaced by the solid-state transistor since its advent in 1947. The second-generation computers were therefore made of transistors. The prototype computer built at the University of Manchester in November 1953 was widely regarded as the first transistor computer. Like the first transistor computer, most other electronic devices built before 1960 were actually based on germanium transistors. Although silicon transistors had already been developed in the mid-1950s, design engineers were more prone to using germanium than silicon. This is because the technology of germanium devices was very well established at that time and the reliability and yields of the silicon transistor were nowhere close to its germanium brethren [8]. Also, germanium switching diodes exhibited lower threshold voltage than silicon devices, allowing electronic devices made from germanium to be switched on at lower voltage drops [8]. The normal operating temperature of germanium devices, however, did not exceed 70°C, whereas silicon devices could operate well beyond 125°C. Hence, silicon was only used by the military establishment at that time for applications which were to operate at high temperature [8]. Besides its tenacity in withstanding temperature, silicon is also found to have lower leakage voltage and higher thermal conductivity than germanium [8]. These, however, were not the precipitating factors for silicon to replace germanium. It was the development of the oxide masking technique by Carl John Frosch and Lincoln Derick of BTL in 1955 which marked the pivoting point for the role played between silicon and germanium. Researchers found that an oxide film could be easily grown on the surface of a silicon substrate, but attempts to grow a stable oxide layer onto the germanium surface ended in total dismay [8]. BTL ceased meaningful research on germanium since then, and by the end of 1960, most of the electronic devices have been dominated by silicon. During these 5 years, researchers achieved several major technological innovations with the applications of the oxide films—some of which include the fabrication of the monolithic integrated circuit and the invention of the metal oxide semiconductor field-effect transistor (MOSFET) [8]. These innovations reinforce the status of silicon as the key element in electronic devices. In 1961, the first computer made from silicon IC chips was dedicated to the US Air Force.

Since the advent of the solid-state transistor and the demonstration on the workability of the IC chip about some 70 years ago, the electronic industries have been prospering hitherto. IC chips are now closely interwoven with human's life. They have, in many aspects, become indispensable to mankind. Indeed, one can easily

find traces of IC chips intermingle into areas which intertwine seamlessly with the fabric of mankind's living hood. Some of these areas include transportation, telecommunication, security, medicine and entertainment, just to name a few.

3. Moore's law

In the article published in April 1965, one of the cofounders of Intel Corporation, Dr. Gordon Earle Moore, predicted that the number of electronic components (which include not just transistors but capacitors, resistors, inductors, diodes, etc. as well) in an IC chip would double every year [9]. Ten years later, Moore revised his prediction to a doubling of every 2 years. Moore's prediction, which is more commonly known as Moore's law nowadays, has been widely used by the IC manufacturers as a tool to predict the increase of components in a chip for the coming generations [10]. To date, Moore's law has been proven to have held valid for close to half a century. **Table 1** tabulates the progressive trend of the integration level for the semiconductor industry. It can be observed from the table that the number of transistors that can be fabricated in a chip has been growing continuously over the years. In fact, this growth has been in close agreement with Moore's law. In order to highlight the technological advancement in the IC industries, each decade since the inception of the semiconductor transistor has been earmarked as a different era. Eight eras have existed hitherto—they are the small-scale integration (SSI), medium-scale integration (MSI), large-scale integration (LSI), very large-scale integration (VLSI), ultra-large-scale integration (ULSI), super large-scale integration (SLSI), extra-large-scale integration (ELSI) and giant large-scale integration (GLSI) eras. During the VLSI era, a microprocessor was fabricated for the first time into a single IC chip. Although this era has now long passed, the VLSI term is still being commonly coined today. This is partly due to the absence of a significant qualitative leap between VLSI and its subsequent eras, and partly, it is also because IC engineers have been so used to this term; they decided to continue adopting it.

Integration level	Year	Number of transistors in a chip
Small-scale integration (SSI)	Late 1940s to late 1950s	Less than 100
Medium-scale integration (MSI)	Late 1950s to late 1960s	Between 100 and 1000
Large-scale integration (LSI)	Late 1960s to late 1970s	Between 1000 and 10,000
Very large-scale integration (VLSI)	Late 1970s to late 1980s	Between 10,000 and 100,000
Ultra-large-scale integration (ULSI)	Late 1980s to late 1990s	Between 100,000 and 1000,000
Super large-scale integration (SLSI)	Late 1990s to late 2000s	Between 1000,000 and 10,000,000
Extra-large-scale integration (ELSI)	Late 2000s to late 2010s	Between 10,000,000 and 100,000,000
Giant large-scale integration (GLSI)	Late 2010s to late 2020s	More than 100,000,000

Table 1.
Integration level of an integrated circuit chip.

4. The field-effect transistors

Today, the transistors fabricated in an IC chip are mostly MOSFETs. The earliest paper describing the operation principle of a MOSFET can be traced back to that reported in Julius Edgar Lilienfeld's patent in 1933 [11]. Unfortunately, the technology at that time was inadequate to allow Lilienfeld's idea to be physically materialized. In 1959, Dr. Dawon Kahng and Dr. Martin M. (John) Atalla at the BTL successfully constructed the MOSFET [12]. In 1963, two engineers from the Radio Corporation of America (RCA) Princeton laboratory, Dr. Steven R. Hofstein and Dr. Frederic P. Heiman, presented the theoretical description on the fundamental nature of the silicon planar MOSFET [13]. In the same year, Dr. Tom Chih-Tang Sah and Dr. Frank Marion Wanlass of Fairchild Semiconductor invented the first complementary metal oxide semiconductor (CMOS) logic circuit [14]. In 1989, Dr. Digh Hisamoto and his team member at Hitachi Central Research Laboratory introduced the fin field-effect transistor or better known as the FinFET—a non-planar MOSFET modified from its planar counterpart. Although the FinFET was found to possess various advantages over the planar MOSFET, it was not adopted by the industries then. This was partly due to the difficulty in fabricating its three-dimensional structure and, partly, also because the planar MOSFETs still had plenty of rooms to be improved further. Having realized that the planar MOSFET was gradually approaching its bottleneck in its technological advancement, chipmakers started to resort to FinFETs in the fabrication of high-end electronic devices (such as microprocessors) in 2011.

4.1 The MOSFET

The MOSFET is nothing more than a device which operates as an electronic switch. **Figure 2** shows the basic structure of the MOSFET. The transistor comprises four terminals, namely, the drain (D), source (S), gate (G) and substrate or body (B) terminals. As can be clearly seen from the figure, the device constitutes three layers—a polysilicon layer (which forms the gate terminal), an oxide layer (known the gate oxide) and a single-crystal semiconductor layer (known as the substrate). In the early days, the gate terminal was made of aluminum. It is from these three layers of materials that the FET device acquired its name. In the mid-1970s, however, the gate material was replaced with polysilicon. When ion implantation was introduced to form the self-aligned source and drain terminals in the 1970s, a high-temperature (higher than 1000°C) annealing process was required to repair the damaged crystal structure at the surface of the substrate, as a result of the energetic dopant ion bombardment and to activate the dopant [15]. IC engineers observed that the aluminum gate melted during the annealing process. This is because aluminum has a melting point of about 660.3°C. In order to overcome this problem, polysilicon which has a melting point of about 1414°C was employed as the replacement for gate material. Although the gate today is no longer made of aluminum, the term MOSFET has been so widely accepted that it stays until today.

The basic operation principle of a MOSFET is actually quite straightforward. When a voltage source is connected in between the drain and source terminals, a conducting channel is to be formed between the two terminals to allow the current to flow. The channel is commonly referred to as the inversion layer since the charges accumulated at the channel oppose those of the substrate. In this case, the gate terminal acts like a switch which controls the formation of the inversion layer. When sufficient voltage drop (and, of course, with the appropriate polarity) is applied to the gate terminal, carriers would be attracted to the gate oxide-substrate interface to form the inversion layer.

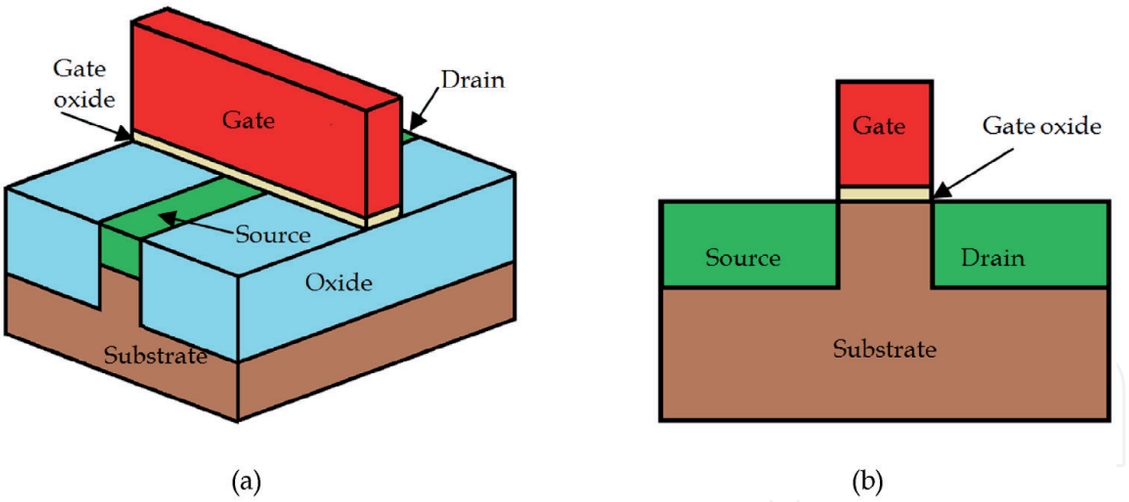

Figure 2.
The (a) basic structure and (b) cross section of a MOSFET.

A MOSFET can be classified into two types, depending on the dopants in the drain and source terminals, as well as the substrate. When both the drain and source terminals, in a p-type substrate, are heavily doped with donator ions (such as phosphorous or arsenic), a negative channel is to be formed in between them to conduct current. On the other hand, when both terminals, in an n-type substrate, are heavily doped with acceptor ions (such as boron), a positive channel is to be formed. The former device is therefore known as a negative channel MOSFET or an NMOS transistor, while the latter is known as a positive channel MOSFET or a PMOS transistor. **Figure 3** shows the circuit symbols of both PMOS and NMOS transistors [4].

The size of a MOSFET transistor is measured by the gate length, which is also commonly known as the feature size or feature length as is denoted by the symbol *L*. The size of the transistor has been shrinking tremendously over the years. This allows a higher number of transistors to be fitted into a single die. Overseen by the Taiwan Semiconductor Industry Association (TSIA), the US Semiconductor Association (SIA), the European Semiconductor Industry Association (ESIA), the Japan Electronics and Information Technology Industries Association (JEITA) and the Korean Semiconductor Industry Association (KSIA), the International Technology Roadmap of Semiconductor (ITRS) is charted to forecast how the technology node is expected to evolve. The purpose of the ITRS is to ensure healthy growth of the IC industries. **Table 2** tabulates the progressive reduction of the feature size published in ITRS 2.0 [16]. In order to provide a clear outline to simplify academic, manufacturing, supply and research coordination regarding the development of electronic devices and systems, the ITRS was continued by the International Roadmap for Devices and Systems (IRDS) in 2018 [17].

4.2 The FinFET

As the feature size reduces to the submicron regimes, fields at the source and drain regions become comparatively high, and this may induce certain adverse effects to the charge distribution. Some of the examples of these short-channel effects are the threshold voltage roll-off in the linear region, drain-induced barrier lowering (DIBL) and bulk punch-through [18]. To suppress these effects, additional steps such as the introduction of retrograde well, the deposition of the sidewall spacers, lightly doped drain (LDD) implantation, halo implantation, etc. have been introduced into the IC fabrication process [19]. As the device continues to shrink,

Figure 3.
The symbol of (a) a PMOS transistor and (b) an NMOS transistor.

Physical gate length	Year						
	2015	2017	2019	2021	2024	2027	2030
High-performance logic (nm)	24	18	14	10	10	10	10
Low-performance logic (nm)	24	20	16	12	12	12	12

Table 2.
Forecast of gate length by ITRS.

curbing the short-channel effects turns out to be a strenuous task. When the feature size approaches the subnanometer range (i.e. 90 nm and below), static leakage current due to the short-channel effects has become a serious problem.

When the technology node reached 22 nm in 2011, Intel Corporation announced the fabrication of the tri-gate transistor, replacing the conventional planar MOSFET. Better known as the FinFET, this device has a three-dimensional transistor structure, as depicted in **Figure 4** [20]. It is apparent from the figure, a FinFET is named so because of the protruding source and drain terminals from its substrate surface, which resemble the fins of a fish. Since the gate wraps around the inversion layer, FinFETs provide higher current flow from the source to the drain terminals. This protruding fin structure also allows better control of the current flow, i.e. it reduces current leakage considerably when the device is at its "off-state" and minimizes short-channel effects at its "on-state". Since the device has lower threshold voltage than the planar MOSFET, a FinFET can also operate at relatively lower voltage drops. In a nutshell, the FinFET shows less leakage, faster switching and lower power consumption in comparison to its planar counterpart.

5. IC design flow

Generally, the design process of an IC chip involves three stages—namely, the (i) behavioral, (ii) logic circuit and (iii) layout representations [4, 21]. At the end of each stage, verification is to be performed before proceeding to the next. Hence, it is common to have repetitions and iterations in the processes [4, 21].

5.1 Behavioral representation

At the initial stage of IC design, it is important to be specific on the functionalities of the chip. The design architecture is to be drawn out. Verilog or SystemVerilog hardware description language (HDL) is used to define the behavior of the IC chip.

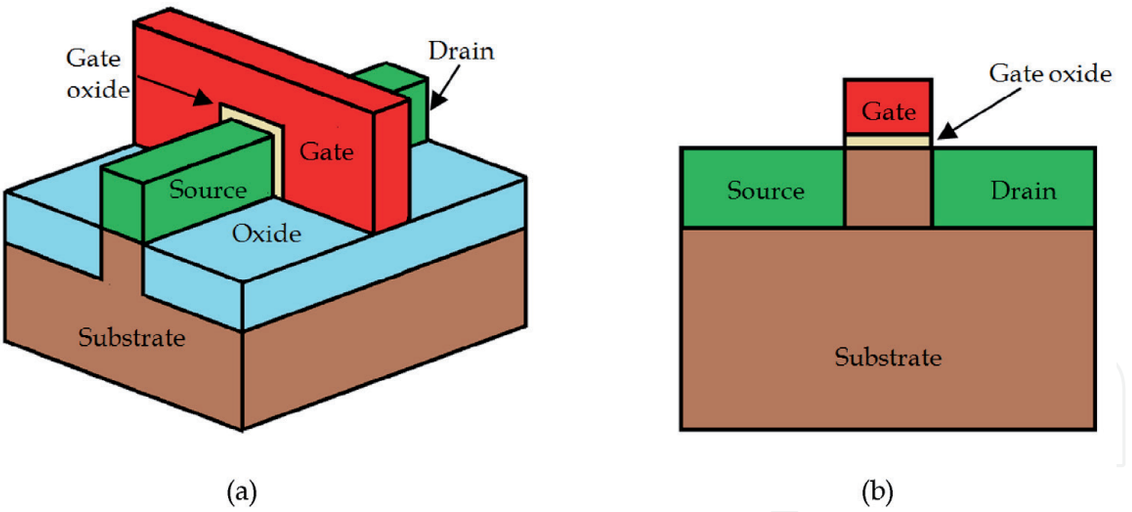

Figure 4.
The (a) basic structure and (b) cross section of a FinFET.

5.2 Logic circuit representation

Once the HDL codes are successfully simulated, functional blocks from standard cell libraries are used to synthesize the behavioral representation of the design into logic circuit representation. Once the design is verified, the gate-level netlist is generated. The netlist consists of important information of the circuit such as the connectivity and nodes and is necessary in order to develop the layout of the design.

5.3 Layout representation

The physical layout of the design is created at the final stage. The process starts with floor planning which defines the core and routing areas of the chip. In order to optimize the design, the building blocks are usually adjusted and orientated by IC designers. This process is known as placement. Once this is completed, a routing process is performed to interconnect the building blocks.

6. Microchip fabrication

To fabricate the chip, the layout is sent to a fab or a foundry. In a fab, a single-crystal semiconductor ingot is first grown. Wafers are then sliced from the ingot. The layout is printed onto the dice in each wafer.

The fabrication process for NMOS and PMOS transistors is similar. The main differences lie within the types and density of dopants applied to the substrate—specifically in the formation of well, threshold voltage V_{TH} adjust implantation, LDD implantation, source/drain implantation, etc. The process flow of fabricating a planar MOSFET is summarized in the following sections, and it is also graphically depicted in **Figure 5**. The process of chip fabrication can be broadly separated into five stages, i.e. (i) well formation, (ii) device isolation, (iii) transistor making, (iv) interconnection and (v) passivation [15].

6.1 Well formation

Initially, a p-type single-crystal silicon wafer is prepared (**Figure 5(i)**). In order to form a P (for NMOS) or N (for PMOS) well, screen oxide is first grown on the surface of the substrate (**Figure 5(ii)**). A high-energy ion implantation is then

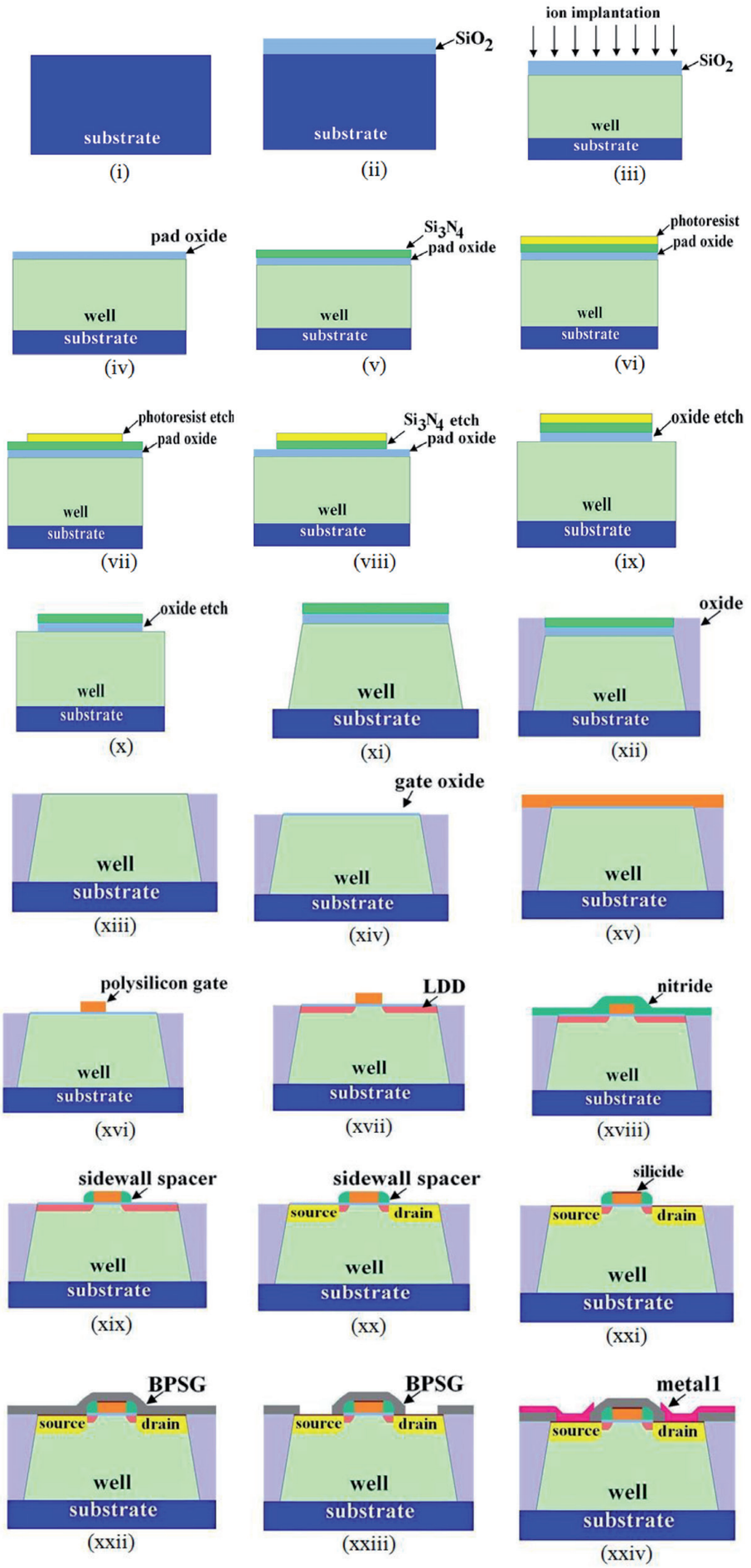

Figure 5.
The fabrication process of a MOSFET.

performed to form the well (**Figure 5(iii)**). The wafer subsequently undergoes annealing and drive-in processes to, respectively, repair the lattice damage caused by the high-energy ion bombardment and to activate the dopant.

6.2 Device isolation

Next, shallow trench isolation STI is employed to isolate neighboring devices. Initially, pad oxide is grown via dry oxidation (**Figure 5(iv)**). Chemical vapor deposition CVD technique is then applied to deposit a layer of silicon nitride Si_3N_4 onto the oxide surface (**Figure 5(v)**). Pad oxide acts as a stress buffer to avoid cracks on the nitride film, whereas nitride film acts as a mask for silicon etching. A layer of photoresist is subsequently deposited onto the nitride layer (**Figure 5(vi)**). Lithography is performed to develop patterns on the photoresist (**Figure 5(vii)**). The nitride film and pad oxide are etched in accordance with the pattern formed at the photoresist (**Figure 5(viii)**and **(ix)**). The area protected under the nitride mask is known as the active region. As soon as the photoresist is stripped (**Figure 5(x)**), the substrate undergoes reactive ion etching (RIE) to form trenches (**Figure 5(xi)**). A thin layer of barrier oxide is grown in the trenches so as to block impurities from diffusing into the substrate during the CVD process. The trenches are then filled with oxide via the CVD process (**Figure 5(xii)**). The oxide at the surface of the substrate is removed using the chemical mechanical polishing (CMP) technique (**Figure 5(xiii)**). The STI is completed after annealing is performed, and the nitride and pad oxide layers are etched.

6.3 Transistor making

A thin layer of gate oxide is applied via dry oxidation (**Figure 5(xiv)**). Threshold voltage V_{TH} adjust implantation is subsequently performed. This is then followed by thermal annealing to repair the lattice damage at the substrate surface. A layer of polysilicon is deposited onto the substrate surface after the annealing process (**Figure 5(xv)**). The polysilicon is then etched according to the dimension of the feature size and annealed to form the polysilicon gate.

Once the gate is formed, LDD is implanted to suppress hot electron effect in deep submicron MOSFETs (**Figure 5(xvii)**). The CVD process is applied to deposit a layer of silicon nitride Si_3N_4 onto the surface of the substrate (**Figure 5 (xviii)**). The nitride film is etched to form sidewall spacers at both sides of the gate (**Figure 5 (xix)**). The source/drain dopant is then implanted into the substrate. The substrate subsequently undergoes annealing after the implantation process (**Figure 5(xx)**). This is then followed by the removal of the thin oxide layer. A layer of titanium or cobalt is then deposited onto the surface. Rapid thermal annealing (RTA) is employed to form the self-aligned silicide layers on the gate and source/drain surfaces. At the final stage of the transistor fabrication process, the unreacted titanium or cobalt layer is etched away (**Figure 5(xxi)**).

6.4 Interconnection

Once the arrays of transistors are fabricated, metallization is required to interconnect the transistors so as to form electrical circuitries. In the interconnection stage, a layer of premetal dielectric (PMD) is first formed by depositing a layer of borophosphosilicate glass BPSG onto the substrate surface (**Figure 5(xxii)**). The PMD acts as the first layer of insulator for multilevel interconnection. After the die is annealed, the BPSG is etched to form source/drain contacts (**Figure 5(xxiii)**). Metallization is applied by depositing and etching aluminum (Al) on the contacts

(**Figure 5(xxiv)**). Phosphosilicate glass PSG is used as the insulator material for the subsequent levels of metal interconnections. The insulator layers after PMD is known as the intermetal dielectric (IMD) layers. Vials filled with tungsten are usually used to interconnect different levels of metal layers.

6.5 Passivation

The passivation layer is the final dielectric layer deposited onto the die after the last metal interconnection is formed. Silicon nitride is usually used as the passivation layer.

7. Packaging

To protect the chip from harsh external environment (e.g. being exposed to UV light or moisture or being scratched), it is essential to encapsulate the chip in a ceramic or plastic package—a process known as packaging. The three most commonly used packaging techniques are (i) wire bonding, (ii) flip chip and (iii) tape-automated bonding (TAB) [10]. IC packaging marks the end of the entire chip manufacturing process. The chip is therefore ready to be released to the market, once the packaging process is completed.

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