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Chapter

Understanding of On-Chip Power Supply Noise: Suppression Methodologies and Challenges

Pritam Bhattacharjee, Prerna Rana and Alak Majumder

Abstract

The on-chip activities of any modern IC are always inhibited due to the occurrence of power supply noise (PSN) in the chip power line. From many decades, researchers are pondering on what are the major issue of this PSN occurrence and how it can be suppressed without interfering the actual chip functioning. In the course of time, it is found that the uncontrolled triggering of the on-chip system clock and the unguarded on-chip power line is instigating the two major factors for the occurrence of PSN i.e., i(t) → instantaneous current and di/dt → current ramp or the rate of change of current over time. Both i(t) and di/dt are also the sub-factors to rise the PSN components like resistive noise and inductive noise respectively. In this chapter, we light upon the occurrence of resistive and inductive noise as well as depict their individual impact on the PSN occurrences. There is also discussion on how PSN is suppressed over the years in spite of facing challenges in the execution of suppression techniques. This chapter even concludes on the suitable ways for mitigating PSN in the contemporary era of delivering complex on-chip features.

Keywords: power supply noise, resistive noise, inductive noise, variable frequency clock, clock gating

1. Introduction

The business of integrated circuit (IC) chip has become an all-time growing venture since the last few decades. In order to continue the legacy, there are always changes and developments in the method of traditional chip design, addressing lot of issues related to the proper functioning of circuits inside the IC. The chip designers and the researchers constantly explore deep into these problem areas to find out their appropriate solution. The basic functioning of all inside the chip circuitries is primarily dependent on the power supply (V_{dd} and ground) lines attached to it. However, these V_{dd} and ground lines are supplied externally through metal pins of the outer package. Not only the proper power supply lines help the circuit performance inside an IC, but also it supports the logic level and signal integrity of all incoming and outgoing signals on and off-chip.

However in actuality, any signal entering the outer package through the metal pin has to experience the current/voltage level deterioration due to the presence of package parasitic resistive and inductive components along the pathway of metal pin, bond wire and bond pads of the IC chip as seen from **Figure 1**. Typically, the external metal pins that are soldered to the bond pads of an IC chip, have improper soldering, create

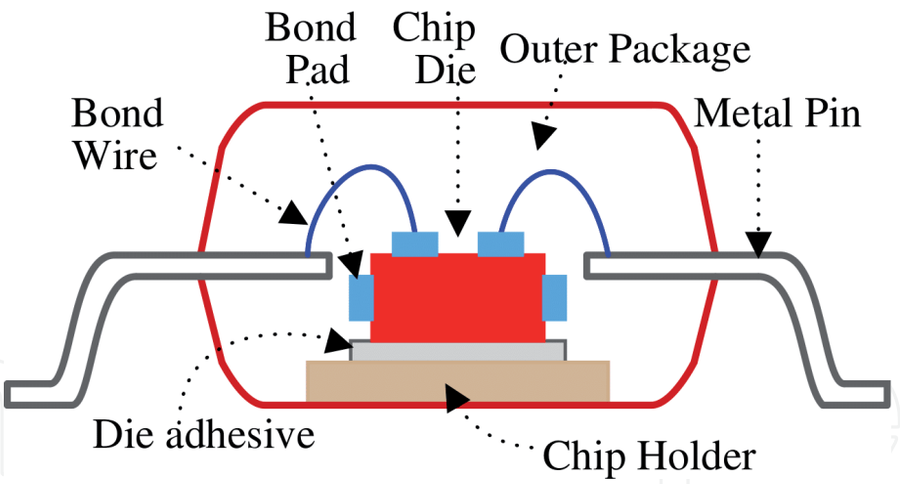

Figure 1.
Cross-sectional view of an IC chip.

tiny gap between the chip and the chip holder. For this reason, insulated adhesives are used to fill up the gaps so as to maintain safe signal transmission. In fact, these insulating adhesives always relieve the soldered joints by providing them strong mechanical connection. But post-manufacturing of the chip, these adhesives wear out with time and there is issue with the appropriateness of signal integrity inside the chip and this is one of the prime reasons for the instigation of power supply noise (PSN) in integrated circuits. The problem of PSN is more accurately stated as the fluctuation in the power supply signals, correlated to the rate of flow of current in any circuit (inside chip) under the influence of resistive and inductive parasitic attached to the circuit PDN (power-delivery-network). Sometimes, the PSN is also referred as switching noise which is the primary source of fluctuation in power supplies and is generally quantified by the maximum droop or peak in the supply voltage with respect to the corresponding nominal value [1]. Even the peak-to-peak supply voltage and the average value of supply voltage are quoted as the measure for PSN [2]. It is to be noted that the critical path delay of logic circuits inside the IC chip is inversely proportional to the rate of flow of supply voltage [3]. Any small-scale drop in the supply voltage induces timing delay for the functioning of logic circuits and if the value of delay is high in magnitude, it can even impose logical error to the operation of IC. For example, if we consider any general clock tree network (distributing clock signal to any of the sequential circuits inside the chip), there ought to be delay in the clock line while there is drop in V_{dd}. Since the clock signal from that clock tree is delayed, there happens to be clock skew with respect to the same clock signal which is transmitting in other lines. Besides, those sequential circuits inside the chip face setup time violation due to the inappropriate arrival of clock, hence always culminating logical error in their functionality. Not only it is the delay which is badly getting impacted, but also the occurrence of PSN drops the performance consistency of many circuits inside the chip as they are sensitive to the requirement of minimum supply voltage [4]. Therefore, it is very important to understand the issues of on-chip PSN resolve them to an efficient level and take a note of what the challenges are along the pathway of solving the issues.

The book chapter is organized as follows: Section 2 and its sub-sections will contain discourse of the exact problems depicted by PSN in IC chips. In Section 3, the on-chip PDN (power-delivery-network) has been discussed which actually distributes the power supply to circuits inside the chip and is one of the major victims of PSN. We talk about the primitive methodologies of suppressing on-chip PSN in Section 4 and highlight the challenges faced during this activity in Section 5. Lastly in Section 6, we have tried to put in our part of solution to the existing PSN problems and end with our concluding remarks.

2. State of art for the on-chip power supply noise problem

As a matter of fact, the amount of PSN along the circuit power line inside the chip is fundamentally the function of switching activity in the circuital nodes and consequently the instantaneous current pumped inside the system. This current pumping happens through the PDN inside the chip and cause voltage drops in the circuit power lines due to the presence of inductive, capacitive and resistive elements in the power distribution grid of the IC chip. The nominal V_{dd} (supplied from the off-chip space) get cut down to some degraded level (as shown in **Figure 2**) by the time it reaches the circuit power line.

Now, such occurrences are prevalent because of two major factors which are as follows: (i) the circuit current pumping is high with certain dip in the nominal V_{dd} and V_{gnd} because of the presence of parasitic resistance and it is often referred as "IR noise" or the "resistive noise", which is denoted by ΔV_R. The relationship of ΔV_R has been depicted in Eq. (1).

$$\Delta V_R = i(t) \times R \tag{1}$$

where, R is the parasitic resistance and i(t) is the instantaneous current. (ii) The rate of change of current across the parasitic inductance resulting "di/dt noise" or the "inductive noise", denoted as ΔV_L. The relationship of ΔV_L has been depicted in Eq. (2).

$$\Delta V_L = L \times \frac{di(t)}{dt} \tag{2}$$

where, L is the parasitic inductance and the rest is current ramp (di/dt) over a certain period, inducing fluctuations to the supply voltage level (specially to the V_{dd}).

In virtue of the relationships stated in Eqs. (1) and (2), it is inferred that higher the logic level switching across the circuital nodes within an IC chip, more is the current drawn in presence of the inductive and resistive effects which result in large PSN along the circuit power lines. This is because PSN happens because of the combined impact of inductive and resistive noise, depicted as $\Delta V_R + \Delta V_L$ [5]. As a matter of fact, PSN is not only a major concern for the mixed-signal systems or the analog circuits, but also it adversely interferes the logic and timing performance of pure digital circuits [6] present inside the chip. The analog circuits which comprise of sensitive bias points fluctuate due to the variation in supply voltages and hence are very prone to the adversities of PSN. It affects important performance circuit parameters like current/voltage gain and defects the linear behavior of most of these circuits. In case of digital circuits, though the adversity due to PSN

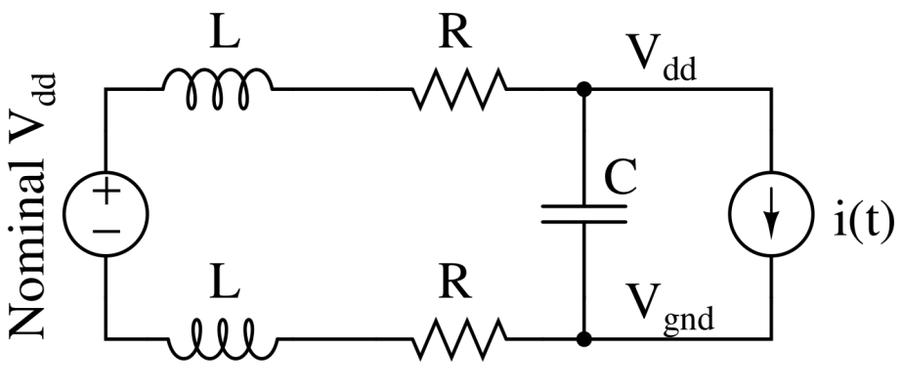

Figure 2.
Simplified circuital scheme of power distribution system.

is less, but there is always a genuine possibility that the noise level is more than the circuit noise margin specifications. Therefore, it is very important for circuits (be it analog, digital or mixed-signal) which reside inside the chip, to have guard against the PSN taint because the consequences are extremely fatal. For example, the critical path delay of circuits is inversely proportional to the amount of supply voltage. In fact, with technology scaling, the gate delay is even more sensitive to the supply voltage variations [7]. A case study which has been reported in [8] depict that 1% of supply voltage variation is causing approximately 4% variation in the delay parameters. In fact, inside the chip storage elements like latches, flip-flops, registers and SRAMs (static random-access-memory) have strict limitation of having a minimum supply of voltage (let us say, V_{min}) which determines the logic level of the stored data. Any sort of deviation in the required value of V_{min}, can lead to error in the stored data.

Another nasty consequence of PSN is that it adversely impacts the timing signals of digital clock propagating inside the chip due to the intrusion of timing jitter. Basically, the digital clock is distributed inside the chip through clock distribution network (CDN) comprising of dense clock trees that are connected to several sequential blocks inside the chip. These clock trees are made of cascaded buffers arranged in various ways based on which it is typecast as either balanced or unbalanced tree or other types [9]. The power supply (V_{dd} and ground) of these individual buffers are connected to the chip power line as shown in **Figure 3** through different tapping points and the buffers draw current while the clock signal is propagating. Now typically, V_{dd} pins of all these individual buffers are never tapped to single tap point of chip power line so as to make sure that the circuit loading is moderate at any particular point.

Now, when the PSN occurrences contaminate the chip power line, it is obvious that there is voltage fluctuation in V_{dd} across each tapping points, however with different intensity. Therefore, it is very likely that the propagation delay of clock signal through different tapping point will have different timing even if the

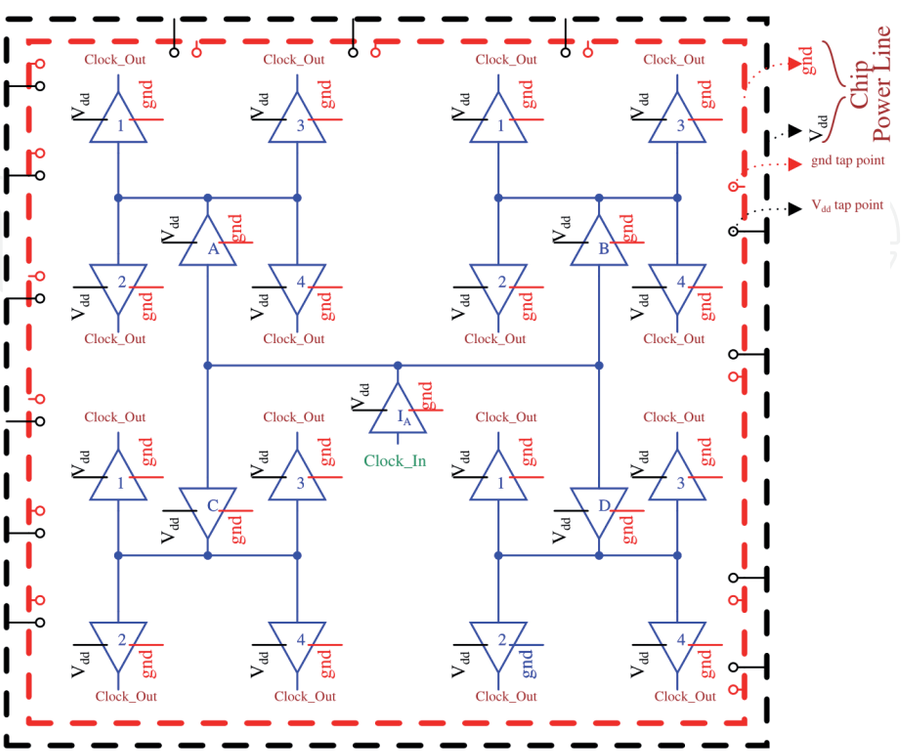

Figure 3.
H-type balanced clock tree network as a part of CDN.

buffers are identical. For example, the clock inserted in the buffer "I_A" outputs the clock signal through the output node of identical buffers "A_1"..."A_4", "B_1"..."B_4", "C_1"..."C_4" and "D_1"..."D_4". But as the V_{dd}-level of these buffers is different due to PSN, their "clock_out" has different pitch time on the sequential blocks to which they are connected. In fact, most of the "clock_out" are considered as "faulty" as per their individual timing, causing clock synchronization error to the operation of sequential blocks. Apart from these types of issues, there also remain anxieties with the circuit performance reliability when the supply voltage is high compared to its expected value. Certain overshoot in the supply voltage even cause electromigration problems [10] and hot carrier effects (HCEs) [11] in the circuit design and disturb its actual functionality. Therefore, the occurrence of PSN is always an apprehension for the circuit designers.

The mitigation of PSN is generally executed by monitoring the voltage-level fluctuations across circuit power line either continuously over time (i.e., active mitigation) or at certain instances in time (i.e., passive mitigation). However, it is also important to get hold of how much supply noise is occurring, i.e., detection of on-chip PSN. For that, the understanding of on-chip power-delivery-network (PDN) is essential which is being discussed in the upcoming section.

3. Discussion on the power delivery network for the chip

There are several ways using which the chip is facilitated by the power line supplies. Basically, the crucial aspect in the design of power delivery network (PDN) is the dedicated routing styles, for example, the ad-hoc style, the grid-like structures or even the power and ground planes. In the ad-hoc style, local circuit blocks are connected to the I/O pads (on the outer boundaries) using customized power/ground lines as shown in **Figure 4(a)**. On the other hand, grid-like PDN approaches which are commonly found in modern high-power ICs [12] is projected in **Figure 4(b)** where generally multiple layers are used in the design of power grid and power/ground lines are interdigitated within each layer and the layers are orthogonal to each other. The reason why these grid-like structures are popular in modern ICs is that the area between the power and ground line has lot of unused place which has the scope to be utilized for signal routing. This makes the power supply level insensitive to the current prerequisites of various circuit blocks. Therefore, some failure in power delivery to any one of the blocks does not prevent flow of power supply to the remaining circuit blocks. In fact, the grid structure supports the possibility of implementing dual type power supply voltages, which is essentially required in high-performance chips so that power consumption can be reduced [13]. The grid structures also facilitate the option for individual supply lines be connected to the appropriate supply voltages.

In fact, there is another design approach of PDN depicted in **Figure 4(c)**, however it is not competent in contrast to the other two approaches even though it

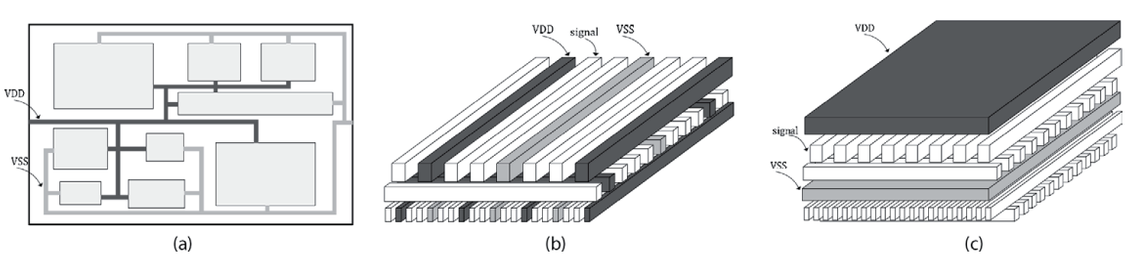

Figure 4.
On-chip PDN styles viz., (a) ad-hoc style (b) grid-like structure and (c) power and ground planes.

provides low impedance path for the current flow. The major setback here is that there is no available space for rigorous signal routing [14]. So, in the recent days the grid-like structure for PDN design is pursued for all types of on-chip architectures.

But it is important to remember while experimenting with the various PDN approaches that the grid impedance should not exceed the targeted limit which is stated in Eq. (3).

$$Z_{target} = \frac{V_{dd} \times ripple}{I_{max}} \tag{3}$$

Here, V_{dd} is the nominal supply voltage delivered from the off-chip area and I_{max} is the maximum on-chip current pumped while the full chip functionality is in execution. In this context, the term "ripple" illustrates the amount of noise (i.e., level of voltage fluctuation/ripple) allowable on the power supply line. Typically, for the case of silicon chip having 1 V power supply with the maximum current pumping of 100 A, the maximum allowable ripple is 10% because of which the Z_{target} is alarmingly low i.e., 1 mΩ. However, there is an important point to be taken care that the Z_{target} at each level of PDN must be relevant across the current transient times [15] or else there is the possibility of PSN contamination. So, in most ideal cases, it is observed that the on-chip current transient times are around 10% of the on-chip clock frequency.

4. Methodologies to suppress on-chip power supply noise

The impact of PSN over on-chip circuits is suppressed using different reduction and isolation techniques. These strategies are broadly classified in three areas as depicted in **Figure 5**.

The very fundamental method of stopping the generation of PSN is to increase the current transient time because that subsequently reduces the di/dt noise. In fact, there is a similar approach which is known as current spreading [16]. This technique spreads out the switching activity over an extended period and thereby decreases the amount of i(t) pumped into the on-chip circuits.

4.1 Circuital approaches

One of the primitive circuital attempts to increase the current transient time is reported in [17]. Stretching the time stamp actually helps to compute the average value of i(t) at moderate level. This helps in dropping the content of resistive noise as well as some part of inductive noise since the value of current ramp – di/dt is also at low range. Hence cumulatively, PSN is diminished. Even the noise immunity to PSN is increased with the incorporation of circuital tweaking [6]. For instance, the weak voltage keepers can be used in the design of dynamic logic based on-chip circuits which can significantly reduce the effects of noise i.e., eliminate the logical failures in these circuits by providing weak feedback to their critical circuital nodes. In case of analog circuits, differential signaling is used to validate the occurrence of PSN as common-mode noise [6]. Since the differential signaling creates an on-chip communication between digital and analog modules inside the chip to have separate individual power supplies from the main supply source, there is least chance that the digital V_{dd} intersecting the analog one. So there is voltage of V_{dd} remain intact. However, in situations where the circuital approaches are not enough to alleviate PSN, people try to incorporate the non-circuital approaches.

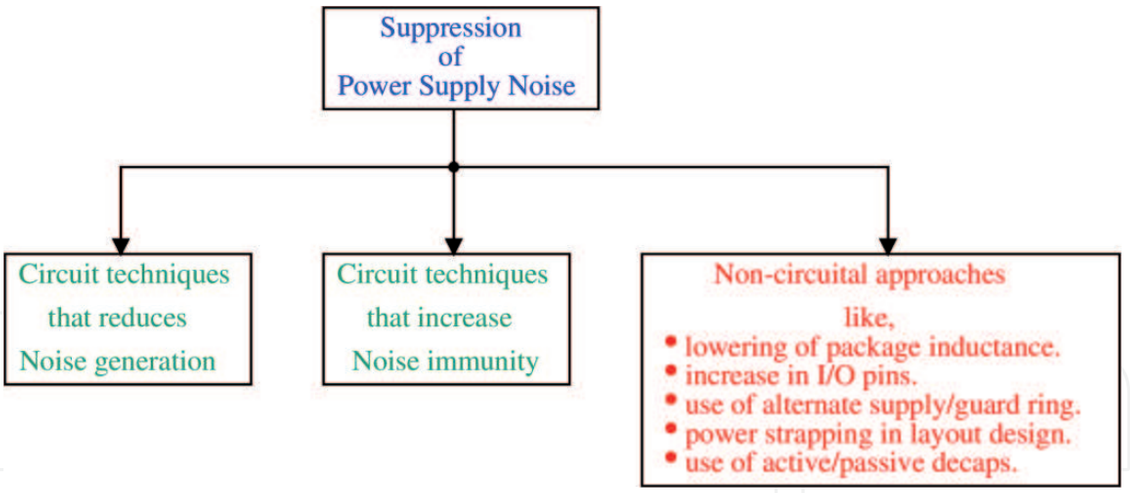

Figure 5.
Various strategies for PSN suppression.

4.2 Non-circuital approaches

Basically, the non-circuital approaches are the ones which can be imposed only during the chip fabrication. Like for example, the level of parasitic inductance in the supply path is lowered by implementing C4 flip-chip technology instead of typical wire-bonding technology. This helps in the reduction of inductive noise and even the resonance effect in any system. Consequently, the occurrence of PSN is suppressed to a substantial level. Another strategical approach is to increase the number of pins assigned for the power supply section. However, in this particular approach there is always physical limitation like the pin count can be predefined. So typically, alternative and multiple power supply sources are used for critical on-chip circuitries, like, the analog domain and digital domain has dedicated and independent power supplies such that the analog circuitries can never get hindered by the noisy digital supplies. Besides, there is always some guard rings to shield the power supplies from the contamination of noise. But the efficacy of these guard rings in most modern process technologies is questionable due to the use of low resistive substrates [18]. Therefore, the physical designers are more enthusiastic to play with the routing schemes of the power supply section which is often referred as power strapping [19]. Apart from this, one of the popular non-circuital approach to suppress PSN is by implementing on-chip decoupling capacitors (abbrev. "decap") which are of two different types viz., active decap and passive decap. The placement of small decaps in contrast to single large device reduces the impact of parasitic resistance and inductance in the supply line [20]. Hence, the rate of PSN is diminished. Typically, the passive decaps are preferred over the active decaps because the rate of noise suppression is higher in case of passive decaps compared to the active decaps [20].

As a matter of fact, the non-circuital approaches are the fixed solution for the alleviation of PSN, but their execution process and engineering is very costly. From the circuit designer point of view, we would prefer circuital tweaking and techniques to reduce PSN, however accepting that there are also challenges.

5. Challenges faced in suppressing on-chip power supply noise

In the earlier sections, there has been discussion on problems asserted by PSN to the proper functioning of on-chip circuitries inside the modern ICs. The typical PSN suppression methodologies was highlighted. But reducing PSN can be very

challenging. For example, the circuital modifications which are planned to be implemented for reducing PSN are rarely process independent. So generally, the extra transistors that are employed for checking the level of PSN, behave different from what is expected and the suppression of PSN is hindered. Another major issue is the scale down of process technology in the recent days. The impact of technology scaling over signal-to-noise ratio (SNR) with respect to the on-chip clock frequency is really adverse because the SNR is never constant in presence of fluctuating clock frequency due to scaling.

It has been mentioned about the use of weak voltage keepers for suppressing PSN. But in actuality, the weak feedback provided by these keepers does not prevent delay failures and hence it cannot be inferred as the general-purpose solution for noise suppression. Even the use of different V_{dd} for analog and digital domain faces problem like the voltage headroom (i.e., voltage range within the V_{dd} and ground plane) is different in each case and wherever the on-chip analog/digital circuits are interfaced, most of the time, there is issues with logic level of the propagating signals. In fact, the differential signaling used by the analog circuits to reduce PSN is only possible if both the analog/digital section share a common ground line. But as per the chip requirement, the analog ground is mostly kept separate from the digital ground so as to avoid resonance. Therefore, the use of differential signaling is conditional and rarely approached for the suppression of PSN.

However, there has been lot expectation with the implementation of decaps in context to the suppression of PSN, but it also faces crucial challenge while doing the job. Basically, the decap absorb supply noise like there happens to be drop in battery potential while the battery is connected to any electrical load. But again, similar to the battery, the decap requires definite time for charging and discharging which oppose the quick changes in supply voltage. In fact, the on-chip reactance of these decaps is so high during low frequency functioning of the chip that as soon as the supply voltage fluctuates, it badly affects the on-chip performance. Therefore, the PSN suppression using decaps is rarely accepted worldwide in the recent days.

In retrospective of the present scenario on how suppression of PSN is facing challenges, both the circuit designers and researchers are looking for appropriate solutions which can mitigate PSN irrespective of any dependencies. From the last decade, there has been some potential circuital approaches coming up which has shown good result in the suppression as well as in the alleviation of PSN.

6. Probable solution to reduce the on-chip power supply noise

An attractive solution to reduce the PSN has been found in recent years with the incorporation of variable frequency signaling (i.e., some MHz to GHz as shown in **Figure 6**) because it has the nice ability to curb random fluctuations in the power supply voltage or current [21].

The variable frequency clock (VFC) as it is popularly known, is used in the timing and control unit of the modern processors to automatically adjust the frequencies of various components inside the processor [22–24]. The measure of frequency directly impacts the switching activity of the on-chip circuital nodes. So, when the frequency is low, and the corresponding current transient time is high, the amount of i(t) and di/dt is less. At a stretch, as the frequency increases, the switching activity increases along with the measure of i(t) and di/dt. But in the average, both i(t) and di/dt has moderate values which is the main reason why PSN get reduced when the conventional system clock (typically in the range of some GHz) is replaced with VFC inside the chip.

Basically, the VFC is inserted to CDN and connect the corresponding clock trees. So, when it is propagating through the lines (like the way shown in **Figure 3**), the buffers draw current from the power supply (V_{dd} and ground). But this time, the buffer input is a VFC rather than a conventional clock, so the average value of voltage fluctuation (which occurs due to PSN) is very nominal and does not impact the timing parameters. Therefore, the inclusion of VFC instead of conventional clock helps the CDN to synchronize the clock signal at each and every sequential block inside the chip.

Apart from this advantage, the inclusion of VFC also help to modulate the flow of i(t) for any inside the chip sequential circuit. Typically, the i(t) plot is similar to what is shown in **Figure 7(a)**. But since the current pumping due to VFC in the initial stages till wake-up is slow and steady, the i(t) plot ideally looks like the one shown in **Figure 7(b)** and after the VFC reach its highest frequency, the current profile is almost similar to that of conventional clocking. This is also an added advantage for the average di/dt and reduces the impact of PSN.

However, the initial designs of VFC could not generate right pattern of clock (like the one shown in **Figure 6**) because of which the values of di/dt as well as the frequency ramp (i.e., change of frequency per unit time) has been random and large, leading to no control over PSN. In 2010, the IBM (International Business Machines Corporation) T.J. Watson Research Center [25] reported a SOI (System-On-Insulator) based VFC which produce frequency starting from 800 MHz to 12GHz with a minimum average frequency ramp of 17.5 MHz/μs and impressively reduced the measure of di/dt as well as PSN. But, the architecture of this VFC comprise of complex circuitries like digital phase locked loop (DPLL) and digitally controlled oscillator (DCO) which are power-hungry designs and derive large instantaneous current over a period of time. In fact, in 2018 also, a group of HKUST – Hong Kong [26] came up with a VFC design (made of time-to-digital convertors and digital loop filters) to generate variable frequencies having tuning range from 82GHz to 108GHz stirring a high start-up current with its peak value being quite high. Though, both these VFC design could successfully reduce PSN, their architectural complexities created scope for other researchers to find out more appropriate solution.

Hence, the work of IBM researchers [25] was carried forward in [27] and their VFC architecture was redesigned to develop a tuning range from 250 MHz to 2GHz with only the involvement of components like flip-flop-based frequency dividers, multiplexers and simple decision circuits. In fact, while checking the performance of this VFC to drive a sequential core, it was found that the peak position of the current drawn inside the core is attained after 40 clock cycles, which is otherwise noted only after 10 clock cycles when steered by the conventional system clock. Thereby, this VFC architecture ascertains long wake-up time for the system clock, thus reducing the i(t) and di/dt. But this VFC failed to attain the current transient time as small as compared to what was achieved by the IBM researchers. So, this VFC architecture was modified by reducing the circuit overhead and distributing the modules and sub-modules of the VFC in different cores of the chip [28]. That helped outstandingly in the improvement of i(t) and di/dt and also reduced the PSN with much effect.

However, as it is noted that the switching activity is a prime facet for the instigation of i(t) and di/dt, we have tried implementing clock gating to the conventional

Figure 6.
Example of a variable frequency signaling.

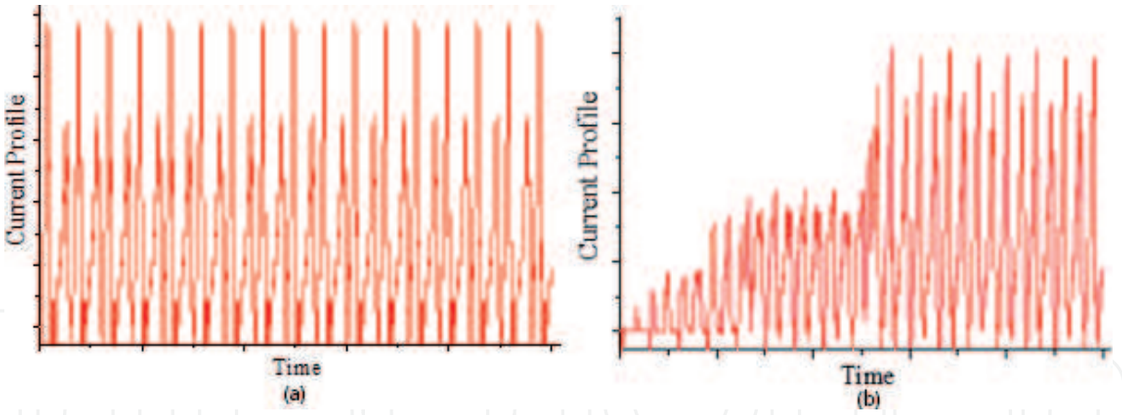

Figure 7.
Instantaneous current flow due to (a) conventional clock (b) VFC.

system clock so as to restrict the activity factor (α). There are many on-chip components which do not function at the same time instance like all the others. But because they are connected to the same system clock, the current pumping (i.e., i(t) and di/dt) happens across these components in spite of they are not participating to the on-chip activity at that point of time. In [29], we have already projected how the implementation of clock gating has helped in the minimization i(t) and di/dt as well as the curbing of PSN. Nevertheless, we have notion that if VFC and the clock gating are used together in an on-chip single platform, then there can be possible reduction of PSN.

7. Conclusion

This chapter is dedicated for the discussion on what are the implications of on-chip PSN and the corresponding ways to mitigate and suppress it quantitatively. Over the years, the impact of PSN has been so adverse on the functioning of on-chip components, that the circuit designers and researchers had to narrow down the best possible options for PSN mitigation and classify these options as circuital and non-circuital approach. However, there is not much scope of deterministic non-circuital solution to the issues brought up by PSN because of the constant upgrading in the semiconductor manufacture.

In case of the circuital approach, it has been pointed out that by manipulating the on-chip clock activity, the major factors of PSN (i.e., i(t) and di/dt) can be in control. Until now, the introduction of VFC and clock gating individually inside the on-chip clock section has been the two most important circuital solutions for the PSN problems. However, this PSN controllability can be further enhanced by incorporating the VFC and clock gating together in place of the conventional system clock assuring that the chip functionalities are not compromised.

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Conflict of interest

The authors declare no conflict of interest.

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