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Graphene Nanowire Based TFETs

*Jayabrata Goswami, Anuva Ganguly, Anirudhha Ghosal
and Jyoti Prakash Banerjee*

Abstract

The present work is aimed at improving the performance potential of tunnel field effect transistors (TFETs), where the carriers are transported by the process of band to band tunneling. The nanoscale TFETs serves the purpose of ULSI integration with high speed and memory. The requirements of new device technology are challenging: for logical switching. In this paper, a p-channel graphene nanoribbon (GNR) TFETs has been analyzed and designed for low power and high performance digital switching application. The energy band diagram of the device is obtained from self-consistent iterative method for numerical solution of one-dimensional Poisson's equation subject to appropriate boundary conditions. It is observed that the optimized p⁺ channel GNR TFET provides high ON-OFF current ratio, low sub-threshold slope for a channel length of 85 nm and channel width of 4 nm.

Keywords: TFET, GNR, sub-threshold slope

1. Introduction

The fundamental limitation of silicon MOSFETs in gigascale integration has led to the proposal of several non-classical transistors as the future replacement. In recent years tunnel field effect transistors (TFETs) are attracting the attention of researchers due to their low sub-threshold slope much below the thermionic limit of 60 mV/decade for silicon MOSFET at room temperature along with their low-voltage application and low power consumption. A low voltage tunnel transistor beyond CMOS logic was proposed by Seabaugh and Zhang [1] in 2010. It is reported that TFETs with Si as channel material exhibit low ON state current density (100 $\mu\text{A}/\mu\text{m}$) [2] due to large bandgap of Si. If a lower band gap material, Ge is used as channel material in TFETs, the ON state current increases to 850 $\mu\text{A}/\mu\text{m}$ [3]. A heterojunction TFET with Si as channel material and lower bandgap semiconductors such as $\text{In}_x\text{Ga}_{1-x}\text{As}$ as source material leads to improved performance of the device. Graphene is an emerged electronic material due to its highest carrier mobility and carrier saturation velocity at room temperature among all semiconductor materials [4]. However, the bulk graphene sheet is a semimetal with a zero bandgap and cannot be used for room temperature transistors with sufficient on/off ratio. The main challenge is to apply graphene for digital electronic or photonic applications. Graphene nanoribbons (GNRs) of sub-10 nm width are found to be semiconducting due to lateral confinement of the electron wave function in the transverse direction with a band gap inversely proportional to the conducting channel width. Further the low-energy electronic states of graphene have two non-equivalent mass less Dirac spectrum. The confinement gap (ΔE) in GNRs is

inversely related with the ribbon width (w_{GNR}) [5]. Thus GNR with narrow widths (15 nm) has been reported as a channel material for room temperature operation of Tunnel Field Effect Transistor (TFET) providing high ON-OFF current ratio [6]. In this paper authors used one dimensional Poisson equation to evaluate energy band diagram, surface potential subject to appropriate boundary conditions. The basic performance parameters of the device such as On-state current, On-Off current ratio, sub-threshold slope are calculated for high performance digital applications.

2. Structure of device

Figure 1 shows a p-channel tunnel field effect transistor using graphene nanoribbon(GNR) with highly doped source, channel and drain region, respectively. Here t_{OX} and t_{GNR} are represented as gate oxide and nanoribbon thicknesses, respectively. A high-k gate dielectric Y_2O_3 is chosen in between of gate and GNR. The channel of the GNR TFET is fully depleted for both in Off and On state of the device. A thin layer of graphene is deposited in the Si substrate to form a graphene nanoribbon as channel material of the device.

Now from numerical solution of following one-dimensional Poisson equation for the purpose of surface potential and energy band diagram of the device is obtained by [7]

$$\frac{d^2\phi_{\text{surf}}(x)}{dx^2} - \frac{\phi_{\text{surf}}(x) - V_{\text{GS}} - V_{\text{BI}}}{\lambda^2} = - \frac{q\rho(x)}{\epsilon_{\text{GNR}}} \quad (1)$$

where V_{GS} is the gate to source potential, V_{BI} is the built-in potential, $\phi_{\text{surf}}(x)$ is the surface potential at position x , λ is the screening length for the particular device structure, $\rho(x)$ is the total charge density and ϵ_{GNR} is the permittivity of GNR.

The screening length λ is

$$\lambda = \sqrt{\frac{\epsilon_{\text{GNR}}}{\epsilon_{\text{OX}}} t_{\text{GNR}} t_{\text{ox}}} = \sqrt{t_{\text{GNR}} t_{\text{ox}}} \quad (2)$$

The boundary conditions are for the calculation of energy band diagram as follows:

- i. The electric field is zero at both side of the device i.e. source and drain ends.
- ii. At the source-channel and drain-channel junction a continuous electric field potential exist.
- iii. $\xi_F - \xi_C = qV_T$ at the source region and $\xi_V - \xi_F = qV_T$ at the drain region.
- iv. At zero gate potential the Fermi level of the device is aligned with the valence band of the channel.

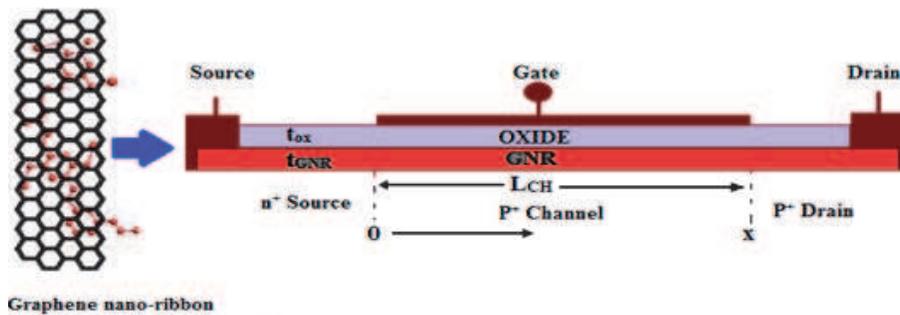


Figure 1.
P-channel tunnel field-effect transistor using graphene nanoribbon.

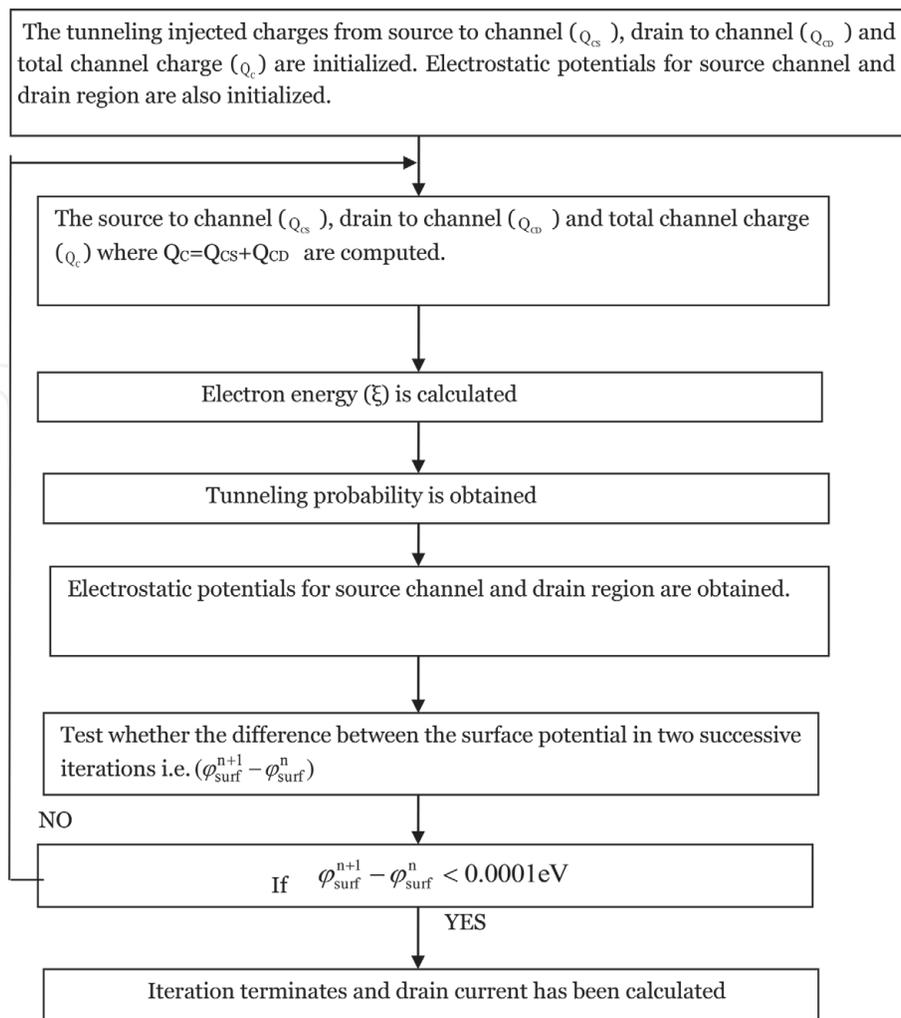


Figure 2.
 Flow chart to obtain the energy band diagram and drain current.

The flow chart for the self-consistent iterative method to obtain the drain current is given in **Figure 2**.

The of tunneling probability as a function of energy is written as

$$T_S(\xi) = \exp\left(-2 \int |k_x| dx\right) \quad (3)$$

where k_x is the wave vector.

The drain current is calculated from following Landauer's equation [8].

$$I_D = \frac{q}{\pi \hbar} \int (f_D(\xi) - f_S(\xi)) T_S(\xi) d\xi \quad (4)$$

where f_s and f_d is the Fermi distribution function regarding source and drain regions and \hbar is the reduce Plank's constant, respectively.

3. Results

The basic energy band diagram of the GNR PTFET is shown in **Figure 3a, b** in Off state ($V_{GS} = 0$ V, $V_{DS} = -0.1$ V) and On state ($V_{GS} = -0.1$ V, $V_{DS} = -0.1$ V) at channel length 85 nm and width 4 nm, respectively.

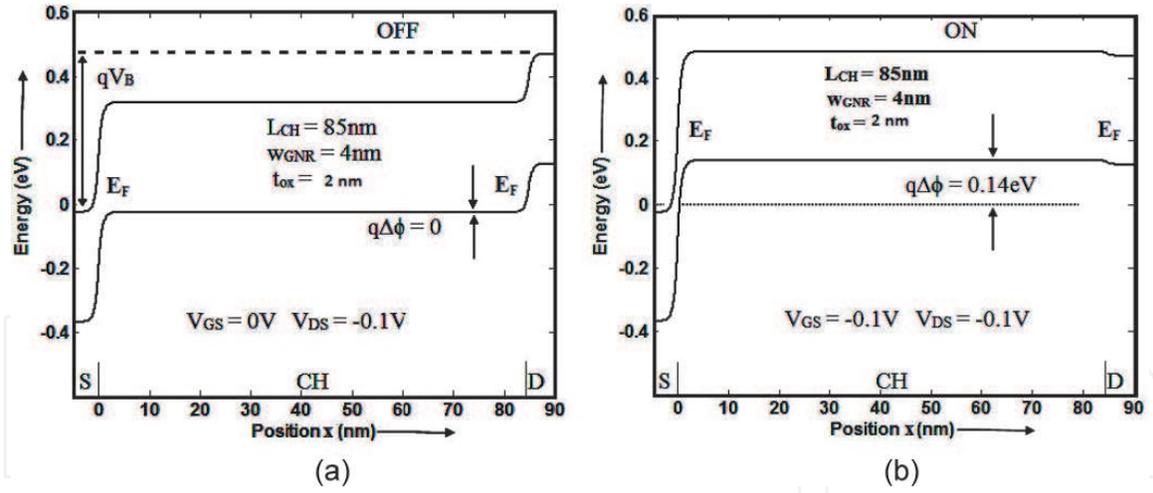


Figure 3.
 (a) Off state energy band diagram of GNR PTFET. (b) On state energy band diagram of GNR PTFET.

Figure 3a shows that no band to band tunneling occurs in the OFF state. But in **Figure 3b** shows that the significant tunneling of carrier can occur properly in ON state of the device.

The OFF current for long channel GNR ($L_{CH} = 85$ nm) arises from thermionic emission over the barrier only and direct source to drain tunneling is negligibly small. Therefore The OFF current in GNR is written as [9]

$$I_{OFF} = [q^2 V_T / \hbar \pi] \exp(-V_B / qV_T) \quad (5)$$

where qV_B is the barrier height and qV_T is the thermal energy.

Figure 4a shows the ON/OFF current ratio versus gate to source bias (V_{GS}) for five different channel lengths from 45 to 85 nm in steps of 10 nm for fixed ribbon width of 4 nm and oxide thickness of 2 nm. It is observed that the ON-OFF current ratio increases with the increase of channel length. The ON-OFF current ratio increases from 2.34×10^3 to 4.96×10^4 at $V_{GS} = -0.1$ V when the channel length

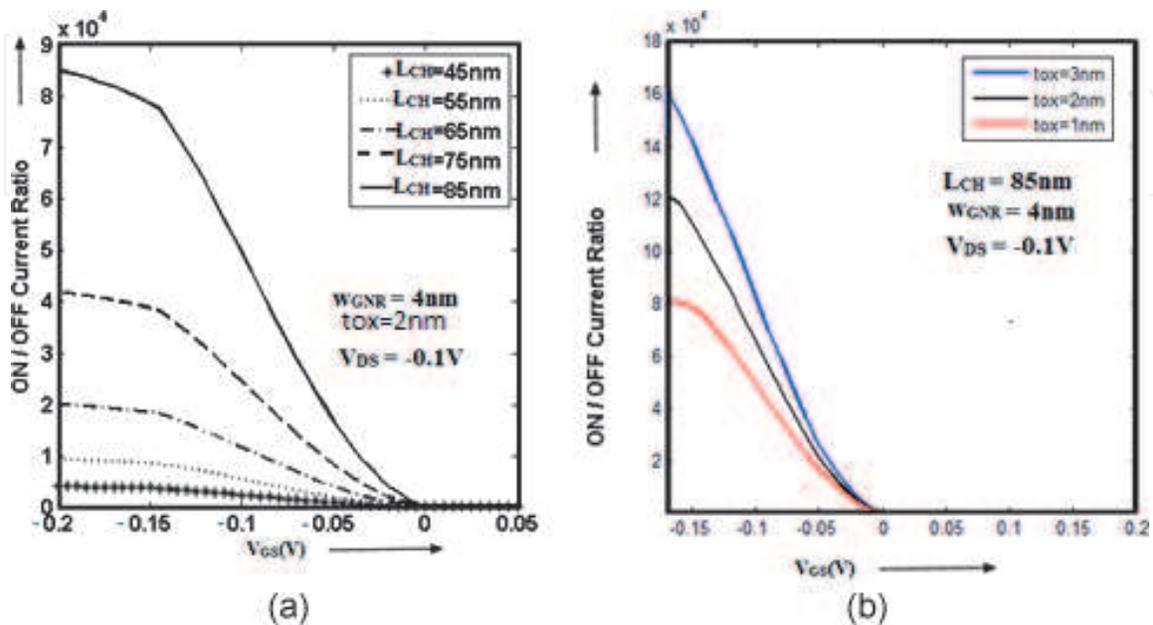


Figure 4.
 (a) ON/OFF current ratio versus V_{GS} for different channel lengths of GNR PTFET. (b) ON/OFF current ratio versus V_{GS} for different oxide thicknesses of GNR PTFET.

increases from 45 to 85 nm. The ON–OFF current ratio reaches a maximum of 4.96×10^4 at $V_{GS} = -0.1$ V for $L_{CH} = 85$ nm. The higher ON–OFF current ratio for longer channel length at a particular gate-to-source bias and fixed ribbon width and oxide thickness can be explained as follows: In case of longer channel length, the total tunneling path length increases since tunneling takes place through all paths from source to drain. Thus tunneling probability will increase as seen from Eq. (3) so that drain current increases. **Figure 4b** shows the ON–OFF current ratio versus V_{GS} for three different gate oxide thicknesses (t_{ox}).

Figure 5 shows On state current versus gate to source voltage of GNR PTFET with different widths. The simulated results show that higher value of ribbon width on current is increase significantly.

Figure 6 shows the on state current density versus V_{GS} for GNR PTFET corresponding to $L_{CH} = 85$ nm, $W_{GNR} = 4$ nm and $t_{ox} = 2$ nm. The maximum on-state current density is found to be $590 \mu\text{A}/\mu\text{m}$ at $V_{GS} = -0.1$ V. The sub-threshold slope is given by

$$SS = \frac{\partial V_{GS}}{\partial(\log I_D)} \quad (6)$$

The sub-threshold slope is found 2.76 mV/decade from equation (6) at channel length 85 nm and ribbon width 4 nm, respectively.

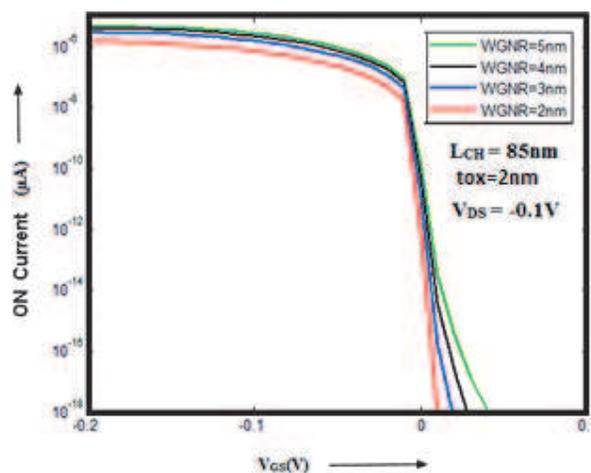


Figure 5.
 ON current versus gate to source voltage of GNR PTFET for different GNR widths.

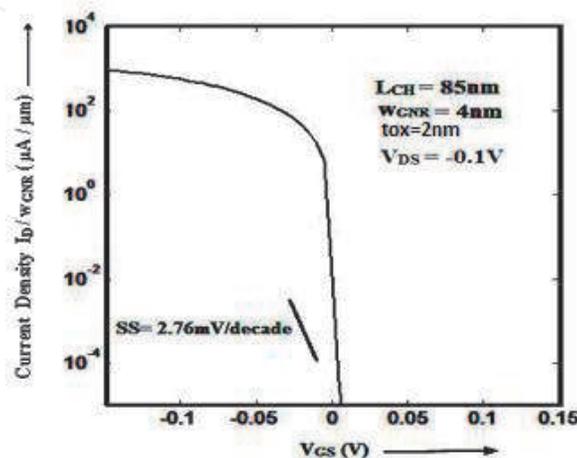


Figure 6.
 ON-state current density versus gate to source voltage (V_{GS}).

Figures of merit	Parameter values with units
Current density I_D/w_{GNR}	590 ($\mu\text{A}/\mu\text{m}$)
Off state current	0.0092 (pA)
$I_{\text{ON}}/I_{\text{OFF}}$ ratio	4.96×10^4
SS	2.76 (mV/decade)

Table 1.
Structural parameters of GNR PTFET.

Table 1 structural parameters of GNR PTFET:

$$L_{\text{CH}} = 85 \text{ nm}, w_{\text{GNR}} = 4 \text{ nm}, t_{\text{ox}} = 2 \text{ nm}$$

$$V_{\text{GS}} = -0.1 \text{ v}, V_{\text{DS}} = -0.1 \text{ v}.$$

4. Conclusion

The results show that the graphene nanoribbon based Tunnel Field Effect Transistor (GNR-PTFET) provides higher on–off current ratio, lower sub-threshold slope for better switching in digital circuits using low voltage power supply. The values of $I_{\text{ON}}/I_{\text{OFF}}$, SS of the optimized device are 4.96×10^4 , 2.76 mV/decade at channel width and length is 4 nm and 85 nm, respectively. Therefore this device is useful for high performance digital switching applications.

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