Chapter

Design of 4-Bit 4-Tap FIR Filter Based on Quantum-Dot Cellular Automata (QCA) Technology with a Realistic Clocking Scheme

Ismail Gassoumi, Lamjed Touil, Bouraoui Ouni and Abdellatif Mtibaa

Abstract

The increasing demand for efficient signal processors necessitates the design of digital finite duration impulse response FIR filter which occupies less area and consumes less power. FIR filters have simple, regular and scalable structures. This paper represents designing and implementation of a low-power 4-tap FIR filter based on quantum-dot cellular automata (QCA) by using a realistic clocking scheme. The QCADesigner software, as widely used in QCA circuit design and verification, has been used to implement and to verify all of the designs in this study. Power dissipation result has been computed for the proposed circuit using accurate QCADesigner-E software. The proposed QCA FIR achieves about 97.74% reduction in power compared to previous existing designs. The outcome of this work can clearly open up a new window of opportunity for low-power signal processing systems

Keywords: QCA technology, QCA designer, FIR filter, low power, QCA pro

1. Introduction

Recently, the design of high-performance digital circuits meeting area, power and speed metrics has become a challenge. On one side, several digital signal processing applications are based on complex algorithm which requires great computational power per silicon area. On the other side, there are stringent portability and energy requirements which further complicate the design task. Therefore, achieving the required computational throughput with minimum energy consumption has become the key design goal, as it contributes to the total power budget as well as reliability of target application. So far, VLSI industry has been successfully following Moore's law. Simultaneous reduction in critical dimensions and operating voltage of CMOS transistors yields higher speed and packaging density while decreasing the silicon area and power consumption [1]. However, this trend of successive transistor scaling cannot continue for long, as the CMOS technology is reaching its fundamental physical limits and entails many challenges [2–4]. Low-power digital design is being investigated at all levels of design abstraction.

At device level, a number of CMOS alternatives are summarized in International Technology Roadmap for Semiconductors (ITRS) report such as quantum-dot cellular automata (QCA), single-electron transistor (SET), carbon nanotube field-effect transistors (CNTFET) and resonant tunneling diodes (RTD) [5]. The use of (QCA) on the nanoscale has a promising future because of its ability to achieve high performance in terms of device density, clock frequency and power consumption [6–9]. Essentially, QCA offers potential advantages of ultralow-power dissipation. QCA is expected to achieve very high device density of 1012 device/cm^2 and switching speeds of 10 ps and a power dissipation of 100 W/cm^2 [10]. These features, which are not offered by CMOS devices, can open new opportunities to save power in mobile systems design. In addition, they can make the proposed QCA approach useful for signal and image processing systems applied on portable communication devices where real-time processing and low-power consumption are needed in today's world in order to extend battery life. Several attempts are made towards the cost-effective realization of QCA circuit in [11–19]. Whereas QCA technology has advantages over CMOS technology, various limitations are identified. Its include placing long lines of cells among clocking zones which leads to thermal fluctuation issue and increases delay of the circuit. Recently, a universal, scalable, and efficient (USE) clocking scheme [20] is a proposed technique to overcome the mentioned limitations. This scheme can design feedback paths with different loop sizes. It is regular and flexible enough to allow placement and routing, besides avoiding thermodynamic effects due to long wires. On the other hand, for designing several digital signal processors (DSP), finite impulse response (FIR) filter is widely used as a critical component. For their guaranteed linear phase and stability, the FIR filter is used for the conception of very highly efficient hardware circuits. Theses circuits perform the key operation in various recent mobile computing and portable multimedia applications. We denote high-efficiency video coding (HEVC), channel equalization, speech processing, software-defined radio (SDR) and others. Indeed, an efficient FIR filter design essentially improves the performance of a complex DSP system. This fact pushed designers to search for new methods to grant low-power consumption for FIR filter [21–28]. QCA logic design circuit is stimulated by its applications in low-power electronic design. It has lately attracted significant attention. All these above factors motivate us to investigate a new architecture around QCA by using USE clocking scheme, which can efficiently perform FIR operation.

The main concern of this paper is to present a new design for FIR filter based on QCA technology which yields significant reduction in terms of power. This paper is organized as follows. Section 2 presents the background of FIR filter structures. Section 3 indulges the preliminaries of QCA technology. Section 4 discusses the FIR filter power optimization by QCA technology. Section 5 shows the discussions and results of the proposed FIR filter-based technology. Finally, conclusions are drawn in Section 6.

2. Background of FIR filter structures

FIR filters are important building blocks among the various digital signal processing applications. Recently, due to the popularity of the portable battery-powered wireless communication systems, low-power and high-performance digital filter designs become more and more important.

An nth order FIR filter performs N-point linear convolution of input sequence with filter coefficients for new input sample. The transfer function of the linear invariant (LTI) FIR filter can be expressed as the following equation:

$$y(n) = \sum_{k=0}^{N-1} h_k x(n-k) \tag{1}$$

where N represents the length of the filter, h_k is the *Kth* coefficient, and $x(n-k)$ is the input data at time instant $(n-k)$.

The z transform of the data output is

$$Y(z) = H(z).X(z) \tag{2}$$

where H (z) is the transfer function of the filter, given by

$$H(Z) = \sum_{k=0}^{N} h_k Z^{-k} \tag{3}$$

Several architectures have been proposed in the last recent years. A filter can be implemented in direct form (DF) or transposed direct form (TDF) [29]. The transposed form and the direct form of a FIR filter are equivalent. It's easy to prove that, in direct form, the word length of each delay element is equal to the word length of the input signal. However, in the transposed form, each delay element has a longer word length than that in the direct form. The transposed structure reduces the critical path delay, but it uses more hardware. DF FIR filter is area-efficient, while the TDF filter is delay-efficient. In this paper, the architecture of the proposed FIR filter is presented. It is based on the transposed direct form FIR filter structure as shown in **Figure 1**. This structure comprises adders, D flip-flops, and multipliers.

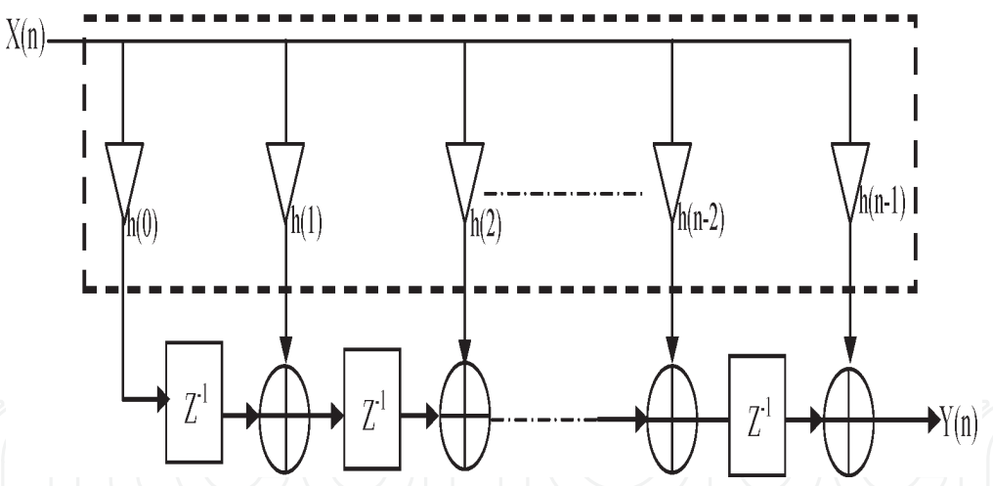

Figure 1.
Transposed direct form FIR filter architecture.

3. QCA review

The QCA approach, introduced in 1993 by Lent et al. [6], is able to replace devices based on field-effect transistor (FET) on nanoscale. This nanotechnology was conceived based on some of Landauer's ideas regarding energy-efficient and robust digital devices [30]. It consists of an array of cells. Each cell contains four quantum dots at the corner of a square which can hold a single electron per dot. Only two electrons diametrically opposite are injected into a cell due to Coulomb interaction [31]. Through Coulombic effects, two possible polarizations (labeled −1 and 1) can be shaped. These polarizations are represented by binary "0" and binary "1" as shown in **Figure 2**. **Figure 3** shows the propagation of logic "0" and logic "1," respectively, from

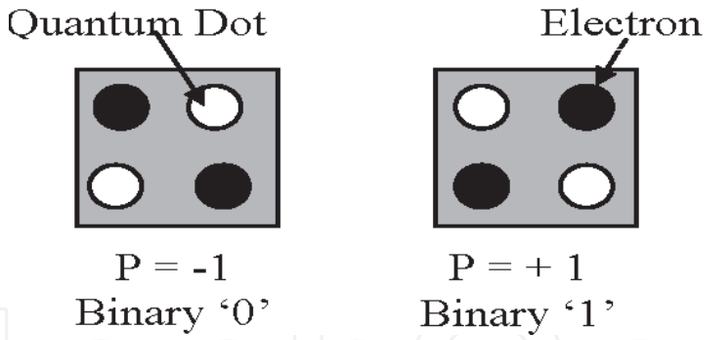

Figure 2.
Two different polarizations of quantum-dot cell.

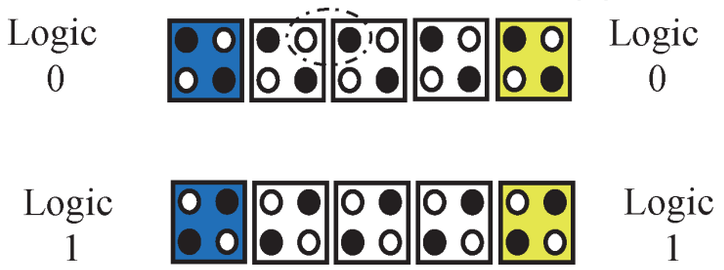

Figure 3.
QCA binary wires.

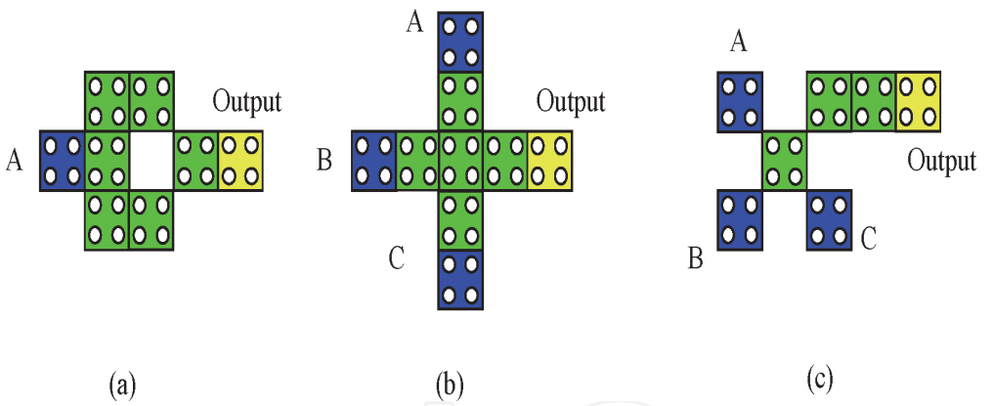

Figure 4.
Standard gates: Inverter gate (a) and majority gate (b, c).

input to the output in QCA binary wires due to the Coulombic repulsion. Generally, in neighboring cells, the coulombic interaction between electrons is used to implement many logic functions which are controlled by the clocking mechanism [32].

A majority and inverter gates are the fundamental logic gates in the QCA implementations which are composed of some QCA cells as shown in **Figure 4** [7, 33]. Furthermore, the majority gate acts as an AND gate and OR gate just by setting one input permanently to 0 or 1. It has a logical function that can be expressed by Eq. (4):

$$MV(a, b, c) = AB + BC + AC \tag{4}$$

3.1 QCA clocking

The clocking system is an important factor for the dynamics of QCA. Its principal functions are the synchronization of data flows and the implementation of

adiabatic cell operation which enables QCA circuits with high energy efficiency [34]. Generally, QCA clocking is presented with four different phases which are switch, hold, release and relax as illustrated in **Figure 5**. During the switch phase, which actual computations are occurred, the barriers are raised, and a cell is affected by the polarization of its adjacent cells, and a distinctive polarity is obtained. During the hold phase, the barriers are high, and the polarization of the cell is retained. During the release phase, the barriers are lowered, and the cell loses the polarity. During the relax phase, the cell is non-polarized [35].

Over recent years, various clocking schemes have been proposed, but they have introduced some difficulties such as long paths for feedbacks [35]. Recently, USE clocking scheme is a proposed technique for clocking and timing of the QCA circuits. It may be implemented using actual fabrication technologies of integrated circuits. This scheme can design feedback paths with different loop sizes, and its routing is flexible [20]. It defines a grid of clock zones, which are consecutively numbered from 1 to 4 as depicted in **Figure 6**. This grid ensures the correct arrangement for the clock zones. Much information about the clocking circuitry are mentioned in [20].

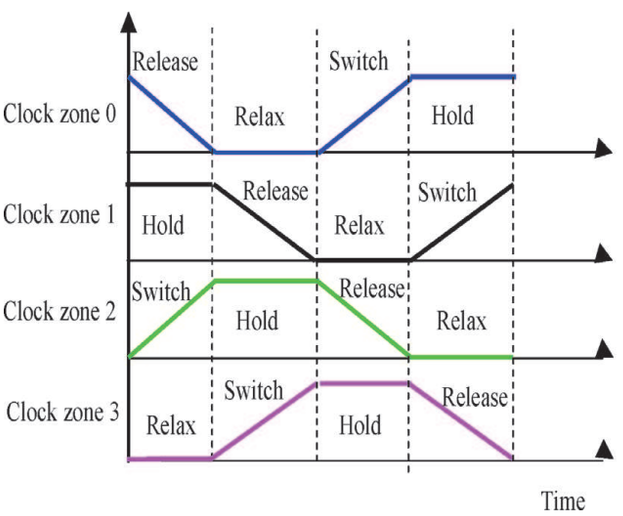

Figure 5.
QCA clock zones.

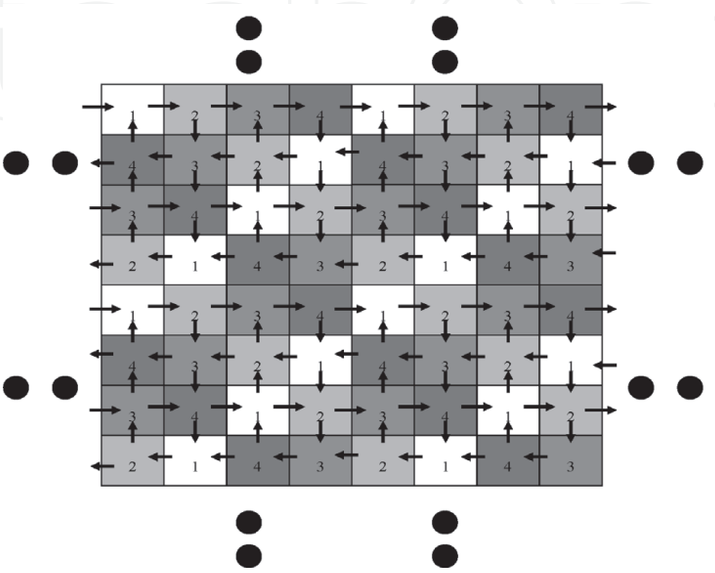

Figure 6.
QCA USE structure.

4. QCA FIR implementation

The proposed QCA FIR filter consists of three principal components:

- A D flip-flop to implement a simple delay
- A multiplier to implement the coefficients
- An adder to sum the nodes at the end of each tap

4.1 QCA D flip-flop

Flip-flop is a circuit that may be used to store state information ("0" or "1" logic value). Here, the structure of the proposed D flip-flop is illustrated in **Figure 7a** which includes three majority gates and one inverter gate. The logic equation of the D flip-flop is represented by the following equation:

$$Q_{(t)} = \mathrm{CLk.D} + \overline{\mathrm{CLk}}.Q_{(t-1)}$$

Figure 7b illustrates the proposed QCA flip-flop. It includes 79 cells with an area of 0.15 μm^2. It takes five clock periods for the inputs to reach the output, and first meaningful output comes on the sixth clock.

4.2 QCA 4 × 4 multiplier

Multiplier plays an important role in DSP systems. In divers' DSP application, it is not needed to utilize all output bits of multiplier. As in most of the FIR implementation, the FIR output can also be obtained using only the MSB bits of the multiplier output [29]. In literature, there are various algorithms of multiplier such as array multiplier, parallel multiplier and booth multiplier [36–39], which consumed more area and could not meet the criteria of propagation delay. This problem has been overcome in this paper by making use of Vedic multiplier which is much faster with minimum propagation delay [40–43]. To design the QCA circuit, we have used the version of the circuit proposed in [44]. **Figure 8** demonstrates the schematic of 4-bit Vedic multiplier architecture where $A = A_3A_2 \ldots A_0$ and $B = B_3B_2 \ldots B_0$ are the inputs and the outputs signal for the multiplication result are $P = P_7P_{6\ldots} \ldots P_0$. The implementation of this multiplier can be done by using four 2 × 2 Vedic multiplier blocks and three 4-bit adder blocks.

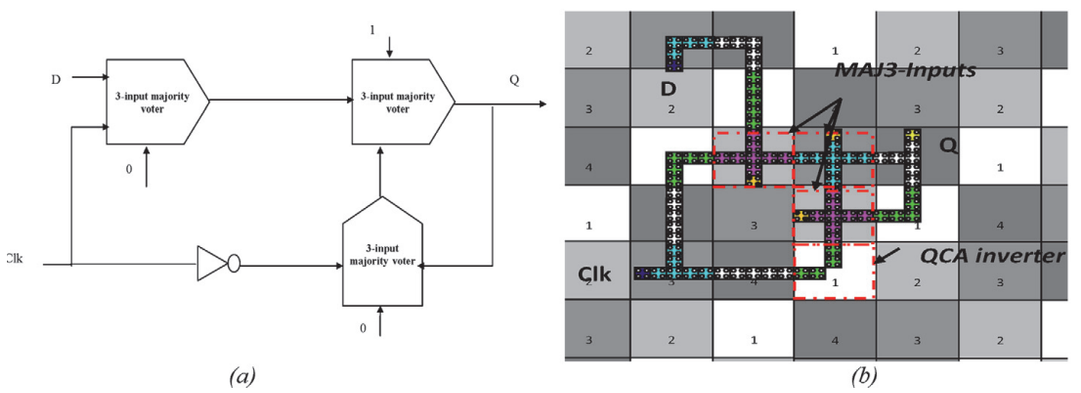

Figure 7.
Proposed (a) logical diagram and (b) QCA layout of D flip-flop.

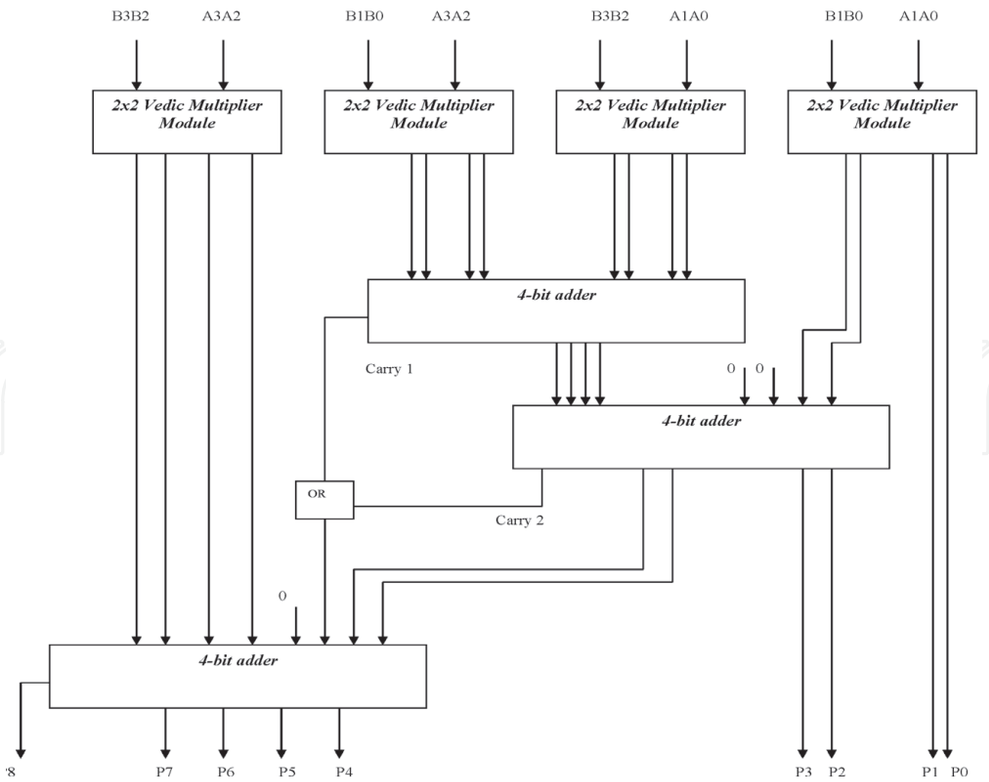

Figure 8.
Block diagram of 4-bit Vedic multiplier.

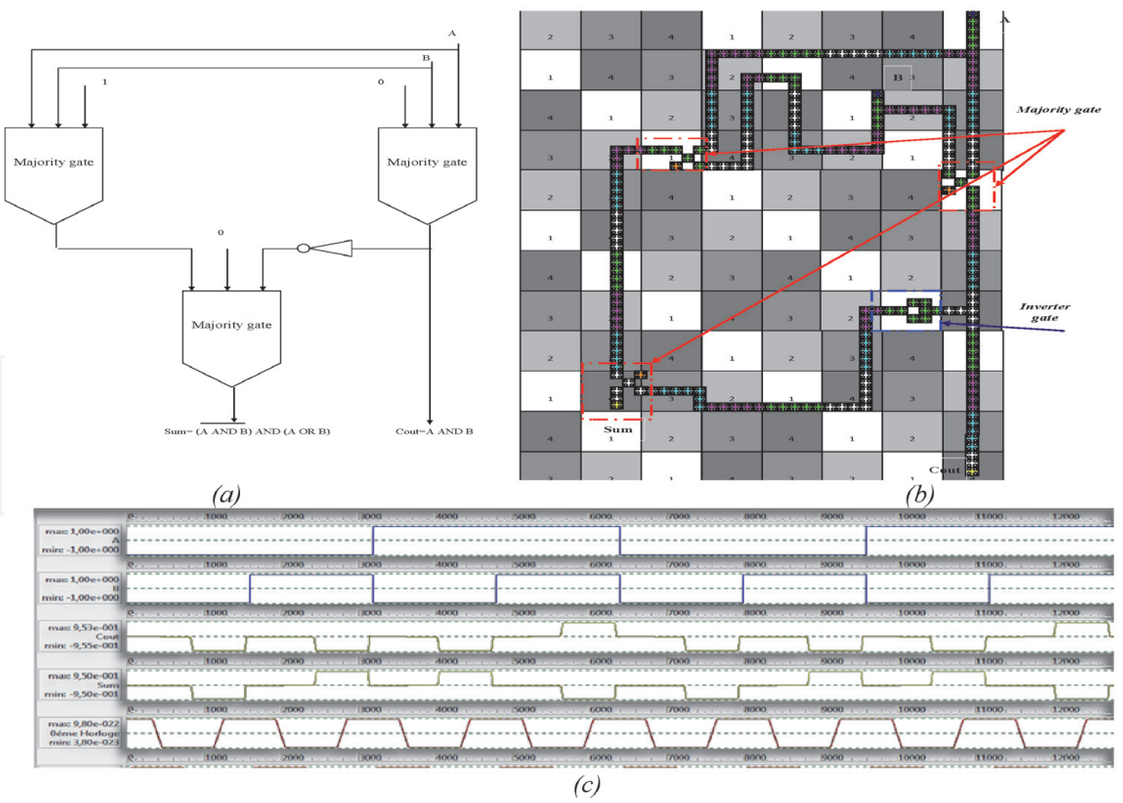

Figure 9.
Proposed (a) logical diagram, (b) QCA layout and (c) timing graph of half adder circuit.

4.2.1 QCA 4-bit parallel adder

The 4-bit adder performs computing function of the FIR filter. Therefore, the half and the full adder are used to construct the 4-bit binary adder. The proposed

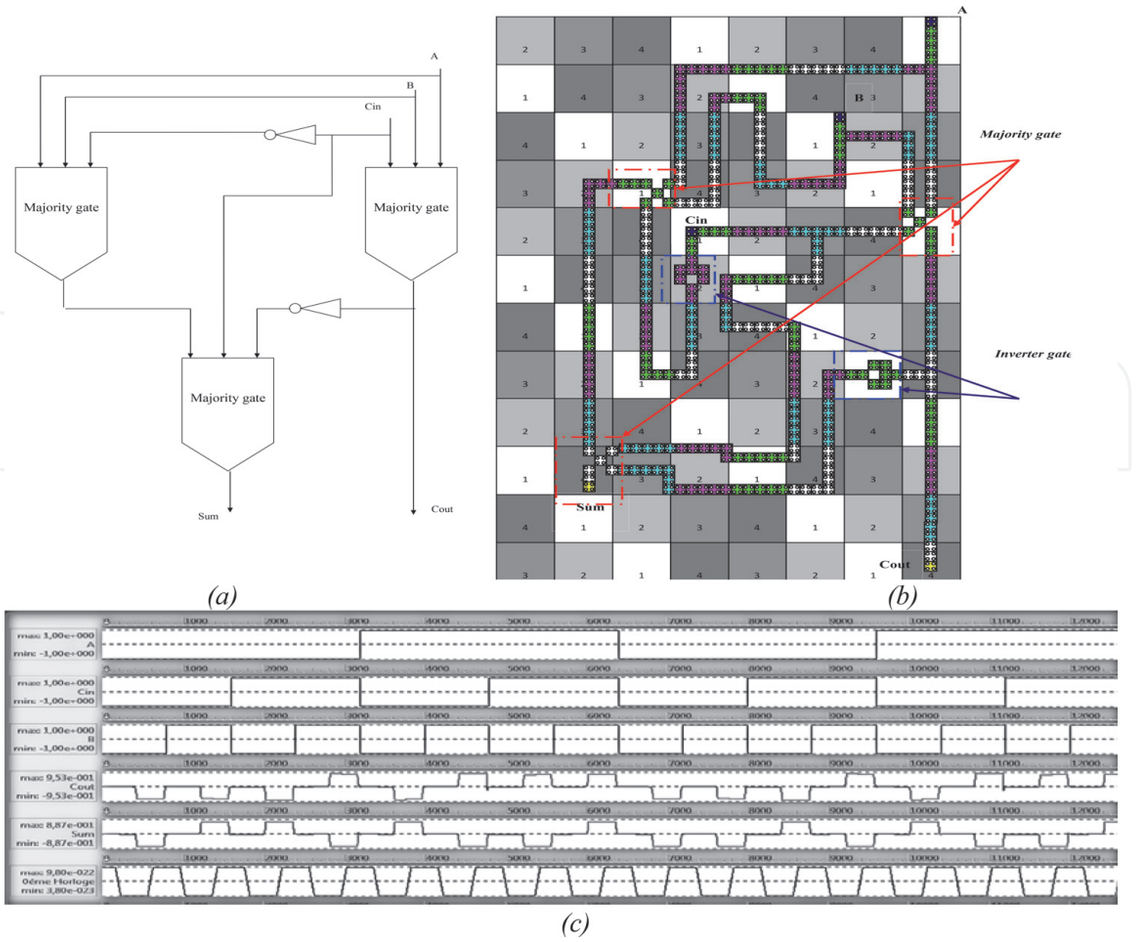

Figure 10.
Proposed (a) logical diagram, (b) QCA layouts and (c) simulation result of full adder circuit.

half adder is composed by three majority gates and one inverter gate. **Figure 9** shows the block diagram and the QCA layout of the proposed half adder. It consists of 232 cells covering an area of 0.76 μm^2. It needs 16 clock phases to generate the sum and carry outputs. In addition, the proposed full adder consists of three majority gates and two inverters. **Figure 10** depicts the block diagram and the QCA layout of the proposed full adder. For the proposed QCA full adder, the required number cells is 349, and the required area is 0.76 μm^2. It requires 16 clock phases. The parallel adder layout in size of 4-bit is depicted in **Figure 11**. It is designed by cascading one-half adder and three 1-bit adders. In this way, the carry out (Cout) is then transmitted to the carry in (Cin) of the next higher-order bit. The final outcome creates a sum of 4 bits plus a carry out (Cout 4). This design uses 2735 cells in its structure. It consists of a circuit area of 11.46 μm^2. This circuit has a critical path length of 61 clock zones which is designated by a blue dashed line.

4.2.2 QCA 2 × 2 vedic multiplier

The block diagram of 2 × 2 bit Vedic multiplier is shown in **Figure 12**. Firstly, B0 is multiplied with A0; the generated partial product is considered as an LSB of final product.

Secondly, B0 is multiplied with A1,and B1 is multiplied with A0. To add the generated partial products (B0*A1+ A0*B1), a QCA half adder is required, which generates a 2-bit result (Carry and S1), in which S1 is considered as the second bit of the final product and Carry is saved as pre-carry for the next step.

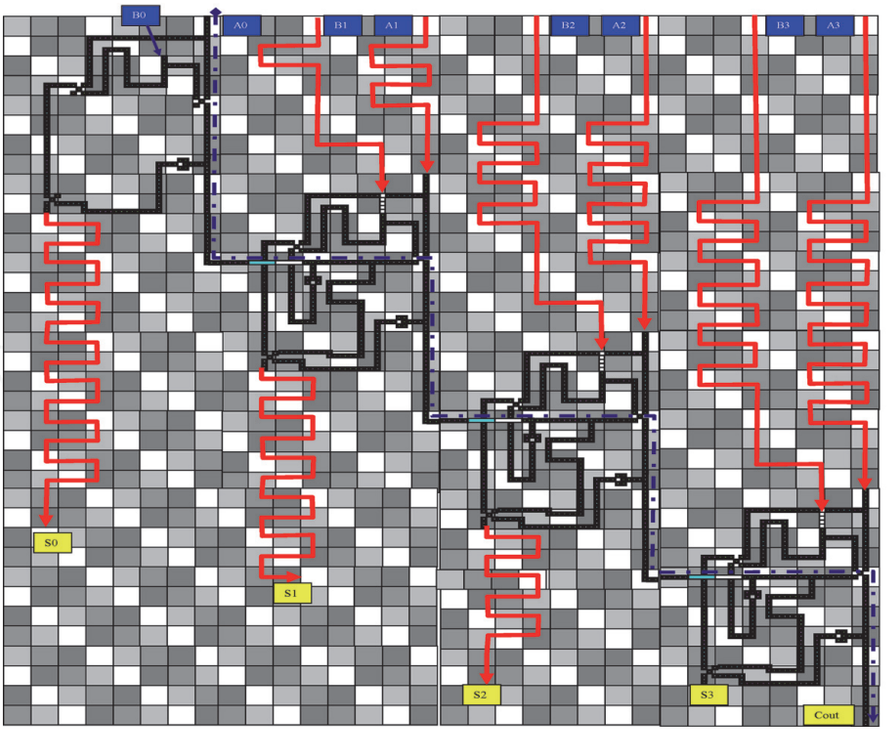

Figure 11.
Proposed QCA layouts of 4-bit parallel binary full adder.

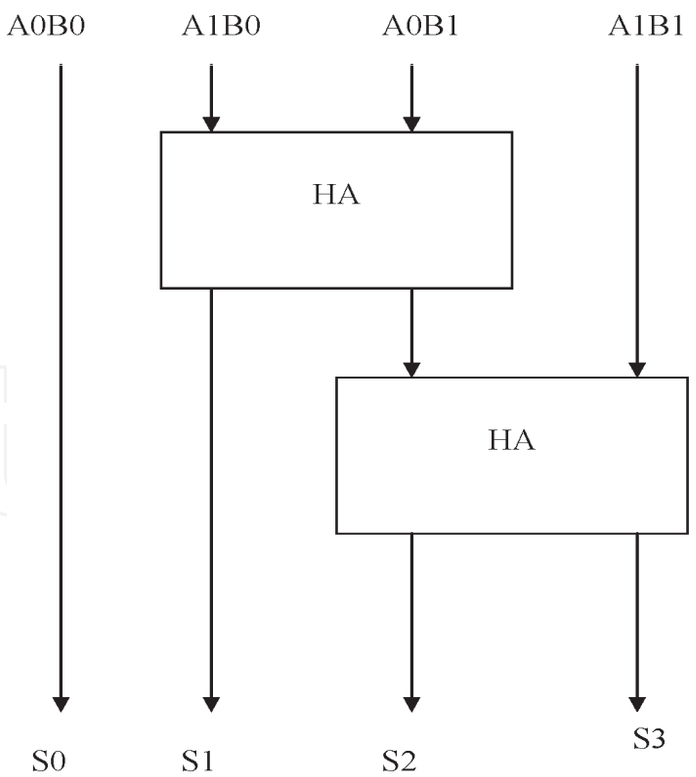

Figure 12.
2 × 2 block diagram.

Finally, B1 is multiplied with A1, and the overall product term will be obtained for 2 × 2 Vedic multiplier. Here, four majority gates and two half adder circuits are used, and the output will be four bits (s0, s1, s2 and s3).

The proposed 2 × 2 multiplier takes only 1683 QCA cells with a region of 8.42 μm^2.The simulated result of the proposed Vedic multiplier confirms that the expected operation is correctly achieved with 60 clock zones delay as depicted in **Figure 13**.

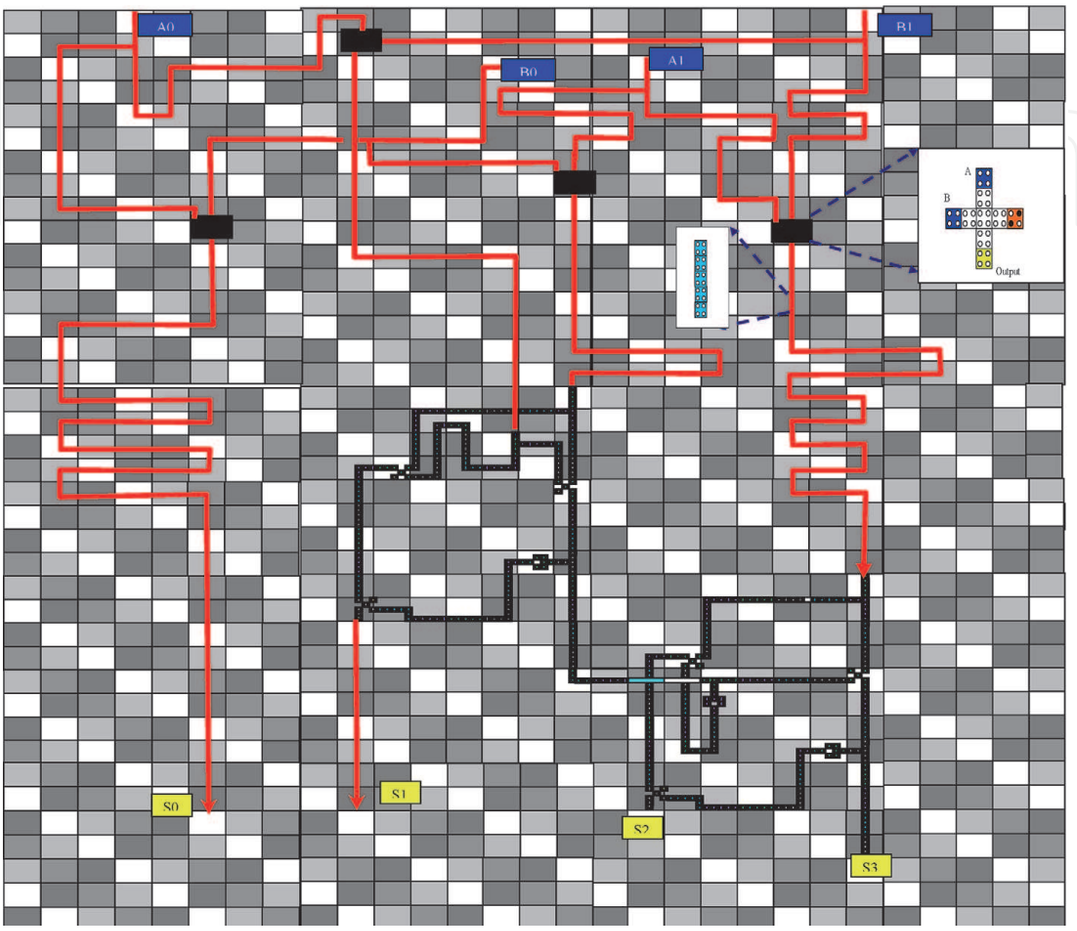

Figure 13.
The QCA implementation of 2 × 2 multiplier.

Parameter	Value
Number of samples	12,800
Convergence tolerance	0.001000
Radius of effect	65,000000 (nm)
Relative permittivity	12,900,000
Clock low	3800000e-023
Clock high	9800000e-022
Clock shift	0,000000e+000
Clock amplitude factor	2,000,000
Layer separation	11,500,000
Maximum iterations per sample	100

Table 1.
Bistable approximation parameter model.

4.3 QCA adder

Since the FIR output can be obtained using only the MSB bits of the Vedic multiplier output, for the proposed structure of FIR filter, we need a 4-bit QCA adder. The same 4-bit adder designed above is used in this subsection (**Table 1**).

5. Results and discussions

The complete QCA FIR design is implemented using the functional units discussed in the previous section. The implementation and the simulation of the proposed hardware designs are achieved by using QCADesigner 2.0.3 tool [45]. The coherence vector simulation engine is used for this purpose. **Table 2** depicts the simulation parameters. In the first step, the sub-module schematic and layout is completed and verified by functional simulations.

These designs have been implemented using a free and a regular USE clock scheme. In addition, we have successfully demonstrated that sub-module design of FIR unit properly satisfies all logic and timing constraints by using the 4×4 USE grid with a square dimension of 5×5 QCA cells. In this direction, with a well-defined methodology and regular timing zones, this design is a standard candidate for fabrication. We note that our proposed entire system requires a huge number of QCA cells mostly due to the long wires necessary to delay compensation. Since the proposed FIR circuit based on QCA technology has started to bloom, we have only compared the full adder module with regular standard scheme circuits. **Table 2** shows a comparison of the proposed full adder with some existing designs [35, 46]. The proposed full adder has 1.13, 56.9 and 11% improvements, respectively, in terms of cell count, area occupation and circuit latency as compared to that reported in [35].

In QCA technology, the power consumption of any circuit depends on the number of majority and inverter gates [47]. Therefore, this technology reduces more power than CMOS technology. The consumption of FIR unit in QCA-18 nm technology is valuing 1.6 mW. This value is carried out using QCADesigner-E software [48].

However, the QCA FIR circuit requires 97.74% lesser power consumption than the previous existing designs [49]. In addition, the proposed design of FIR filter can operate at a higher frequency (upper than 1 GHz) than the conventional solution, and it can be useful for future digital signal processing applications for providing excellent processing speed. The overall performance of the proposed QCA design is therefore superior to the existing techniques in terms of power consumption. In this way, we think that this work forms an essential step in the building of QCA circuits for low-power design in this area.

Influence of temperature variations on the polarization of the proposed design has also been investigated. **Figure 14** illustrates the effect of polarization on output of FIR circuit due to temperature variations. QCADesigner tool is used to observe this effect. By increasing temperature the AOP of any output cell of the QCA circuit

Design	Cell count	Area (μm^2)	Clock no. cycle
Full adder [35]	353	1.764	18
Full adder [46]	324	0.77	18
Proposed full adder	349	0.76	16

Table 2.
Comparison of various full adders.

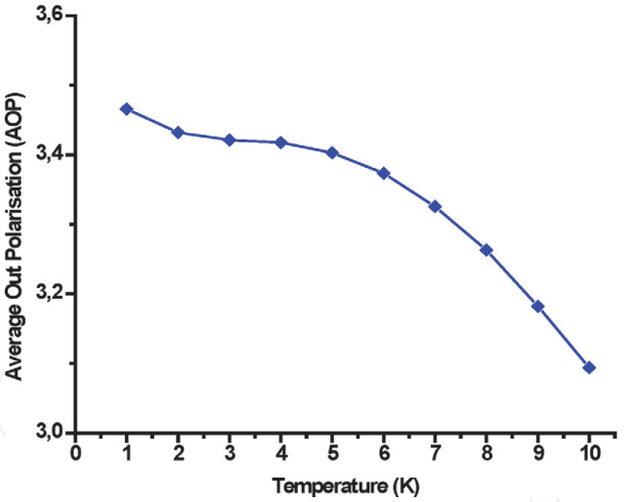

Figure 14.
Effect of polarization on output of FIR filter due to temperature.

is decreased. Therefore, between 1 K and 7 K, the FIR circuit works efficiently. Over 7 K, the circuit falls down radically and produces incompatible outputs.

6. Conclusion

Design of low-power high-speed FIR filter is always a challenge for DSP applications. In this article, a novel design of FIR filter architecture in the QCA technology has been presented. The functionality of the proposed circuits has been verified with QCADesigner version 2.0.3 software. The proposed QCA FIR achieves up to 1 GHz frequency and consumes 1.6 mW power. By comparison of previous designs and the proposed design, it could be concluded that the proposed design has appropriate features and performance. Therefore, this work will provide better silicon area utilization, maximization of clock speed and very low-power consumption than traditional VLSI technology. It should be an important step towards high-performance and low-power design in this field. Future extensions, such as various applications based on this QCA FIR unit, could be investigated.

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References

[1] Dennard RH, Gaensslen FH, Yu HN, Rideovt VL, Bassous E, Leblanc AR. Design of ion-implanted MOSFET's with very small physical dimensions. IEEE Solid-State Circuits Society Newsletter. 2007;**12**(1):38-50

[2] Bernstein K, Cavin RK, Porod W, Seabaugh A, Welser J. Device and architecture outlook for beyond CMOS switches. Proceedings of the IEEE. 2010; **98**(12):2169-2184

[3] Bondy PK. Moore's law governs the silicon revolution. Proceedings of the IEEE. 2002;**88**(1):78-81

[4] Haron NZ, Hamdioui S. Why is CMOS scaling coming to an END? In: 3rd IEEE International Design and Test Workshop (IDT); 2008, pp. 98-103

[5] International Technology Roadmap for Semiconductors, Process Integration Devices and Structures (PIDS). Available from: http://www.itrs.net/Links/ 2011ITRS/Home2011.htm, 2011 Edition

[6] Lent CS, Tougaw PD, Porod W, Bernstein GH. Quantum cellular automata. Nanotechnology. 1993;**4**: 49-57

[7] Angizi S, Sarmadi S, Sayedsalehi S, Navi K. Design and evaluation of new majority gate-based RAM cell in quantum-dot cellular automata. Microelectronics Journal. 2015;**46**:43-51

[8] Azghadi MR, Kavehie O, Navi K. A novel design for quantum-dot cellular automata cells and full adders. arXiv preprint arXiv:1204.2048; 2012

[9] Berzon D, Fountain TJ. A memory design in QCAs using the SQUARES formalism. In: Great Lakes Symposium on VLSI. 1999. pp. 166-169

[10] Walus K, Vetteth A, Jullien G, Dimitrov V. Ram design using quantum-dot cellular automata. In: Technical Proceedings of the Nanotechnology Conference and Trade Show, vol. 2. 2003. p. 160163

[11] Lamjed T, Ismail G, Radhouane L, Bouraoui O. Efficient design of BinDCT in quantum-dot cellular automata (QCA) technology. IET Image Processing. 2018;**12**(6):1020-1030

[12] Kim SW, Swartzlander EE. Parallel multipliers for quantum-dot cellular automata. In: Nanotechnology Materials and Devices Conference; Traverse City. 2009. pp. 68-72

[13] Kim SW, Swartzlander EE. Multipliers with coplanar crossings for quantum-dot cellular automata. In: Conference on Nanotechnology; Seoul. 2010. pp. 953-957

[14] Balali M, Rezai A, Balali H, Rabiei F, Emadi S. Towards coplanar quantum-dot cellular automata adders based on efficient three-input XOR gate. Results in Physics. 2017;**7**:1989-1995

[15] Sasamal TN, Singh AK, Mohan A. Efficient design of reversible alu in quantum-dot cellular automata. Int J Light Electron Optics. 2016;**15**: 6172-6182

[16] Sasamal TN, Singh AK, Ghanekar U. Design of non-restoring binary array divider in majority logic-based QCA. Electronics Letters. 2016;**52**(24): 2001-2003

[17] Kianpour M, Nadooshan RS. A novel modular decoder implementation in quantum-dot cellular automata (QCA). In: International Conference on Nanoscience Technology and Societal Implications (NSTSI). 2011. pp. 1-5

[18] Kianpour M, Nadooshan RS. A novel quantum dot cellular automata X-bit x 32-bit SRAM. In: IEEE Transactions on

Very Large Scale Integration (VLSI) Systems; March 2016. pp. 827-836

[19] Chougule PP, Sen B, Dongale TD. Realization of processing in-memory computing architecture using quantum dot cellular automata. Microprocessors and Microsystems. 2017;**2**:49-58

[20] Campos C, Marciano A, Vilela OP, Sill Torres F. Use: A universal, scalable, and efficient clocking scheme for QCA. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. 2016;**35**(3):513-517

[21] Mahesh R, Vinod AP. New reconfigurable architectures for implementing FIR filters with low complexity. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. 2010;**29**(2): 275-288

[22] Park SY, Meher PK. Efficient FPGA and ASIC realizations of a DA-based reconfigurable FIR digital filter. IEEE Transactions on Circuits and Systems II: Express Briefs. 2014;**61**(7):511-515

[23] Gustafsson O. A difference based adder graph heuristic for multiple constant multiplication problem. In: Proceedings of the IEEE International Symposium on Circuits Systems. 2007. pp. 1097-1100

[24] Mahesh R, Vinod AP. A new common subexpression elimination algorithm for realizing low-complexity higher order digital filters. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. 2008;**27**(2):217-229

[25] Chitra E, Vigneswaran T. An efficient low power and high speed distributed arithmetic design for FIR filter. Indian Journal of Science and Technology. 2016;**9**(4):1-5

[26] Yu Z, Yu ML, Azadet K, Wilson AN. A low power FIR filter design technique using dynamic reduced signal representation. In: Proceedings of the International Symposium on VLSI Technology, Systems, and Applications. 2001. pp. 113-116

[27] Padmapriya S, Lakshmi VP. Design of an efficient dual mode reconfigurable FIR filter architecture in speech signal processing. Microprocessors and Microsystems. 2015;**39**:521-528

[28] Hong Y, Lian Y. A memristor-based continuous time digital FIR filter for biomedical signal processing. IEEE Transactions on Circuits and Systems I: Regular Papers. 2015;**62**(5):1392-1401

[29] Hsiao SF, Jian ZH, Chen MC. Low-cost FIR filter designs based on faithfully rounded truncated multiple constant multiplication/accumulation. IEEE Transactions on Circuits and Systems II: Express Briefs. 2013;**60**(5): 287-291

[30] Lent CS, Snider GL. The development of quantum-dot cellular automata. In: Anderson NG, Bhanja S, editors. Field-Coupled Nanocomputing: Paradigms, Progress, and Perspectives. Berlin, Heidelberg: Springer Berlin Heidelberg; 2014. pp. 3-20

[31] Tougaw PD, Lent CS. Logical devices implemented using quantum cellular automata. Journal of Applied Physics. 1994;**75**:1818-1825

[32] Lent CS, Isaksen B. Clocked molecular quantum-dot cellular automata. IEEE Transactions on Electron Devices. 2003;**50**(9):1890-1896

[33] Momenzadeh M, Huang J, Lombardi F. Design and Test of Digital Circuits by Quantum-Dot Cellular Automata. Norwood, MA: USA. Artech House; 2008. pp. 37-67

[34] Lent CS, Tougaw PD. A device architecture for computing with

quantum dots. Proceedings of the IEEE. 1997;**85**(4):541-557

[35] Vankamamidi V, Ottavi M, Lombardi F. Two dimensional schemes for clocking/timing of QCA circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. 2008;**27**(1):34-44

[36] Manjunath KE, Harikiran V, Manikanta K. Design and implementation of 16×16 modified booth multiplier. In: IEEE (IC-GET). 2015

[37] Yang Z, Xiao J. The design and simulation of array multiplier improved with pipeline techniques. In: IEEE (EMEIT). 2011

[38] Darjn E et al. On the use of approximate adders in carry-save multiplier-accumulators. In: IEEE International Symposium on Circuits and Systems (ISCAS). 2017

[39] Kokila JB, Nithish KV, Pavithra S. Low power wallace tree multiplier using modified full adder. In: IEEE (ICSCN). 2015

[40] Tiwari HD, Ganzorig G, Chan MK. Multiplier design based on ancient Indian Vedic mathematics. In: International Conference on SoC Design. 2008. pp. 65-68

[41] Huddar SR, Rupanagudi SR, Kalpana M. Novel high speed Vedic mathematics multiplier using compressors. Kottayam, India: IEEE International multi Conference. 2013: 465-469

[42] Akhter S. VHDL implementation of fast N × N multiplier based on vedic mathematic. 2007 18th European Conference on Circuit Theory and Design. 2007. DOI: 10.1109/ecctd.2007.4529635

[43] Verma P. Design of 4 × 4 bit vedic multiplier using EDA tool. International Journal of Computer Application. 2012; **48**(20):32-35

[44] Kumar KS, Swathi M. 128-Bit Multiplier with Low-Area High-Speed Adder Based on Vedic Mathematics. Lecture Notes in Electrical Engineering. Singapore; 2017. pp. 163-172. DOI: 10.1007/978-981-10-4280-5_17

[45] Walus K, Dysart TJ, Jullien GA, Budiman RA. QCADesigner: A rapid design and simulation tool for quantum-dot cellular automata. IEEE Transactions on Nanotechnology. 2004; **3**:26-31

[46] Trindade A, Ferreira R, Nacif JAM, Sales D, Neto OPV. A Placement and routing algorithm for Quantum-dot Cellular Automata. 2016 29th Symposium on Integrated Circuits and Systems Design (SBCCI). 2016. DOI: 10.1109/sbcci.2016.7724048

[47] Liu W, Srivastava S, Lu L, et al. Are QCA cryptographic circuits resistant to power analysis attack? IEEE Transactions on Nanotechnology. 2012; **11**(6):1239-1251

[48] Frank ST, Robert W, Philipp N, Rolf D. An energy-aware model for the logic synthesis of quantum-dot cellular automata. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. 2018;**37**:1-11

[49] Krishnamoorthy R, Saravanan S. A novel flip-flop based error free, area efficient and low power pipeline architecture for finite impulse recursive system. Cluster Computing. 2018:**22**: 1-11. DOI: 10.1007/s10586-018-2513-4