Chapter

Numerical Simulation and Compact Modeling of Thin Film Transistors for Future Flexible Electronics

Arun Dev Dhar Dwivedi, Sushil Kumar Jain, Rajeev Dhar Dwivedi and Shubham Dadhich

Abstract

In this chapter, we present a finite element method (FEM)-based numerical device simulation of low-voltage DNTT-based organic thin film transistor (OTFT) by considering field-dependent mobility model and double-peak Gaussian density of states model. Device simulation model is able to reproduce output characteristics in linear and saturation region and transfer characteristics below and above threshold region. We also demonstrate an approach for compact modeling and compact model parameter extraction of organic thin film transistors (OTFTs) using universal organic TFT (UOTFT) model by comparing the compact modeling results with the experimental results. Results obtained from technology computer-aided design (TCAD) simulation and compact modeling are compared and contrasted with experimental results. Further we present simulations of voltage transfer characteristic (VTC) plot of polymer P-channel thin film transistor (PTFT)-based inverter to assess the compact model against simple logic circuit simulation using SmartSpice and Gateway.

Keywords: OTFTs, numerical simulation, compact modeling, flexible electronics

1. Introduction

The interest in organic thin film transistors (OTFTs) has increased significantly in the past few years and has been proven for various applications such as flexible low-cost displays [1], organic memory [2], key components of RFID [3] tags, low-end electronic products, and polymer circuits and sensors [4]. Flexible electronics is a new technology that builds electronic circuits by depositing electronic products on flexible substrates like plastics, paper, and even cloth. Compared with inorganic electronics, organic or flexible electronics have the various following advantages. First, it can be manufactured at a very low cost at low temperatures. Second, it is thin, lightweight, foldable, and bendable and has a strong light absorption, no crushing, mechanical flexibility, low energy consumption, and high emission efficiency. Third, the cost is lower due to cheaper materials and lower-cost deposition processes [5], and it is also used for large area applications. Actually a stack of organic semiconductors (OSC) and low-temperature polymer gate dielectrics and

the rapid annealing process are suitable with high-throughput, low-cost printing manufacturing [6]. Researchers replaced semiconductors with organic materials such as DNTT [7], poly(3-octylthiophene) (P3OT), poly(3-hexylthiophene) (P3HT), and poly(3-alkylthiophene) layers, and dielectric layers are used to create complete flexibility. A bigger challenge is to enhance the real performance of organic devices so as to expand their usage in real-time commercial applications [8]. To enhance the speed of the device, a very great deal of the research efforts has been dedicated to increasing the mobility of organic materials by improving the deposition conditions [9]. In addition to mobility, other methods of improving OTFT performance include scaling the length of channel and changing the active layer thickness. The OTFT is usually fabricated in an inverted structure with gate at the bottom, and source and drain will be at the top. Gundlach et al. [10] show that the bottom contact structure has a strong dependence on the contact barrier and due to the different nature of the interface between the channel and the insulator, the device exhibits different electrical properties [11]. Recently, for p-type OSCs, very high mobility values of several tens of $cm^2\ V^{-1}\ s^{-1}$ have been reported for polymers and small molecules indicating that OSC has great potential for improved performance through chemical structures and process optimization [12]. In addition to performance, deep understanding of instability issues of OTFTs and finding stable and reliable solutions for OTFT is therefore very important [13]. Since the systematic cost of experimental investigation is very high and it requires a lot of time also, technology computer-aided design (TCAD) simulation of semiconductor devices is becoming very important for investigating the design and electrical characteristics of the device prior to fabrication of the device. Organic semiconductor technology has emerged in the past 20 years. Depending on the model, these devices have been developed and studied over the past decade. Compared to the silicon industry, for which public model is clearly defined and commonly used to provide designers with a relatively good description of the process, organic transistors still lack to have complete device models that can fully describe their electrical characteristics. Therefore TCAD simulation and compact modeling of organic transistors become very important.

In this chapter we present 2D device simulation of low-voltage DNTT-based OTFT using Silvaco's ATLAS 2D simulator which uses Poisson semiconductor device equation [14–22] continuity equation for charge carriers, drift diffusion transport model, and density of defect states model for simulation electrical characteristics of the device. Silvaco's UTMOST IV model parameter extraction software is used to get compact model parameters using UOTFT model [23]. Also TCAD simulation results and compact modeling results were compared and contrasted with the experimentally measured results of the device. Compact model has been applied for logic circuit simulation, and voltage transfer characteristics of PTFT-based inverter circuit have been simulated using the compact model parameters extracted from UOTFT model. This chapter contains five sections. This section introduces the content of the paper. The device structure and simulation are described in Section 2. The compact modeling, model verification, and parameter extraction are explained in Section 3. The results and discussion are explained in Section 4. Finally, conclusions drawn are given in Section 5.

2. Simulation

2.1 Device structure and finite element-based numerical simulation

The OTFT is designed on the bottom-gate top-contact of a flexible PEN substrate. A gate dielectric composed of a 3.6-nm-thick aluminum oxide layer and a

1.7-nm-thick n-tetradecylphosphonic acid self-assembled monolayer (SAM) was used [24]. Next, an organic semiconductor layer having a thickness of 11 nm was placed on the AlOx/SAM gate dielectric. The AlOx/SAM gate dielectric (5.3 nm) is very small in thickness and has a large capacitance per unit area, so transistors and circuits can operate at a low voltage of about 3 V. The OTFT has a channel length of 200 μm and a channel width of 400 μm, Lov = 10 μm.

The energy band diagram of a metal insulator semiconductor (MIS) structure is given in **Figure 1**. Maximum valence band energy (E_V) and minima of conduction band energy (E_C) of the inorganic semiconductor are substantially similar between the HOMO and the LUMO of the organic semiconductor. Especially for DNTT,

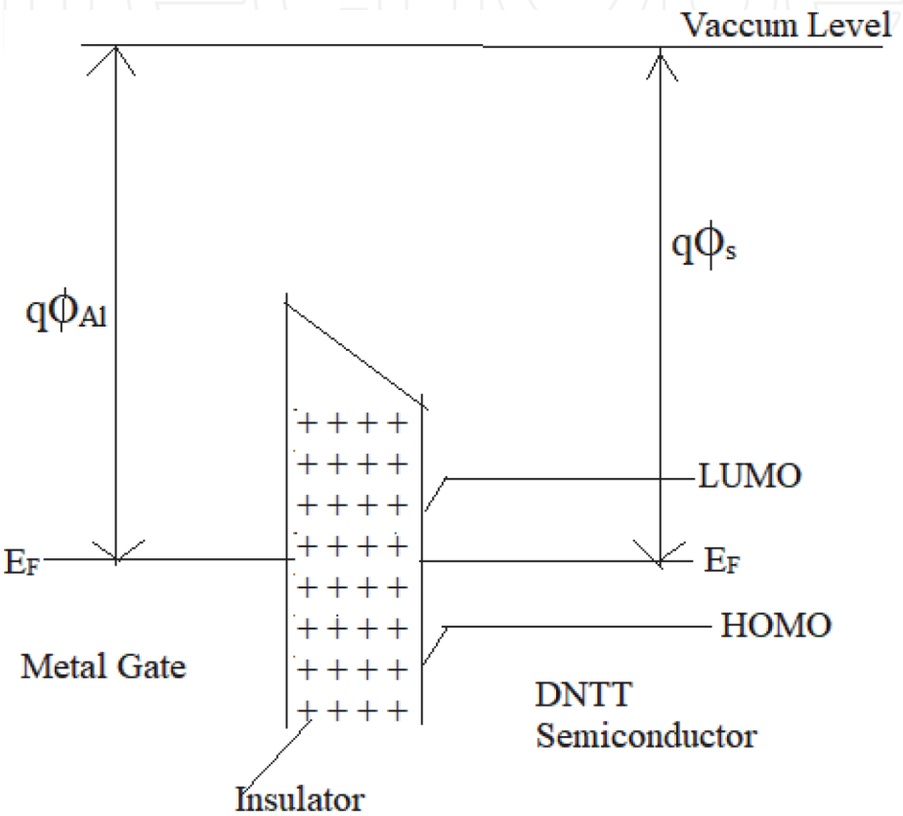

Figure 1.
Energy band diagram of a metal insulator semiconductor (MIS) structure.

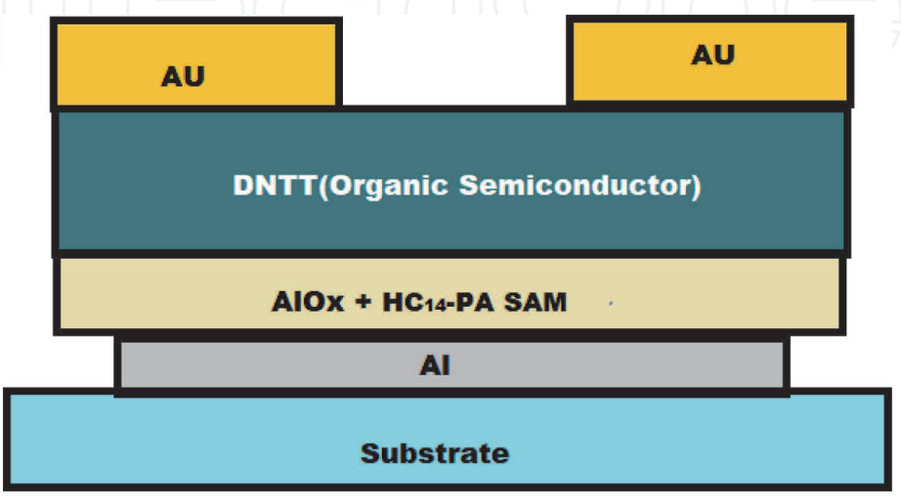

Figure 2.
Schematic cross-sectional diagram of organic TFTs along with the chemical structure of SAM and organic semiconductor.

HOMO is approximately −5.19 eV, and LUMO is about −1.81 eV [7, 24]. This introduces a large enough 3.38 eV HOMO-LUMO energy gap, which is sufficient for transistor operation.

To start the ATLAS simulation, we defined the physical structure and device dimensions, including the location of the electrical contacts. **Figure 2** shows a cross-sectional view of the bottom-gate, top-contact DNTT-based OTFT.

2.2 Device physical equation

We can calculate these charge carrier densities by solving basic device equations simultaneously including Poisson equation [14–22], electron and hole continuity equation, charge transfer equation, and defect density of states equation. The first three equations are the default equations that ATLAS uses to find the electrical behavior of the device.

The Poisson equation determines the electric field intensity in the given device based on the internal movement of the carriers and the distribution of the fixed charges given by Eq. (1):

$$\nabla.\mathrm{E} = -\mathrm{div}(\nabla\Psi) = \frac{\rho(\mathrm{x},\mathrm{y})}{\in} \tag{1}$$

where $\in$ is the permittivity of the region and ρ(x,y) is the charge density given by.

$$\rho(\mathrm{x},\mathrm{y}) = \mathrm{q}\left[\mathrm{p}(\mathrm{x},\mathrm{y}) - \mathrm{n}(\mathrm{x},\mathrm{y}) + {\mathrm{N_D}}^{+}(\mathrm{x},\mathrm{y}) - {\mathrm{N_A}}^{-}(\mathrm{x},\mathrm{y})\right] \tag{2}$$

where p(x,y) is the hole density, n(x,y) is the electron density, N_D^+(x,y) is the ionization donor density, and N_A^- (x,y) is the ionization acceptor density.

To account for the trapped charge, Poisson equations are modified by adding an additional term Q_T, representing trapped charge given in (A):

$$\mathrm{div}(\varepsilon\nabla\Psi) = -\rho(\mathrm{x},\mathrm{y}) = \mathrm{q}\left[\mathrm{n}(\mathrm{x},\mathrm{y}) - \mathrm{p}(\mathrm{x},\mathrm{y}) - {\mathrm{N_D}}^{+}(\mathrm{x},\mathrm{y}) + {\mathrm{N_A}}^{-}(\mathrm{x},\mathrm{y})\right] - \mathrm{Q_T} \tag{3}$$

where $Q_T = q(N^+_{tD} + N^-_{tA})$, N^+_{tD} = density × F_{tD}, and N^-_{tA} = density × F_{tA}. Here, N^+_{tD} and N^-_{tA} are ionized density of donor-like trap and ionized density of acceptor-like traps, respectively, and F_{tD} and F_{tA} are probability of ionization of donor-like traps and acceptor-like traps, respectively.

Due to charge accumulation, a potential is generated, which affects the intensity of electric field distribution and current. The voltage applied to the gate electrode generates an electric field that attracts a few or majority carriers. In addition, for OTFTs, the voltage potential between the source and the drain establishes another electric field along the channel that drives the charge carriers and produces a current.

The continuity equation describes the dynamics of charge carrier distribution over time as given in Eqs. (4) and (5):

$$\frac{\partial \mathrm{n}}{\partial \mathrm{t}} = \frac{1}{\mathrm{q}}\nabla.J_n + G_n\text{–}R_n \tag{4}$$

$$\frac{\partial \mathrm{p}}{\partial \mathrm{t}} = -\frac{1}{\mathrm{q}}\nabla.J_p + G_p\text{–}R_p \tag{5}$$

In these equations, q is the magnitude of the electronic charge, n is the electron carrier density, p is the hole carrier density, J is the corresponding current density, G is the corresponding charge generation rate, and R is the corresponding charge recombination rate. For organic/metal oxide semiconductor field-effect transistors (MOSFETs), there is no optical absorption, so the term is simplified and the properties of the material are described by the minority carrier recombination lifetime. Since MOSFETs are majority carrier devices, the characteristics of carrier generation and recombination are relatively unimportant. The physical properties of organic semiconductors depend on the generation and movement of polarons [25].

A third important set of equations for describing the device physics for the charge carrier is given by

$$J_p = \mathrm{qn}\mu_p E - qD_p \nabla p \tag{6}$$

$$J_n = \mathrm{qn}\mu_n E + qD_n \nabla n \tag{7}$$

It contains drift and diffusion parts. These equations determine the current density based on the carrier mobility (μ), the electric field (E), the carrier density (n, p), and the diffusion coefficient of the carrier (D). Diffusion coefficient operators are related to Einstein's mobility relationship:

$$D_n = \frac{kT}{q}\mu_n \tag{8}$$

$$D_p = \frac{kT}{q}\mu_p \tag{9}$$

In summary, the ATLAS software solves Poisson equations, continuity equations, and current density equations [26, 27] at each node in a two-dimensional grid for a given device structure simultaneously with itself and is subject to boundary conditions (including those applied at the contacts). With the help of ATLAS, the electric field distribution and electron and hole current density are calculated at each node and terminal current at electrode.

2.3 Density of defect states model

The assumed total density (DOS), g(E), consists of four bands: two tail bands (analogous to acceptor-like conduction band and donor-like valence band) and two deep energy bands (one donor-like and the other acceptor-like); they are modeled using a Gaussian distribution [15–22, 28]:

$$g(E) = g_{TA}(E) + g_{TD}(E) + g_{GA}(E) + g_{GD}(E) \tag{10}$$

Here, E is the trap energy, *EC* is the conduction band energy, *EV* is the valence band energy, and the subscripts (*T*, *G*, *A*, *D*) stand for tail, Gaussian (deep level), acceptor, and donor states, respectively:

$$g_{TA}(E) = NTA \exp\left[\frac{E - E_c}{WTA}\right] \tag{11}$$

$$g_{TD}(E) = NTD \exp\left[\frac{E_v - E}{WTD}\right] \tag{12}$$

$$g_{GA}(E) = NGA \exp\left[-\left[\frac{EGA - E}{WGA}\right]^2\right] \tag{13}$$

$$g_{GD}(E) = NGD \exp\left[-\left[\frac{E - EGD}{WGD}\right]^2\right] \tag{14}$$

For exponential tails, DOS is defined by its conduction and valence band edge intercept densities (NTA and NTD) and by its characteristic attenuation energy (WTD and WTA).

For Gaussian distribution, DOS is given by the total state density (NGD and NGA), its characteristic attenuation energy (WGD and WGA), and its peak energy distribution (EGD and EGA).

2.4 Trapped carrier density

The ionized densities of donor and acceptor states are given by Eqs. (14) and (15):

$$n_T = n_{TD} + n_{GD} \tag{15}$$

$$p_T = p_{TA} + p_{GA} \tag{16}$$

where p_{TA}, p_{GA}, n_{TD}, and n_{GD} are given below

$$p_{TA} = \int_{Ev}^{Ec} g_{TA}(E) f_{t_{TA}}(E,n,p) dE \tag{17}$$

$$p_{GA} = \int_{Ev}^{Ec} g_{GA}(E) f_{t_{GA}}(E,n,p) dE \tag{18}$$

$$n_{TD} = \int_{Ev}^{Ec} g_{TD}(E) f_{tTD}(E,n,p) dE \tag{19}$$

$$n_{GD} = \int_{Ev}^{Ec} g_{GD}(E) f_{tGD}(E,n,p) dE \tag{20}$$

$f_{tGA(E,n,p)}$ and $f_{tTA(E,n,p)}$ are the ionization probabilities for the Gaussian acceptor and tail DOS, while $f_{tTD(E,n,p)}$ and $f_{tGD(E,n,p)}$ are defined as the probability of occupation of a trap level at energy E for the Gaussian and tail acceptor, and donor states in steady state are given by following equations [24–27]:

$$f_{tTA}(E,n,p) = \frac{v_n SIGTAE.n + v_p SIGTAH.n_i \exp\left[\frac{E_i - E}{kT}\right]}{v_n SIGTAE\left(n + n_i \exp\left[\frac{E_i - E}{kT}\right]\right) + v_p SIGTAH\left(p + n_i \exp\left[\frac{E_i - E}{kT}\right]\right)} \tag{21}$$

$$f_{tGA}(E,n,p) = \frac{v_n SIGGAE.n + v_p SIGGAH.n_i \exp\left[\frac{E_i - E}{kT}\right]}{v_n SIGGAE\left(n + n_i \exp\left[\frac{E_i - E}{kT}\right]\right) + v_p SIGGAH\left(p + n_i \exp\left[\frac{E_i - E}{kT}\right]\right)} \tag{22}$$

$$f_{tTD}(E,n,p) = \frac{v_{\mathrm{p}}\, SIGTDH.p + v_n\, SIGTDE.n_i \exp\left[\frac{E-E_i}{kT}\right]}{v_n SIGTDE\left(n + n_i \exp\left[\frac{E-E_i}{kT}\right]\right) + v_p SIGTDH\left(p + n_i \exp\left[\frac{E_i-E}{kT}\right]\right)} \tag{23}$$

$$f_{tGD}(E,n,p) = \frac{v_p\, SIGGDH.p + v_n\, SIGGDE.n_i \exp\left[\frac{E-E_i}{kT}\right]}{v_n SIGGDE\left(n + n_i \exp\left[\frac{E-E_i}{kT}\right]\right) + v_p SIGGDH\left(p + n_i \exp\left[\frac{E_i-E}{kT}\right]\right)} \tag{24}$$

where v_n is the thermal velocity of electron, v_p is the thermal velocity of hole, and n_i is intrinsic carrier concentration. SIGGAE and SIGTAE are the electron capture cross sections subject to the Gaussian states and main tail, respectively. SIGGAH and SIGTAH are hole trap cross sections of the Gaussian states and acceptor tail, respectively. SIGTDE, SIGGDE, SIGTDH, and SIGGDH are the equivalent for donor states [8].

2.5 Poole-Frenkel mobility model

Firstly, Miller et al. [29] described the rate of monophonic jumps for simulating hopping in inorganic semiconductors. Later, Vissenberg et al. [30] studied the dependency related to carrier transport on the energy distribution and the jump distance in amorphous transistors, which further helps to find the carrier mobility. The very popular Poole-Frenkel mobility model [31] is given by

$$\mu_{n_{PF}(E)} = \mu_{n0} \exp\left(-\frac{DELTAEN.PFMOB}{kT_{neff}} + \left(\frac{\mathrm{BETAN} \cdot \mathrm{PFMOB}}{kT_{neff}} - \mathrm{GAMMAN.PFMOB}\right)\sqrt{|E|}\right) \tag{25}$$

$$\mu_{p_{PF}(E)} = \mu_{p0} \exp\left(-\frac{DELTAEP.PFMOB}{kT_{peff}} + \left(\frac{\mathrm{BETAP} \cdot \mathrm{PFMOB}}{kT_{peff}} - \mathrm{GAMMAP.PFMOB}\right)\sqrt{|E|}\right) \tag{26}$$

where $\mu_{p_{PF}(E)}$ and $\mu_{n_{PF}(E)}$ are the Poole-Frenkel mobilities for holes and electrons, respectively; μ_{n0} and μ_{p0} are defined as the zero-field mobilities for electrons and holes, respectively; and E is the electric field. DELTAEN.PFMOB and DELTAEP.PFMOB are the activation energy at zero electric field for electrons and holes, respectively. BETAN.PFMOB is the electron Poole-Frenkel factor, and BETAP.PFMOB is the hole Poole-Frenkel factor. *Tneff* is the effective temperature for electrons, and *Tpeff* is the effective temperature for holes.

3. Compact modeling, model parameter extraction, and model verification

The technology and operation of organic thin film transistors (OTFTs) have various unique features that require a dedicated compact TFT model. The important features of OTFT include operation in carrier accumulation mode, exponential density of states, interface traps and space charge-limited carrier transport, nonlinear parasitic resistance, source and drain contacts without junction isolation, dependence of mobility on career concentration, electric field, and temperature. The universal organic TFT (UOTFT) model [23] is a modeling expression that

extends the uniform charge control model (UCCM) previously used for a-Si and poly-Si TFTs [23, 32] to OTFTs and introduces a general expression of modeling for conductivity of channel of OTFTs [30, 33]. In this way, the UOTFT model is applicable to various OTFT device architectures, specifications of material, and manufacturing technologies.

3.1 Model features

UOTFT model depends on a general-purpose compact modeling approach [23, 32], which provides smooth interpolation of drain currents between linear and saturated operating regions including channel length modulation effects and also provides the unified expression of the gate-induced charge in the conductive channel which is valid in all operating states. This model also gives a unified charge-based mobility description, drain-source current, and gate-to-source and gate-to-drain capacitances.

3.2 Model description

The control equation for the UOTFT model for the n-channel OTFT case is described here. The p-channel condition can be obtained by direct change in voltage, charge polarity, and current.

The charge accumulation in channel per unit area at zero-channel potential $(-Q_{acc})_o$ is calculated by the help of the solution of the UCCM equation given by [34].

$$(-Q_{acc})_o = C_i.V_{gse} \tag{27}$$

$$V_{gse} = \mathrm{VO(T)}.\ln\left[1+\frac{e^{u+1}}{1+k(u+2)\ln\left(1+e^{u+1}\right)}\right] \tag{28}$$

$$u = \frac{V_{gs}-VT(T)}{VO(T)} \tag{29}$$

$$k(x) = 1-\frac{84.4839}{x^2+150.864} \tag{30}$$

$$C_i = \in_0 \frac{EPSI}{TINS} \tag{31}$$

where C_i is the gate insulator capacitance per unit area, Vgse is the effective intrinsic gate-source voltage, Vgs is the gate-source voltage (intrinsic), VT is the temperature-dependent threshold voltage parameter, and VO is characteristic voltage (temperature-dependent); for carrier density of states including the influence of interface traps, $\in_0$ is the vacuum permittivity, and EPSI and TINS are model parameters representing the relative permittivity and thickness of the gate insulator, respectively.

3.3 Effective channel mobility

For accurate modeling of OTFTs, we should consider the characteristic power-law dependence of mobility on carrier concentration. According to the results of percolation theory [30], effective channel mobility is expressed in the UOTFT model as

$$\mu_C = MUACC(T).\left(\frac{(-Q_{acc})_0}{C_i.VACC}\right)^{GAMMA(T)} \tag{32}$$

MUACC, VACC, and GAMMA are model parameters. MUACC is a temperature-related parameter which defines effective channel mobility at the onset of strong accumulation of channel. This onset point is controlled by model parameter VACC. The power-law dependence of the mobility on carrier concentration is defined by the temperature-dependent model parameter GAMMA.

3.4 Intrinsic drain-source current

Drain-source current of intrinsic transistor due to charge carriers accumulated in the channel is defined by general interpolation expressions [23]:

$$I_{ds}^{acc} = G_{ch}.V_{dse} \tag{33}$$

$$Vdse = \frac{V_{ds}}{\left[1+\left(\frac{G.V_{ds}}{I_{sat}(1+LAMBDA.Vds)}\right)^{MSAT}\right]^{\frac{1}{MSAT}}} \tag{34}$$

where G_{ch} is the effective channel conductance in the linear region, V_{dse} is the effective intrinsic drain-source voltage, V_{ds} is the intrinsic drain-source voltage, parameter LAMBDA defines the finite output conductance in the saturation region, and MSAT is the model parameter that provides a smooth transition between linear and saturated transistor operation. I_{sat} is the ideal intrinsic drain-source saturation current, and the effective channel conductance in the linear region G_{ch} is obtained in the following way:

$$G_{Ch} = \frac{G_{ch0}}{1+G_{cho}.R_{ds}} \tag{35}$$

$$G_{ch0} = \frac{W_{eff}}{L_{eff}}.\mu_{c.}(-Q_{acc})_0 \tag{36}$$

$$R_{ds} = \frac{RDS(T)}{1+\frac{V_{gse}}{VRDS}} \tag{37}$$

where G_{ch0} is the intrinsic effective conductance of channel in the linear region and R_{ds} is the nonlinear bias-dependent series resistance for intrinsic channel region defined by temperature-dependent model parameter RDS and the model parameter VRDS; on the other hand, Weff and Leff are effective channel widths and length, respectively.

The drain saturation current I_{sat} is determined by the following formula:

$$I_{sat} = G_{ch}.V_{sat} \tag{38}$$

where V_{sat} is the saturation voltage obtained as

$$V_{sat} = \frac{ASAT(T)}{C_i}\left[\frac{(-Q_{acc})_0}{GAMMA(T)+2}+\frac{C_iVO(T)}{GAMMA(T)+1}\right] \tag{39}$$

where $ASAT$ is the temperature-dependent model parameter.

The drain-source leakage current is obtained as

$$I_{ds}^{leak} = \frac{w_{eff}}{L_{eff}}\{\mathrm{IOL(T)}.\left[\exp\left(\mathrm{NSDL}.\frac{V_{ds}}{V_{th}}\right)-1\right].\exp\left(-\mathrm{NSGL}\frac{V_{gs}}{V_{th}}\right)+\mathrm{SIGMAO}.V_{ds} \tag{40}$$

The IOL is a temperature-dependent leakage saturation current model parameter; NGSL and NDSL are non-ideal factors for gate and drain bias, respectively, and SIGMAO is a model parameter representing zero-bias drain-source conductivity:

$$V_{th=}\frac{kT}{q} \tag{41}$$

where V_{th} is the thermal voltage at device operating temperature.
The total intrinsic drain-source current is

$$I_{ds} = I_{ds}^{acc} + I_{ds}^{leak} \tag{42}$$

4. Results and discussion

4.1 Material parameters used for DNTT

The DNTT-based OTFT is designed in a bottom-gate, top-contact configuration. The designed structure has a channel length of 200 μm and a channel width of 400 μm with L_{ov} = 10 μm as shown in **Figure 2**. For the simulation of DNTT-based OTFT structure, the following parameters [24] used are listed in **Table 1**.

4.2 Comparison of TCAD-based numerical simulation characteristics and compact model-based simulation characteristics with experimental characteristics

Figure 3 shows the transfer characteristics obtained for the TCAD-based numerical simulation, compact model-based simulation of DNTT-based organic thin film transistor, and the measured characteristic of DNTT-based OTFT [24]. The transfer characteristics are obtained by varying the gate-to-source voltage (V_{GS}) from 0 to −3 V keeping drain voltage constant at −2 V. There is very good agreement between TCAD-based numerical simulation, compact model-based simulation of the transfer characteristics of OTFT, and experimental transfer characteristics of the fabricated device. **Figure 4** shows the output characteristics obtained from the TCAD-based numerical simulation, compact model-based simulation of DNTT-based organic thin film transistor, and the measured output characteristics of DNTT-based OTFT [24]. Output characteristics are obtained by varying the

Material simulation parameters	Value
DNTT energy band gap (eV)	3.38 eV
Occupied molecular orbital Of DNTT (highest)	−5.19 eV
Occupied molecular orbital Of DNTT (lowest)	−1.81 eV
Intrinsic p-type doping in DNTT	10^{16} cm^{-3}
Fixed interface charge concentration	5×10^{16} cm^{-3}
Work function of aluminum gate	4.1 eV
Work function of Au contact	5.0 eV
Semiconductor thickness of DNTT	11 nm
Dielectric thickness	5.3 nm

Table 1.
Simulation parameters of material of the OTFT [17].

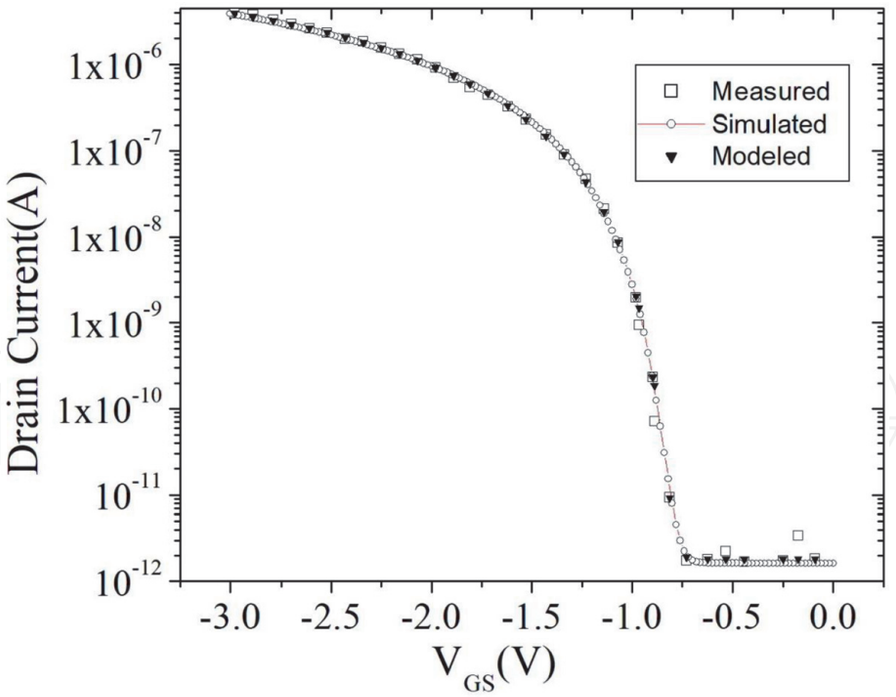

Figure 3.
Comparisons of transfer characteristics of the measured data, the TCAD-simulated data, and the modeled data.

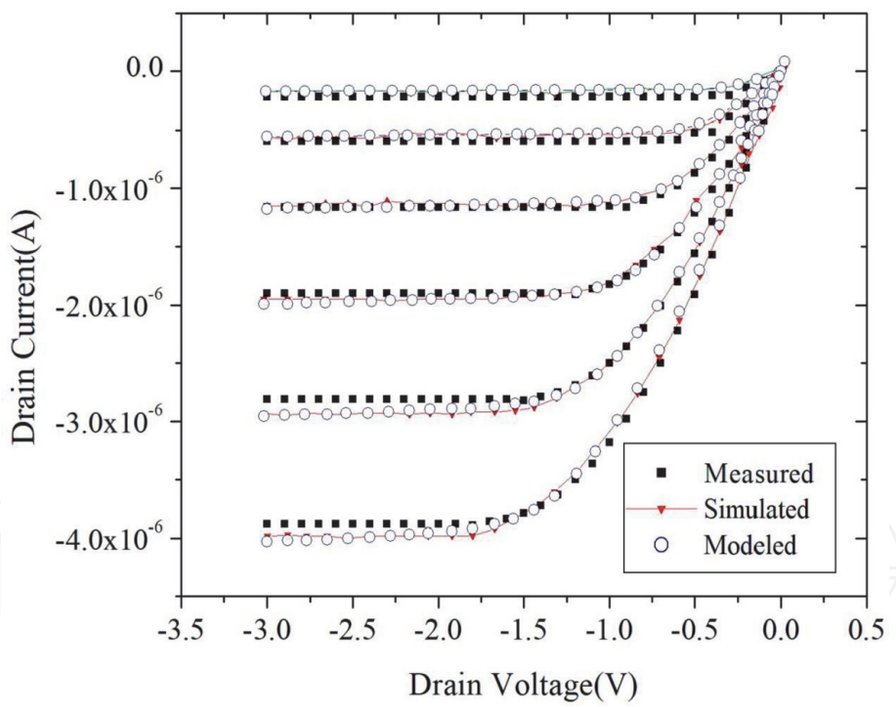

Figure 4.
Comparisons of output characteristics of the measured data, the TCAD-simulated data, and the modeled data.

drain-to-source voltage (V_{DS}) from 0 to −3 V and keeping the gate-to-source voltage (V_{GS}) constant at −1.5, −1.8, −2.1, −2.4, −2.7, and −3.0 V. The simulated output characteristic matched with the experimental output characteristic of the fabricated device.

4.3 Parameter extraction

Extracted OTFT model parameters for low-voltage DNTT-based OTFT using UOTFT model is given in **Table 2**. The extraction process starts with the collection

Parameter name	Symbol	UNIT	Typical values
The thickness of gate insulator	TINS	m	5.3×10^{-9}
Relative dielectric permittivity of the insulator at gate	EPSI	—	3.37
Relative dielectric permittivity of the semiconductor	EPS	—	3.0
Zero-bias threshold voltage	VT	V	−0.884542
Trap density states characteristic voltage	VO	V	0.0314021
Characteristic effective accumulation channel mobility	MUACC	cm^2/Vs	1.85
Characteristic voltage of the effective mobility	VACC	V	1.0
Output conductance parameter	LAMBDA	1/V	0.0
Knee-shape parameter	MSAT	—	5.0
Saturation modulation parameter	ASAT	—	1.52
Leakage saturation current	IOL	A	1×10^{-10}
Contact resistance	RS + RD	Kilo Ohm	116.892

Table 2.
Model parameters extracted for UOTFT model.

of data for I_D-V_G and I_D-V_D characteristic and providing it in UTMOST IV database in .uds format. Further we performed simulation of I_D-V_D and I_D-V_G characteristic using UOTFT model and optimization of this characteristic using Levenberg–Marquardt optimization technique with respect to experimental data for extraction of model parameters.

4.4 Simulation of logic circuit

For UOTFT model validity, simple logic circuit has been implemented and simulated based on p-type OTFTs only. The schematic in **Figure 5** shows the simple inverter circuit used in the simulation of a load transistor with auxiliary gate voltage

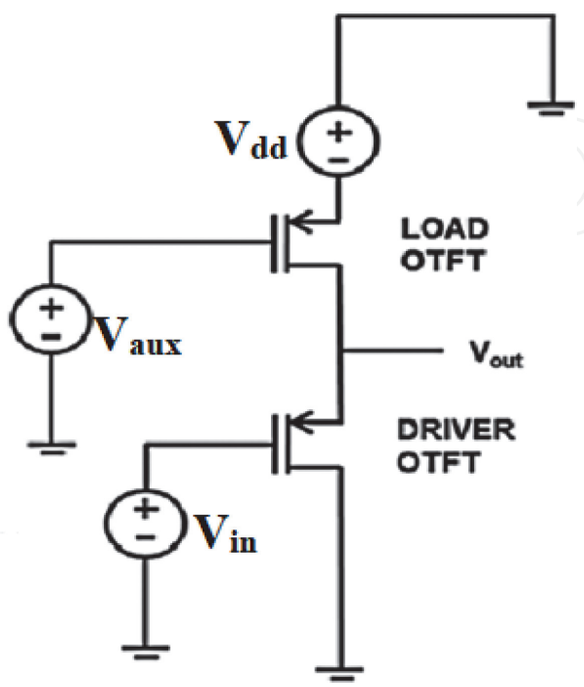

Figure 5.
A circuit diagram of the inverter circuit used for assessing the simulation results.

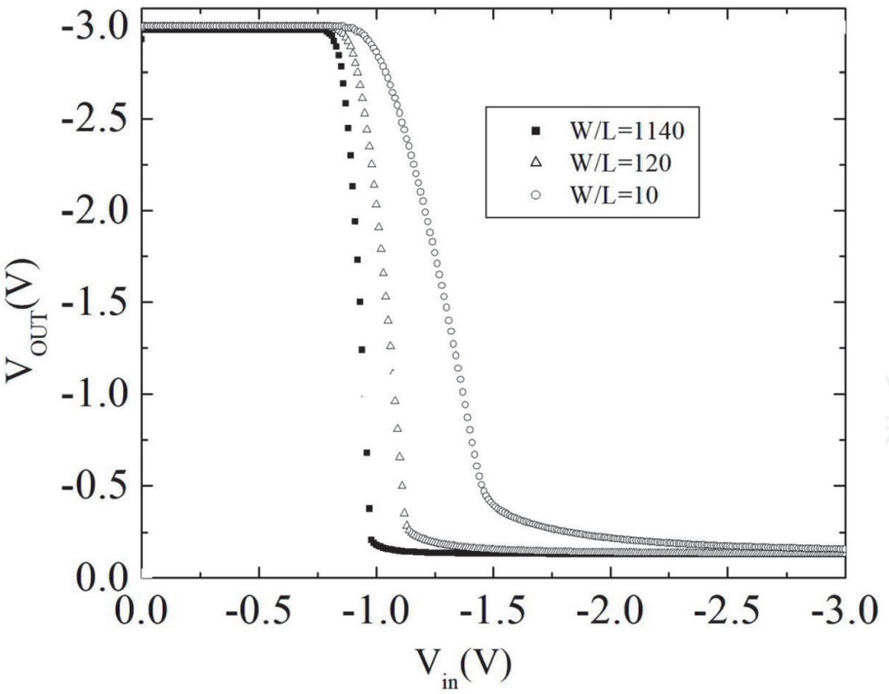

Figure 6.
Voltage transfer characteristics of inverter circuit shown for different W/L ratios of driver OTFT.

(V). The given inverter circuit works like a potential divider between the driver and the load OTFT. When the input voltage is lower than the threshold voltage (more positive than VT), the driver OTFT turns off. On the other side, when it is more than the threshold voltage (more negative than VT), the driver OTFT turns on. The operation of the inverter also depends on load TFT size relatively with the driver TFT. To assess whether the simulation correctly reproduces this dependence, the size of load OTFT and its gate voltage (V) remain at the same value, while the size and gate voltage of driver OTFT change. **Figure 6** shows the voltage transfer characteristic (VTC) plot of the inverter circuit under consideration for W/L ratio of 10, 120 1140 of driver TFT. As W/L ratio of the driver OTFT increases, its impedance decreases, and the transition between high and low states becomes clearer.

5. Conclusion

We presented a finite element method (FEM)-based device simulation of low-voltage DNTT-based OTFT by considering field-dependent mobility model and double-peak Gaussian density of states model using device simulator ATLAS. We also presented the application of UOTFT model and parameter extraction method to organic TFTs. We can also conclude that numerical simulations, experiments, and compact modeling-based simulation characteristics demonstrate the same behavior as matched in **Figure 3** and **Figure 4**. We simulated an OTFT based on DNTT and demonstrated the application of the UOTFT model to organic TFTs and also use experimental data from DNTT-based OTFTs to extract parameters for Silvaco's general-purpose organic TFT compact model. The model has been verified against logic circuit simulation. It has been concluded that UOTFTs provide more accurate modeling of the simpler parameter extraction methods for various organic TFTs. The results show that the UOTFT model correctly simulates the behavior of the devices reported in this study and is expected to be used for more complex circuits based on organic thin film transistors.

Acknowledgements

The authors are thankful to SERB, DST, Government of India, for the financial support under Early Career Research Award (ECRA) for Project No. ECR/2017/000179.

Author details

Arun Dev Dhar Dwivedi*, Sushil Kumar Jain, Rajeev Dhar Dwivedi and Shubham Dadhich
Department of Electrical and Electronics Engineering, Poornima University, Jaipur, India

*Address all correspondence to: adddwivedi@gmail.com

References

[1] Mizukami M, Hirohata N, Iseki T, Ohtawara K, Tada T, Yagyu S, et al. Flexible AMOLED panel driven by bottom-contact OTFTs. IEEE Electron Device Letters. 2006;**27**:249

[2] Takamiya M, Sekitani T, Kato Y, Kawaguchi H, Someya T, Sakurai T. An organic FET SRAM with back gate to increase static noise margin and its application to braille sheet display. IEEE Journal of Solid-State Circuits. 2007;**42**:93

[3] Cantatore E, Geuns TCT, Gelinck GH, Veenendaal EV, Gruijthuijsen AFA, Schrijnemakers L, et al. A 13.56 MHz RFID system based on organic transponers. IEEE Journal of Solid-State Circuits. 2007;**42**:84

[4] Brianda D, Opreab A, Courbata J, Barsanb N. Making environmental sensors on plastic foils. Materials Today. 2011;**14**:416

[5] Lodha A, Singh R. Prospects of manufacturing organic semiconductor-based integrated circuits. IEEE Transactions on Semiconductor Manufacturing. Aug 2001;**14**(3)

[6] Petti L et al. Metal oxide semiconductor thin-film transistors for flexible electronics. Applied Physics Reviews. 2016;**3**(2):021303

[7] Yamamoto T, Takimiya K. Facile synthesis of highly π-extended heteroarenes, dinaphtho[2,3-b,2′,3’f] chalcogenopheno[3,2-b] chalcogenophenes, and their application to field-effect transistors. Journal of the American Chemical Society. 2007; **129**(8):2224-2225

[8] Jeon J, Murmann B, Bao Z. Fully inkjet-printed short-channel organic thin-film transistors and inverter arrays on flexible substrates. IEEE Electron Device Letters. 2010;**31**:1488

[9] Han CY, Ma YX, Tang WM, Wang XL, Lai PT. A study on pentacene organic thin-film transistor with different gate materials on various substrates. IEEE Electron Device Letters. 2017;**38**(6)

[10] Gundlach DJ, Zhou L, Nichols JA, Jackson TN. An experimental study of contact effects in organic thin film transistors. Journal of Applied Physics. 2006;**100**:024509

[11] Street RA, Salleo A. Contact effects in polymer transistors. Applied Physics Letters. 2002;**81**:2887

[12] Lee BH, Bazan GC, Heeger AJ. Doping-induced carrier density modulation in polymer field-effect transistors. Advanced Materials. 2016; **28**(1):57-62

[13] Nikolka M et al. High operational and environmental stability of high-mobility conjugated polymer field-effect transistors through the use of molecular additives. Nature Materials. Dec. 2017;**16**:356-362. DOI: 10.1038/ nmat4785

[14] Buonomo A, di Bello C. On solving Poisson’s equation in two-dimensional semiconductor devices. Electronics Letters. 1984;**20**:4

[15] Dwivedi ADD. Numerical simulation and spice modeling of organic thin film transistors (OTFTs). International Journal of Advanced Applied Physics Research. 2014;**1**:14-21

[16] Vyas S, Dwivedi ADD, Dwivedi RD. Effect of gate dielectric on the performance of ZnO based thin film transistor. Superlattices and Microstructures. 2018;**120**:223-234

[17] Dwivedi ADD, Dwivedi RD, Dwivedi RD, Vyas S, Chakrabarti P. Numerical simulation of P3HT based

organic thin film transistors (OTFTs). International Journal of Microelectronics and Digital Integrated Circuits. 2015;**1**:13-20

[18] Kumari P, Dwivedi ADD. Modeling and simulation of pentacene based organic thin film transistors with organic gate dielectrics. Journal of Microelectronics and Solid State Devices. 2017;**4**:13-18

[19] Kushwah NS, Dwivedi ADD. Computer modeling of organic thin film transistors (OTFTs) using Verilog-A. Journal of Microelectronics and Solid State Devices. 2018;**5**:1-7

[20] Dwivedi ADD, Kumari P. Numerical simulation and characterization of pentacene based organic thin film transistors with top and bottom gate configurations. Global Journal of Research in Engineering-F. 2019;**19**:7-12

[21] Dwivedi ADD, Kumari P. TCAD simulation and performance analysis of single and dual gate OTFTs. Surface Review Letters. 2019;**1950145**:1-7. DOI: 10.1142/S0218625X19501452

[22] Dwivedi ADD, Dwivedi RD, Dwivedi RD, Zhao Q. Technology computer aided design (TCAD) based simulation and compact modeling of organic thin film transistors (OTFTs) for circuit simulation. International Journal of Advanced Applied Physics Research. 2019;**6**:1-5

[23] Fjeldly A, Ytterdal T, Shur M. Introduction to Device Modeling and Circuit Simulation. New York, NY, USA: Wiley; 1998

[24] Zaki T, Scheinert S, Hörselmann I, Rödel R, Letzkus F, Richter H, et al. Accurate capacitance modeling and characterization of organic thin-film transistors. IEEE Transactions on Electron Devices. 2014;**61**:98

[25] Hertel D, Bässler H. Photoconduction in amorphous organic solids. ChemPhysChem. 2008;**9**(5):666

[26] van Roosbroeck W. Theory of the flow of electrons and holes in germanium and other semiconductors. The Bell System Technical Journal. 1950; **29**:560

[27] Juengel A. Drift-Diffusion Equations. Springer; 2009. pp. 99-127. Chap. 5

[28] SILVACO. ATLAS User's Manual—Device Simulation Software. USA; 2010

[29] Miller A, Abrahams E. Impurity conduction at low concentrations. Physics Review. 1960;**120**:745

[30] Vissenberg MCJM, Matters M. Theory of the field-effect mobility in amorphous organic transistors. Physical Review B. 1998;**57**:964

[31] Shim CH, Maruoka F, Hattori R. Structural analysis on organic thin-film transistor with device simulation. IEEE Transactions on Electron Devices. 2010; **57**:195

[32] Iniguez B, Picos R, Veksler D, Koudymov A, Shur MS, Ytterdal T, et al. Universal compact model for long- and short-channel thin-film transistors. Solid-State Electronics. 2008;**52**:400

[33] Estrada M, Cerdeira A, Puigdollers J, Resendiz L, Pallares J, Marsal LF, et al. Accurate modeling and parameter extraction for organic TFTs. Solid-State Electronics. 2005;**49**:1009

[34] UTMOST IV Spice Models Manual. Santa Clara, CA, USA: Silvaco International; 2018