Chapter

Electrostatic Discharge, Electrical Overstress, and Latchup in VLSI Microelectronics

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Abstract

Electrostatic discharge (ESD), electrical overstress (EOS), and latchup have been an issue in devices, circuit and systems for VLSI microelectronics for many decades and continue to be an issue till today. In this chapter, the issue of ESD, EOS and latchup will be discussed. This chapter will address some of the fundamental reasons decisions that are made for choice of circuits and layout. Many publications do not explain why certain choices are made, and we will address these in this chapter. Physical models, failure mechanisms and design solutions will be highlighted. The chapter will close with discussion on how to provide both EOS and ESD robust devices, circuits, and systems, design practices and procedures. EOS sources also occur from design characteristics of devices, circuits, and systems.

Keywords: electrical overstress, electrostatic discharge, latchup, system failure, component failure

1. Introduction

Electrostatic discharge (ESD) and electrical overstress (EOS) have been an issue with electrical systems even prior to semiconductors and VLSI technology [1–25]. With the scaling of semiconductor components, ESD continues to be a manufacturing and design issue [2], while latchup also became a reliability and design issue with the introduction of CMOS technology [1–25].

In this chapter, we will address why certain choices and circuit directions are made. This chapter will hopefully provide some insight from a person who has done extensive work in the ESD design and chip development.

In electronic design, a plethora of electrical events can occur. **Figure 1** illustrates the type of topics including ESD, EOS, latchup as well as electromagnetic interference (EMI), and electromagnetic compatibility (EMC). In this chapter, the focus will only be on ESD, EOS, and latchup.

2. Qualification of semiconductor components—electrostatic discharge (ESD)

ESD is a common form of component level failure and system level from manufacturing, shipping, and handling. Historically, the ESD sources in manufacturing

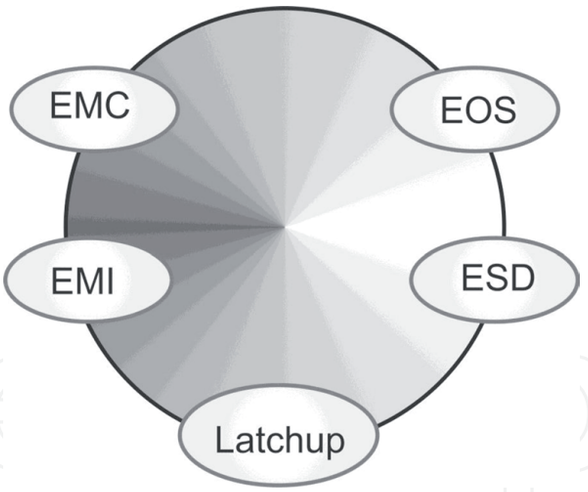

Figure 1.
ESD, EOS, latchup, EMI and EMC.

exceeded the ESD robustness of products leading to component failures. Significant improvements in manufacturing environments as well as ESD solutions in circuit design reduced the concern of component failure levels for many years. Manufacturing charging occurred due to inadequate ionization, material properties, and charging processes from cutting, etching, and dicing. Today, the ESD models performed for qualification and shipping of semiconductor components are as follows [4]:

- human body model (HBM); and
- charged device model (CDM).

With the introduction of VLSI microelectronics, additional qualification of components includes [4]:

- latchup; and
- transient latchup.

CMOS latchup was a large concern in space applications. For low power, CMOS technology was introduced into high density VLSI products. The chapter will address the successes and mistakes made in the industry that lead to latchup failures.

2.1 The human body model (HBM)

Today, the human body model (HBM) is the most established standard for the reliability of components in the semiconductor industry [2–4, 6]. The HBM test is integrated into the qualification and release process of the quality and reliability teams for components in corporations and foundries [6] and is fundamental in the semiconductor chip development cycle.

The human body model (HBM) is regarded as an electrostatic discharge (ESD) event, not an electrical overstress (EOS) event [1–11]. The human body model (HBM) represents a model of a human beings electrical discharge to a semiconductor component. The model assumes that the human being is charged and discharges to the component.

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Additionally, HBM failures occur in the power rails and the ESD "power clamps" between the power rails. HBM failures can occur in digital, analog, or radio frequency applications. The failure signature is typically isolated to a single device, or a few elements. HBM failures occur for both positive and negative polarity discharges.

ESD circuits respond to a specific pulse width to mitigate the ESD pulse event. ESD circuits guide the ESD current away from the signal path and to an "alternate current path" through the power grid and ESD power clamp. ESD circuits are "tuned" to be responsive to specific pulse widths.

HBM ESD failures can occur in the following:

- MOSFET active devices;
- diode active devices;
- bipolar junction transistors (BJT) devices;
- resistor passive elements;
- capacitor passive elements;
- inductor passive elements;
- interconnect wiring;
- Vias;
- contacts;
- power rails; and
- decoupling capacitors.

The key question is what is the best choice for providing ESD protection that

- achieves good ESD robustness;
- does not impact circuit functionality;
- does not a reliability concern;
- wide application space for many different designs; and
- migratable to the next technology without significant changes or re-work.

ESD events can be of positive or negative polarity. ESD events can be singular polarity or oscillatory. As a result, ESD protection networks must be able to address both polarity types. In an oscillatory pulse, the positive current flows through the alternate current path through the VDD power grid, and for negative polarity, current flows through the VSS power grid. Additionally, they remain off during normal functional operation of a semiconductor chip.

An example of an ESD protection network is a dual-diode network [3]. The dual-diode ESD network is a commonly used network for complimentary metal

oxide semiconductor (CMOS) technology because it has the following essential features:

- low turn-on voltage;
- low capacitance;
- responds to both positive and negative polarity events;
- remains off during functional operation.;
- migratable technology to technology; and
- small area required.

For ESD engineers and technologists, a large advantage of the dual-diode ESD network is that it is easy to migrate from one technology generation to another technology generation. For corporations that used MOSFETs for ESD protection strategies, they generate a large amount of work to be successful, and many times, they are unsuccessful. With MOSFET ESD networks, there is not a scalable strategy that guarantees migration from one generation to another.

Additionally, in CMOS technology, the shallow trench isolation (STI) structure is scalable. In CMOS technology with STI isolation, the breakdown voltage does not change with STI scaling but remains a constant. This allows for suitable migration without issues and without failure or re-work.

The second key advantage is that it has a low turn-on voltage of 0.7 V. The low turn-on voltage allows for discharge of the current through the alternate current loop and redirects the current away from the signal path. The third advantage is that it can be designed with low capacitance, making it suitable for CMOS, advanced CMOS, and RF technologies; this minimizes the impact to chip performance. The fourth advantage is that it does not contain MOSFET gate dielectric failure mechanisms. Unlike MOSFET ESD protection solutions, there is no dielectric, and hence no dielectric failure mechanisms.

A commonly used ESD networks is the grounded gate n-channel MOSFET device [3]. As the technology scales, the MOSFET snapback voltage reduces, leading to an earlier turn-on of the MOSFET. Unfortunately, the dielectric breakdown and overstress are problems in this circuit. Hence, although used in many applications, it is limited in migration to advanced technologies.

A commonly used ESD power clamp is the RC-triggered ESD MOSFET power clamp. Why is it widely used?

- Early turn-on based on the frequency dependent transient impulse from an ESD event.
- Establishes alternate current loop away from the signal path.
- Works well in conjunction with ESD double-diode network on the input node.
- Circuit impedance scales with the MOSFET width in the RC-triggered clamp.

The reason is that the RC-triggered ESD MOSFET power clamp turns on the MOSFET in response to an HBM ESD event. This RC-triggered clamp responds to

the ESD current in the power rail leading to turn-on of the MOSFET as opposed to MOSFET breakdown. This element works well with the ESD double-diode network that is used on the signal pins. Additionally, this circuit scales with MOSFET width, and is not dependent on MOSFET second breakdown response.

2.2 Charged device model (CDM)

The charged device model (CDM) is an electrostatic discharge (ESD) test method that is part of the qualification of semiconductor components. The charged device model (CDM) event is associated with the charging of the semiconductor component substrate and package. The charging of the package occurs through direct contact charging, or field-induced charging process (e.g., the field induced charge device model (FICDM)).

The charged device model (CDM) pulse is regarded as the fastest event of all the ESD events [4, 12–15]. Note that the CDM pulse waveform is influenced by the test platform and measurement metrology.

The CDM event has a significantly different characteristic from the HBM event, and requires different ESD circuit solutions. First, the CDM event is oscillatory. Second, the discharge is fast.

CDM event damage occurs in the semiconductor chip through the substrate. It can also occur through the power supply. Charge is stored on the package and the substrate; then, the power supply rapidly discharges through the grounded pin. Since the charge storage is through the entire substrate, it is distributed phenomena and hence spatially dependent. The CDM failure mechanism can be small "pin-hole" in a MOSFET gate structure; this can occur in receiver networks, as well as metal interconnects.

The current path for charged device model (CDM) in components is significantly different from other electrostatic discharge (ESD) events. In the case of the charged device model (CDM), the package and/or chip substrate is charged through a power or ground rail. The component itself is charged slowly to a desired voltage state. As a result, the current flows from the component itself to the grounded pin during ESD testing. This is significantly from other ESD tests (e.g., HBM events) that ground a reference and then apply an ESD event to a signal or power pin. As a result, the current path that a CDM event follows is from inside the component to the pin that is grounded during test.

3. Qualification of semiconductor components—electrical overstress (EOS)

A second area of interest is electrical overstress (EOS). Electrical overstress (EOS) has been an issue in devices, circuits, and systems for VLSI microelectronics for many decades, as early as the 1970s, and continues to be an issue today [1]. Due to a wide variety of pulse events, slow progress has been made at improving EOS robustness.

Electrical overstress (EOS) sources exist from natural phenomena and power distribution [1, 14–25]. Switches, cables, and other power electronics can be a source of electrical overstress. EOS sources exist in devices, circuits, and systems.

3.1 Safe operating area

Figure 2 illustrates the safe operating area (SOA) of a semiconductor device. There is a current limit and a voltage limit on the borders of the SOA. At the corner of the

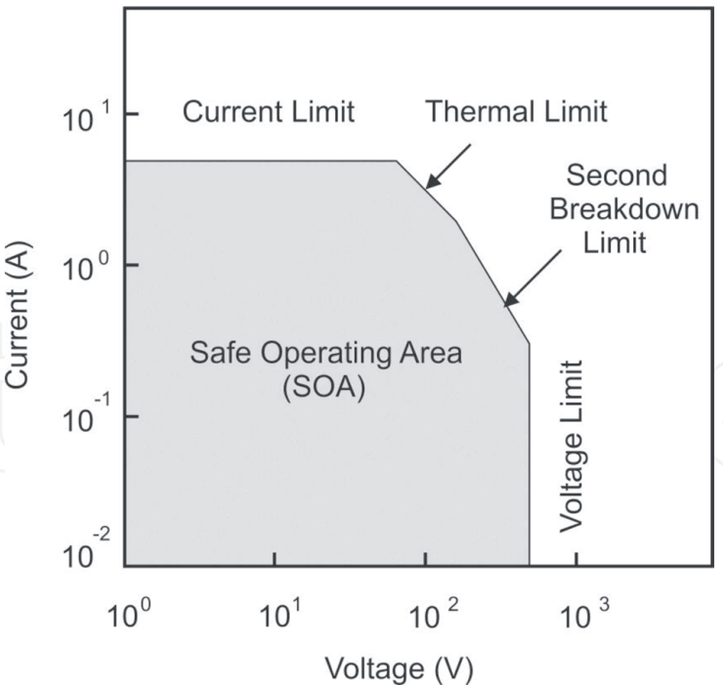

Figure 2.
Safe operating area (SOA).

SOA, the limitation is a thermal limit and a second breakdown limit. The thermal limit has to do with the thermal capacity of a semiconductor device prior to failure. Second breakdown has to do with thermal breakdown limit of a device prior to failure.

Electrical over-voltage (EOV), electric over-current (EOC), and electrical over-power (EOP) can lead to failure mechanisms; these can lead to melted packages, blown single component capacitors and resistors, ruptured packages, blown bond wires, cracked dielectrics, fused and melted metal layers, and molten silicon.

3.2 EOS failure mechanisms

Visual external or internal inspection can be applied to evaluate EOS failure mechanisms. Visual damage signatures can include package lead damage, foreign material, cracks, discoloration, and corrosion. Visual damage can also be evaluated from internal inspection. For internal inspection, visual damage signatures are melted metallurgy, cracked inter-level dielectrics, and molten silicon.

There are certain categories of failures that electrostatic discharge (ESD) does not typically cause and EOS events do cause. Failures that are typically caused by EOS phenomena but not ESD include printed circuit board (PCB), package pin, and wire bond damage.

3.3 EOS protection devices

Electrical overstress (EOS) protection devices are supported by a large variety of technology types. Although the material and device operations may differ between the EOS protection devices, the electrical characteristics can be classified into a few fundamental groups [16–25].

EOS protection networks can be identified depending on whether it is suppressing voltage, as a voltage suppression device, or the current, as a current-limiting device. The voltage suppression device limits the voltage magnitude observed on the signal pins, or power rails of a component, preventing electrical over-voltage (EOV). The current-limiting device prevents a high current from reaching sensitive nodes, hence avoiding electrical over-current (EOC) [1].

Voltage suppression devices can also be sub-divided into two major classifications [1]. Voltage suppression devices can be segmented into devices that remain with a positive differential resistance region and those that undergo a negative resistance region. For a positive differential resistance, these devices can be referred to as "voltage clamp" devices where dI/dV remains positive for all states. For the second group, there exists a region where dI/dV is negative. The first group can be classified as "voltage clamp devices," whereas the second group can be referred to as an "S-type I-V characteristic device," or as a "snapback device." In the classification of voltage suppression devices, the second classification can be associated with the directionality; a voltage suppression device can be "uni-directional" or "bi-directional."

The choice of electrical overstress (EOS) device to use in an application is dependent on the parameters, such as electrical characteristics, cost, and size. The electrical characteristics that are of interest are the breakdown voltage and the forward conduction [1].

The types of voltage suppression devices used electrical overstress (EOS) include transient voltage suppression (TVS) diodes [22], thyristor devices, varistor devices [21], polymer voltage suppression (PVS) devices, and gas discharge tube (GDT) devices [23]. Current-limiting devices can be used in a series configuration for electrical overstress (EOS) protection [16–24]. The choice of the current-limiting EOS protection device is a function of the cost, size, rated current, time response, I^2t value, rated voltage, voltage drops, and application requirements.

4. CMOS latchup

Latchup is a condition where a semiconductor device undergoes a high current state as a result of interaction of a pnp and a npn bipolar transistor [5]. The pnp and npn transistors can be natural to the technology, or parasitic devices. In CMOS technology, these are typically parasitic devices.

When interaction occurs between a pnp and a npn bipolar transistor, or parasitics of CMOS transistors, regenerative feedback between the two transistors can lead to electrical instability. When the two transistors, parasitic or non-parasitic are coupled, the combined device acts as a four-region device of alternating p- and n-doped regions with three physical p-n metallurgical junctions, forming a pnpn structure. When these parasitic pnpn elements undergo a high current state, latchup can initiate thermal runaway and can be destructive.

Latchup events can lead to destruction of a semiconductor chip, package, or system.

There are many reasons why latchup is an issue in today's semiconductor chips. The reason why it is a concern in some corporations differs based on the choices made in the semiconductor technology, latchup design strategy, as well as the latchup methodology.

These are just some of the reasons why today CMOS latchup is not "cured" and remains an issue in today's semiconductor chips. In this text, we will address many of these issues in the future chapters.

5. Conclusions

In conclusion, significant advancements have been made in the understanding of ESD, EOS, and latchup failure mechanisms, as well as solutions to address them have been applied in semiconductor electronics.

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