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Integrated Biosensor and Interfacing Circuits

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1. Introduction

Driven by the demand of the bioelectronics market, many biosensors need to work in parallel or in a controllable way to achieve complicated biodetections, however the limited scale, speed, cost, complex signal processing, and bulky circuit routing problems prohibit the discrete biosensor solutions (Drummond et al., 2003). Nowaday biosensor are usually integrated on the same substrate to form biosensor array to improved the scale and efficiency, and solve the signal routing difficulties.

CMOS technology emerges since the mid-1960s, and rapidly captured the IC market. The aggressive scaling of CMOS technology following the famous Moore's Law enables the realization of high-speed digital circuits, analog and mixed-signal circuits, as well as radio-frequency (RF) communication circuits. A single chip monotonically integrating all components of a complex electronics systems or laboratory systems which contain digital, analog, mixed-signal, and RF communication, microelectromechanical systems (MEMS), and other experimental functions, i.e. lab-on-a-chip (LOC) is avidly to be implemented to possess the capabilities of high-efficiency characterization, high-speed complex signal processing and communication, mass production, large scale, low cost, and low power as well. Fortunately, most of the fabrication processes of biosensors are compatible with the standard CMOS technology either directly or via the post-CMOS processes, e.g. DNA sensors fabricated on Si-nanowire (Li et al., 2004) and gold surface (Cheng et al., 2005) etc, which makes it possible to integrate the biosneosr arrays and CMOS IC on a single chip as a CMOS integrated biosensing system (IBS) (Augustyniak et al., 2006; Prakash et al., 2006; Thewes et al., 2005; Han et al., 2007).

The CMOS IBS usually composes of four parts in its system circuitry: integrated biosensor array, interfacing circuits, analog-to-digital (A/D) conversion, and digital signal processor (DSP), as shown in Fig. 1(a). In some system requiring feedback controlling during the characterization, digital-to-analog (D/A) converters are also included depending on the applications, as shown in Fig. 1(b). In the system architecture of CMOS IBS, the overall performance such as noise, bandwidth, sensitivity etc are mainly governed by the performances of interfacing circuits which controls the electrolyte potential and directly acquires signals from the integrated biosensor array.

The three electrode system, as shown in Fig. 2, is the most popular electrode architecture of the integrated biosensor array in nowadays CMOS IBS. The system is composed of reference electrode, working electrode, and counter electrode (it is also called auxiliary electrode sometimes).

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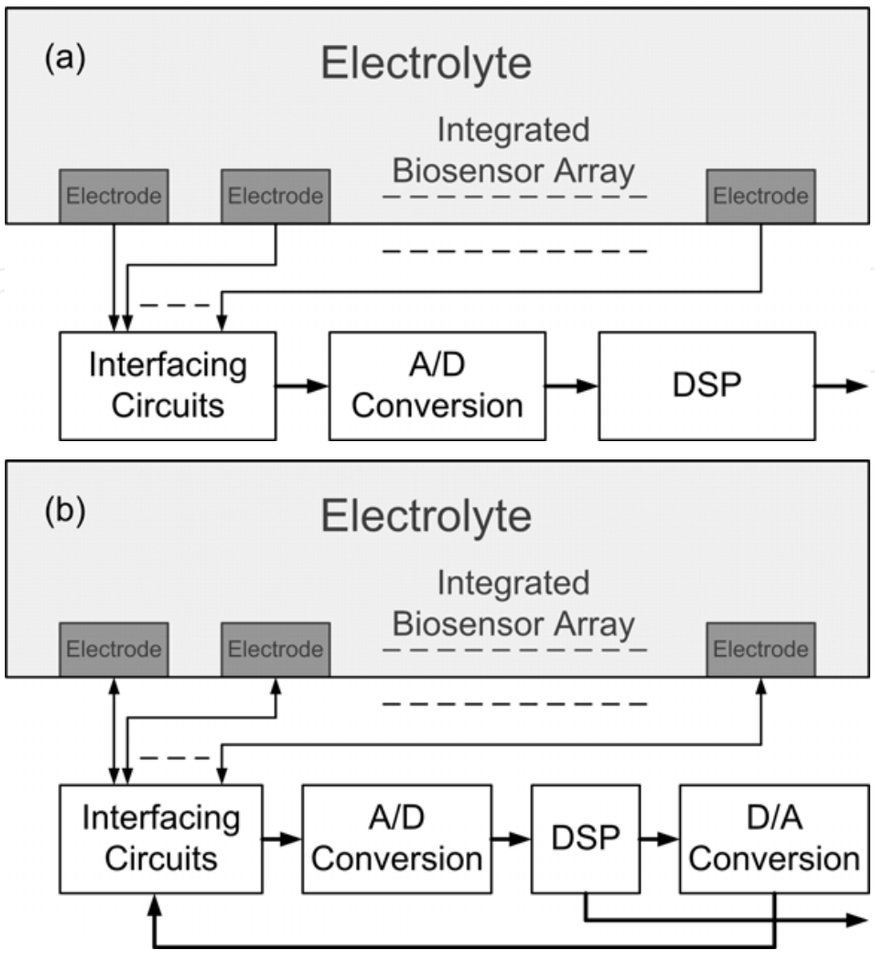


Fig. 1. System architectures of CMOS IBS. (a) Feedforward sensing. (b) Feedback controlled sensing.

Reference electrode is an electrode with a stable and well-known electrode potential. There are many types of reference electrode used in electrochemical systems, such as hydrogen electrode, copper-copper(II) sulphate electrode, silver chloride electrode etc, among which the silver chloride (Ag-AgCl) electrode is commonly employed in the IBS. In some systems with feedback stabilization, the reference electrode made from inert metals such as gold (Au), platinum (Pt) etc are also utilized to simplify the fabrication process.

Working electrode is an electrode in the IBS on which reaction of interest is occurring. Common working electrode is usually implemented in inert metals such as Au, Ag, Pt, etc. Most biosensors apply a control voltage on the working electrode in contact with the electrolyte while measuring the current by a signal acquisition circuit, as shown in Fig. 2.

Counter electrode is an electrode used in the IBS from which the sensing current is expected to flow and is also made from inert metals in most cases. The potential on this electrode is opposite in sign to that of the working electrode. Counter electrode is usually connected with the reference electrode by a potentiostat in a negative feedback loop to stabilize the electrolyte potential with respect to a reference during the biosensing process, as shown in Fig. 2. In some systems, acquisition circuit is combined into the potentiostat, but which is not against the architecture of the interfacing circuits we are discussing here.

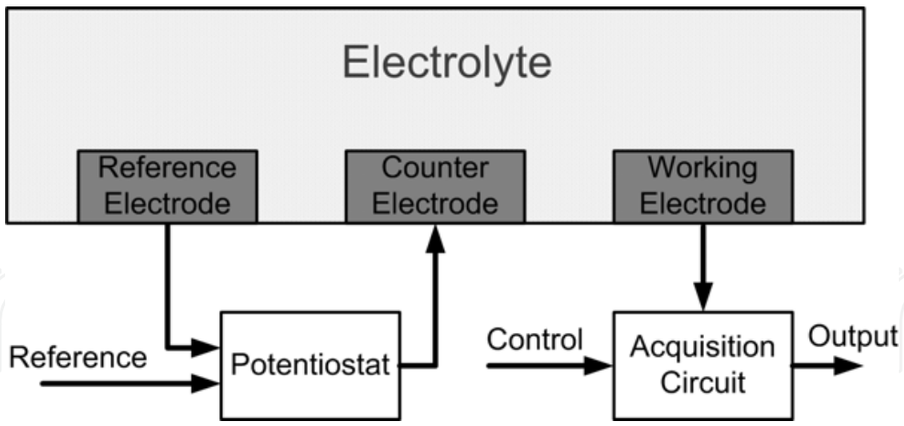


Fig. 2. Interfacing circuits in the CMOS IBS.

2. Potentiostat

The on-chip potentiostat circuit serving for stabilizations of electrolyte potential and accommodation of electrochemical current (Augustyniak et al., 2006; Prakash et al., 2006; Thewes et al., 2005) is one of the major components in the IBS, which is usually realized as an operational transconductance amplifier (OTA) (Zhang et al., 2009). Table 1 shows the specifications of the potentiostat OTA from a typical biosensor system based on nano-particle assembly.

Typical assembling voltage	1.8 ± 0.2 V
Min. assembling voltage	~1 V
Electrolyte potential range	0 to 1.8 V
Max. potential variation	5 mV
Assembling current range	~10 nA to ~100 μA
Max. signal bandwidth	< 100 kHz

Table 1. Sepcifications of potentiostat OTA from the experiment.

It can be seen that the assembling voltage range falls in the typical supply voltage range of standard CMOS technology, but due to the aggressive scaling of CMOS technology, typical supply voltage of mainstream CMOS process can barely satisfy the specifications in Table 1. For this reason, a potentiostat OTA with rail-to-rail input common-mode range is highly preferred in the CMOS IBS. On the other hand, considering the loading capability required by the assembling current range, a Class-AB output stage should also be incorporated for its bidirectional loading capability and high power efficiency.

The potentiostat OTA has been designed and illustrated in Fig. 3. The potentiostat OTA uses the complimentary folded-cascode input stage composed of transistor M_0 to M_{13} to achieve the rail-to-rail input common-mode range to enable the required assembling voltage, and reduce the input-referred noise to stabilize the potential as well, while incorporates the Class-AB output stage composed of transistor M_{29} to M_{32} to provide the maximized loading capability and accommodate the assembling current requirement. Transistors M_{14} to M_{21} function as the common-mode feedback circuit and provide biasing voltage for the folded-

cascode input stage. M_{25} to M_{28} are two source follower to match the DC voltage between stages, while the other biases are served by M_{22} to M_{24} from a current I_B. Simulation results show that biasing at a current of I_B=1 μA the circuit is capable of providing a rail-to-rail input and output dynamic range and a unit gain bandwidth up to 42.7 MHz, while the output current headroom, I_{max}, is over 450 μA, which meet the specifications in Table 1.

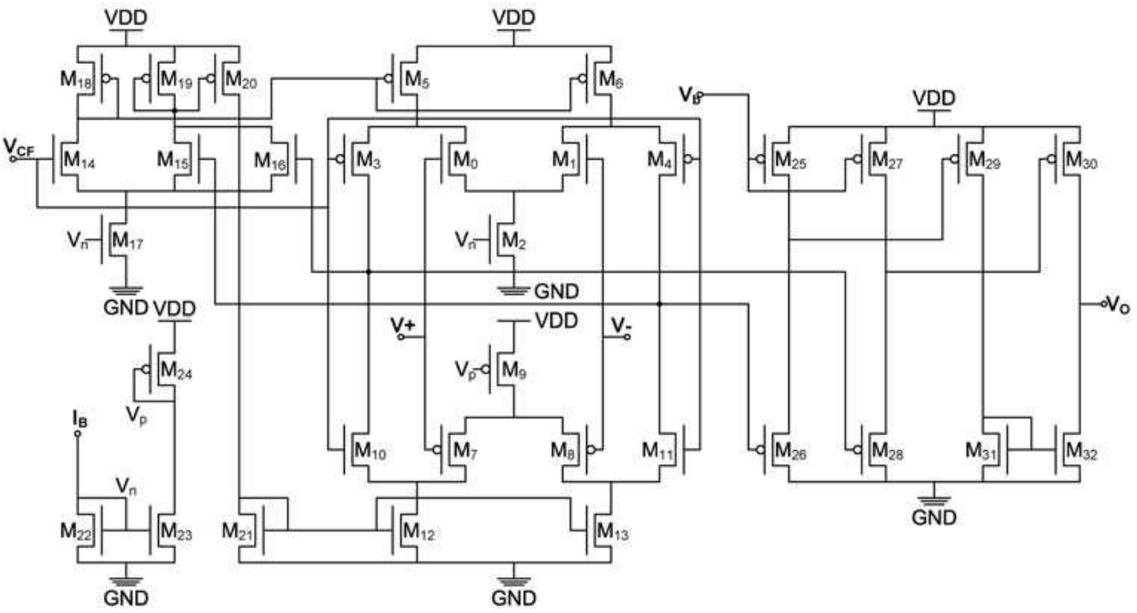


Fig. 3. Transistor level implementation of the potentiostat OTA with rail-to-rail input common-mode range and Class-AB output stage.

The potential variation is due to: (I) finite transconductance of the potentiostat OTA, (II) input referred noise, and (III) the input referred offset. If G_m^{DC} is the DC transconductance of the potentiostat OTA, the potential variation, V_{ft}, due to (I) can be expressed as

$$V_{ft} = \frac{I_{\max}}{G_m^{DC}} \tag{1}$$

According to the noise theory, transistors M_0, M_1, M_5, M_6, M_7, M_8, M_{12}, and M_{13} in the first stage contribute to the overall noise. The noise power spectral density, S_I, in a MOS transistor is given by (Linares-Barranco et al., 2003; Linares-Barranco et al., 2004)

$$S_I = \frac{4\gamma kTg_m + K_F I_{ds}^{A_F}}{f^{E_F} C_{ox} WL} \tag{2}$$

where γ is the thermal noise parameter, g_m is the transconductance, I_{ds} is the drain-source current, C_{ox}, W, and L are the gate capacitance per unit area, transistor width and length, respectively, and k, T, and f are the Boltzman constant, temperature, and frequency, respectively. K_F, A_F, and E_F are flicker noise parameters with the typical values of 2×10^{-25}, 2, and 1, respectively. Since the corner frequency f_c, where thermal noise and flicker noise exhibit the same power density, is calculated as 5.4 Hz by using parameters provided by the foundry, much smaller than the unit gain bandwidth, therefore, flicker noise is negligible in the proposed OTA, and the input referred noise voltage V_{irn} can be characterized by

$$\overline{V_{irn}^2} = \frac{8\gamma kT\left(g_{m0} + g_{m5} + g_{m7} + g_{m12}\right)}{\left(g_{m0} + g_{m7}\right)^2} \tag{3}$$

where g_{mj} is the transconductance of transistor M_j, j = 0, 1,…, 32.
V_{irn} can be diminished by increasing the biasing currents and aspect ratios of the input differential pairs, but trades off with the power consumption and the physical area. The spectral density input referred noise of proposed OTA on different common-mode input voltages are shown in Table 2.
Monte-Carlo simulation is also performed to characterize the input referred offset by utilizing the mismatch parameters provided by the foundry, and the results are also shown in Table 2. In the worst case with V_{CM} = 0 V, the overall potential variation due to the above three issues is 4.12 mV, which implies an 8 bit of potential resolution and satisfies the boundary condition in Table 1. The other circuit performances are summarized in Table 2.

Parameters	V_{CM} = 0 V	V_{CM} = 0.9 V	V_{CM} = 1.8 V
DC transconductance	2.22 S	5.43 S	3.90 S
3-dB bandwidth	1.97 kHz	2.07 kHz	1.94 kHz
Phase margin	>75°	>80°	>75°
Max. output pull current	451 μA	451 μA	–
Max. output push current	–	459 μA	459 μA
Input referred offset	3.51 mV	1.60 mV	2.75 mV
Input referred noise	61.8 nV/√Hz	38.2 nV/√Hz	57.7 nV/√Hz
Overall potential variation	4.12 mV	1.93 mV	3.24 mV
Potential resolution	8 bit	9 bit	9 bit
DC power dissipation	40.4 μW	50.3 μW	58.0 μW
Power supply	1.8 V	1.8 V	1.8 V

Table 2. Summary of performances of the potentiostat OTA

3. Acquisition circuits

The design of acquisition circuits in the IBS is circumscribed by the sensing mechanism of the biosensor. In the electrical biosensing, there are two major schemes in analyte detection: direct current (DC) sensing and alternative current (AC) sensing.
In the DC sensing, a DC voltage is usually applied to the working electrode in an IBS, and the current flowing from counter electrode to the working electrode is measured (Augustyniak et al., 2006; Thewes et al., 2005). This method suffers from the large background noise in the electrolyte seriously, which prevent it from the applications requiring high sensitivities of biosensing.
In the AC sensing, the acquisition circuit senses the AC modulation current by applying an AC voltage superimposed on a DC biasing on the working electrode (Huang & Chen, 2008).

Since only the background noise within the band-of-interest deteriorates the signal-to-noise ratio, the AC sensing has much better sensitivity than the DC sensing scheme.

DNA releasing voltage	0.9 V
DNA modulation voltage	±0.5 V
Current headroom	±100 nA
Current sensitivity	~100 pA
Max. signal bandwidth	10 kHz
Min. sensor impedance	~5 MΩ

Table 3. Specifications of a typical DNA IBS

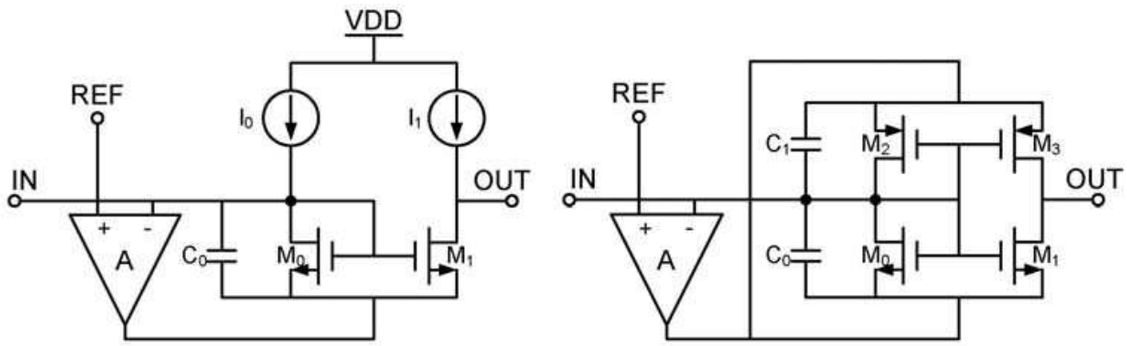
A desirable acquisition circuit should usually accommodate both schemes of biosensing, however, as summarized in Table 3, the fastidious requirements, such as sensitivity, bandwidth, input range, etc., for the following circuits make great challenges to analog integrated circuit designers. There are various methods and circuits dealing with the ultralow current in biosensing applications, e.g., current integrator (sometimes it is called as potentiostat) (Ayers et al., 2007; Narula & Harris, 2006), transimpedance amplifiers (Rodriguez-Villegas, 2007; Basu et al., 2007), and ultralow current-mode amplifiers (ULCA) (Zhang et al., 2007; Ramirez-Angulo et al., 2004; Steadman et al., 2006; Zhang et al., 2009). The current integrator is capable of providing sub-picoampere sensitivity, however, the circuit bandwidth is typically below 1 kHz, which cannot fully accommodate the bandwidth of AC sensing. Transimpedance amplifiers possess wider bandwidth and good sensitivity, however, its dynamic range is limited by the supply voltage, which becomes a serious issue along with the scaling of supply voltage in today's CMOS technology. The ULCA turns out to be a favorable candidate with high sensitivity, sufficient bandwidth, and wide dynamic range for IBS with AC sensing capabilities.

3.1 Circuit design of ULCA

In ULCA design, conventional transistor-strong-inversion-based current-mode circuits are out of consideration due to the large noise background induced by the dc quiescent current, and weak-inversion-based (subthreshold) current-mode circuits emerge as the candidates. Since the subthreshold circuits suffer from supply voltage fluctuations and die-to-die process fluctuations (Mead, 1989), they are usually closely integrated with other adjacent stages on a single die and share the same supply voltage, along with careful considerations on the matching, symmetry, and biasing issues (Linares-Barranco et al., 2003; Linares-Barranco et al., 2004; O'Halloran & Sarpeshkar 2004).

Some ULCA topologies have been reported (Zhang et al., 2007; Ramirez-Angulo et al., 2004; Steadman et al., 2006), as shown in Fig. 4. The circuit in Fig. 4(a) is working in the Class A mode. It uses a regulated current mirror to achieve the current amplification. The quiescent currents are provided by current sources, whereas the bandwidth is limited by capacitor C_0. Although the circuit provides good linearity over the input range, since the quiescent current I_0 should be low enough to reduce the noise level and meet the requirement of sensitivity, the specified current headroom (in both positive and negative directions) can hardly be achieved. One can certainly introduce the Class B complementary topology in Fig.

4(b) to meet the headroom requirement and increase the sensitivity by removing the noise background induced by I_0; however, this comes at the cost of substantially losing bandwidth in the low-input cases.



(a) (b)

Fig. 4. Conventional current-mode amplifier topologies.

To meet the specifications in Table 3, a Class AB ULCA aiming at biosensing amplification has been designed and verified in SMIC 0.18-μm CMOS mixed-signal technology (Zhang et al., 2009). The design elaborately considered the issues and tradeoffs over gain, bandwidth, noise, and offset. The experimental results show that the ULCA can completely satisfy the requirements of typical DNA-based IBS and is eligible to serve for the preamplification of ultralow biosensor signals in the IBS.

The ULCA schematic is shown in Fig. 5. In this circuit, the current from DNA biosensors is input to a complementary regulated current mirror consisting of an N-type opamp A_{N0}, a P-type opamp A_{P0}, and transistors M_0, M_1, M_3, and M_4, where it is amplified by a factor of 10 (20 dB). The opamps A_{N1} and A_{P1} and the transistors M_6–M_{11} compose a voltage limiter.

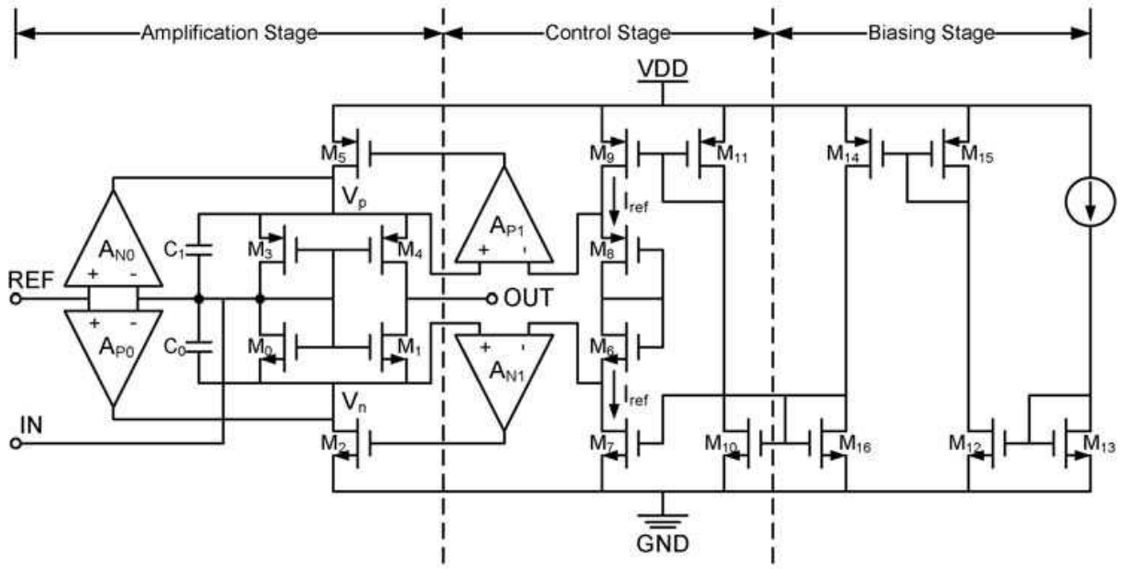


Fig. 5. Circuit schematic of the ULCA.

Due to the "virtual short" mechanism, "IN" is fixed at "REF" by A_{N0} and A_{P0}, and a quiescent current of I_{ref} is established in M_0 and M_3 by A_{N1} and A_{P1}. When a positive input is applied V_n, the output of the opamp A_{N1} reduces, thus turning off M_2. The current of M_0 and M_1 is sunk by A_{P0}. On the other hand, since V_p tends to drop down, the current provided by A_{N0} becomes smaller. However, M_5 is turned on by A_{P1} to compensate the current at node V_p, which limits V_p from dropping and maintains the quiescent current of M_0 and M_3 equal to the reference current I_{ref} provided by M_6−M_9, even if the input current I_{IN} is much larger than I_{ref} . A similar conclusion can also be made for the negative input cases.

It can be seen that M_2 and M_5 alternatively sustain the quiescent current for the current mirror, which in turn keeps a constant bandwidth as the input varies between positive and negative directions. Furthermore, I_{ref} can be designed small enough to achieve the required sensitivity and noise level without being restricted by the current headroom, since the current headroom no longer depends on the magnitude of the quiescent current in the ULCA. Therefore, the circuit can provide an extremely high sensitivity and a large current headroom at the required bandwidth. Due to the variation and pad leakage issues, I_{ref} is unpractical to be provided off-chip. Therefore, three steps of current mirroring are introduced by M_{12}−M_{16} in the biasing stage, where each step achieves a conversion factor of 0.1. A microampere-level off-chip current is downconverted 1000 times to relax these unwanted impacts. Capacitors C_0 and C_1 serve for frequency compensation and bandwidth limitation purposes in the circuit.

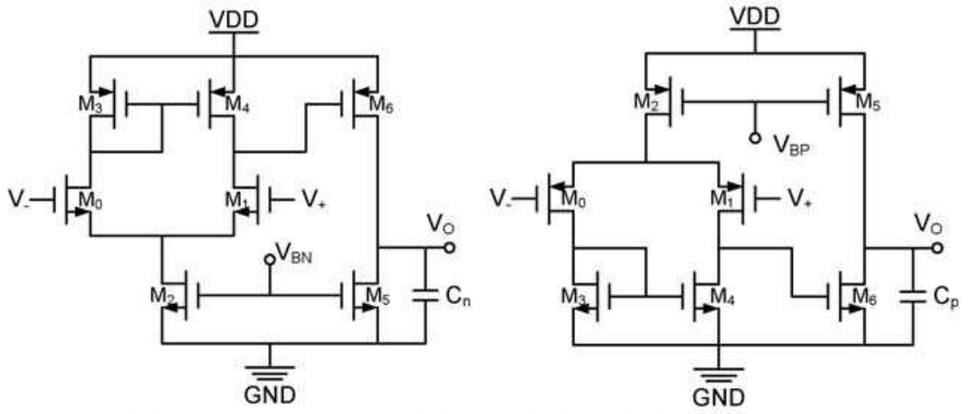


Fig. 6. Auxiliary N- and P-type opamps in the ULCA.

The auxiliary N- and P-type opamps are shown in Fig. 6(a) and (b). In the circuit, M_0, M_1, M_3, and M_4 consist of a differential input stage. M_0 and M_1 are biased in their subthreshold regions for the purpose of noise reduction; meanwhile, they are chosen as large dimensions to improve the matching and reduce the offset and flicker noise. Transistors M_5 and M_6 consist of a transconductance output stage that provides current for the following circuits. Capacitors C_n and C_p represent the load capacitances of the opamp.

As shown in Fig. 5, when a positive input is applied, the gain is provided by the regulated current mirror consisting of M_0, M_1, and opamp A_{P0}, whereas M_3−M_5 and opamp A_{P1} are serving as current sources providing the quiescent current for the stage, which can be simplified to the circuit shown in Fig. 7(a). A complementary discussion of the negative input case leads to the topology shown in Fig. 7(b).

3.2 Small signal AC analysis

The small-signal equivalent circuit for ac analysis is shown in Fig. 7(c). In this circuit, g_m, g_{mb}, g_o, and C_{gs} are the gate transconductance, body transconductance, output conductance, and gate capacitance of the MOSFET, and g_{oa}, C_{ia}, and C_{oa} are the output conductance, input capacitance, and output capacitance of the opamp, respectively. C_i is defined as $C_{gs0} + C_{gs1} + C_0$ (or C_1). The transconductance of the opamp is modeled as $g_{ma}(s)$, considering the delays introduced by the parasitic capacitances of its internal nodes. As suggested in (Linares-Barranco et al., 1992), $g_{ma}(s)$ can be written as

$$g_{ma}(s) = g_{ma}\left(1 - \frac{s}{\omega_a}\right) \tag{4}$$

where g_{ma} is the DC transconductance, and ωa models the delay.

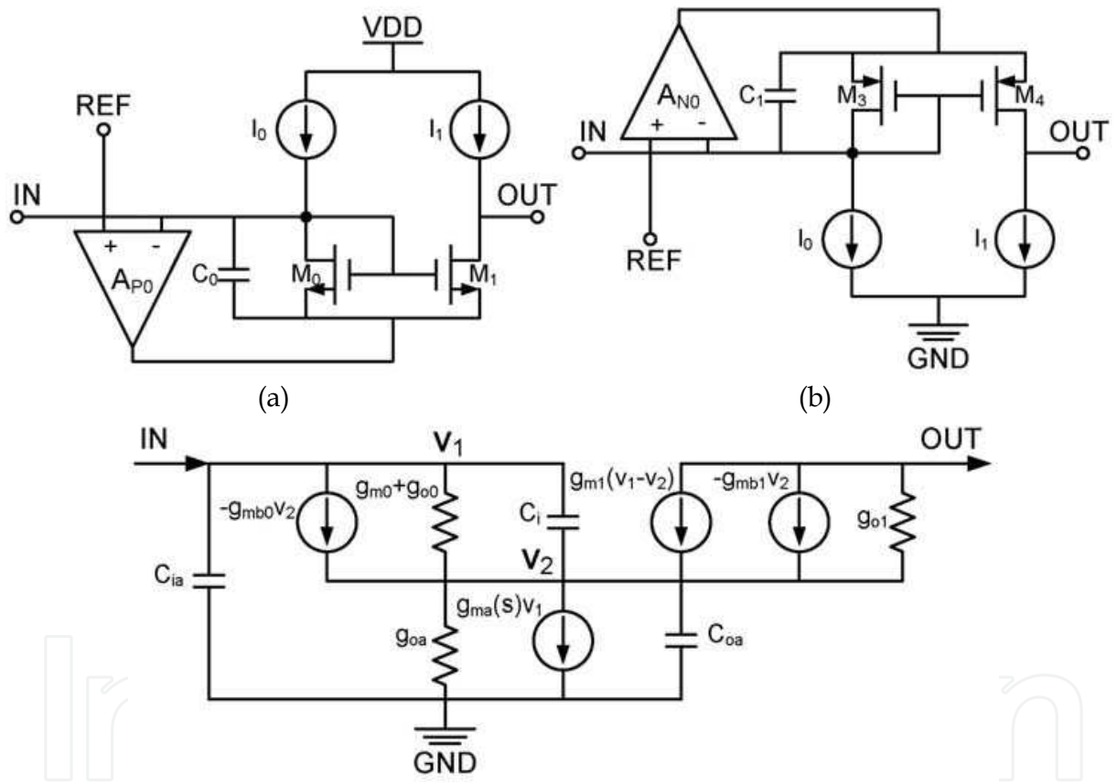


Fig. 7. (a) Simplified circuit of ULCA when a positive input is applied. (b) Simplified circuit of ULCA when a negative input is applied. (c) Small-signal equivalent circuit of a simplified ULCA.

Detailed analysis of the equivalent circuit results in the characterization function of $as^2+bs+\underline{c}=0$, where:

$$a = C_{ia}\left(C_i + C_{oa}\right)\omega_a + C_i\left(C_{oa} - \frac{g_{ma}}{\omega_a}\right)\omega_a \tag{5}$$

$$b \approx C_{ia}\left(g_{m0}+g_{m1}+g_{oa}\right)\omega_a+\left(g_{m0}+g_{o0}\right)\left(C_{oa}-\frac{g_{ma}}{\omega_a}\right)\omega_a \tag{6}$$

$$c \approx g_{mb0}\left(g_{ma}-g_{m1}\right)\omega_a+g_{m0}\left(g_{mb1}+g_{oa}+g_{ma}\right)\omega_a \tag{7}$$

and the parameters are defined as follows:

C_{ia}: Input capacitance of opamp.
C_{oa}: Output capacitance of opamp (C_n or C_p).
C_i: $C_{gs0}+C_{gs1}+C_0$ (or C_1).
g_m: Transconductance of MOSFET.
g_{mb}: Body transconductance of MOSFET.
g_o: Output conductance of MOSFET.
g_{oa}: Output conductance of opamp.

To maintain the ac stability, all the poles of the circuit transfer function must be placed in the left-hand side of the Laplace plane, i.e. $a>0$, $b>0$, $c>0$ must be satisfied, resulting in the conditions of g^N_{ma}, $g^P_{ma} > g_{m1}$, $C_0 > g^P_{ma}/\omega_a$, and $C_1 > g^N_{ma}/\omega_a$. Moreover, it can be found that provided the quiescent current I_{ref} , by adjusting C_0 and C_1, the bandwidth of the ULCA can be confined at the expected value.

3.3 Noise characterization

It is known that three kinds of noises are considered in the CMOS circuit: thermal noise and shot noise, which are white noise, and flicker noise or $1/f$ noise. According to the noise theory and the characterizations in (Linares-Barranco et al., 2003) and (Linares-Barranco et al., 2004), the subthreshold noises in the MOSFET are basically contributed by shot noise and flicker noise, and the noise power density S_{ID} is given by

$$S_{ID} = 2qI_D + \frac{KI_D^2}{WLC_{ox}^2}\frac{1}{f} \tag{8}$$

where I_D is the drain–source current of the MOSFET, W and L are the channel width and length, C_{ox} is the gate capacitance per unit area, and q, f, and K represent the unit charge, frequency, and a process-dependent parameter, respectively. In the 0.18-μm technology, the typical value of C_{ox} is about 1.08×10^{-2} F/m², and K is 2×10^{-24} F²/m² for nMOS and 4×10^{-26} F²/m² for pMOS.

By equaling the two terms in (8), one can derive the noise corner frequency as $f_c = KI_D/2qWLC^2_{ox}$. In a $W = 10$ μm and $L = 1$ μm sized nMOS, f_c is around 8 Hz when biased at $I_D = 1.5$ nA, which is no more than 0.1% of the required 10-kHz bandwidth, whereas for pMOS, f_c is two orders lower. In the DNA biosensor, the modulation signal is usually band limited with a typical bandwidth of 10 kHz and a lower frequency of 10 Hz; therefore, shot noise dominates over the whole signal band of interest from the above design.

The noise performance of the ULCA can be characterized by two noise sources v_n and i_n with the corresponding power densities of S_{vn} and S_{in}, which can be calculated as usual by evaluating the output noise current with the input open or shorted to the ground and dividing by the gain. The simplified expressions are reported as

$$S_{in} = 4qI_{\text{ref}}\left(1+\frac{1}{A}\right) \tag{9}$$

$$S_{vn} = \frac{4qAI_{\text{ref}}}{g_{ma}^2} + 2S_{va} \tag{10}$$

where A is the current gain of the ULCA, and S_{va} is the input referred noise power density of the opamp. From (9) and (10), S_{in} and S_{vn} can be reduced by decreasing the input-referred noise of the opamp and the quiescent current I_{ref}, however trading with the power consumption and the bandwidth of the ULCA.

3.4 Mismatch considerations

The performances of the practical circuit also suffer from process fluctuations due to transistor mismatches, e.g., variations of W, L, and threshold voltage V_T , which would induce the input-referred offset (IRO) I_{off}, gain error δA, and bandwidth variation δBW of the ULCA. More specifically, one can find that I_{off} is due to the IROs V_{off} of opamps A_{N0} and A_{P0} and the mismatches of M_0, M_1, M_3, and M_4; δA is caused by mismatches of M_0, M_1, M_3, and M_4; whereas δBW is mainly induced by V_{off} of opamps A_{N1} and A_{P1}. It is known that the variances of W, L, and V_T due to process fluctuations are inversely proportional to the area of the MOSFET; therefore, as a first-order approximation, I_{off}, δA, and δBW are inversely proportional to $\sqrt{WL}$, which can be reduced by increasing the sizes of M_0, M_1, M_3, and M_4 and the input differential pairs of opamps in the ULCA, provided that the bandwidth specification is satisfied.

Incorporating the above considerations on stability, noise, and mismatch, HSPICE simulations are made on the circuit to meet the circuit specification in Table 3, and the optimized quiescent current is designed as I_{ref} = 1.5 nA, whereas capacitors C_0 and C_1 are set to 1 pF. Monte Carlo simulation based on the design kit of SMIC 0.18-μm CMOS technology also shows that I_{off} and BW are within −30~120 pA and 12~16 kHz, whereas $\delta A/A$ is less than ±5%, when the channel length is chosen as L = 1 μm, and the aspect ratios (W/L) of N and P transistor units are 10 and 20, respectively.

3.5 Experiment and discussions

The ULCA is realized in the SMIC 0.18-μm CMOS mixed-signal technology, and Fig. 8 shows the die micrograph of the chip. The box encloses the ULCA circuitry, which occupies about 230 × 80 μm² of the chip area. The performance of the ULCA is measured in terms of gain, bandwidth, noise, offset, etc. The results are shown and discussed in this section.

To test the performance of the ULCA, very large resistors (from 1 to 10 GΩ) are used to convert the voltage into input currents down to the picoampere or sub-nanoampere range, which may further keep the input noise current small since the input noise current spectrum density due to the resistor is inversely proportional to the resistance. The whole circuit is placed in an aluminum box with Bayonet Neill-Concelman (BNC) connectors to shield from unwanted interferences. In the experiment, V_{REF} is biased at 0.9 V to provide maximized input range on both positive and negative directions while satisfying the voltage range specifications in Table 3. The input voltage varies between 1.9 and −0.1 V to provide the positive and negative input currents by replacing the resistors.

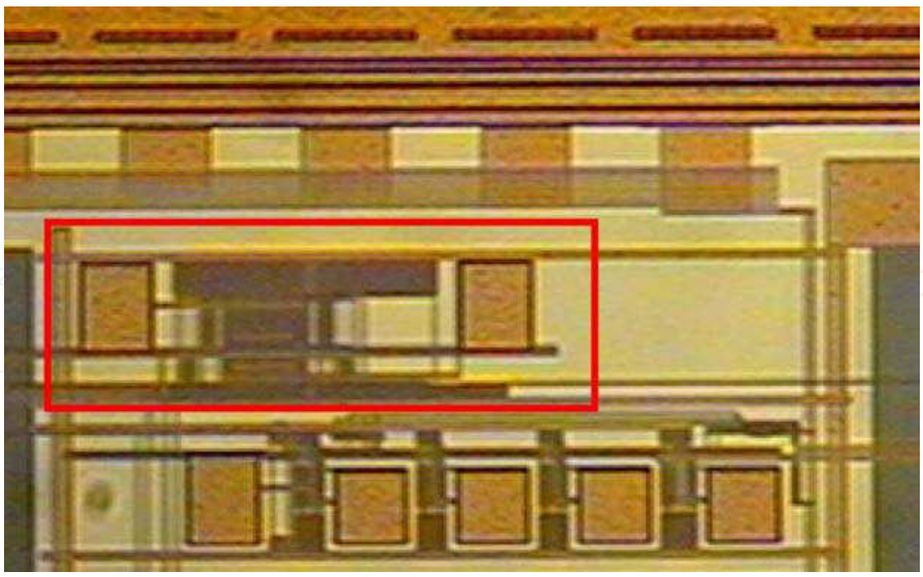


Fig. 8. Die micrograph of the ULCA circuit.

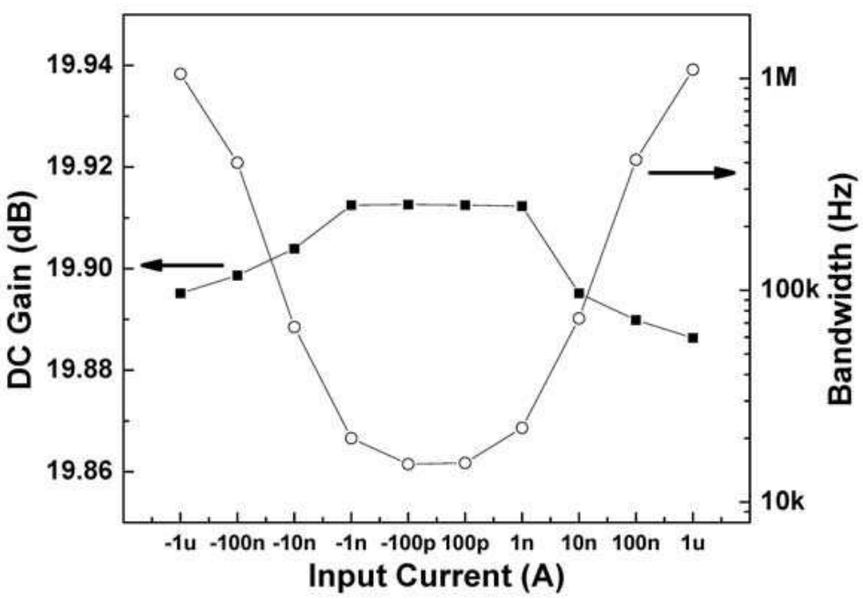


Fig. 9. DC gain and bandwidth as functions of input currents ranging from −1 to 1 μA. The black squares represent the dc gain, whereas the circles illustrate the bandwidth.

The DC gain as a function of input currents ranging from −1 to 1 μA is plotted in Fig. 9, which is 0.5% lower than the designed value of 20 dB and implies about 2% of the overall mismatch on transistors M_0, M_1, M_3, and M_4 due to fabrication variations. The gain error over the input range is less than 0.3%. One can certainly increase the transistor dimensions to further reduce the mismatch and achieve better linearity, however trading with the bandwidth performance.

The bandwidth has been characterized by analyzing the step response of the ULCA, which is cascaded by a commercial transimpedance amplifier, and the result as a function of input

currents is also illustrated in Fig. 9. It can be seen that the bandwidth basically linearly increases with the input current levels on both positive and negative directions from around 20 kHz to 1 MHz. The minimal bandwidth of 15 kHz occurs in the low-input cases, satisfying the 10 kHz requirement in the application. The overshoot of the bandwidth is because the offset of opamps A_{N1} and A_{P1} and the threshold mismatch shift the actual quiescent current of M_0 and M_3 up to around 2 nA (estimated value) from the designed value of 1.5 nA. A larger bandwidth may slightly degrade the noise performance and sensitivity, but it could be adjusted by somewhat tuning the biasing current I_{ref} down for compensation.

The IRO is analyzed by keeping the input open while measuring the mean current at the output and dividing by the gain, which is found to be 96.6 pA at V_{OUT} = 0.9 V. The IRO corresponds to the offsets of opamps and mismatches at the output node; however, it is not critical for the application. One can either slightly modify V_{OUT} for compensation or do the calibration after acquisition and analog-to-digital conversion in the digital domain by a simple subtraction.

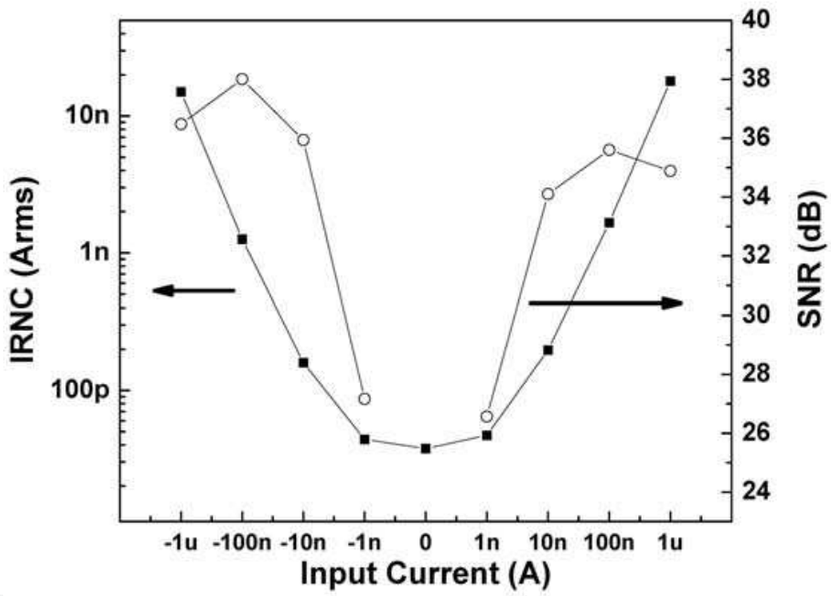


Fig. 10. IRNC and SNR as functions of input currents ranging from −1 to 1 μA. The black squares represent the IRNC, whereas the circles illustrate the SNR.

The noise performance of the ULCA is characterized in terms of the input-referred noise current (IRNC) by measuring the mean-square-root value of the output current fluctuation at each input current level and dividing by the gain. The result is shown in Fig. 10. It is noticed that the IRNC of the ULCA starts at 37.6 pArms at zero input and basically remains at the same level for $|I_{in}| < 1$ nA, whereas it linearly increases for larger input levels. The target current sensitivity of ~100 pA is satisfied. The signal-to-noise ratio (SNR) increases for $|I_{in}| < 10$ nA and gradually saturates at values around 36 dB for larger input levels. The SNR is smaller on the positive input side than on the negative side; this is due to the fact that nMOS exhibits a higher current noise than pMOS. It is worth mentioning that the minimal noise current is larger than the simulated value of 12 pArms but falls in the range provided by Monte Carlo simulation by utilizing parameters from the foundry, which can

be explained from two aspects: 1) the actual quiescent current of M_0 andM_3 is slightly larger than the designed value due to offsets of the opamp; and 2) the mismatches of M_0, M_1, M_3, and M_4 degrade the symmetry of the ULCA topology, thus increasing the noise level.
Linearity is presented by the gain versus input characteristic in Fig. 11. The gain approximately remains at 19.9 dB for the input range of −100 to 100 μA and degrades for larger input levels. The maximal input current is estimated to about ±0.4 mA as determined by the 1-dB (or 10% in the linear scale) degrading point of gain, which implies 141 dB of headroom-to-noise ratio or equivalent to 23 bit. Moreover, depending on the electric properties of the DNA sensor and the buffer solution, the minimal impedance from the biosensor electrode is around 5 MΩ. The input impedance of the ULCA is measured as 15.5 kΩ, which is much lower than the biosensor impedance in the application, satisfying the interface condition.

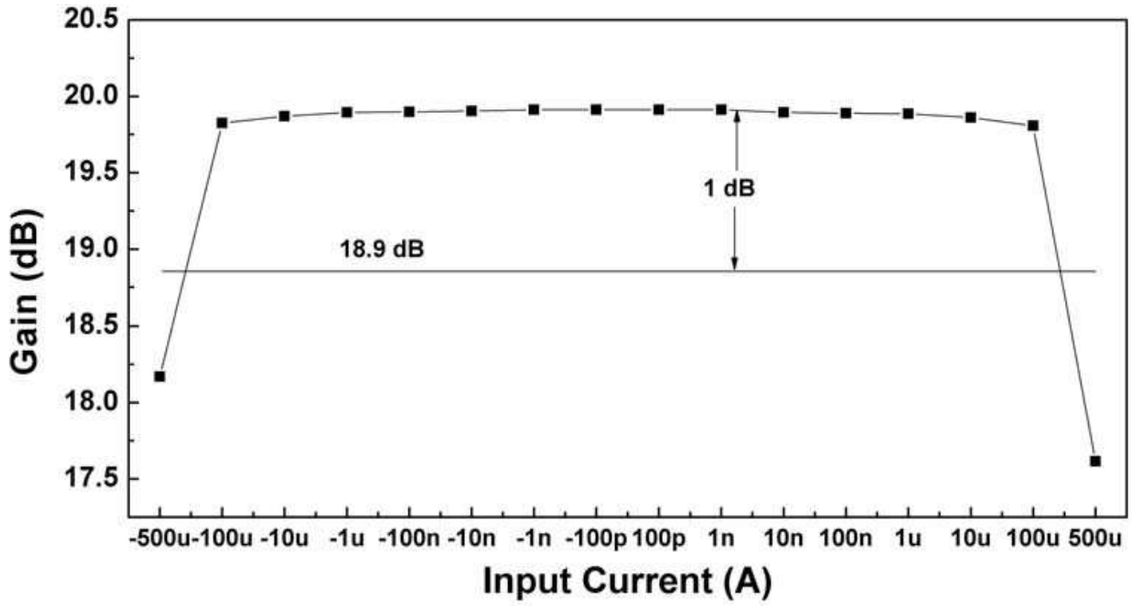


Fig. 11. Gain versus input current over the entire input range.

DC gain	19.9 dB
3-dB bandwidth	15 kHz
Current sensitivity	37.6 pArms
Potential variation	583 nVrms
Input-referred offset	96.6 pA
Input impedance	15.5 kΩ
Max. input current	±0.4 mA
Input dynamic range	141 dB
DC power consumption	35 μW
Power supply	1.8 V

Table 4. Summary of circuit parameter of the ULCA.

A novel subthreshold Class AB ULCA aiming at the application of signal preamplification in the IBS has been demonstrated in SMIC 0.18-μm CMOS technology. Experimental results show that the ULCA completely accommodates the application and can provide a current gain of 19.9 dB, 3-dB bandwidth of 15 kHz, and an input range of −0.4 to 0.4 mA, whereas the IRO and the noise current are less than 96.6 pA and 37.6 pArms, respectively. Table 4 shows the summarized parameters of the circuit. The ULCA can also be used for ultralow current amplification in other types of biosensor interfaces, nanoscale device sensing, and optical sensing in the future.

4. Discussion

4.1 A few trade-offs

In order to accurately acquire signals during the sensing process, CMOS IBS has to work on a stable electrolyte potential, which is precisely controlled by the potentiostat through the reference and counter electrodes from a negative feedback mechanism. The potential variation is mainly due to the offset and noise of the potentiostat OTA. Offset can be reduced by increasing the size of input differential pair of the OTA, or introducing a digital correction circuit via a D/A converter and logics, but trades with the circuit area. On the other hand, noise can be reduced by either increasing the size or biasing current of input differential pair, but trades with the area and power, respectively.

The sensitivity of CMOS IBS is mainly governed by the acquisition circuits, which translates to the IRNC of ULCA. One can reduce IRNC by reducing the DC quiescent current, but trading with the bandwidth required in the biosensing. In some biosening systems with low electrolyte impedance, noise voltage (potential variation on the working electrode) of ULCA also becomes a concern, which also trades with the power and area of the circuit.

In general, interfacing circuits is the bottle neck of the CMOS IBS design. A good design comes with various requirements of a specific biosensing system, which differs from one system to another. Various trade-offs must be considered in the circuit design according to the system specifications as well as power and area budgets.

4.2 Future research

Future research of CMOS IBS covers a number of directions to further improve the efficiency and performance of the system. One of the methods is to incorporate a preamplification step such as polymerase chain reaction (PCR) or rolling circle amplification (RCA) before the electrical sensing, which increases the analyte concentration in the electrolyte and biosensing current level, thus relaxing the sensitivity requirements of the interfacing circuit. Keeping the same sensitivity, one can further shrink the dimension of electrodes and increase the scale of IBS to improve the throughput and sensing efficiency.

As the scale of IBS growing up, asymmetry due to the electrode layout also becomes an issue, because the current density distributes from the counter electrode to all the working electrodes in the electrolyte, which could be quite different from each other depending on the positions. Some structures such as multiple counter electrodes, interlacing electrodes, partition, etc are being investigated. Further research also needs to be invested to characterize the current distribution in the electrolyte for a specific electrode layout when the number of electrode scales up.

From the circuit angle, the sensitivity can be further improved by using the lock-in filtering, which extracts the current only at the vicinity of frequency-of-interest therefore minimizing

the background noise contributions and maximizing the signal-to-noise ratio. The challenge part is that a high resolution A/D conversion is required to translate current signals into digital domain before the digital lock-in filtering. Logarithmic transimpedance amplification is another candidate to achieve high sensitivity and satisfying the bandwidth requirements, while ameliorating the dynamic range limitations by compressing output voltage range. The signal decompress can be realized by digital circuits after the voltage digitization.

5. Conclusion

The CMOS IBS research and production continue to offer a fertile ground for innovation. In this chapter, design considerations on the CMOS IBS interfacing circuits, including the integrated biosensor array, potentiostat, and acquisition circuits, have been introduced. A number of circuit design trade-offs between potential variation, sensitivity, speed, dynamic range, power, and physical area have also been discussed. Finally, future research directions to further improve the IBS performances in terms of efficiency and sensitivity are reviewed.

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Biosensors

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A biosensor is defined as a detecting device that combines a transducer with a biologically sensitive and selective component. When a specific target molecule interacts with the biological component, a signal is produced, at transducer level, proportional to the concentration of the substance. Therefore biosensors can measure compounds present in the environment, chemical processes, food and human body at low cost if compared with traditional analytical techniques. Bringing together researchers from 11 different countries, this book covers a wide range of aspects and issues related to biosensor technology, such as biosensor applications in the fields of drug discovery, diagnostics and bacteria detection, optical biosensors, biotelemetry and algorithms applied to biosensing.

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