Chapter

# A Balanced Slew-Rate High-Voltage Integrated Bipolar Pulse Generator for Medical Ultrasonic Imaging Applications

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## Abstract

This chapter describes the use of silicon-on-insulator (SOI) technology to develop balanced slew-rate pulse generators for medical ultrasound scanners, especially for multi-channel portable systems. Since ultrasonic transducers are usually composed of piezoelectric materials, most of which are capacitive, and the resonant frequency is usually in the order of tens of MHz, it is preferred to convert the high-frequency excited signals into high-voltage pulses to efficiently drive the transducers. In addition, the second harmonic leakage of the high-voltage pulse signal output by the pulse generator needs to be controlled such that the pulse generator can be applied to tissue harmonic imaging. Based on these considerations, the pulse generator architecture with balanced rising and falling edges proposed in this chapter is designed by synthesizing low-power, high-speed level shifters and a high-voltage H-bridge output stage to output high-voltage pulse signals with low harmonic distortion. The entire circuit integrates an 8-channel pulse generator, producing pulse signals >100 Vpp. The rise and fall times of the pulses are within 18.6 and 18.5 ns, respectively. The overall quiescent current is <60 uA (including the on-chip power supply). The output current drive capability is >2 A and the second harmonic distortion is as low as −40 dBc, indicating that the integrated pulse generator can be used in advanced, portable ultrasonic harmonic imaging systems.

**Keywords:** high-voltage pulse generator, ultrasound transmitter, medical imaging, harmonic distortion, low-power on-chip supply

## 1. Introduction

Compared with computed tomography (CT), X-ray and magnetic resonance imaging (MRI), medical ultrasound imaging is relatively fast, inexpensive, portable and radiation-free, and has become one of the most popular modalities in clinical examination. Currently, besides conventional B-mode and Doppler ultrasonic modality, advanced imaging formation method, such as photo-acoustic (PA) imaging, elasto-graphic imaging, as well as harmonic imaging is gradually becoming an important medical assessment tool for these echo-graphic systems. PA imaging offers unique capabilities in studying biological tissue based on optical absorption

contrast [1]. This method converts a laser-induced ultrasonic signal into a measurable signal by means of a detector made of piezoelectric material. However, due to the sensitivity and bandwidth effects of the laser-excited ultrasonic signals to obtain high-quality and high-resolution PA images, they usually require broadband capabilities with frequencies above several hundred MHz, which is challenging in integrating PA imaging with conventional ultrasonic imaging modalities. Elastography is an imaging technology sensitive to tissue stiffness that was first described in the 1990s [2]. It has been further developed and improved to achieve a quantitative assessment of tissue stiffness. Elastography methods mainly utilize elastic changes in soft tissue caused by specific pathologies or physiological processes. However, currently the operator has to exert manual compression on the tissue with the ultrasound transducer to increase the imaging sensitivity. Manual compression works fairly well for superficial organs such as the breast and thyroid but is challenging for assessing elasticity in deeper located organs such as the liver, which practicality in medical instruments is not high. Harmonic imaging, however, based on the selective imaging of the harmonic frequency, especially using second harmonic signals for image formation [3]. Compared with PA imaging and elastographic imaging, second harmonic imaging can be easily implemented with conventional B-mode imaging and possesses higher lateral resolution and lower side lobes, and is, therefore, less sensitive to clutter and off-axis distortions [4].

However, since the echo signals detected by tissue harmonic imaging are generated by the nonlinear characteristics of the transmission medium according to the input fundamental wave signal, they are more susceptible to various harmonic sources. For example, the nonlinearity caused by the transmitted waveform, the bandwidth of the medical transducer, and the distorted echo signal can induce harmonic leakage and affect the overall performance of the imaging [5]. Several methods have been proposed in the literature to study the effects of harmonic leakage and to address sensitivity issues such as coded excitation, bandpass filter separation techniques [6] and pulse inversion [7]. These techniques have one thing in common, that is, they ultimately request Gaussian-type transmit signals with low harmonic content. Generating such signals typically requires a digital-to-analog converter (DAC) and a high-voltage linear power amplifier [8–10], which is not cost effective and power hungry, especially for compact devices applications such as portable ultrasound scanners. In order to reduce system power consumption, it is usually a good choice to use a pulse generator. However, as indicated in [11], the power of the second harmonic signal is at most 20 dB less than the power of the fundamental frequency signal. In fact, due to the bandwidth limitations of the ultrasonic transducer, this difference has become even larger [12]. Therefore, achieving the signal-to-noise ratio required for harmonic imaging requires the harmonic signal generated by the pulse generator itself as low as possible.

Generating low-power, low harmonic leakage, gated high-voltage pulse waves is not easy, and from a distortion perspective, the pulse generator must be carefully designed because the excitation device designed to drive the medical ultrasound transducer needs to be maintained a high voltage (>50–100 Vpp) output with faster switching capability than a few MHz. In most of the past, high voltage pulse generators implemented using discrete components for ultrasound imaging systems have demonstrated superior performance [13, 14]. Traditional off-the-shelf pulse generators typically operate below 10 MHz and are limited in size in multi-channel transmitter applications [15]. Recently, integrated pulse generators for multi-channel, portable and compact ultrasonic scanners have been developed [16–20]. For these devices, if harmonic distortion is not considered, it can be easily developed using a high voltage CMOS compatible process. For example, bipolar pulse

generators are less sensitive to even harmonic distortion and can produce lower harmonic pulses. However, if the transmitter is designed without regard to the slew rate of the rise and fall times and the positive and negative conduction times of the output voltage, a large second harmonic would be generated [21]. Some prior works employed multiple voltage-level pulse generators to reduce harmonic distortions [22–24], and these techniques usually require couples of voltage sources, thus increasing design complexity. In this chapter, we presented our design of a pulse generator architecture with a balanced slew-rate both in rising and falling edges to improve second harmonic distortion, and develop this pulse generator using CMOS-SOI technology for medical ultrasound scanners, especially for harmonic imaging applications.

This chapter is organized as follows. Section 2 considers the pulse excitation signals required in harmonic imaging systems. Section 3 describes the detailed design and circuit level implementation of the high voltage pulse generator. In Section 4, the experimental results of driving a medical grade piezoelectric transducer (PZT) with a designed pulse generator are given. The conclusion is given in Section 5.

## 2. Pulse excitation signals in harmonic imaging system

Since high-voltage excitation signals such as square waves or trapezoidal waveforms can efficiently drive ultrasonic transducers, harmonic components of such waveforms need to be considered in order to achieve low harmonic output for our applications. Given the nature of these ideal waveforms, Fourier analysis makes it easier to display their spectrum and explore the possibility of generating such a waveform. Basically, slew-rate limiting signals can reduce radiated emissions (electromagnetic interference and radio frequency interference) and harmonics of its fundamental portion. Therefore, we can consider a digital signals, $f(t)$, that are not ideal square waves, but may be approximated by trapezoidal waveforms with finite rise and fall times, $t_r$ and $t_f$, as shown in **Figure 1**. This waveform employs characteristics of many digital signals, including clock pulses and PWM waveforms. In **Figure 1**, "$A$" stands for the amplitude of the signal, $T_{period}$ is the signal's period, $T_{on}$ and $T_{off}$ set for the turn-on and turn-off time, respectively. The waveform can be expanded in a Fourier series as shown in Eq. (1) and the expansion coefficients are given by Eq. (2).

$$f(t) = C_0 + \sum_{n=1}^{\infty} C_n \cos\left(n\omega_0 t + \varnothing_{cn}\right) \tag{1}$$

$$C_n = \frac{1}{T}\int_{t_0}^{t_0+T} f(t)e^{-jn\omega_0 t}dt \tag{2}$$

$$\text{where } C_0 = \frac{AT_{on}}{T_{period}} - \frac{A}{2} \tag{3}$$

For $n \neq 0$ and if $t_r = t_f$, the magnitudes of the Fourier coefficients, $C_n$, are given by

$$C_n = 2\frac{AT_{on}}{T_{period}}\left|\frac{\sin\left(\frac{n\pi t_r}{T_{period}}\right)}{\frac{n\pi t_r}{T_{period}}}\right|\left|\frac{\sin\left(\frac{n\pi T_{on}}{T_{period}}\right)}{\frac{n\pi T_{on}}{T_{period}}}\right| \tag{4}$$

From (Eq. (4)), it can be observed that the waveform's harmonic energy at high frequencies is less than that of an ideal square wave if the rise and fall times are finite. Moreover, if the pulse has equal duty cycles for the turn-on and turn-off period, i.e.,

$$T_{0n} = T_{off} = \frac{1}{2} T_{period} \tag{5}$$

$$\left| \frac{\sin\left(\frac{n\pi T_{on}}{T_{period}}\right)}{\frac{n\pi T_{on}}{T_{period}}} \right| = \left| \frac{\sin\left(\frac{1}{2} n\pi\right)}{\frac{n\pi}{2}} \right| \tag{6}$$

Equation (6) is equal to zero for even $n$, which stands for NO even harmonics when the duty cycle of the excitation pules is 50% (This is a reasonable assumption and can be easily achieved by generating such a signal.).

The value of $t_r$ in Eq. (4) affects the higher order terms of $C_n$. While in the general case of $t_r = t_f$, the larger the $t_r$ ($t_f$), the lower the harmonic terms at high frequency, which, in fact, has a low-pass filtering effect. When deriving the spectrum of this pulse train, the case of equal rise and fall times is often assumed. However, the difference between the rising edge and the falling edge causes excessive harmonics, and even if the duty ratio remains 50%, even harmonics still occurs due to such a nonlinear effect.

In order to model the effects of higher order harmonic terms at high frequencies due to non-linear rising and falling edges, a repetitive trapezoidal waveforms with slew-rate limited rise and fall times and a normalized −1.0 to +1.0 V peak-to-peak voltage swing can be modeled using Eq. (7). It is generally happened when the switching FET has a non-linear on-resistance, causing the output waveform an unsymmetrical rise and fall times, which is a phenomenon that often occurs with pulse generators. To simulate the effects of different slew-rates, the rise and fall times can be readjusted by changing the boundary conditions of each section in Eq. (7). The simulated bipolar pulse signals with unbalanced slew-rates are shown in **Figure 2** [21]. The pulses in **Figure 2** assume uniform amplitude envelopes. The bandwidth of such waveforms is inversely proportional to the time period, $T_{period}$, in **Figure 2**, and for simplified illustrations of slew-rate effects, the center frequency of the pulse signal is fixed to 2 MHz.

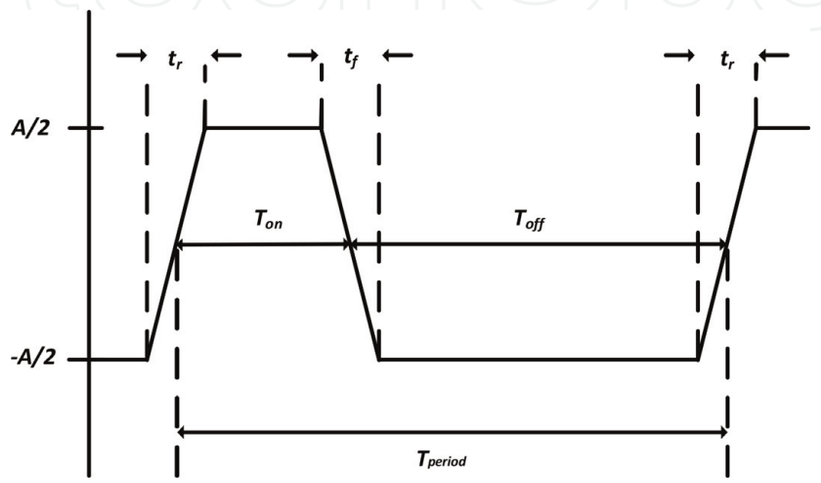


**Figure 1.**
*A typical trapezoidal waveform or square waveform with the limited rise/fall time.*

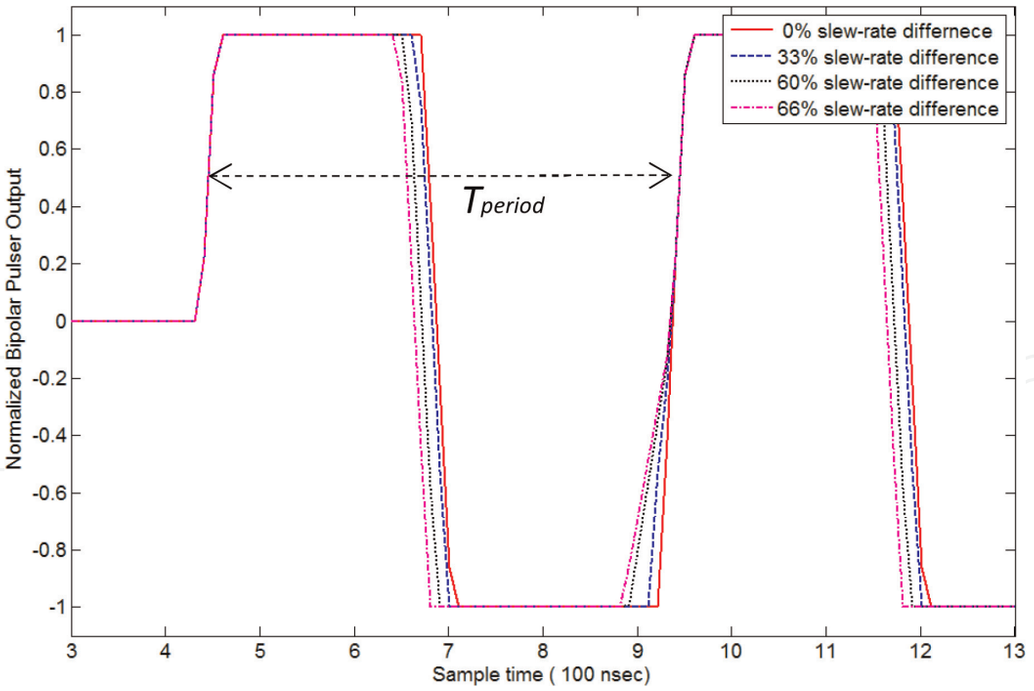


**Figure 2.**
*Modeling of a bipolar pulse waveform with different slew-rates (rise/fall times) [21].*

$$f_{trapezoid}(x) = \begin{cases} -4 - \dfrac{4x}{\pi} & \text{if } -\pi \le x < -3\pi/4 \\ -1 & \text{if } -3\pi/4 \le x < -\pi/4 \\ \dfrac{4x}{\pi} & \text{if } -\pi/4 \le x < +\pi/4 \\ +1 & \text{if } +\pi/4 \le x < +3\pi/4 \\ 4 - \dfrac{4x}{\pi} & \text{if } +3\pi/4 \le x < +\pi \end{cases} \tag{7}$$

In **Figure 2**, the slew-rate difference in percentage (SRDP) of the Rising_time and Falling_time can be defined in Eq. (8) as an important factor in evaluating signal harmonic damage. In Eq. (8), the Rising_time and Falling_time are defined as the pulse response to rise/fall from 10/90 to 90%/10% of its final values.

$$\text{SRDP} = \frac{|\text{Rising time} - \text{Falling time}|}{\text{Falling time}} \times 100\%. \tag{8}$$

Fourier analysis of this trapezoidal waveform provides harmonic magnitudes similar to that for an unsymmetrical square wave, except that there is an additional term that limits the high frequency content. **Figure 3** shows the spectrum of the excitation signals with equal on_time and off_time but different slew-rates, as shown in **Figure 2**, after mixing with the impulse function of the ultrasound transducer [21]. A unit-gain ultra-wideband transducer is assumed here without loss of generality to investigate the frequency components of the transmit signals. The spectrum shown in **Figure 3** presents that the second harmonic portion is damaged by signals with unequal slew-rates. For instance, the desired SRDP should be <33% in order to keep the second harmonics 40 dB lower than the fundamental tones.

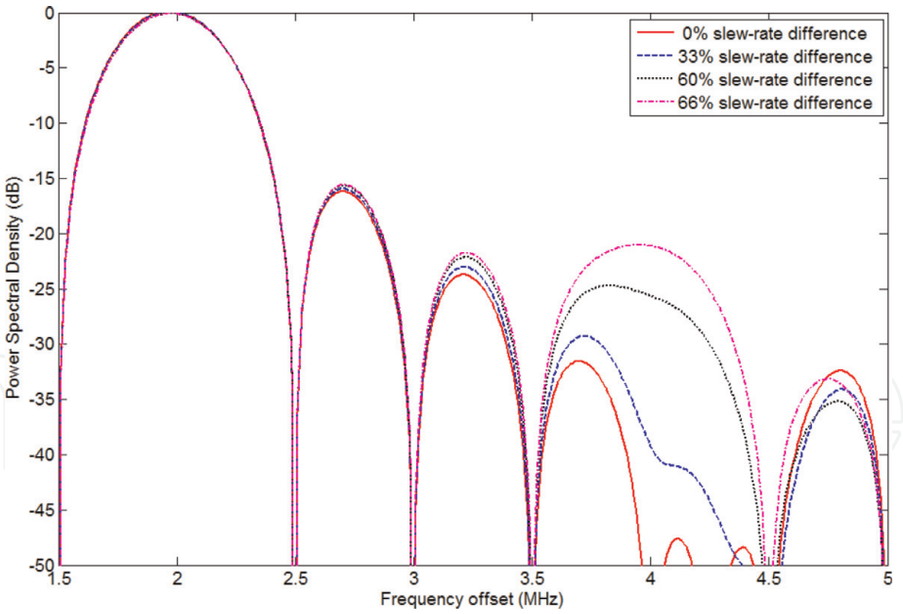


**Figure 3.**
*The frequency spectra of the bipolar pulse waveforms with the different slew-rates (rise/fall time) [21].*

Therefore, in order to maintain an excitation signal having a low second harmonic content, it is essential to control the pulse generator's slew-rate during the rising and falling edges.

## 3. High-voltage pulse generator for medical ultrasound

A diagnostic medical ultrasound image is acquired by transmitting acoustic waves and receiving echoes that are reflected from cell boundaries [20]. **Figure 4** shows a typical ultrasound analog front-end diagram comprises an HV pulse generator, an HV multiplexer (HV MUX), a T/R switch, a low noise amplifier (LNA), a variable-gain amplifier (VGA) and an analog-to-digital converter (ADC) [24]. The digital signal processor generates a sequence of low-voltage transmit signals with different delays for the pulse generator. The pulse generator drives the transducer at a high voltage level that, after exciting the array of ultrasonic probes, transmits a focused beam to the subject. Since the tissue of each part of the human body has discontinuous impedances to sound waves, the frequency and speed at which the transducer receives reflected sound energy from the body will result in distinguishable conditions. The T/R switch is used to reduce the interference at the receiving

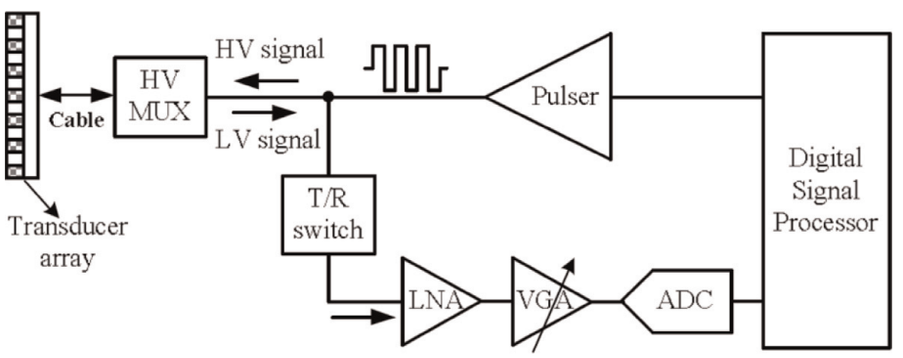


**Figure 4.**
*A typical ultrasound system block diagram.*

end of the LNA from the high voltage transmitter. When the pulse generator sends a high voltage transmitting pulse, the LNA is isolated from the pulse generator and the transducer by turning off the T/R switch, and when these echo signal is sent to the LNA via the T/R switch, the system is in receive mode, the pulse generator is disabled and the T/R switch is turned on, and the LNA and the follow-up VGA amplify the received signal and send the signal to the ADC. The digital signal processor generates information such as images or Doppler sound waves based on the output data of the ADC. In order to increase the strength of the echo signal, typically, multichannel transceivers are indispensable in modern ultrasound systems, which inevitably increase system complexity and power budget. The generation of multiple high voltage pulses, however, has been historically a challenge in the ultrasonic imaging system, particularly for today's portable solution. In the following section, we focused on the design and implementation of an integrated high-voltage pulse generator for multi-channel ultrasonic systems.

### 3.1 Single-chip high-voltage pulser architecture

The schematic of the integrated high-voltage pulse generator is shown in **Figure 5**. It mainly consists of three stages, including the input stage, on-chip floating power supplies, and H-bridge power driver. Several techniques are employed in this high-voltage pulse generator design to achieve low static power and low harmonics at the output. These techniques are described in the next section.

#### *3.1.1 Input stage*

The input stage, as shown in **Figure 6**, consists of signal conditioners (buffers), a dead time generator, and a return-to-zero controller. The input stage deals with the control of the pulse generator and produces HSDP, LSDN, RTZP, RTZN four signals to switch on/off the following H-bridge power driver. The two input control signals, IN1 and IN2, are generated separately from the outside signal generator or a DAC with synchronized phases. One of the control signals is a half cycle delay from the other to drive the push-pull stage at the output. The advantage of this architecture is that by adjusting the duty cycle of the input signals of IN1 and IN2, respectively, the error between on_time and off_time can be reduced, as shown in Eq. (6).

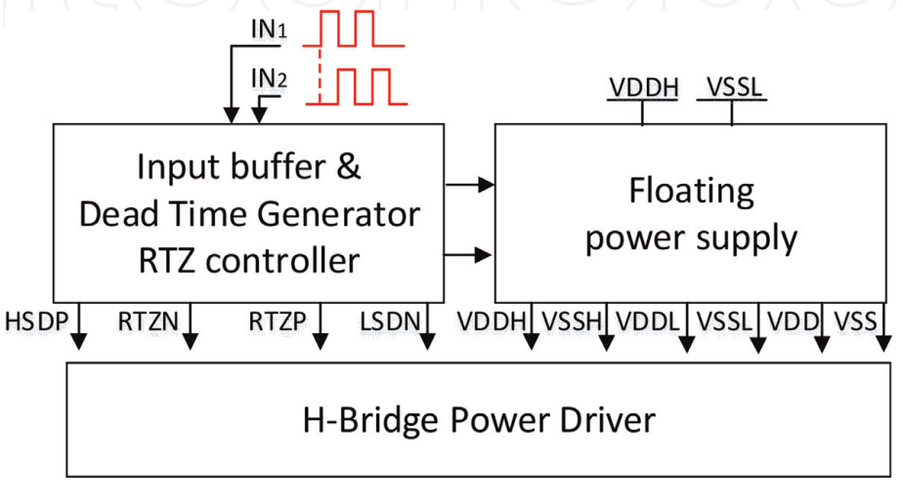


**Figure 5.**
*Proposed architecture of the integrated bipolar pulse generator.*

### 3.1.2 H-bridge power driver

The H-bridge power driver, as shown in **Figure 7**, composed of level shifters, pre-drivers, two high-voltage diodes (D1/D2), and four power transistors (MP1/2 and MN1/2). The low voltage and high voltage levels of the input control signal are 0 and 5 V, respectively. When the voltage level of IN1 is high, MN1 is turned off and MP1 is turned on. MP1 drives the output to a high voltage, VDDH. When the voltage level of IN2 is high, power transistor MN1 pulls the output down to a low voltage level VSSL. The voltage levels of IN1 and IN2 are low during steady state and the output returns to zero voltage level via MP2 or MN2. To exclude shoot-through current between MP1 and MN1, a dead-time control circuit is used as shown in **Figure 6**, in which, the outputs of the dead time generator are not simultaneously "high." Level-Shifter #1 and Level-Shifter #2 then boost these two output signals to the voltage levels of VDDL to VSSL and VSSH to VDDH, respectively. Due to the large capacitive load at the gates of the final stage power inverters MP1 and MN1, two pre-drivers are used to improve the slew rate. In addition, to avoid ringing of the output in a steady state, a fast return to zero signal is required. The return-to-zero circuit includes a return-to-zero controller, Level-Shifter #3, delay circuit, two pre-drivers, two power transistors (MP2 and MN2), and two high-voltage diodes (D1 and D2) to prevent false conduction. To avoid affecting the reception of echo signals when the ultrasound system is in receive mode, the output of the pulse generator must quickly return from the voltage level of VDDH or VSSL to zero voltage level. As shown in **Figure 6**, the return-to-zero controller can be composed of a simple XOR gate and an inverter.

Generating a pulse signal with low second harmonic contents is not easy, requiring balanced rising and falling times at all operating frequencies and very accurate duty cycles. In order to control the balanced slew-rate of the output pulses,

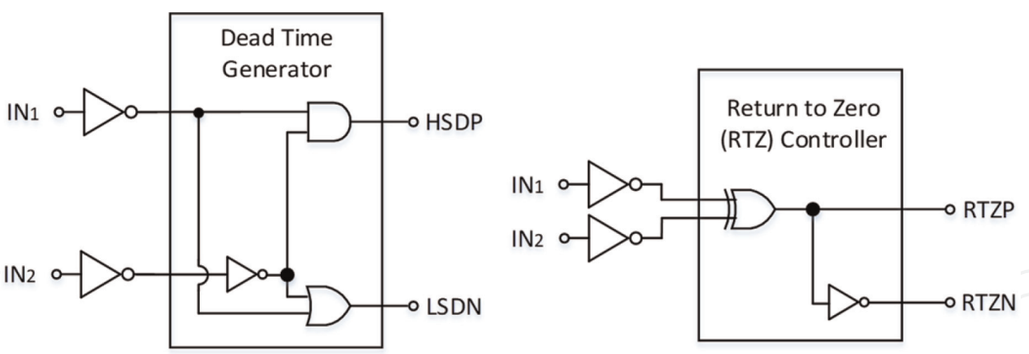


**Figure 6.**
*Input stage of the bipolar pulse generator.*

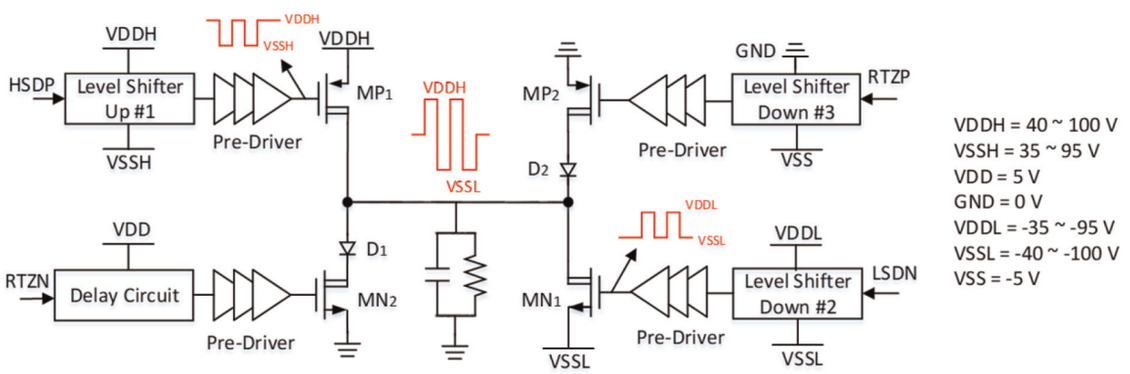


**Figure 7.**
*The H-bridge power driver.*

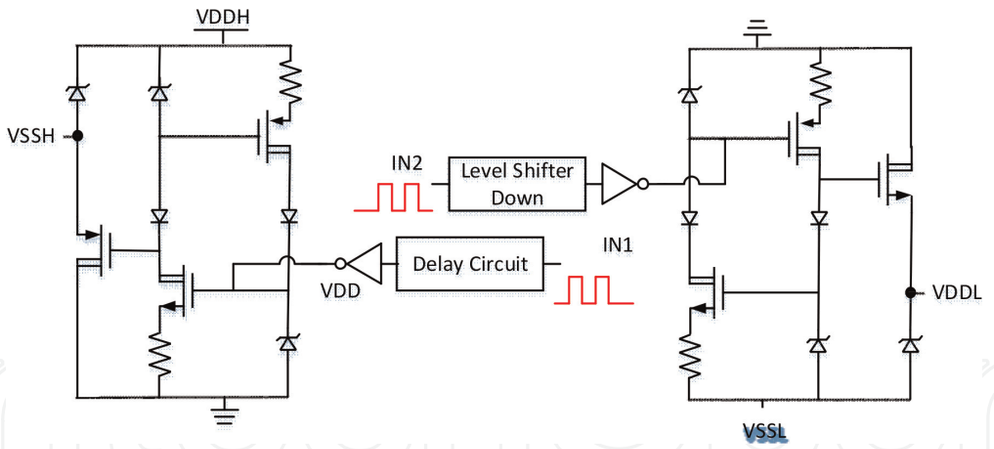


**Figure 8.**
*Floating power supply schematic and its controller.*

the rise/fall time of the level-shifters and output power inverters were carefully investigated. Sections 3.1.4 and 3.1.5 will describe in detail the design considerations of those key components.

### *3.1.3 Low-power floating power supply design*

Since the output stage uses a push-pull architecture, a pair of high-voltage PMOS and NMOS devices are employed as the output stage. Design of their driver stages can also use push-pull architectures to efficiently drive the output stage. Since the gate voltage of high-voltage PMOS/NMOS devices is limited by the maximum operating voltage of Vgs, the output voltage swing of the driver has to be within 5 V. Therefore, each driver requires a set of 5 V rail-to-rail power supplies to provide a source/sink current to the output. In order to simplify the power supplies, a floating voltage source architecture is employed. **Figure 8** shows two floating voltage sources generated by the VDDH and VSSL to ground, respectively. A pair of high-voltage PMOS/NMOS devices in series with two sets of Zener and high-voltage diodes form a voltage divider loop and outputs two voltages respective to the voltage drop of the Zener diode. Another two high-voltage PMOS/NMOS in parallel with the divider loop is functioned as the source follower to provide stable output voltages. For instance, the output voltage VDDL and VSSH, are generated by VSSL and VDDH as shown in Eqs. (9) and (10), respectively.

$$\mathrm{VSSH} = \mathrm{VDDH} - \mathrm{V_{Zener}} \tag{9}$$

$$\mathrm{VDDL} = \mathrm{VSSL} + \mathrm{V_{Zener}} \tag{10}$$

One of the advantages of this architecture is its fast settling and stable output even though the output voltage is not accurately regulated. However, it dissipates power once the VDDH or VSSL is applied and degrade the efficiency of the overall system. Therefore, a switch generated by the input signals are employed. The floating power supply can only work following the input signal's commands. When there is no input signal for a period of time, the floating power supply can be turned off to reduce the power dissipation.

### *3.1.4 Capacitive-coupled floating level-shifter design*

Level shifters are used in applications that require interfaces between different voltage domains. There are two types of level shifters: full-swing and floating,

which can be distinguished by whether the voltage domain shares a common ground potential. **Figure 9** shows the schematic of a conventional latch-based full-swing level shifter, which is to boost the input signal from a "Vlow" level to a "Vhigh" level. The inverter chain (M1–M12) is used to reconstruct the rail-to-rail digital signal from the off-chip input control signal. The cross-couple pair (M15 and M16) can latch the "high" digital signal level. When the input signal switches to a "low" level, M16 and M17 are turned off, and M15 and M18 are turned on. The output voltage is 0 V. However, as the input signal becomes to a "high" level, M16 and 17 are switched on, and M15 and M18 are switched off. The output voltage becomes to Vhigh.

The full-swing level shifter shown in **Figure 9** is not appropriate for PMOS/NMOS gate driver design since the gate driver needs a floating rail to switch on/off the last stage of the PMOS/NMOS devices. Floating level shifters, however, can shift the potential of control signals from circuits of a low voltage power rail to the potential with floating and ground rails, and therefore, the floating level shifters are often used in the gate drivers to drive output stages. **Figure 10** shows the designed capacitive-coupled level shifter architecture employed for the H-bridge power driver.

**Figure 10** shows the schematic of the floating level shifter for level shifter #1 to shift the signal voltage levels of 0 V and VDD to VSSH and VDDH, respectively. The level shifter consists of a pair of inverters (Mi1–Mi4), two coupling capacitors (C1 and C2), a latch (M19–M22), an output inverter (M23–M24), and a dummy inverter Mdum1 and Mdum2, which is to keep the same output impedance seen by inverters of M21 and M22. The pair of inverters is operated under 0 and 5 V power supplies, while the latch, the dummy inverter, and the output inverter are supplied with VSSH and VDDH power source. The pair of inverters and the latch are isolated by these two coupling capacitors, which couple through the control signals to the output stages. **Figure 11** shows the simplified model of the latched stage with the capacitive coupling between the input and the leveled outputs, in which, $G_m$ represents the sum of the trans-conductance of M19 and M20 (same as M21 and M22). $C_L$ is the input capacitance of M23 and M24. $R_L$ represents the output node impedance

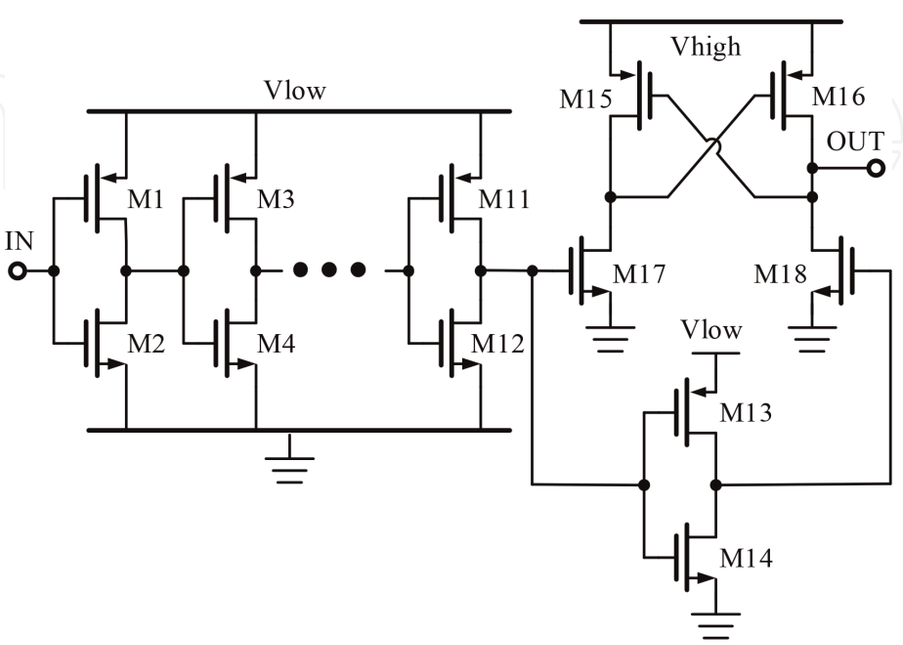


**Figure 9.**
*Schematic of a latch-based level-shifter.*

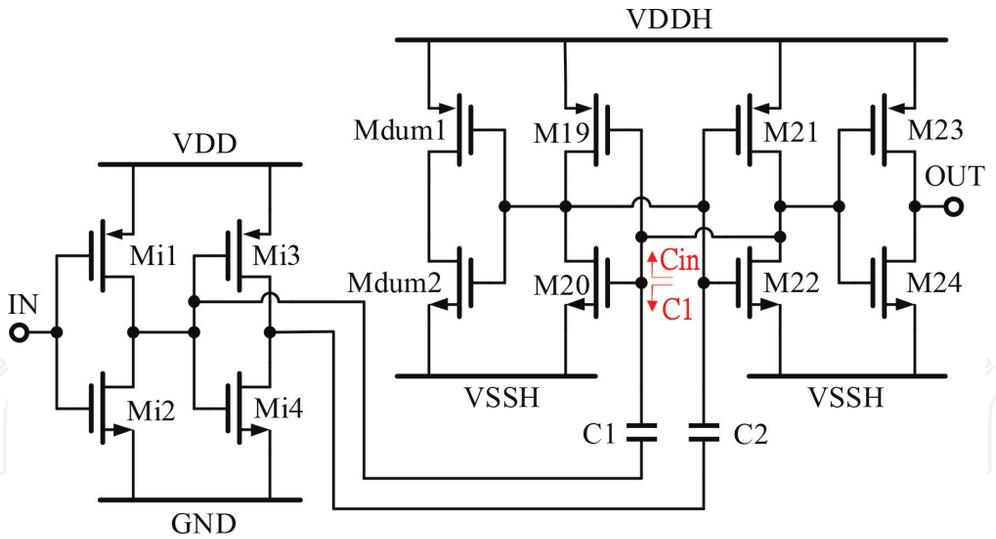


**Figure 10.**
*Schematic of a latch-based capacitive-coupled floating level-shifter.*

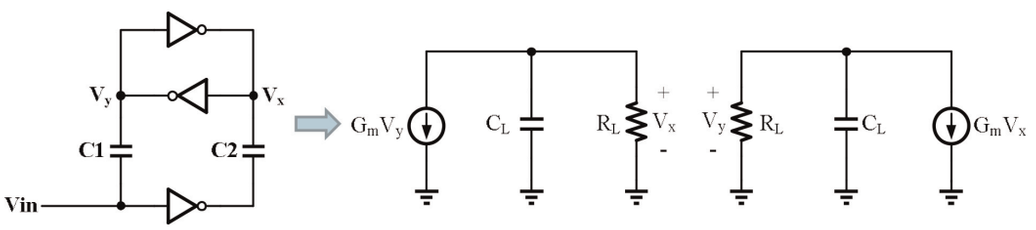


**Figure 11.**
*Simplified schematic of the floating level shifter.*

of M19 and M20. Following **Figure 11**, the dynamic behaviors of the latch output, $V_x$ and $V_y$, can be written in Eq. (11) and Eq. (12).

$$G_m V_y = -C_L\left(\frac{dV_x}{dt}\right) - \left(\frac{V_x}{R_L}\right). \tag{11}$$

$$G_m V_x = -C_L\left(\frac{dV_y}{dt}\right) - \left(\frac{V_y}{R_L}\right). \tag{12}$$

By replacing $R_L$ and $C_L$ with $\tau = R_L C_L$, $A_v = G_m R_L$, and reorder the formula, Eqs. (13) and (14) represents the cross correlation between $V_x$ and $V_y$.

$$\tau\left(\frac{dV_x}{dt}\right) + V_x = -A_v V_y. \tag{13}$$

$$\tau\left(\frac{dV_y}{dt}\right) + V_y = -A_v V_x. \tag{14}$$

From Eqs. (13) and (14), we can solve

$$\delta V = \delta V_0 * e^{\frac{(A_v-1)t}{\tau}} \tag{15}$$

where $\delta V$ is the voltage difference between the input and output of the Latch, i.e., $V_x$–$V_y$ in our design, and $\delta V_0$ is the initial voltage difference at the beginning of the latch phase. The transition time of the latch can be solved in Eq. (15) as

$$T_{latch} \cong \frac{C_L}{G_m} * \ln\left(\frac{\delta V}{\delta V_0}\right) \tag{16}$$

The slew-rate of the level-shifter can then be defined as in (Eq. (17))

$$SR^{+/-} = \frac{\delta V}{T_{latch}} \tag{17}$$

Since the latched time is reversed logarithmic proportional to $\delta V_0$, $T_{latch}$ will be too large to affect the desired slew-rate if $\delta V_0$ is a small value. From **Figure 10**, we can find $\delta V_0 = \frac{C_1}{C_1+C_{in}}$VDD; the capacitance ratio between the coupling capacitance and the input capacitance of the latches affects the latched time. The value of $C_1$ can be, therefore, designed comparable to that of $C_{in}$ to avoid a small $\delta V_0$. In addition, in order to have a balanced slew-rate of the level-shifters, the coupling capacitance ratio of between $C_1$ and $C_2$ can be another important factor after the latches have been designed. **Figure 12** shows the simulated slew-rate of the level-shifter as the value of the coupling capacitance is varied accordingly, which the optimal design can be found by choosing the corresponding coupling capacitance with $SR^+$ equal to $SR^-$. Since the coupling capacitor has to withstand a large voltage drop between VDDH and VDD, on-chip MOM capacitors were employed in series to increase the withstand voltage to 100 V for such applications. **Figure 13** shows the schematic diagram and layout of the on-chip MOM capacitor.

### *3.1.5 Final stage power inverter design*

The external slew rate of the pulse generator is also affected by the final stage design in addition to the balanced slew rate design of the level shifter. In order to coordinate the final slew-rate, the size of one power transistor, MN1 shown in **Figure 7**, is fixed, and the size of the other transistor, MP1, is swept accordingly. The output package effect is considered when sweeping the size of the transistor.

The package type used for the pulse generator is QFN-88L. The corresponding parasitic components are obtained using the ANSYS Q3D extractor. The outline of the QFN-88L package is shown in **Figure 14**. **Figure 15** shows the slew-rate of the rising and falling edges of the final stage as the device size of MP1 changes in the

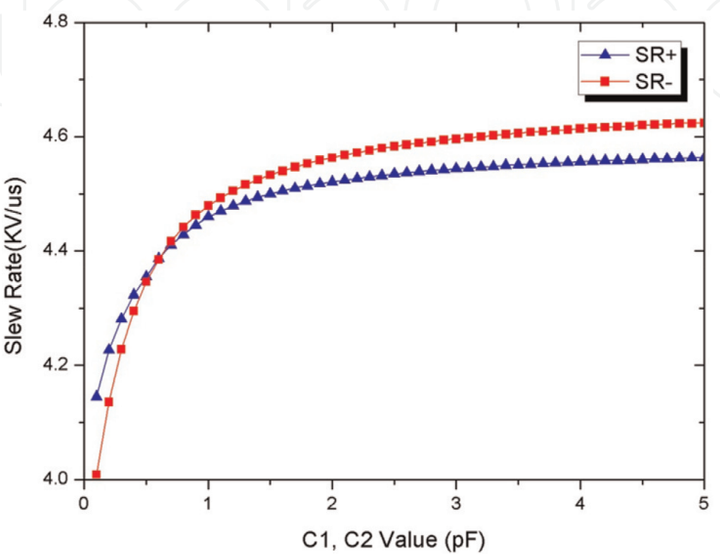


**Figure 12.**
*Simulated slew-rate of rising and falling edge of the level-shifter.*

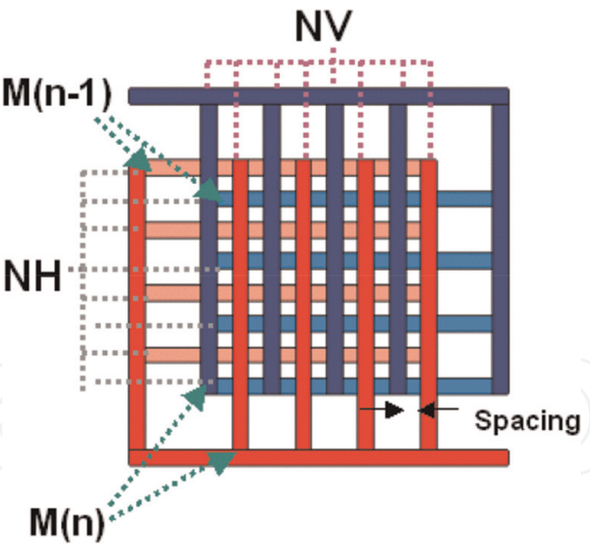


**Figure 13.**
*Schematic of the on-chip MOM capacitor (M presents the layer of the overlapping fingers).*

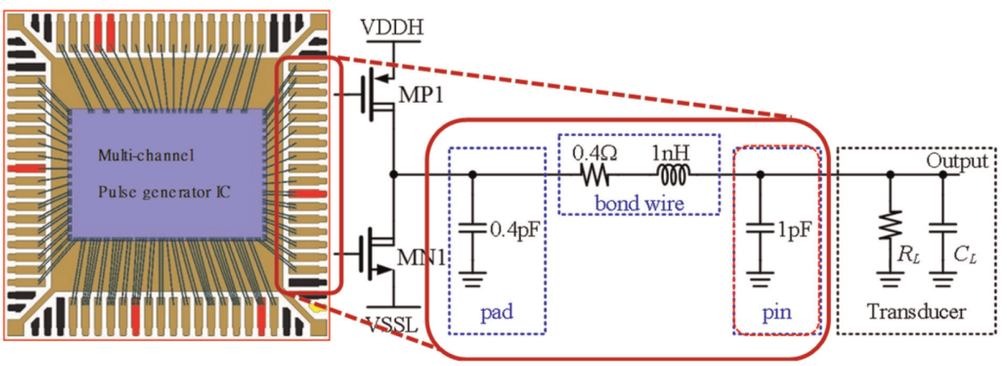


**Figure 14.**
*Package/chip joint design with the parasitic parameter extractions.*

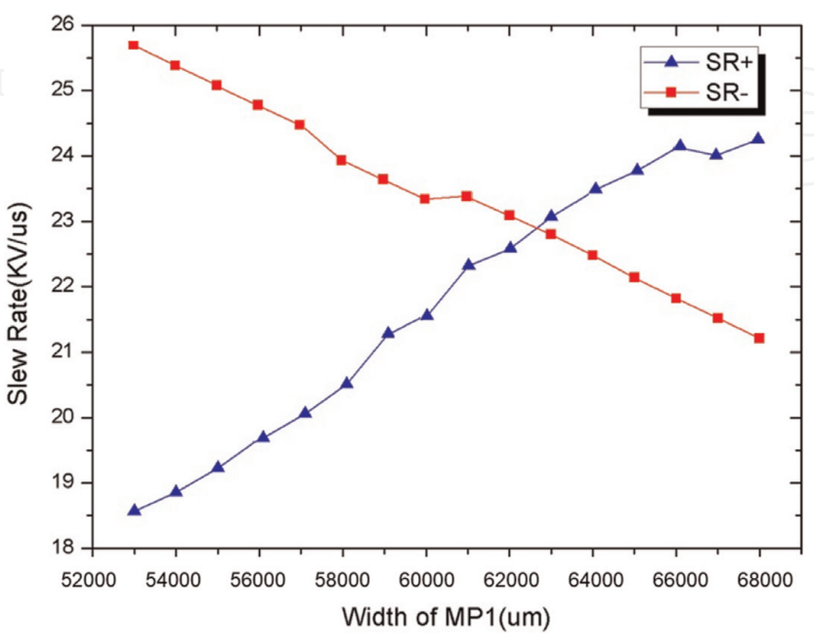


**Figure 15.**
*Simulated slew-rate of rising and falling edge of the final stage MOSFETs.*

simulated models. The optimum design width for this application is ~12,700 μm so that the final stage power MOSFETs operate at the same slew rate.

## 4. Experimental results

The proposed high-voltage pulse generator was fabricated in an 0.5 μm SOI-CMOS technology, which allows mixing different structures such as CMOS for digital circuits and high-voltage MOS structures for power and high-voltage applications on the same wafer with buried isolation layer [25]. **Figure 16** shows a cross-section of the SOI-CMOS process, and the high-voltage MOS transistors are fully compatible with the existing CMOS process. The final stage power transistors used

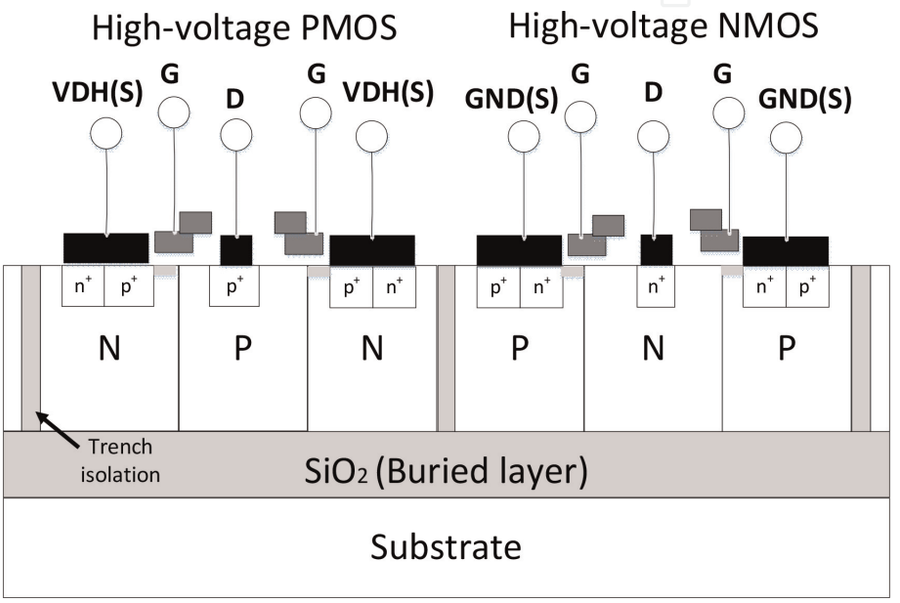


**Figure 16.**
*The cross-section view of high-voltage devices in a SOI-CMOS process.*

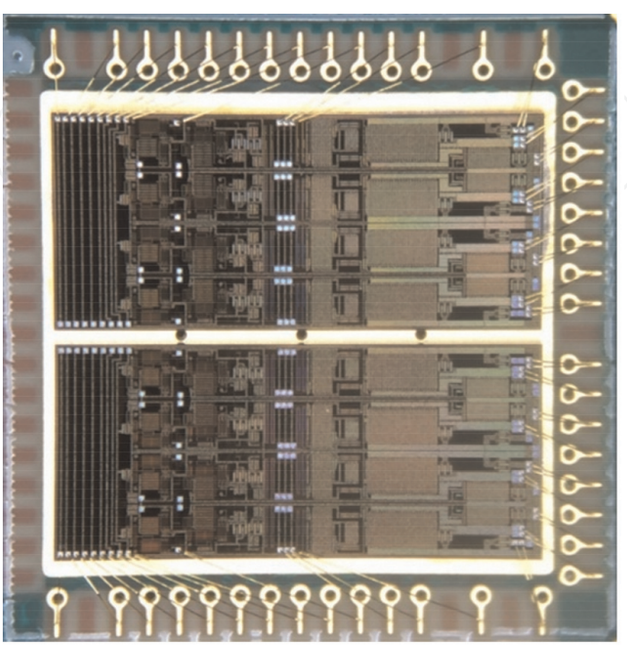

**Figure 17.**
*The photo of the integrated 8-channel pulse generator.*

in the design are 150-V N- and P-channel drain-extension field-effect transistors (FETs). The chip micrograph of the designed 8-channel pulse generator is shown in **Figure 17**, and it measures 8000 × 3510 μm area. The performance verification of the high voltage pulse generator was carried out by electrical and acoustic field measurement, which will be introduced in the next section.

### 4.1 Electrical performance verifications

The performance of the high voltage pulse generator is measured with a phased array probe using a 3.5 MHz gated input signal. The probe under test was Broadsound BS7L3, which has a fractional bandwidth of over 60%. **Figure 18** shows the measured bipolar voltage waveform and its spectrum diagram is shown in **Figure 19**. The second harmonic distortion is down to −40 dBc. The output voltage

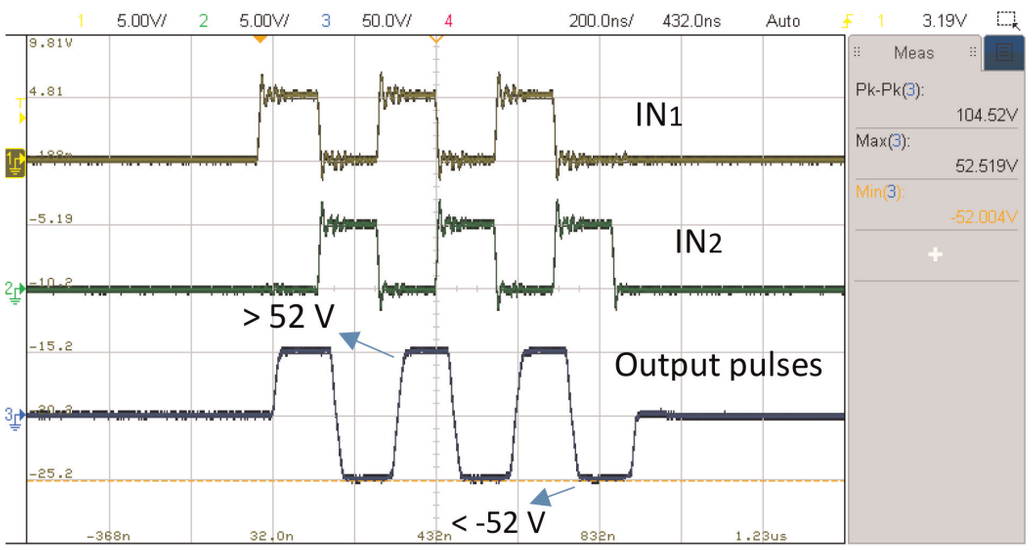


**Figure 18.**
*Measured input signals and output waveform of the proposed pulse generator under a 1-K ohm resistance in parallel with a 220-pF capacitance load.*

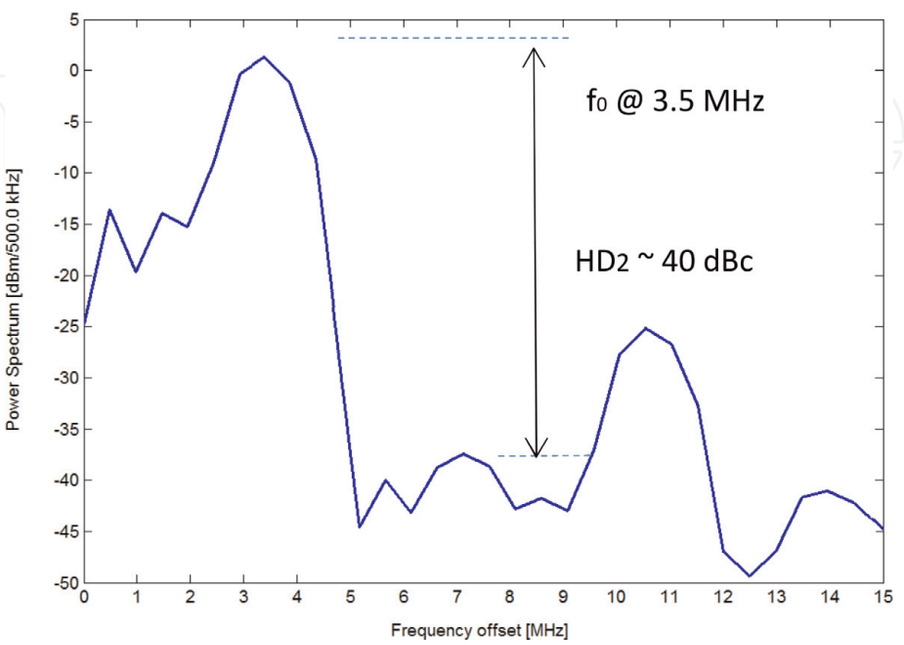


**Figure 19.**
*Spectrum analysis of the measured transmit waveform in **Figure 18**.*

| | This work | LM96550 | MAX14808 | MD2130 |
|---|---|---|---|---|
| Voltage level | 3 | 3 | 5 | Continuous |
| Technology | 0.5 μm CMOS-SOI | N/A | N/A | CMOS (discrete) |
| Output voltage (V) | 0 to ±70 | 0 to ±50 | 0 to ±100 | 0 to +125 |
| Operating frequency (MHz) | up to 20 | up to 15 | up to 10 | up to 15 |
| Peak current (A) | > 2 | 2 | 2 | 3 |
| Rising time (nsec) | 18.6 | 18 | 21 | - |
| Falling time (nsec) | 18.5 | 18 | 21 | - |
| Slew-rate (V/μsec) | 4.4 K | 2.2 K | 3.8 K | - |
| Output load | 1 kΩ//220 pF | 100 Ω//330 pF | 1 kΩ//240 pF | 1 kΩ//220 pF |
| HD2 (dBc) | -40 | -40 | -43 | -46 |
| Standby power (mW)/channel | 6 | 32 | 17 | 152 |

**Table 1.**
*Measured performance summary and comparison.*

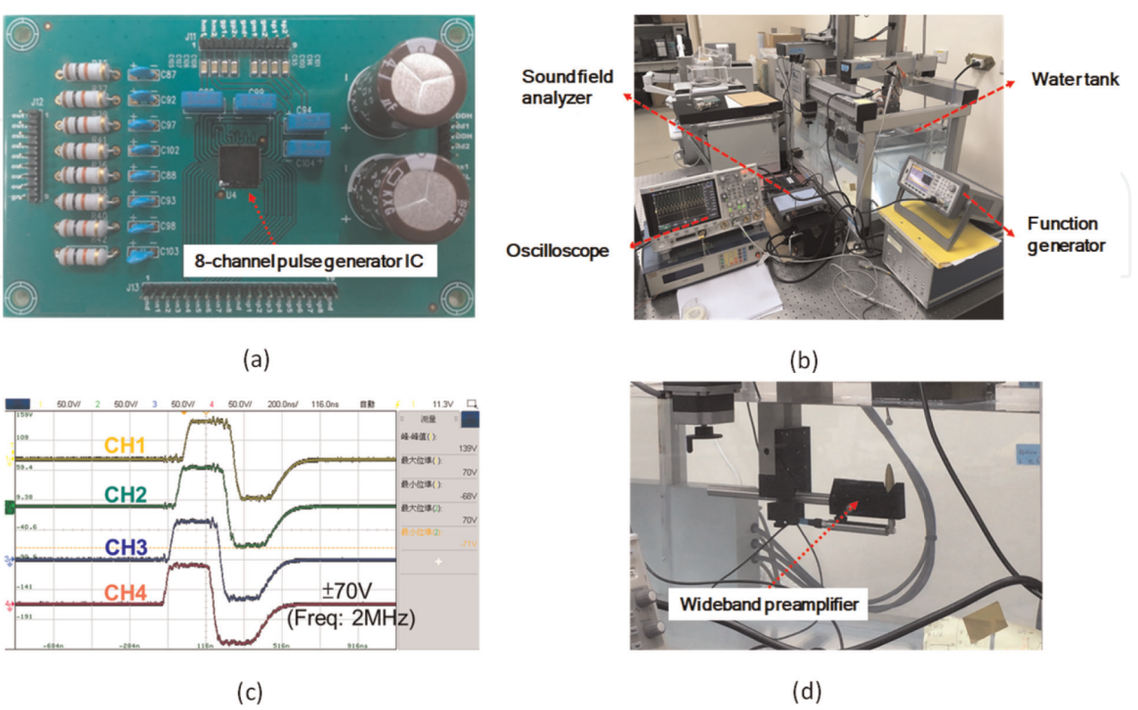


**Figure 20.**
*The 8-channel pulse generator in a single package and its assembly (a), ONDA acoustic field calibration system (b), multiple-channel delayed high-voltage pulse output (c), and the wideband receiver of the sound field measurement (d).*

can reach 100 Vpp with rising and falling times of 18.6 and 18.5 nsec, respectively. The static DC current provided to the pulse generator is about 60 uA per channel, which dissipates roughly 6 mW DC power. **Table 1** summarizes a performance comparison with several published works.

### 4.2 Acoustic field measurement results

The integrated 8-channel pulse generator test board for verifying transmit beamforming was assembled. The experiment was performed using an ONDA acoustic field calibration system. **Figure 20a** shows a picture of the designed 8-channel transmitter test board, and **Figure 20b** shows the picture of the measurement setup, mainly including a water tank to model the underwater environment and a sound filed analyzer to synthesize the beamforming results. After generating the input beamforming signals of different delay times by FPGA encoding, transducers are excited by these eight sets of high-voltage pulses. A wide dynamic range preamplifier is used to measure the sound field produced by the PZT probe after excitation by the pulse generator. **Figure 20c** presents the four-channel high-voltage output (±70 V) with certain preset delay. **Figure 20d** presents the wide-band receiver for the acoustic field measurements. **Figure 21** shows the measurements of transmit beamforming. The maximum 4 MPa was obtained at the focal

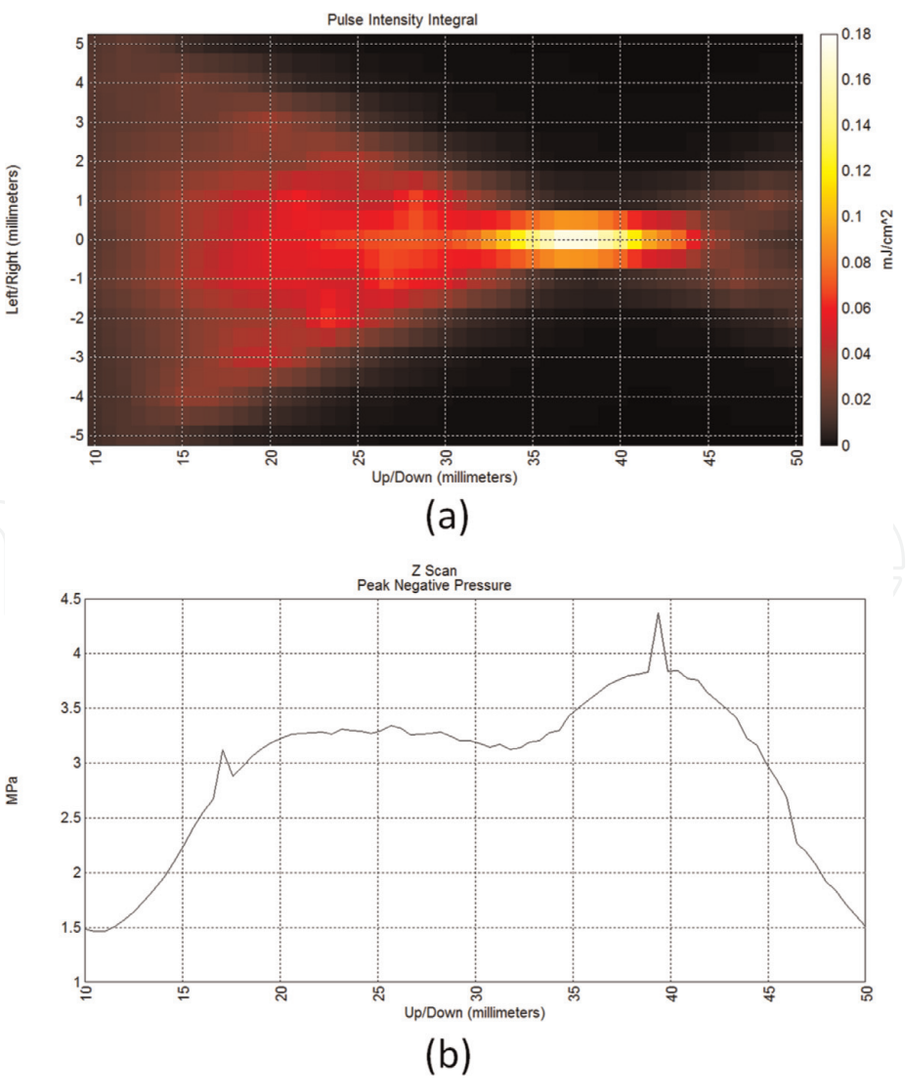


**Figure 21.**
*Measured underwater acoustic field using the 8-channel pulse generator (a) and the maximum 4 MPa was obtained at the focal plane after beamforming (b).*

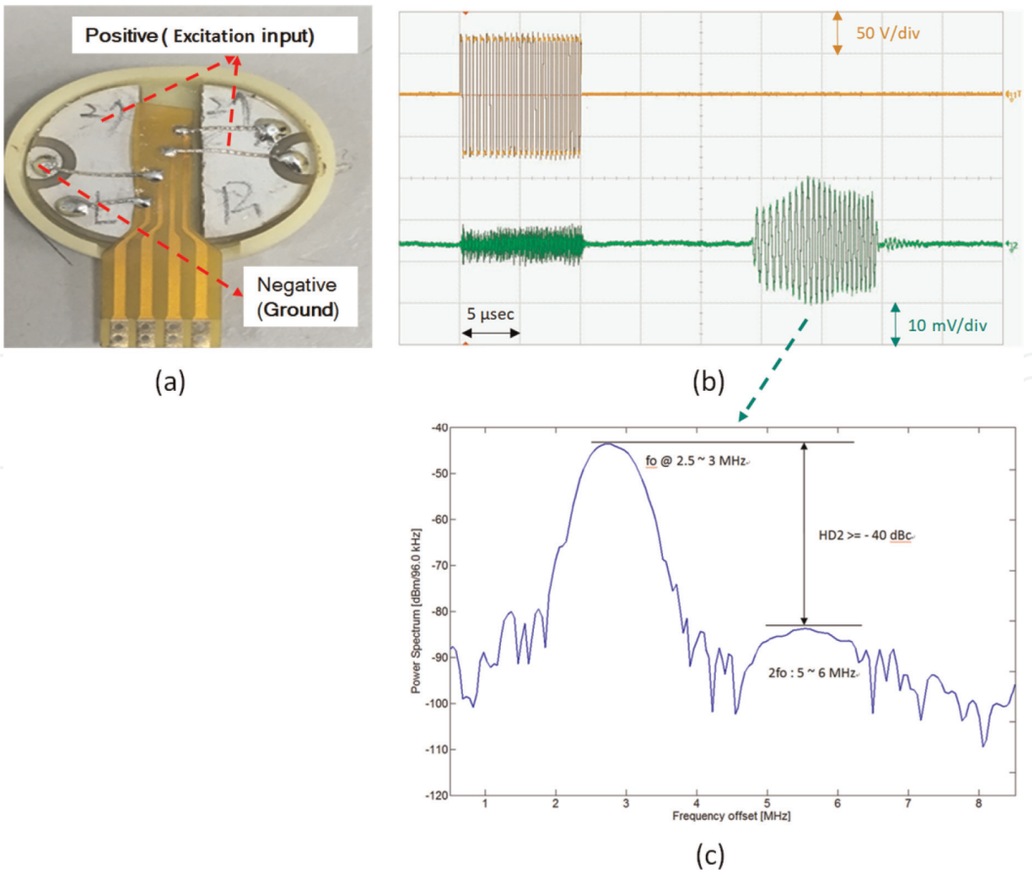


**Figure 22.**
*The pulse-echo second harmonic leakage verification measurement setup with a patch transducer as the load of the pulse generator (a), high-voltage bipolar pulses as transmitting signals (orange) and the receiving signals (green) (b), and the spectrum analysis of the echo signals (c).*

plane after beamforming. At a focal plane 3.5–4.0 cm away from the probe, the beam intensity is about 180 μJ/cm$^2$.

In order to verify the harmonic contents of the echo signal, another measurement setup was carried out using a single-channel patch transducer with the designed pulse generator. **Figure 22** shows the measured echo signals after exciting the patch transducer with the designed pulse generator. The existence of the received green signal under the high-voltage transmitted pulses is due to the leakage of the T/R switch. The second harmonic leakage at the receiver compared to the fundamental signal is <40 dB, making the pulse generator suitable for harmonic imaging applications.

## 5. Conclusions

Design and implementation of an integrated multiple channel high-voltage bipolar pulse generator for medical ultrasound transmitter applications were well addressed in this chapter. The proposed pulse generator can, assuming a capacitive ultrasound probe, generate output pulses >140 Vpp with rise and fall times of 18.6 and 18.5 ns, respectively. The resulting second harmonic distortion of the high-voltage pulse exceeds −40 dBc, meeting the requirements of ultrasonic transmitters in harmonic imaging applications. The performance of the integrated 8-channel ultrasonic pulses using the designed pulse generator was verified using the ONDA sound field calibration system. Experimental results show that the architecture can be used for advanced harmonic imaging ultrasound systems.

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