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Chapter

# Combined Crosstalk Avoidance Code with Error Control Code for Detection and Correction of Random and Burst Errors

*Ashok Kumar Kummary, Perumal Dananjayan, Kalannagari Viswanath and Vanga Karunakar Reddy*

## Abstract

Error correction codes are majorly important to detect and correct occurred errors because of various noise sources. When the technology is scaling down, the effect of noise sources is high. The coupling capacitance is one of the main constraints to affect the performance of on-chip interconnects. Because of coupling capacitance, the crosstalk is introduced at on-chip interconnecting wires. To control the single or multiple errors, an efficient error correction code is required. By combining crosstalk avoidance with error control code, the reliable intercommunication is obtained in network-on-chip (NoC)-based system on chip (SoC). To reduce the power consumption of error control codes, the bus invert-based low-power code is integrated to network interface of NoC. The advanced work is designed and implemented with Xilinx 14.7; thereby the performance of improved NoC is evaluated and compared with existing work. The 8×8 mesh-based NoC is simulated at various traffic patterns to analyze the energy dissipation and average data packet latency.

**Keywords:** NoC, CAC, ECC LPC, SoC, FPGA

## 1. Introduction

As technology is scaling up, a number of circuits are integrated in on-chip. The intercommunication among the on-chip devices is majorly important because of millions of integrated devices in the system on chip (SoC). The communication architectures of SoC are not efficient to provide high performance; thereby network-on-chip (NoC) is the new paradigm introduced [1]. Because of parallelism, the NoC is providing high performance in terms of scalability and flexibility even in the case of millions of on-chip devices. Still, NoC suffers with design parameters that affect the performance of NoC. As technology is scaling up, the performance of NoC is mainly affected with coupling capacitance. The effect of crosstalk capacitance is more in horizontal than in vertical; thereby the crosstalk errors frequently occur in on-chip interconnecting wires [2]. An efficient error correction code is required to control the crosstalk error that may occur once or multiple times. The crosstalk avoidance codes (CAC) are popularized to control the error in on-chip interconnects; thereby a reliable communication is obtained.

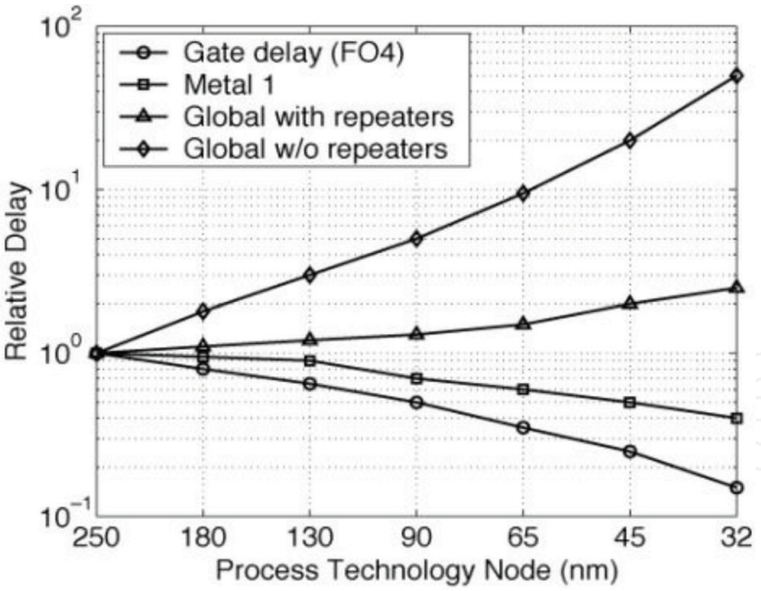



**Figure 1.**
*Trend of relative delay with scaling of technology [3].*

The CAC reduced the worst-case switching capacitance in on-chip interconnects by avoiding the switching transitions of data that is 010-101. This condition reduced the worst-case capacitance from $(1 + 4\lambda)\, C_L$ to $(1 + 2\lambda)\, C_L$; hence, the energy dissipation is reduced from $(1 + 4\lambda)\, C_L \alpha V_{dd}^2$ to $(1 + 2\lambda)\, C_L \alpha V_{dd}^2$ where λ is the ratio of coupling capacitance to total capacitance, $C_L$ is the self-capacitance of interconnection wire, α is the transition factor, and $V_{dd}$ is the supply voltage for the system. The energy dissipation is reduced by reducing the transition activity of interconnection wires for the data packet. The behavior of relative delay with scaling of technology is shown in **Figure 1**.

International Technology Roadmap for Semiconductor (ITRS-2011) predicted that when the delay from the gates is reduced, the delay from wires is increased with scaling of technology because the interconnecting wires are affected more when scaling of technology is less than 45 nm [3]. Hence, the interconnecting wires affected the performance of NoC-based SoC in terms of delay as well as energy consumption, and it is huge in case of the errors.

The errors mainly occur in interconnecting wires because of coupling capacitance; thereby strong error correction code (ECC) is required to detect and correct errors [4]. The error may occur once or multiple times, and also multiple errors occurred in interconnection wires; hence, the ECCs are not enough to detect and correct errors. In literature, different techniques are proposed for detection and correction of multiple errors. The parity check, dual rail (DR), modified dual rail (MDR), boundary shift code (BSC), and CAC are popularized among various techniques for control of multiple errors in interconnection wires.

The remaining chapter is as follows: Section 2 includes the related work of error control methods and also discussed the merits and demerits. Section 3 presented the proposed encoder and decoder of combined CAC-ECC method. Section 4 gives the advanced encoding and decoding of NoC router with combined LPC-CAC-ECC scheme. Section 5 discussed the implementation of proposed work in NoC architecture, and finally, Section 6 concludes the chapter.

## 2. Related work

The detection and correction of errors present in the on-chip interconnects are majorly important because it leads to drop or block data packet; hence the performance

of NoC architecture is reduced. Huge research is going on for the error detection and correction of on-chip interconnects. Parity code is used to detect 1-bit error in data packet. It is simple but errors are not corrected. Hamming code is proposed for detection of 2-bit errors and also correction of 1-bit error [5]. Various error control codes are introduced with the help of hamming code because it is easy to implement.

To reduce delay in on-chip interconnects, forbidden overlap condition (FOC), forbidden transition condition (FTC), and forbidden pattern condition (FPC) of crosstalk avoidance code are used [6]. The crosstalk avoidance codes are reduced delay from $(1 + 4\lambda) C_L$ to $(1 + 2\lambda) C_L$ and also energy dissipation. Still, the area utilization has increased because the extra bits are added to the original data packet. To control multiple errors, duplicate parity (DAP) is proposed by duplicating data packets, and then hamming code is used for transmission of duplicated data [7]. The average data packet latency is reduced by DAP-based method, although the power consumption has increased because the number of interconnecting wires is increased. To reduce the power consumption in the case of crosstalk avoidance codes, Sridhara and Shanbhag [8] proposed and combined a low-power code (LPC) with crosstalk avoidance codes.

The FOC, FTC, and FPC are used for detection and correction of errors due to crosstalk; thereby the data packet latency is reduced. To reduce power consumption, bus invert-based technique is used and combined with error control codes. The joint LPC-CAC code improved the performance of NoC, but still, area utilization has increased. To obtain reliable on-chip communication, Single Error Correcting-Burst Error Detecting (SEC-BED) with Hybrid Automatic Repeat reQuest (HARQ) is proposed. The single random error is detected and corrected, whereas the retransmission is requested when double random and burst errors are detected. The SEC-BED scheme detected errors efficiently, although the delay, area, and power consumption have increased because of Ex-Or-based tree structure used in calculating parity check bits and go-back-N-based retransmission used in HARQ.

To reduce worst-case bus delay, joint crosstalk avoidance with triple error correction (JTEC) code is proposed. In encoding operation, the code word is used with hamming code and then duplicated. Because hamming code is duplicated, the decoder detected 4-bit errors and corrected 3-bit errors. Because JTEC required large area, JTEC is advanced as JTEC-simultaneous quadruple error detection (JTEC-SQED). The JTEC-SQED replaced hamming codes into Hsiao codes; thereby the performance is improved when compared with JTEC. To increase error control capability, triplicate add parity (TAP) is used for encoding data and compared with sent parity bit in decoder to detect and correct the errors in interconnecting wires [9]. The TAP-based error control scheme efficiently detected and corrected 1-bit, 2-bit, and some 3-bit errors. Still, the power consumption has increased because the required number of interconnecting wires increases.

To reduce the power consumption with TAP-based scheme, this chapter proposes joint LPC-CAC-ECC scheme to detect and correct 1-bit, 2-bit, and some 3-bit burst errors efficiently, and also the power consumption of codec module is reduced with the help of BI technique. The proposed work is mainly concentrated on controlling of multiple errors and also improving of NoC communication architecture.

## 3. Joint CAC-ECC

The ability of error control method is determined by the reliable communication which is provided in the presence of errors. By embedding the error control schemes, the performance of the system is reduced when compared with error control scheme-less system. The data packet latency and power consumption

affect more in the presence of error control schemes. To detect and correct multiple errors efficiently, the CAC-ECC methods are combined. In this chapter, the 1-bit and 2-bit errors due to crosstalk are detected and corrected and also some of the 3-bit errors.

Triplicate add parity (TAP)-based encoder is used to transfer the data from source to destination through the interconnection wires. **Figure 2** depicts TAP-based encoder of joint CAC-ECC scheme. The 32-bit data triplicates to encode to the destination through interconnection wires. In the advanced encoder, each data bit triplicates and also calculates overall parity of 32-bit data; hence, a total of 97-bits of data are encoded to the decoder section. By triplication, the errors are efficiently controlled in the interconnecting wires.

The parity bit is also measured with Ex-Or operation and encoded to the decoder section to check the parity of received data. By the comparison of parity, the errors are detected and corrected efficiently. The decoder structure of joint CAC-ECC scheme is shown in **Figure 3**.

The decoder divides encoded data into three groups, and parity of each group is calculated and compared with sent parity bit. The encoded data are divided into three groups of 32-bit data with the help of group separator, and sent parity bit (p0) is used to compare with the parity of each group (p1, p2, p3). The 1-bit and 2-bit errors are detected when parity of group changed from sent parity. **Table 1** depicts the different possibilities of errors at data bits in interconnection wires. The 1-bit errors are detected with its parity. The 2- and 3-bit errors are identified by considering the following instances:

Instance I: p1 = p2 and p2 ≠ p3.

To find out error-less group, the parity of group 1 is compared with sent parity (p0). If p0 is equal to p1, then group 1 is considered as error-less, otherwise group 3 is considered as error-less.

Instance II: p1 ≠ p2 and p2 = p3.

To find out error-less group, the parity of group 1 is compared with sent parity. If p0 is equal to p1, then group 1 is considered as error-free, otherwise group 2 is error-free.

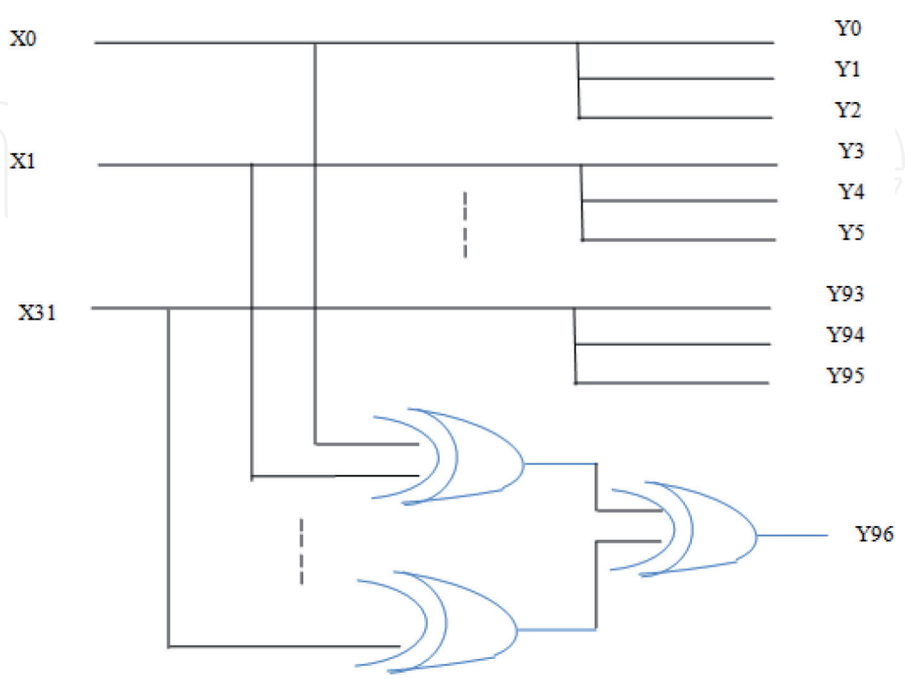



**Figure 2.**
*TAP-based encoder of proposed scheme.*

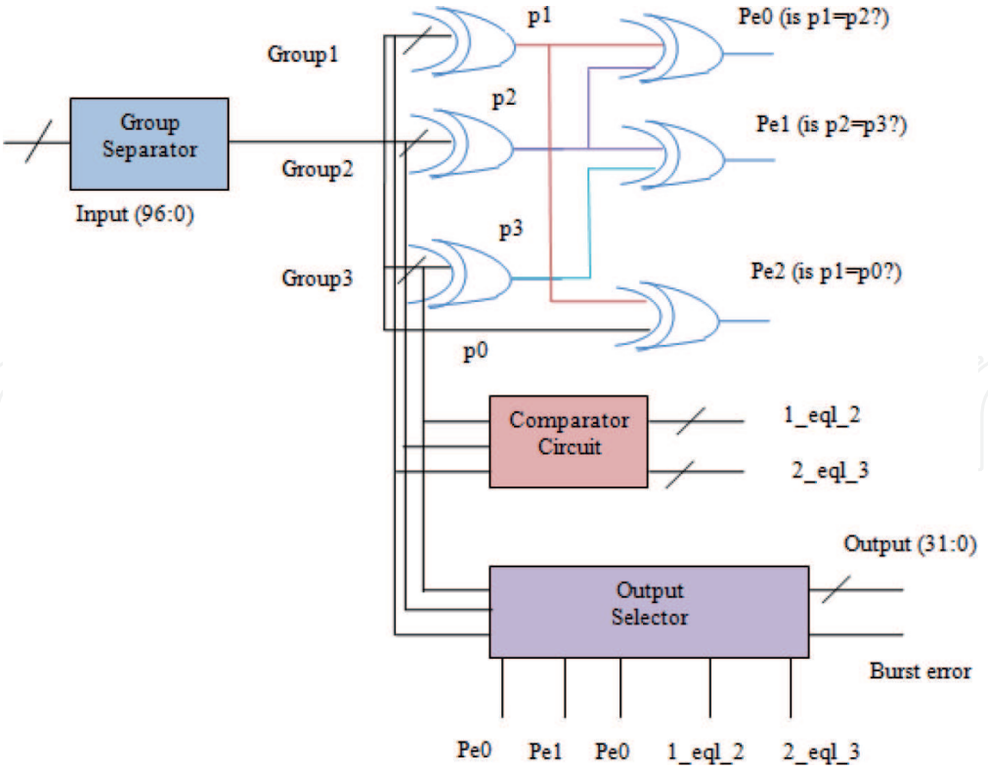



**Figure 3.**
*Decoder structure of joint CAC-ECC scheme.*

Instance III: p1 ≠ p2 and p2 ≠ p3.

To find out error-less group, the parity of group 1 is compared with sent parity. If p0 = p1, then the group is considered as error-free, otherwise group 2 is error-free.

Instance IV: p1 = p2 and p2 = p3.

The error bits highlighted in **Table 1** are considered for this instance. Because of not detecting the even parities, the error bits having even parities are divided into two categories. (i) 1-bit error in three groups is called burst error. When p0 = p1 and p1 = p2, then burst error is detectable or else consider another category.
(ii) The original data of group 1, group 2, and group 3 are compared to select error-free group. When group 1 is equal to group 2, then group 2 is selected as error-free or else group 2 and group 3 are compared again. When group 2 is equal to group 3, then group is considered as error-free or else group-1 is considered as error-free.

The number of detection and correction bits of ECC depended on the hamming distance of technique. The hamming distance of TAP-based scheme is four; that is, the triplication of data is presented, the hamming distance is three, and also one is from added parity bit. If the hamming distance of original data packets is k, then

| | **1-bit error** | | | | **2-bit errors** | | | | | | | | **3-bit errors** | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Group 1 (p1) | 1 | 0 | 0 | 1 | 0 | 1 | **2** | **0** | **0** | **1** | 0 | 1 | 0 | 3 | 0 | 0 | 1 | 2 | 2 |
| Group 2 (p2) | 0 | 1 | 0 | 1 | 1 | 0 | **0** | **2** | **0** | **1** | 1 | 0 | 2 | 0 | 3 | 0 | 2 | 1 | 0 |
| Group 3 (p3) | 0 | 0 | 1 | 0 | 1 | 1 | **0** | **0** | **2** | **1** | 2 | 2 | 1 | 0 | 0 | 3 | 0 | 0 | 1 |
| | Correct | | | | Correct | | | | | | | | Correct | | | | | Incorrect | |

**Table 1.**
*Different possible error bits in interconnecting wires.*

the number of detection error bits is k – 1 and the number of correction bits is $\frac{k-1}{2}$; hence, CAC-ECC scheme detected three error bits and corrected two error bits.

Though the CAC-ECC scheme has detected and corrected crosstalk errors efficiently, the power consumption and data packet latency have huge increase because more number of interconnecting wires are used in the advanced error control scheme. Because of triplication of original data, the combined CAC-ECC scheme used more number of wires; thereby the power consumption of advanced method has increased.

## 4. Advanced NoC router

The errors affect more on the performance of NoC-based SoC because of more number of interconnection links involved for parallel processing. The combined CAC-ECC scheme is embedded in the network interface (NI) of router; thereby the errors are controlled and also avoided to propagate to remaining network. The encoder of error control scheme is embedded to transmit NI (TX-NI), and decoder of error control scheme is added to the receive NI (RX-NI); thereby the original data are transferred efficiently. Because of embedded combined CAC-ECC in the NI, the router of NoC presented huge power consumption; hence, there is a need of reducing the power consumption in NoC. By analyzing various error control schemes in NI, flexible unequal error control (FUEC) methodology is introduced and generalized to any kind of error control codes [10].

### 4.1 Combined LPC-CA-ECC scheme

To reduce power consumption in NoC architecture in the case of error control schemes, the low-power code is added to the error control codes; thereby the power consumption is reduced and also errors are corrected efficiently. Bus invert (BI) method is used to reduce the transition activity of interconnecting wires; thereby the power consumption is reduced. The power consumption is given in eq. (1).

$$P_d = \alpha C_L f_c V_{dd}^2 \tag{1}$$

where α is the transition activity, $C_L$ is the load capacitance, $f_c$ is the maximum clock frequency, and $V_{dd}$ is the supply voltage. From Eq. (1), it is known that the dynamic power consumption is directly proportional to the transition activity.

The bus invert-based low-power code (LPC) is shown in **Figure 4**. The BI technique reduced the number of transitions by using the hamming distance of original data packet; thereby the original data are inverted before encoding. The original data are inverted when the hamming distance is more than half, otherwise it is sent to encoder without inverting. The majority of voter circuit with combination of Ex-Or gates inverted the data when it is required. The majority of voter circuit is composed of a number of full-adders, which increases the size of circuit.

### 4.2 HARQ

The combined LPC-CAC-ECC scheme detected and corrected multiple crosstalk errors and also reduced the power consumption of on-chip interconnects. The error control scheme does not correct some of the 3-bit errors; hence, the hybrid automatic retransmission request (HARQ) is enabled to retransfer the data from source to destination. The HARQ resend the data packets when the receiver asserted continuous three negative acknowledgments (NACK).

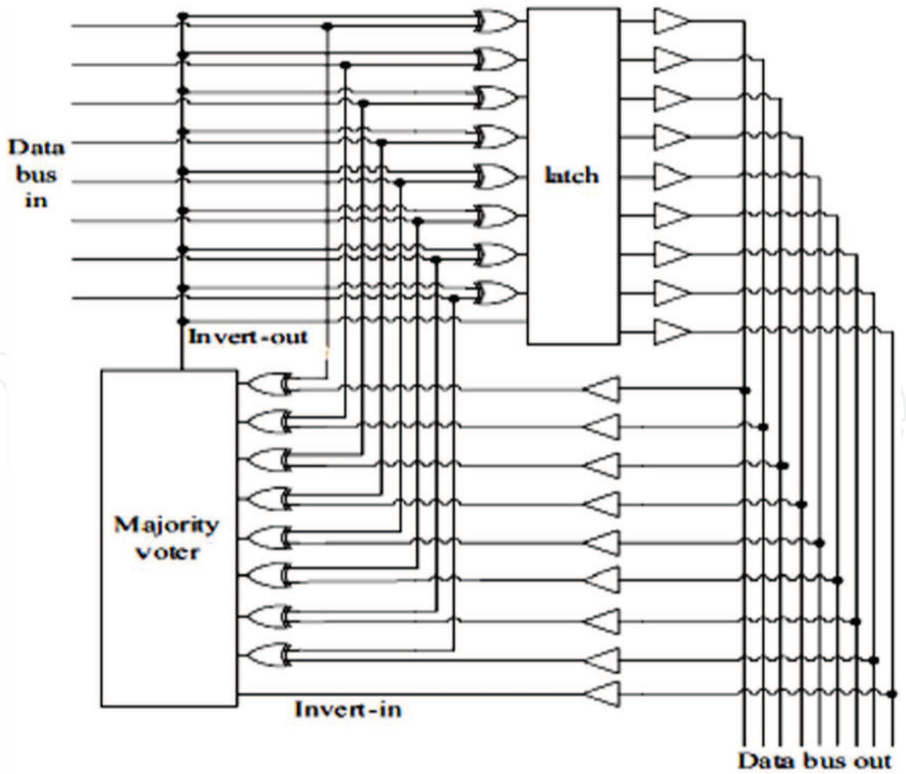



**Figure 4.**
*Bus invert method of low-power code.*

The advanced work of error control scheme is embedded in the NI of the NoC, and also codec module is responsible for encoding and decoding of the data without errors. To improve the data transfer speed of NoC, each router is added with an extra PE; thereby the number of router required to complete data transfer is reduced. To control arbitration among ports of router, the advanced scheduling algorithms are used in arbiter. The selected port transferred the data to the output through crossbar switch. To avoid deadlock error, each port of router is composed of buffer memory and its controller. A store and forward packet switching (SF) and minimal routing algorithm are used to improve the performance of mesh-based NoC architecture [11].

## 5. Implementation

The advanced error control scheme is designed in Xilinx 14.7 and implemented on Virtex-6 Field Programmable Gate Array (FPGA) target device. The simulation and synthesis are demonstrated for each module of NoC. The performance of NoC is evaluated in terms of area utilization (occupied slices, LUT-FF pairs, and bonded IOBs), latency (delay), and power consumption. **Table 2** shows the performance of encoder and decoder of joint CAC-ECC scheme. The area utilization and delay of codec module are increased linearly with the increase of data width because of the number of interconnection wires in encoder and also the number of cycles required to detect and correct error in decoder.

The data transfer of the encoder is more than the decoder because of the number of rounds required to detect and correct. The required cycles increase more in the case of more number of error bits and also higher data width. **Tables 3** and **4** show the performance of NoC router with CAC-ECC scheme and joint CAC-ECC-LPC scheme. From **Table 3**, it is inferred that the data transfer speed of NoC in the presence of soft errors decreased with the increase of data width because more number of interconnecting

| Family | Number of occupied slices | | Number of slice LUTs | | Number of bonded IOBs | | Delay (ns) | |
|---|---|---|---|---|---|---|---|---|
| | Encoder | Decoder | Encoder | Decoder | Encoder | Decoder | Encoder | Decoder |
| 8-bit | 1 | 15 | 2 | 39 | 35 | 36 | 1.01 | 2.82 |
| 16-bit | 3 | 24 | 2 | 42 | 67 | 68 | 1.37 | 3.15 |
| 32-bit | 7 | 49 | 7 | 79 | 131 | 132 | 1.53 | 3.20 |

**Table 2.**
*Area utilization and delay of codec module of CAC-ECC scheme.*

| Family | Number of slice registers | Number of slice LUTs | Number of fully used LUT-FF pairs | Latency (ns) | Power consumption (mW) |
|---|---|---|---|---|---|
| 8-bit | 814 | 566 | 375 | 3.70 | 9.56 |
| 16-bit | 952 | 636 | 453 | 5.52 | 47.42 |
| 32-bit | 1858 | 1485 | 676 | 6.06 | 89.55 |

**Table 3.**
*Performance of NoC router with CAC-ECC scheme.*

wires are required for encoder of CAC-ECC scheme and also more number of cycles are required in decoder to detect and correct the soft errors in on-chip interconnecting wires. Hence, the power consumption is huge when data width is large.

From **Table 4**, it is clear that the low-power code is reducing the total power consumption even in the case of error control schemes. It is observed that the data transfer speed of NoC maintained the same and the power consumption is reduced from little to huge when data width is increased. Still, the area utilization is increased in joint LPC-CAC-ECC scheme because of a number of combinational circuits required in BI method to reduce the power consumption.

As BI code worked based on hamming distance of original data, the area utilization is increased. Still, it is reduced when hamming distance of original data is less than half; hence, the performance of NoC is improved.

**Table 5** shows the comparison of proposed error control scheme with recent schemes for 32-bit of data width. From **Table 5**, it is observed that the proposed method shows better results than the existing error control methods. The comparison is shown with various parameters such as number of wires used, number of error detection and correction, swing voltage of interconnect, delay for detection and correction, and also power consumption. Among all methods, CADEC provided better results than the proposed work. Still, detection and correction of CADEC are limited to 2-bit errors. The power consumption of proposed work has improved to 11% than JTEC.

| Family | Number of slice registers | Number of slice LUTs | Number of fully used LUT-FF pairs | Latency (ns) | Power consumption (mW) |
|---|---|---|---|---|---|
| 8-bit | 823 | 635 | 440 | 3.70 | 9.40 |
| 16-bit | 996 | 764 | 518 | 5.52 | 46.90 |
| 32-bit | 1926 | 1599 | 1014 | 6.06 | 81.64 |

**Table 4.**
*Performance of NoC router with joint LPC-CAC-ECC method.*

| S. no. | Coding scheme | Data width | Number of wires used | Error detection | Error correction | Link swing voltage (V) | Delay | Power consumption (μW) |
|---|---|---|---|---|---|---|---|---|
| 1 | Hamming | 32 | 38 | Double | Single | 1.02 | 1 + 4λ | 49.30 |
| 2 | Hsiao SEC-DED [12] | 32 | 39 | Double | Single | 1.02 | 1 + 4λ | 51.60 |
| 3 | DAP [13] | 32 | 65 | Double | Single | 1.02 | 1 + 2λ | 16.22 |
| 4 | CADEC [7] | 32 | 77 | Random and burst error of two | 1-bit and 2-bit errors | 0.89 | 1 + 2λ | 26.77 |
| 5 | JTEC [14] | 32 | 77 | Random and burst error of three | 1-bit and 2-bit errors | 0.81 | 1 + 2λ | 39.49 |
| 6 | Joint LPC-CAC-ECC | 32 | 97 | Random and burst error of three | 1-bit, 2-bit errors, and some of 3 | 0.61 | 1 + 2λ | 34.86 |

**Table 5.**
*Comparison of advanced error control scheme with recent work.*

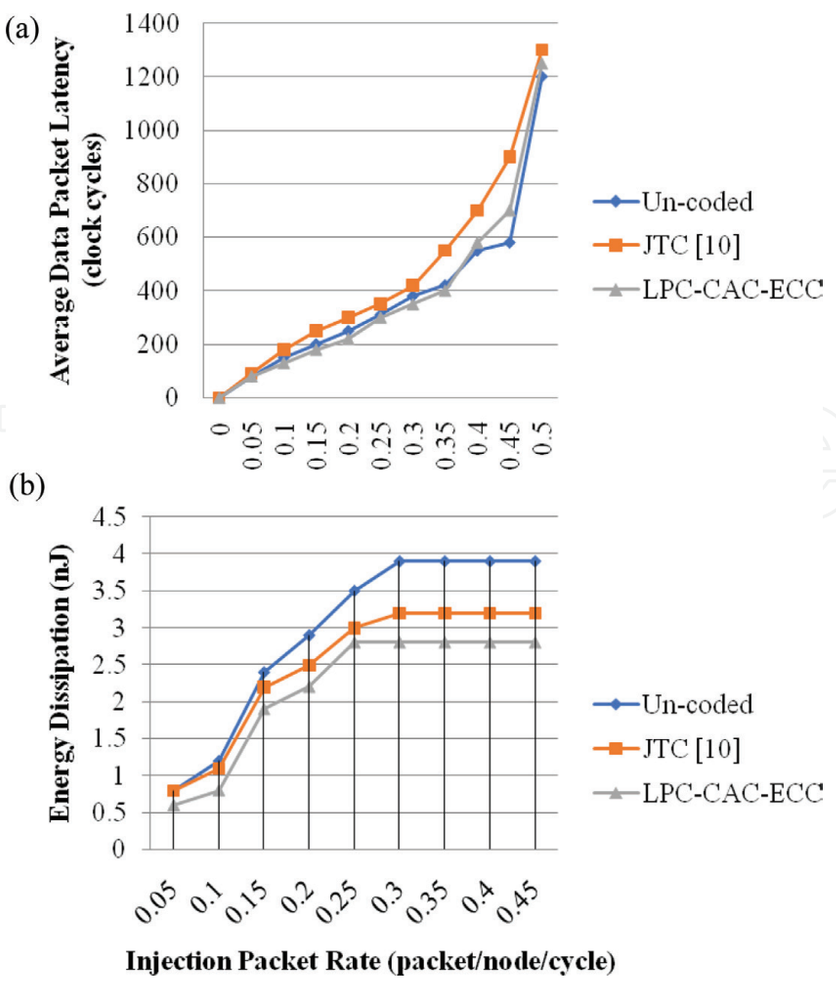



**Figure 5.**
*Simulation results of data packet latency (a) and energy dissipation (b) of advanced NoC with others.*

To analyze the data packet latency and energy dissipation, the advanced NoC architecture is simulated 32 times at uniform-random traffic in Riviera-pro windows version. Each experiment of simulation showed less latency and less energy dissipation. The 8×8 mesh-based NoC is simulated and compared with recent NoC, that is, JTC [14], and also uncoded NoC. From **Figure 5**, it is clear that the advanced NoC has lesser data packet latency and has greater than uncoded because the advanced router transfers the data with joint CAC-ECC scheme in case of occurred errors; otherwise it transfers without error control scheme. The energy dissipation of advanced NoC is lesser than both existing works because the BI-based LPC is utilized in router in case of error control code being embedded in the NI.

## 6. Conclusion

The scaling of technology introduces number of errors in on-chip interconnects. The crosstalk errors majorly affected the performance of NoC communication architecture due to the coupling capacitance between the interconnecting wires. This chapter discussed number of errors and their control schemes. To control multiple errors, joint CAC-ECC scheme is embedded in NI; hence the errors are controlled and avoided to propagate remaining network. As error control scheme presented more power consumption, the BI-based method of low-power code used to reduce the case of error control scheme is used. The performance of advanced NoC is simulated and compared with recent work; thereby 11% improvement is shown when compared with JTC. To analyze the data packet latency and energy dissipation, the 8×8 mesh-based NoC architecture is simulated and compared with recent work; thereby the advanced NoC architecture shows better results than the recent NoC.

## Conflict of interest

It is declared that this article has no "conflict of interest."

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