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ANN Application to Modelling of the D/A and A/D Interface for Mixed-mode Behavioural Simulation

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1. Introduction

The design of electronic and telecommunication integrated circuits is unavoidably faced with the simulation of analog subsystems of ever rising complexity as a result of building more and more complex mixed-signal systems containing both analog and digital parts. The design of such systems requires simulation tools that are both fast and accurate at the same time.

The main obstacle to this requirement is related to the difficulties in high-level modelling of the analog part, and sufficiently accurate modelling of the digital-analog (D/A) and analog-digital (A/D) interfaces which are frequently encountered in such systems (Trihy & Kundert, 1995; Kundert, 1999). We will consider here analog mixed-level behavioural modelling as a special case of the behavioural modelling of mixed-signal systems.

According to McAndrew: "It is difficult to develop complete, accurate, numerically robust models that work properly with numerical algorithms in simulators and with the CAD tools in an IC design system" (McAndrew et al., 1998). Modelling dynamic non-linear networks is practically the most difficult. One needs to solve not only the problem of the approximations to be used (modelling) and the method of evaluation of the coefficients within them (characterisation) but also to determine appropriate test signals able to activate the complete non-linear and dynamic properties of the circuit to be modelled.

Considering Fig. 1., we may have two distinct situations. First, for the A/D interface, we need the voltage and the current at the interface so that the input impedance of the digital part can be modelled. Modelling of the input impedance of a CMOS circuit is, to our knowledge, usually considered simple: a capacitor is used as a model. However, this capacitance is highly non-linear so that there is need for more realistic modelling as we propose in the next. Second, at the D/A interface, we need an electrical circuit to model the digital output driving the analog load. That model should perform D/A signal conversion and maintain electrical compatibility. Among the solutions available in the literature are an approach where time-varying resistors have been used (Petković & Litovski, 1989; Petković & Litovski, 1991), and a macromodelling procedure which has difficulties in characterising the reactive part of the non-linear output impedance of the model (Nichols et al., 1992; Brown et al., 1994). Recently, while attempting to enable high-level behavioural simulation of complex combinational CMOS circuits, successful techniques have been developed for

equivalent inverter or equivalent transistor synthesis represented as a non-linear voltage controlled current source (Chatzigeorgiou et al., 1999). Here an alternative, algorithmically simpler procedure, but robust and with broader scope of application, is proposed based on use of artificial neural networks (ANNs).

After the first application of ANNs for modelling electronic components, it became clear that this concept could be successfully used for modelling dynamics too (Litovski et al., 1992). The dynamics in a micro-electro-magneto-mechanical actuator were modelled first, taking advantage of the fact that the dynamic and the resistive properties may be expressed separately (Litovski et al., 1997a).
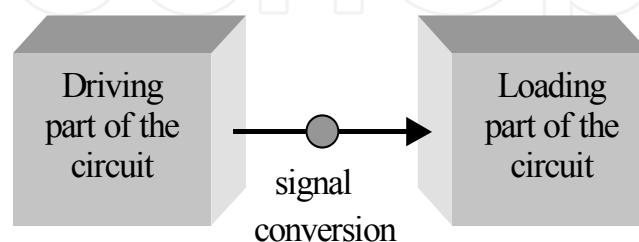

Fig. 1. Schematic depiction of the interface to be modelled between analog and digital parts of the circuit.

Full non-linear dynamic modelling using ANNs was described later – the approximation being performed in the frequency domain using direct and inverse Fourier transforms repeatedly (Citterio et al., 1999). Here we propose, for the first time, ANNs to be used for be-havioural modelling of the digital output with modelling performed in the time domain.

The proceedings in the next will go in two directions. First we will describe the solution to the problem of A/D interface modelling. Since we assume that the digital (loading) part of the interface has no own feedback to its input, we will use its input impedance as the load to the analog part. In that way the problem of modelling of the A/D interface will be reduced to the problem of modelling the input impedance of the digital part. Second, the solution to the problem of the D/A interface will be proposed. In this case a complete new analog circuit will be proposed that will model the output behaviour of the digital driver at the interface. It will be shown by inspection that despite the fact that the model was developed for unloaded digital part, it behaves perfectly for every load used as a control.

2. Modelling the A/D interface

The simplest circuit representing input impedance of a MOS logic circuit is shown in Fig. 2. Here and on, for simplicity, the very conversion (analog to digital value) of the signal is not shown. The circuit is linear, with constant element values, what is not good enough approximation of the real MOS input impedance.

Input resistance and capacitance of bipolar circuits is nonlinear, so the simplest input TTL circuit is diode. Fig. 3. shows one solution with diodes (Corman & Wimborow, 1988).

The problem of an analog circuit output can be generally solved by connecting nonlinear resistance and nonlinear capacitance in parallel controlled by the voltage of the analog part of A/D interface, Fig. 4., (Petković & Stojanović, 1992). A special procedure is proposed in order to get the characteristics of the nonlinear elements depicted.
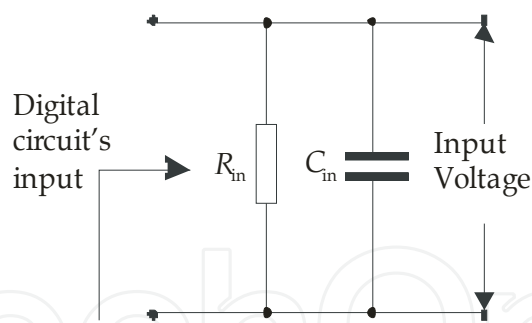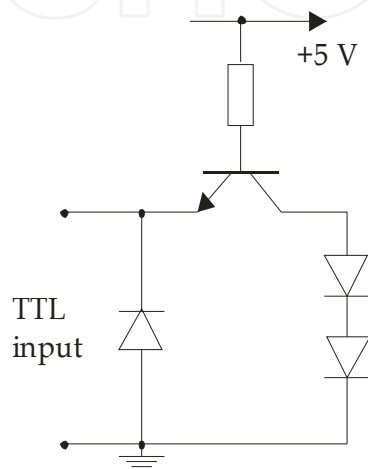
Fig. 2. RC input circuit
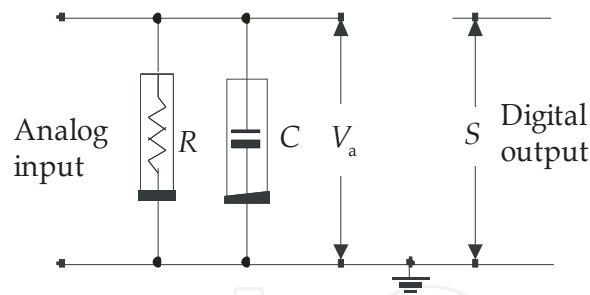
Fig. 3. Input circuit-one possible solution

Fig. 4. A/D interface model

In the following (Litovski & Andrejević, 2002) we will show that MOS circuit input impedance is highly nonlinear, so more precise method of modelling is required. In order to get more information concerning our problem, as an example of two-terminal non-linear dynamic circuit, the input of an inverter is considered, as shown in Fig. 5. It is capacitive but highly non-linear, the non-linearity coming mostly from the Miller effect. As shown in Fig. 6., the inverter's gain is strongly non-linear, so that the Miller capacitances have to be too.

Inverter has only one input, so we are modelling only one input impedance. When there are more inputs, we have to model as many impedances as there are circuit inputs.

We attacked the problem of implementation of ANNs to analog modelling by first solving the simulation of an electro-magneto-mechanical actuator, as mentioned above. Thereafter, the problem of modelling linear dynamic networks was solved (Ilić et al., 2000). Two main ideas were implemented. First, to enable application of ANNs for implementation of the

model the so-called recurrent time-delay structure was used. It is already proven (Chow & Li, 2000) "that any finite time trajectory of a given *n*-dimensional dynamical continuous system with input can be approximated by the internal state of the output units of a continuous time recurrent neural network".
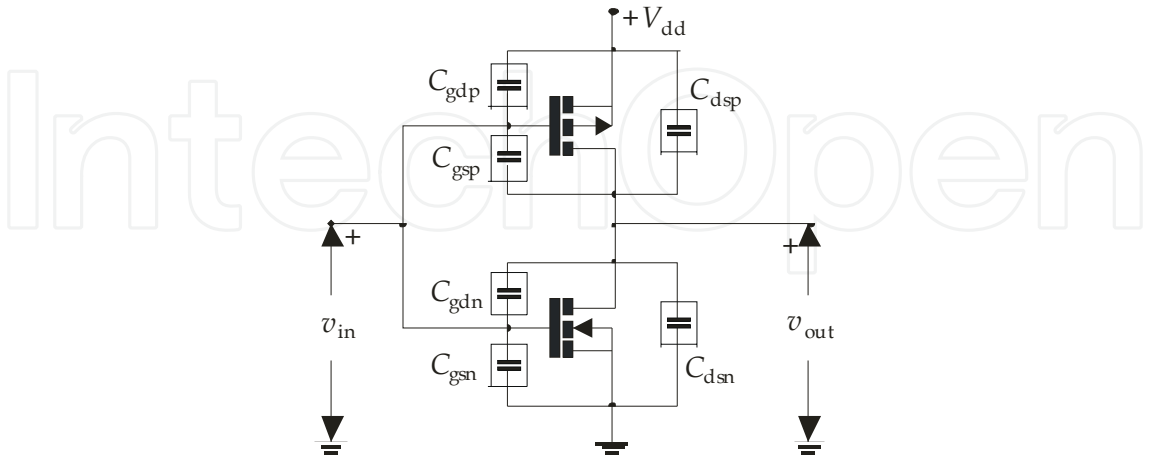

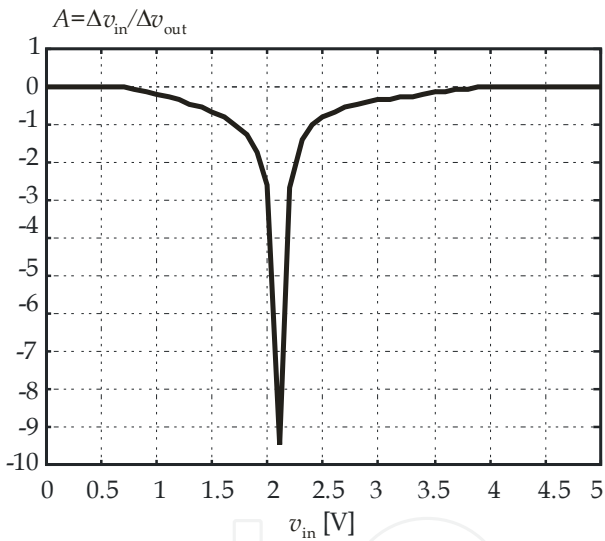Fig. 5. CMOS inverter with non-linear capacitances.

Fig. 6. The dependence of the inverter's gain on the input signal.

The structure of such a network is depicted in Fig. 7. The need for both time-delay and recurrence comes from the theory of dynamic system modelling (Bernieri et al., 1994). In our experience, however, time delay of the input signal facilitates modelling of the nonlinear properties while recurrence better accounts for the memory property of the system to be modelled. The core of the structure is a feed-forward ANN that, apart of the input layer, has one hidden layer having neurons with sigmoidal activation function, and output layer with a single linear output neuron. In the special case of modelling a two-terminal device, x in Fig. 7. stands for the exciting current while y denotes the response (voltage). The discretization time step is Δt.

Second, to capture the dynamic behaviour of the circuit to be modelled, a chirp signal (i.e., a frequency-modulated sinusoidal signal) was used as excitation. It has evenly-distributed spectral components across the "passband" of the circuit. If the change in frequency is

sufficiently slow, one gets the proper time-domain response of the dynamic system that is being modelled. This response is then used for training the ANN described above. The generalisation property of the ANN was verified by testing the models obtained as above with new signals, such as square pulses (Ilić et al., 2000). In order to model non-linear circuits with the concept described above, one needs amplitude large enough of the chirp signal to encompass all non-linearities encountered during excitation.
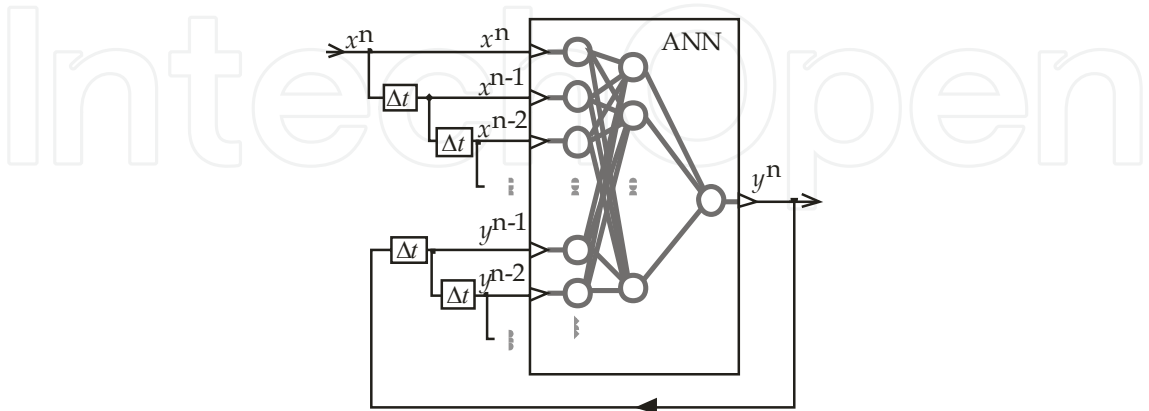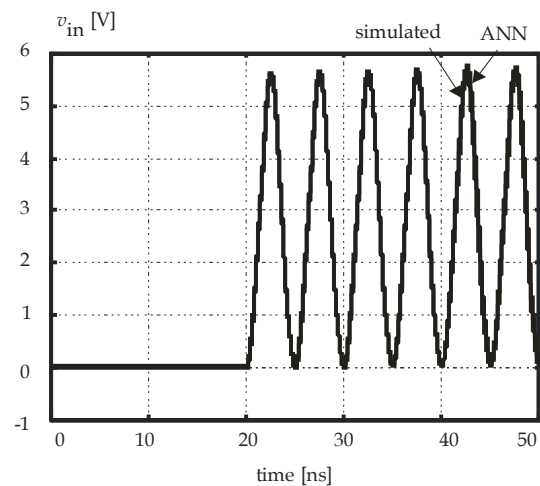

Fig. 7. The topology of the proposed ANN.

Fig. 8. Response (voltage) at the inverter's input obtained for sinusoidal excitation. Here "simulated" denotes the circuit simulation of the inverter of Fig. 5., while "ANN" stands for the response of the model.

The response observed was the input voltage of the inverter. The modelling results are shown in Fig. 8. where the difference between the simulated circuit and the model response is difficult to discern.

For the example used here, five inputs (three direct input connections and two feed-backs from the output as shown in Fig. 7.), four hidden units, and one output neuron are incorporated in the ANN. Note that the input units are simply distributing signals to the hidden layer. The hidden units have sigmoidal activation functions, while the output neuron is linear. Table 1. shows the weights and the thresholds of the neurons. A modified steepest-descent learning algorithm was used to train the ANN (Zografski, 1991). Other details of the training procedure are practically the same as described elsewhere (Bernieri et al., 1994).

No.	Hidden-layer neurons (First figure stands for the input neuron)	Output neuron (First figure stands for the hidden neuron)
1	$w^1(1,1) = -1.15618$ $w^1(2,1) = 0.303841$ $w^1(3,1) = 0.801999$ $w^1(4,1) = -0.655468$ $w^1(5,1) = -0.112933$ $\theta_1^1 = 1.69522$	$w^2(1,1) = -1.24339$ $w^2(2,1) = 1.41557$ $w^2(3,1) = -1.98177$ $w^2(4,1) = -2.18655$ $\theta_1^2 = 2.91066$
2	$w^1(1,2) = 0.138613$ $w^1(2,2) = -1.16098$ $w^1(3,2) = 1.01521$ $w^1(4,2) = -0.128065$ $w^1(5,2) = 0.915597$ $\theta_2^1 = -0.890606$	
3	$w^1(1,3) = -0.537022$ $w^1(2,3) = 1.64986$ $w^1(3,3) = -1.1164$ $w^1(4,3) = -2.64625$ $w^1(5,3) = 1.49825$ $\theta_3^1 = -1.15733$	
4	$w^1(1,4) = -1.13048$ $w^1(2,4) = 1.87005$ $w^1(3,4) = -0.716303$ $w^1(4,4) = -3.13684$ $w^1(5,4) = 2.4126$ $\theta_4^1 = 1.53233$	

Table 1. Weights and thresholds of ANN used to model the inverter in Fig. 5.

3. Generalisation capabilities

To show the quality of the approximation procedure and the generalisation capabilities of the ANN, a new example circuit is now considered. It consists of two inverters. The first (the driver) is considered to be analog as in Fig. 5. The second (the load) is considered to be digital. The whole is depicted in Fig. 9a. The voltage at the A/D interface (v_1) is of interest here. The excitation used is depicted in Fig. 10.

To get reference data for modelling, the logic part was substituted by its circuit equivalent as shown in Fig. 9b. SPICE-like simulation was performed and the results are depicted in Fig. 11 denoted as "simulated". Here the *Alecsis* simulator was used for all simulations (Litovski et al., 2001). Now, the logic branch presents effectively infinite impedance so that the second analog inverter is responsible for all loading effects.

Implementation of the model for mixed-signal simulation is depicted in Fig. 9c. Here the loading effects are modelled by the ANN. The simulation results are given in Fig. 11. denoted by "ANN". Note that for multi-input circuits separate models (tables similar to Table 1.) have to be created for every distinct input terminal. One needs a behavioural simulator to exercise such a model (Litovski et al., 2001). This concludes the discussion related to modelling of the A/D interface.
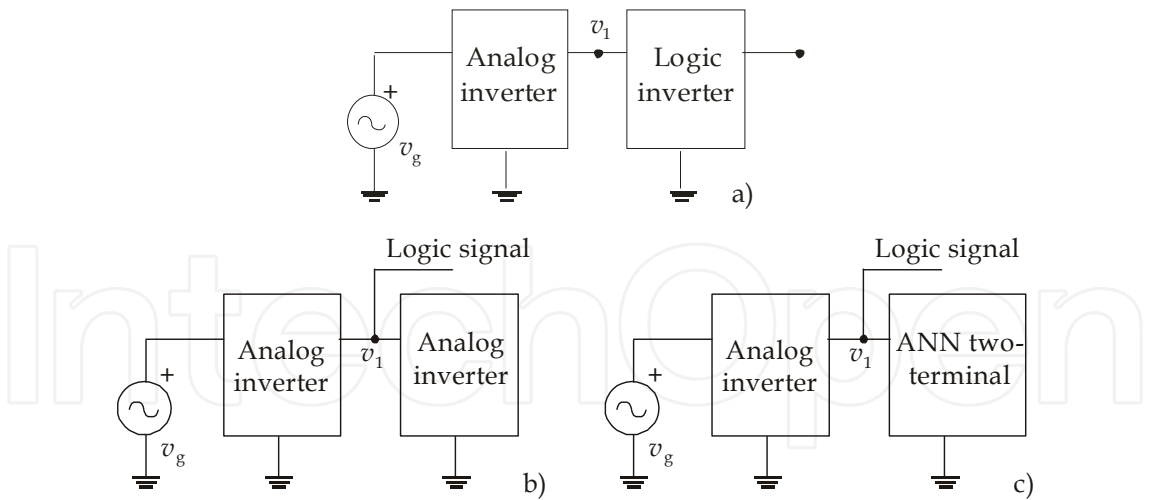
Fig. 9. Circuits used for verification. a) Analog inverter loaded by logic inverter, b) analog inverter loaded by analog inverter that generates reference signal v_1, and c) analog inverter loaded by ANN model.
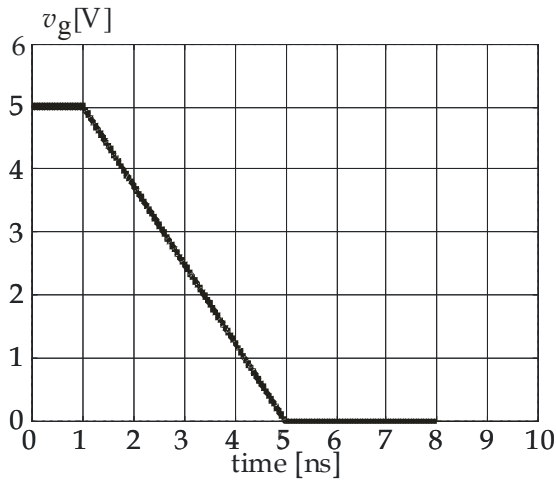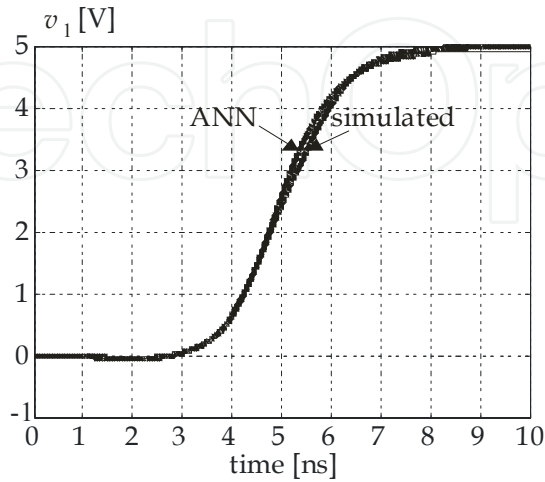

Fig. 10. Signal exciting the circuits in Fig. 9a.

Fig. 11. Response (v_1) obtained by simulation of the circuit of Fig. 9b. (simulated) and the circuit of Fig. 9c. (ANN).

4. Modelling the D/A interface

For modelling of the D/A interface, the output circuit of the digital part is to be represented by a circuit that is supposed to drive an analog load. Note that mixed-mode simulation is considered. This means that an event scheduler is active, marking the controlling input of the digital circuit (Litovski & Zwolinski, 1997b). The event scheduler does not allow for two inputs to be active simultaneously because that is considered as a hazard. Hence, modelling the output of an inverter is general enough for verification of the modelling procedure.
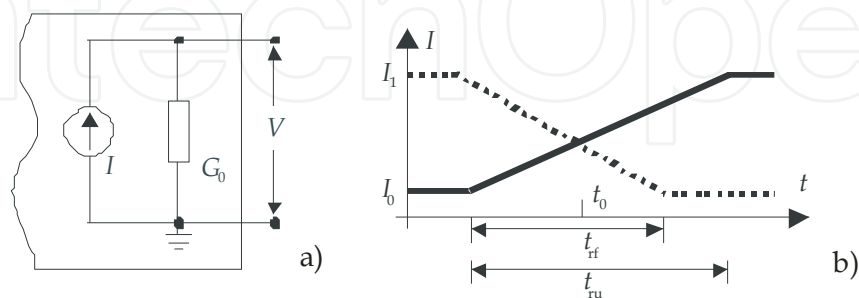

Fig. 12. a) Simple D/A conversion circuit, b) Current generator waveform t_{ru} stands for the rising edge while t_{rf} for the falling edge duration of the transition

Modelling of the D/A interface is more complex problem than modelling of the A/D interface, because we need to generate voltage waveform that excites the analog part of the circuit out of a set of logic states. Conversion algorithms are mostly based on synthesis of an electronic circuit that replaces the logic element's output, and is connected as an excitation to the particular node. Logic gate's delays also need to be considered and extracted by the event scheduler.

The simplest solution of the D/A conversion is illustrated in Fig. 12. (Zwolinski et al., 1989). There is a branch consisting of a constant conductance G_0 and current generator I, and it is applied to D/A node. The delay time is denoted by t_0.

Ratios I_1/G_0 and I_0/G_0 correspond to levels of logic 1 and logic 0, respectively, and different transition times from logic 1 to 0 and vice-versa, are permitted. Current waveforms for transitions from logic 1 to 0 and vice-versa are given in Fig. 12b.

A more complex output circuit is shown in Fig. 13. (Arnout & De Man, 1978). There are two voltage generators (E_0, R_0) and (E_1, R_1) applied to the analog node depending on logic element's output state. This function is realized by a switch controlled by Boolean function. R_0 and R_1 are logic gate's output resistances, when there are logic 0 or 1 at the output, respectively, meaning that there are two different resistance values, in contrast to previous case, when G_0 was used in both cases. The logic gate's delay is included in the switching time instant.
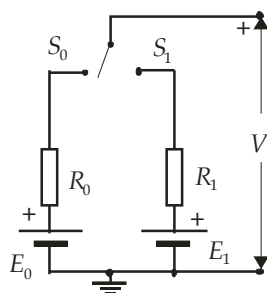

Fig. 13. D/A conversion with voltage levels

To further improve accuracy one may use the meliorated version depicted in Fig. 14. (Acuna et al., 1990). Sequence of pairs (E_i, R_i) and voltage controlled switch are used.
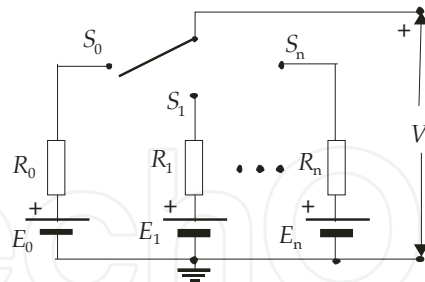

Fig. 14. Conversion when using several signal states on the logic gate output
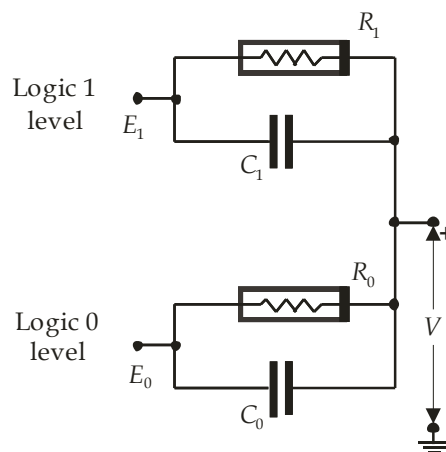

Fig. 15. D/A conversion using pair of voltage controlled resistors

In the circuit in Fig. 15. (Corman & Wimborow, 1988), the logic gate's output is observed as a voltage divider output. The capacitance values are constant and determined by the user if needed, and resistances are nonlinear and determined by user. In the circuits depicted in Figs. 14. and 15., the logic signal is firstly converted into electrical one and then values of this analog signal are discretized by comparing to sequence of thresholds. On that basis switches (Fig. 14.) or resistors values (Fig. 15.) are controlled. The circuits in previous examples approximate analog signal by discontinuous functions, what is inappropriate for most nonlinear circuit analysis methods.

Example of an output circuit approximated by analytical function is given in (Petković & Litovski, 1989; Petković & Litovski, 1991). Only nonlinear resistance is included, and using an approximation procedure, analytical expressions were produced expressing the output resistance dependence on the output voltage. Fig. 16. represents the output resistance of a CMOS inverter as a function of the output voltage. The dashed line is an approximation that was expressed in closed form.

The circuit depicted in Fig. 17. (Petković & Stojanović, 1992) includes output capacitances also. It consists of a nonlinear controlled ideal voltage generator E, a nonlinear resistor R and two output nonlinear capacitors C_0 and C_1. The transfer function, delays, output resistance and capacitances of digital gates are precisely modelled. While in (Petković & Litovski, 1989; Petković & Litovski, 1991) two constant values representing the logic level were used only, here the transfer characteristics and the delay are expressed in a more sophisticated way. Namely, a ramp signal, obtained by conversion of the logic output signal (similarly to Fig. 12b), is first delayed and as such, it represents a controlling signal for the

nonlinear generator *E*, whose dependence on the controlling voltage is actually the static transfer characteristic of an equivalent inverter. C_0 and C_1 are space-charge capacitances of the complementary transistors in the equivalent inverter.
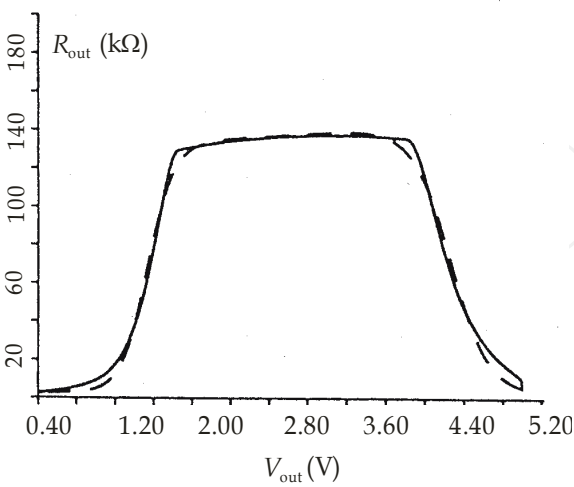

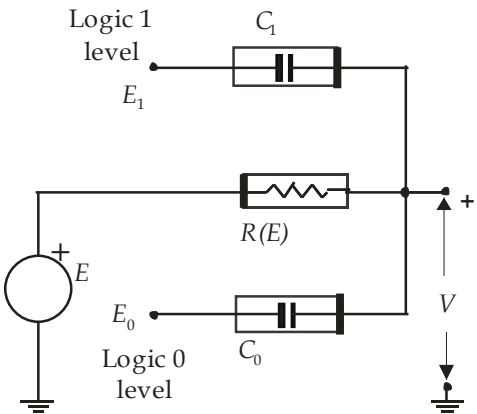Fig. 16. Output resistance approximation

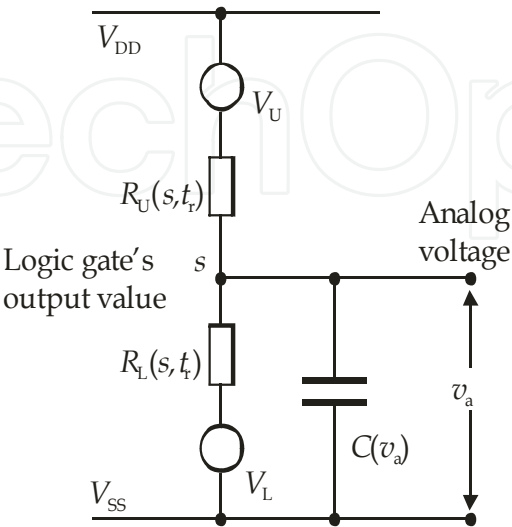Fig. 17. D/A conversion using nonlinear reactive part

Fig. 18. Output impedance model

Time-dependent resistors are used in (Nichols et al., 1992). The model of the output impedance of a logic gate is shown in Fig. 18. The values of the resistances R_U and R_L depend on value *s*, as well as on transition time t_r, but not on the analog output voltage v_a. On the other side the capacitance *C* depends on this voltage. The voltages V_{DD} and V_{SS} are logic gate supply voltages. V_U and V_L are fixed offset values for the given type of logic gate. The resistances R_U and R_L linearly change their values from minimum to maximum and reversely, depending on time t_r. Linear change does not cause problems in analog simulation, because the analog voltage value is continuous. The parameter t_r is chosen large enough in order to hinder too fast analog voltage change, even if the capacitance value reaches zero. The capacitance change is given in (Nichols et al., 1992).

Similar solution where resistors change their values is given in (Brown et al., 1994).

In the next, solution based on artificial neural networks is given. Main property of this solution is its topological generality. Namely, we have no need to look for the topology of the model depending on the approximation procedure or on the topology of the digital original. Simply, the topology is always the same. In addition, the approximating function is general in the sense that only the parameters within the approximating function are mapping the properties of the instantiated digital circuit.

The topology of the new model is depicted in Fig. 19. In the figure, v_{in} stands for a controlling ramp-shaped voltage-waveform:

$$i(v_{in}) = I_{max}[1 - \tanh(v_{in} - v_T)], \tag{1}$$

and *Z* is a recurrent time-delay neural network approximating the function:
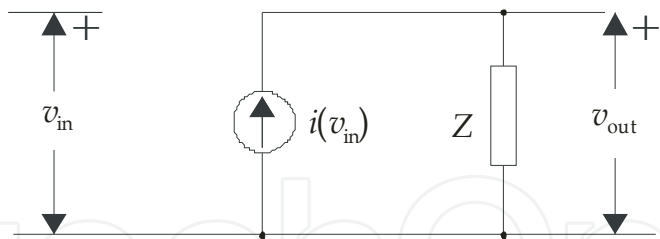
$$v_{out} = Z(i). \tag{2}$$

Fig. 19. Circuit representation of the model expressed by (1) and (2)

Here, I_{max} is the maximum supply current during the transition in the inverter, and v_T is (usually) equal to $V_{DD}/2$, V_{DD} being the supply voltage. Obviously, the ANN model of *Z* has one input (current) and one output (voltage) terminal. The network is trained using input-output pairs [$i(t)$, $v_{out}(t)$], where $i(t)$ is calculated from (1) while $v_{out}(t)$ is obtained by simulation using the *Alecsis* simulator of the circuit to be modelled (here an inverter). Note that we need the electrical schematic of the digital part during the modelling phase.

First results are shown in Fig. 20. Here the output waveforms of the original inverter and the model are shown to illustrate the quality of the approximation procedure. Unloaded circuits are simulated. The ANN has five input units (their role being the same as in Table 1.), three hidden units, and one output unit. Weights and thresholds are given in Table 2.

No.	Hidden-layer neurons (First figure stands for the input neuron)	Output neuron (First figure stands for the hidden neuron)
1	$w^1(1,1) = 2.28185$ $w^1(2,1) = -3.51137$ $w^1(3,1) = 1.36815$ $w^1(4,1) = 3.54312$ $w^1(5,1) = -1.37367$ $\theta_1^1 = -1.3177$	$w^2(1,1) = 0.644039$ $w^2(2,1) = 0.644042$ $w^2(3,1) = 0.644043$ $\theta_1^2 = -0.408248$
2	$w^1(1,2) = 2.28187$ $w^1(2,2) = -3.51135$ $w^1(3,2) = 1.36816$ $w^1(4,2) = 3.54312$ $w^1(5,2) = -1.37366$ $\theta_2^1 = -1.31769$	
3	$w^1(1,3) = 2.28187$ $w^1(2,3) = -3.51135$ $w^1(3,3) = 1.36816$ $w^1(4,3) = 3.54313$ $w^1(5,3) = -1.37366$ $\theta_3^1 = -1.31769$	

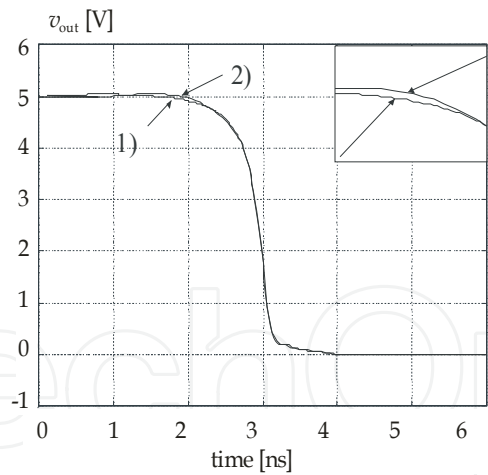Table 2. Weights and thresholds of ANN used to model the inverter circuit.

Fig. 20. Responses: 1) of unloaded CMOS inverter (considered as digital output) and 2) of the new model.

5. Further examples

The following three examples are intended to check the modelling procedure based on situations not present during training. The first trace (marked 1)) in Fig. 21. is the output voltage of an inverter being loaded by an inverter, all modelled by regular transistor models, i.e., obtained by regular circuit simulation. The second one (marked 2)) represents the

response of the same circuit with the ANN model used for the driving part and circuit model for the loading. This situation was not encountered in the training process. Excellent agreement was obtained, especially in the steepest part of the response that defines both the gain and the delay of the loaded inverter.

Further, Fig. 22. gives a similar comparison the loading element here being a transmission line modelled by a π-RC network (Chatzigeorgiou et al., 2001). Finally, a TTL load (diode) was used to demonstrate the success of the ANN model in the case of a 'large' non-linear dynamic load, Fig 23. Note the average value of the output voltage is less than 0.5 V while the difference is still smaller than 10 mV. Once again, the ANN model was developed using an unloaded inverter.
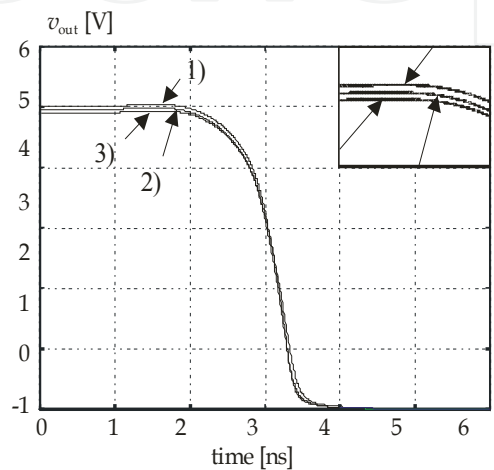

Fig. 21. Responses of 1) inverter loaded by inverter, 2) a model loaded by inverter, and 3) an ANN (modelling the output) loaded by an ANN modelling the input of an inverter.
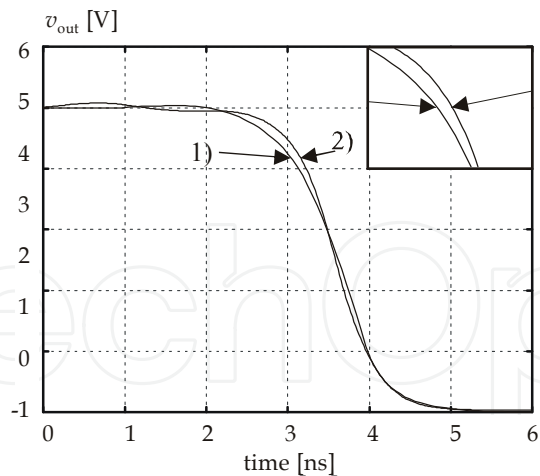

Fig. 22. Responses of 1) an inverter loaded by RC π-network and 2) a model loaded by RC π-network.

6. Application to high level analog simulation

Mixed-level analog behavioural modelling may need application of both concepts. In some situations, one will need to model the output circuit of the driver but in other cases, one will need to model the input circuit of the load; at very high levels of presentation, one will need

both. Such an example for the D/A interface is given in Fig. 21. Here trace 3) represents a response obtained by behavioural simulation using ANN models for both the driver and the load. In this way, the type of modelling we propose offers the opportunity to be implemented in analog behavioural simulation at any level.
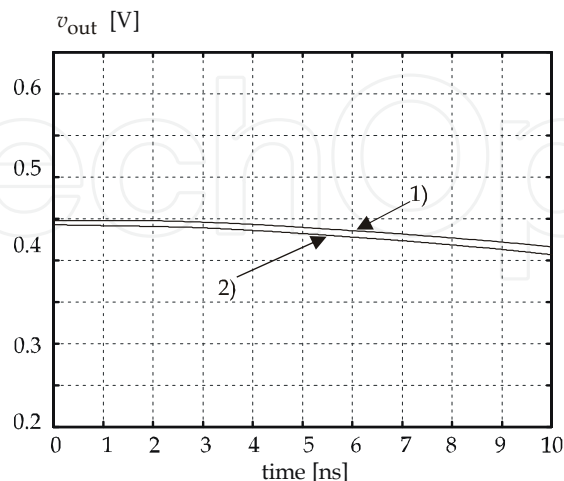

Fig. 23. Responses of a) inverter loaded by a diode and b) ANN model loaded by a diode.

7. Conclusion

An approach to the modelling of the A/D and D/A interface in mixed-mode circuit using ANNs has been described. The main difference in these two is the type of the input signal used for capturing the dynamic properties of the circuit to be modelled. For the D/A interface we use a ramp being, simply, the natural signal, while a sinusoidal signal was used for the input impedance modelling at the A/D interface in conjunction with general two-terminal non-linear dynamic modelling.

To summarise, a new method for modelling non-linear dynamic electronic circuits is described and applied to the modelling of A/D and D/A interfaces for mixed-signal simulation. It is *general and robust*. From the point of view of speed of simulation, one should bear in mind that ANNs are complex structures with exponential non-linearities requiring additional evaluation time compared to linear models. However, having in mind the complexity of modern models of MOS transistors (the BSIM3v3 model that is used in most modern electronic simulation capabilities needs more than a hundred parameters); we claim that the ANN approach is both efficient and convenient.

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