19

Implications of Negative Bias Temperature Instability in Power MOS Transistors

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1. Introduction

As the device dimensions in metal-oxide-silicon (MOS) technologies have been continuously scaled down, a phenomenon called negative bias temperature instability (NBTI), which refers to the generation of positive oxide charge and interface traps in MOS structures under negative gate bias at elevated temperature, has been gaining in importance as one of the most critical mechanisms of MOS field effect transistor (MOSFET) degradation. NBTI effects are manifested as the changes in device threshold voltage (V_T), transconductance (g_m) and drain current (I_D), and have been observed mostly in p-channel MOSFETs operated under negative gate oxide fields in the range 2 - 6 MV/cm at temperatures around 100°C or higher (Huard et al., 2006; Stathis & Zafar, 2006; Schroder, 2005; Alam & Mahapatra, 2005; Schroder & Babcock, 2003; Kimizuka et al., 1999; Ogawa et al., 1995). The phenomenon itself had been known for many years, but only recently has been recognised as a serious reliability issue in state-of-the-art MOS integrated circuits. Several factors associated with device scaling have been found to enhance NBTI: *i*) operating voltages have not been reduced as aggressively as gate oxide thickness, leading to higher oxide electric fields and increased chip temperatures; *ii*) threshold voltage scaling has not kept pace with operating voltage, resulting in larger degradation of drain current for the same shift in threshold voltage; and *iii*) addition of nitrogen during the oxidation process has helped to reduce the thin gate oxide leakage, but the side effect was to increase NBTI (Stathis & Zafar, 2006).

Considering the effects of NBTI related degradation on device electrical parameters, NBT stress-induced threshold voltage shift (ΔV_T) seems to be the most critical one, and a couple of basic questions, which are to be addressed now, are why the NBTI appears to be of great concern only in p-channel devices, and why the negative bias causes more considerable degradation than positive bias. The bias temperature stress-induced V_T shifts are generally known to be the consequence of underlying buildup of interface traps and oxide-trapped charge due to stress-initiated electrochemical processes involving oxide and interface defects, holes and/or electrons, and variety of species associated with presence of hydrogen as the most common impurity in MOS devices (see e.g. (Schroder & Babcock, 2003)). An interface trap is an interfacial trivalent silicon atom with an unsaturated (unpaired) valence electron at the SiO_2/Si interface. Unsaturated Si atoms are additionally found in SiO_2 itself, along with other oxide defects, the most important being the oxygen vacancies. Both oxygen

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vacancies and unsaturated Si atoms in the oxide are concentrated mostly near the interface and they both act as the trapping centers responsible for buildup of oxide-trapped charge. Interface traps readily exchange charge, either electrons or holes, with the substrate and they introduce either positive or negative net charge at interface, which depends on gate bias: the net charge in interface traps is negative in n-channel devices, which are normally biased with positive gate voltage, but is positive in p-channel devices as they require negative gate bias to be turned on. On the other hand, charge found trapped in the centers in the oxide is generally positive in both n- and p-channel MOS transistors and cannot be quickly removed by altering the gate bias polarity. The absolute values of threshold voltage shifts due to stress-induced oxide-trapped charge and interface traps in n- and p-channel MOS transistors, respectively, can be expressed as (Ma & Dressendorfer, 1989):

$$\Delta V_{Tn} = \frac{q\Delta N_{ot}}{C_{ox}} - \frac{q\Delta N_{it}}{C_{ox}}, \tag{1}$$

$$\Delta V_{Tp} = \frac{q\Delta N_{ot}}{C_{ox}} + \frac{q\Delta N_{it}}{C_{ox}}, \tag{2}$$

where q denotes elementary charge, C_{ox} is gate oxide capacitance per unit area, while ΔN_{ot} and ΔN_{it} are stress-induced changes in the area densities of oxide-trapped charge and interface traps, respectively. The amounts of NBT stress-induced oxide-trapped charge and interface traps in n- and p-channel devices are generally similar (Stathis & Zafar, 2006), but above consideration clearly shows that the net effect on threshold voltage, ΔV_T, must be greater for p-channel devices, because in this case the positive oxide charge and positive interface charge are additive. As for the question on the role of stress bias polarity, it seems well established that holes are necessary to initiate and/or enhance the bias temperature stress degradation (Huard et al., 2006; Stathis & Zafar, 2006; Schroder, 2005; Alam & Mahapatra, 2005; Schroder & Babcock, 2003; Kimizuka et al., 1999; Ogawa et al., 1995), which provides straight answer since only negative gate bias can provide holes at the SiO_2/Si interface. Moreover, this is an additional reason why the greatest impact of NBTI occurs in p-channel transistors since only those devices experience a uniform negative gate bias condition during typical CMOS circuit operation.

Several models of microscopic mechanisms responsible for the observed degradation have been proposed (Huard et al., 2006; Stathis & Zafar, 2006; Schroder, 2005; Alam & Mahapatra, 2005; Schroder & Babcock, 2003; Ogawa et al., 1995), but in spite of very extensive studies in recent years, the mechanisms of NBTI phenomenon are still not fully understood, so technology optimization to minimize NBTI is still far from being achieved. With reduction in gate oxide thickness, NBT stress-induced threshold voltage shifts are getting more critical and can put serious limit to a lifetime of p-channel devices having gate oxide thinner than 3.5 nm (Kimizuka et al., 1999), so accurate models and well established procedure for lifetime estimation are needed to make good prediction of device reliable operation.

Though the gate oxide in nanometre scale technologies is continuously being thinned down, there is still high interest in ultra-thick oxides owing to widespread use of MOS technologies for the realisation of power devices. Vertical double-diffused MOSFET (VDMOSFET) is an attractive device for application in high-frequency switching power supplies owing to its superior switching characteristics which enable operation in a megahertz frequency range

(Baliga, 1987; Benda et al., 1999). High-frequency operation allows the use of small-size passive components (transformers, coils, capacitors) and thus enables the reduction of overall weight and volume, making the power VDMOSFETs especially suited for application in power supply units for communication satellites, but they are also widely used as the fast switching devices in home appliances and automotive, industrial and military electronics. Degradation of power MOSFETs under various stresses (irradiation, high field, and hot carriers) has been subject of extensive research (see e.g. (Stojadinović et al., 2006) and references cited therein), but very few authors seem to have addressed the NBTI in these devices (Demesmaeker et al., 1997; Gamerith & Polzl, 2002; Stojadinović et al., 2005; Danković et al., 2006; Danković et al., 2007; Danković et al., 2008, Manić et al., 2009). However, power devices are routinely operated at high current and voltage levels, which lead to both self heating and increased gate oxide fields, and thus favour NBTI. Accordingly, NBTI could be critical for normal operation of power MOSFETs though they have very thick gate oxides.

Given the above considerations, this chapter is to cover the NBTI implications on reliability of commercially available power VDMOSFETs. In the next section, we will describe the experimental procedure for accelerated NBT stressing applied in our study and analyse typical results for the threshold voltage shifts observed in stressed devices. Applicability of some empirical expressions for fitting the dependences of stress-induced threshold voltage shifts on stress conditions (voltage, temperature, time) to our experimental data will be discussed as well. Third section is to describe in details the results of the procedure applied to fit the experimental data and estimate the device lifetime by means of several fitting and extrapolation models. Impacts of stress conditions, failure criteria, models used for fitting and extrapolation, and intermittent annealing on lifetime projection will be discussed as well. The extrapolation models available in the literature offer only extrapolation along the voltage (or electric field) axis and provide lifetime estimates only for the temperatures applied during the accelerated stressing, so in the next section we propose a new approach, which requires double extrapolation along both voltage and temperature axes, but can estimate the device lifetime for any reasonable combination of operating voltages and temperatures, including those falling within the ranges normally found in usual device applications. Finally, most important findings presented in the chapter will be summarized in the conclusion section.

2. NBT stress-induced threshold voltage shifts

Devices used in our study were commercial p-channel power VDMOSFETs IRF9520, encapsulated in TO-220 plastic cases, with current and voltage ratings of 6.8 A and 100 V, respectively. Devices were built in standard silicon-gate technology with 100 nm thick gate oxide, and had the threshold voltage V_T = -3 V. Several sets of devices have been stressed up to 2000 hours by applying negative voltages in the range 30 – 45 V to the gate, with drain and source terminals grounded, at temperatures ranging from 125 to 175°C. A conventional methodology, based on periodic breaks during the stress to measure the device transfer *I-V* characteristics, was applied to characterize the NBT stress effects. Threshold voltage values were estimated from the above-threshold transfer characteristics as the intersections of extrapolated linear region of $\sqrt{I_D} - V_{GS}$ curves with V_{GS} - axis.

Typical transfer *I-V* characteristics of p-channel power VDMOSFETs measured during the NBT stressing are shown in Fig. 1. It can be seen that, as the stressing progresses, the characteristics are being shifted along the V_{GS} axis towards the higher voltage values, which is the consequence of stress-induced buildup of oxide-trapped charge. The shifts are more significant in the early phase of stressing and gradually become smaller with tendency to saturate in the advanced stress phase. At the same time, the slope of the curves slightly decreases, indicating that interface traps are being generated as well.

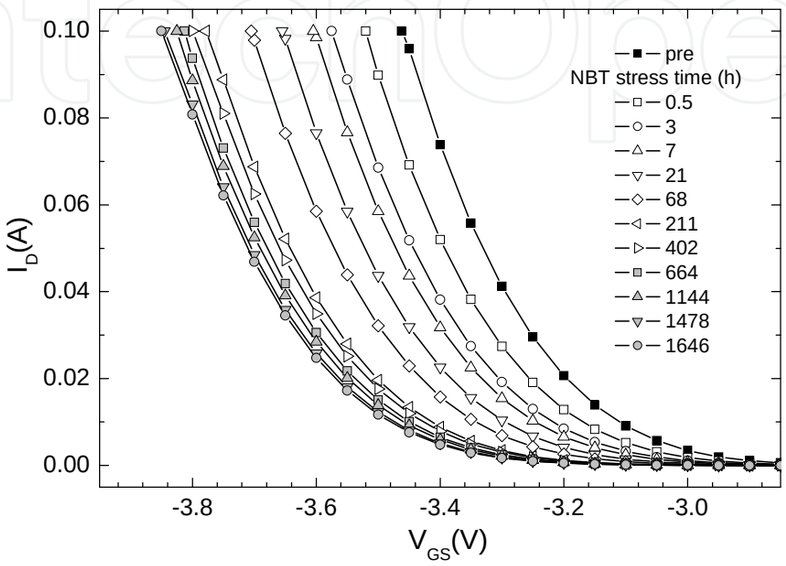

Fig. 1. I_D-V_{GS} characteristics of p-channel power VDMOSFETs during NBT stressing with V_G = - 40 V at 150°C.

In line with observed shift of transfer characteristics along the voltage axis, NBT stressing was found to cause significant threshold voltage shifts in our devices. Two characteristic sets of data, for IRF9520 devices stressed with - 40 V at different temperatures and with different voltages at 150°C, are shown in Figs. 2 and 3, respectively. Apparently, more pronounced shifts are observed in devices stressed at higher temperatures (Fig. 2) and/or with higher stress voltages (Fig. 3). In all cases, ΔV_T time dependences have been found to follow the t^n power law, with three distinct phases (as indicated by the dashed lines), which can be clearly distinguished depending on the value of parameter n (Stojadinović et al., 2005; Danković et al., 2006; Danković et al., 2006a). In the first (early) stress phase, n strongly depends on both stress bias and temperature, varying from 1.14 to 0.4. In the second phase, n is almost independent on bias and temperature, and ΔV_T follows the well-known $t^{0.25}$ law (Jeppson & Svensson, 1977; Ogawa et al., 1995; Schroder, 2005; Huard et al., 2006; Stathis & Zafar, 2006). The second phase begins earlier in devices stressed with higher voltages and/or at higher temperatures so the first phase might even disappear if more severe stress conditions had been applied. Finally, in the third phase, n becomes bias and temperature dependent again and gradually decreases from 0.25 to 0.14, whereas ΔV_T tends to saturate. The ΔV_T in saturation after near 2000 hours of stressing was found to vary from about 4.4 % in devices stressed at 125°C with - 30 V) up to 19.8 % in those stressed at 175°C with - 45 V (Stojadinović et al., 2005).

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$$\Delta V_T = C_2 e^{\beta V_G} t^n \exp(E_a/kT), \quad (4)$$

$$\Delta V_T = C_3 E^m t^n \exp(E_a/kT), \quad (5)$$

where V_G, E, t, and T denote stress voltage, corresponding oxide electric field, stress time, and temperature, respectively, E_a is activation energy, k is the Boltzmann constant, whereas C_2, C_3, β, m, and n are the fitting parameters. Activation energy and fitting parameters assume different values for each of the three phases mentioned above, and these expressions can be used to calculate stress-induced threshold voltage shift in IRF9520 devices for a random combination of voltages and temperatures within the voltage and temperature ranges investigated (Stojadinović et al., 2005; Stojadinović et al., 2007).

3. NBTI effects on device lifetime

As already mentioned, degradation associated with NBTI could put serious limit to a lifetime of devices operated at elevated temperatures under the increased gate oxide field. Our goal is to estimate the lifetime of investigated power VDMOSFETs under normal operating conditions by using the obtained results from accelerated NBT stressing. However, the standard procedure requires to extract first the values of lifetime the devices would have if operated under the experimental conditions, and these experimental lifetime values are then used for extrapolation to normal operating conditions. Accordingly, this section will begin with estimation of the lifetime under experimental conditions, to be followed by a procedure for extrapolation to normal operating bias conditions, including detailed discussion of various factors affecting the lifetime estimated in this way. The effect of intermittent annealing on lifetime will also be additionally discussed.

3.1 Extraction of experimental lifetime data

To estimate the device lifetime it is necessary to choose one of device parameters affected by the stress, which will be used to monitor the level of stress-induced degradation and to define the failure criterion (FC) as a maximum change of the chosen parameter, which could be critical for device and/or reliable operation. Various parameters such as threshold voltage, transconductance, drain current, can be used as a degradation monitor (Schlunder et al., 2005; Stojadinović et al., 2005). We will use threshold voltage, which has been shown in previous sections to be affected by NBT stressing, and also has been widely accepted as a well-suited parameter, so the device lifetime for practical power VDMOSFETs studied here will be estimated from the experimental results of NBT stress-induced threshold voltage shifts. As shown in Fig. 4, experimental data obtained as the stress time required for $|\Delta V_T|$ reaches the predetermined value of FC (100 mV in this case). Experimental lifetime values, t_{exp}, are extracted from the plots shown in the figure and are used to plot the gate voltage dependence as in the inset graph, which is further used for extrapolation to a normal operating voltage.

A proper choice of failure criterion, which is discussed in more details later, is important. For example, it can be seen in Fig. 4 that the value of FC was higher then about

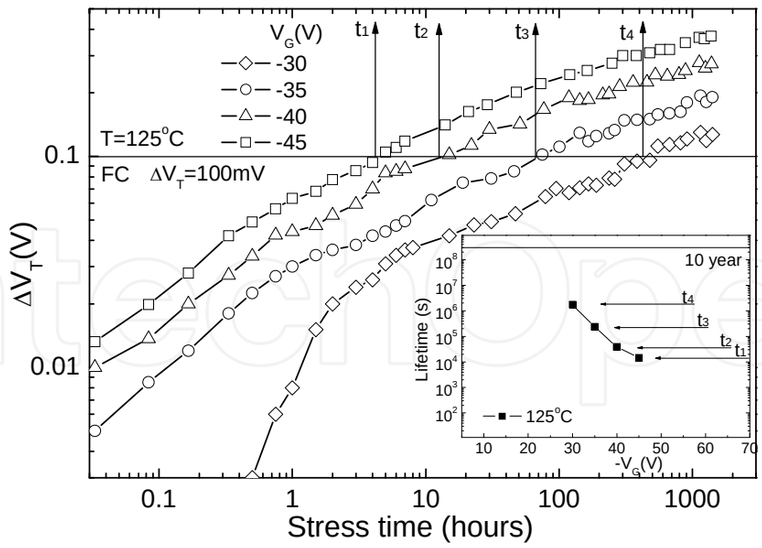


Fig. 4. Extraction of experimental lifetime data and illustration of extrapolation to a normal operating voltage (inset).

the experiment in this case was not sufficient to achieve ΔV_T as high as FC, which means the stress time should have been extended to exceed the device lifetime for a given combination of stress bias and temperature. However, this could require the stressing to be done beyond the reasonable time limit so in such cases it is convenient to use an adequate fitting model capable to provide reliable prediction of ΔV_T on the basis of available data. The simplest way is to use regular exponential model (Liu et al., 2001; Liu et al., 2002; Krishnan & Kol'dyaev, 2002):

$$\Delta V_T(t) = \Delta V_{T\max}[1-\exp(-t/\tau)], \tag{6}$$

where ΔV_{Tmax} is the saturation level of threshold voltage shift and τ is the characteristic time constant. However, as shown in Fig. 5, this model (dotted line) in our case yields very poor agreement with experimental data and significantly underestimates ΔV_T in saturation. Since the ΔV_T time dependences in our devices exhibit the discontinuities manifested as three distinct stress phases (Figs. 2 and 3), better agreement with experimental data is expected from the modified version of the above model, which is known as the 2-tau exponential model and is given by (Liu et al., 2001; Liu et al., 2002):

$$\Delta V_T(t) = \Delta V_1[1-\exp(-t/\tau_1)] + \Delta V_2[1-\exp(-t/\tau_2)], \tag{7}$$

where the fitting parameters τ_1 and τ_2 represent the time constants closely related to transitions from early to the second stress phase and from the second phase to saturation, respectively, whereas ΔV_1 and ΔV_2 are associated with corresponding V_T shifts. This model is suitable for processes which have two distinct mechanisms operating one after the other with $100\tau_1 < \tau_2$. As can be seen in Fig. 5, the 2-tau model (dashed line) yields fairly good agreement with experimental data. However, this model appears very sensitive to small fluctuations in experimental data (the fit looks "wavy" in the second stress phase) and tends to exaggerate saturation in the case of devices stressed with - 30 V at 125°C, which does not seem justified by the experimental data.

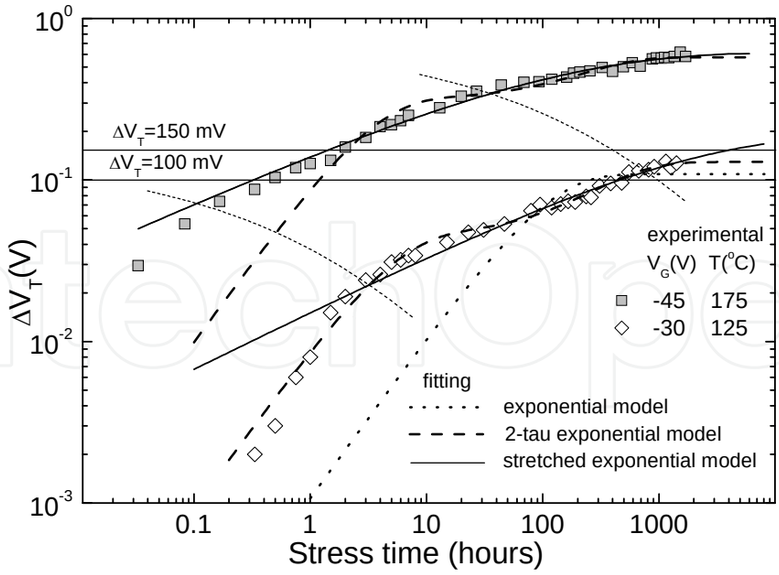


Fig. 5. Fitting of the NBT stress-induced V_T shifts by means of various models. Symbols denote the measurement data and lines are the fits.

Trying to resolve the problem, we have also considered the so-called stretched exponential model, given by (Van de Walle, 1996; Zafar et al., 2003; Zafar et al., 2004):

$$\Delta V_T(t) = \Delta V_{T\max}[1 - \exp(-(t/\tau_o)^{\beta})], \tag{8}$$

where ΔV_{Tmax}, τ_o, and β are the fitting parameters. The stretched exponential model predicts ΔV_T would saturate and reach the maximum value only after a very prolonged stressing, so the ΔV_{Tmax} can be taken as a measure of ΔV_T at ten year device lifetime. Parameter β is defined as a measure of distribution width, and τ_o represents a characteristic time constant of the distribution. This model is suited for processes that, either have two or more distinct mechanisms each with its own τ, or have a single mechanism with statistically distributed values of τ (Van de Walle, 1996).

As can be seen in Fig. 5, the stretched exponential model (solid line) yields very poor agreement with our experimental data in the early phase of stressing, especially for the lower stress voltage. However, this disagreement tends to decrease with increase in stress voltage and/or temperature and, more importantly, the model is in excellent agreement with experimental data in the second stress phase and in saturation, which is of greatest practical importance since we need reliable prediction for ΔV_T at prolonged stress time to estimate the device lifetime. A practical consequence is that stretched exponential fit, if properly constructed, may replace the experimental data in saturation and shorten the experiment execution time, while also allowing the use of higher FC, e.g. 150 mV, as shown in Fig. 5. Figure also shows that time points associated with transitions from the early to second stress phase, which had been determined on the basis of parameter n in the t^n power law dependences, correspond to the points at which the stretched exponential fitting curves start agreeing with experimental data, which confirms the phase feature of NBT stress-induced degradation in power VDMOSFETs (Stojadinović et al., 2005; Danković et al., 2006).

The values of parameter β in the stretched exponential fit of our experimental results obtained on VDMOSFETs are found to vary in the range 0.35~0.39 independently on stress

conditions, whereas τ_o decreases with increasing the stress voltage and temperature, which all is in good agreement with findings reported in (Zafar et al., 2003; Zafar et al., 2004). The calculated values of maximum threshold voltage shifts in saturation, ΔV_{Tmax}, are listed in Table 1. As expected, these values, which represent a measure of ΔV_T at ten year lifetime, are found to increase with both NBT stress voltage and temperature.

ΔV_{Tmax} (V)		V_G (V)			
		- 30	- 35	- 40	- 45
T (°C)	125	0.1858	0.2518	0.3109	0.4169
	150	0.2073	0.3241	0.4074	0.5563
	175	0.3188	0.3319	0.4584	0.5694

Table 1. Values of ΔV_{Tmax} in the stretched exponential fit of data obtained on NBT stressed p-channel power VDMOSFETs

3.2 Extrapolation to normal operating bias conditions

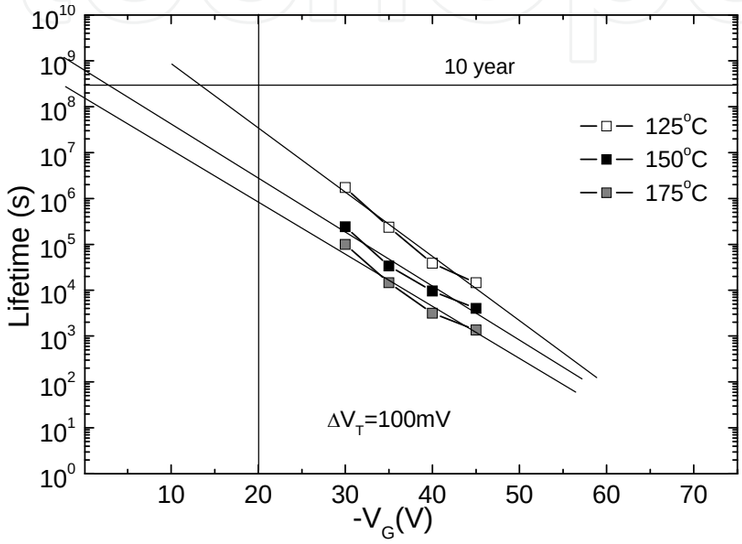
The extracted values of the lifetime under experimental conditions are used as the input data for extrapolation to normal operating gate bias conditions. However, the results obtained in this way, which represent the device lifetime values projected to normal conditions, may be strongly affected by several factors, such as the failure criterion, the range of gate voltages applied during the stress, and the mathematical function (i.e. model) used in extrapolation (Aono et al., 2005; Ershov et al., 2005), which are now to be addressed.

3.2.1 Failure criterion

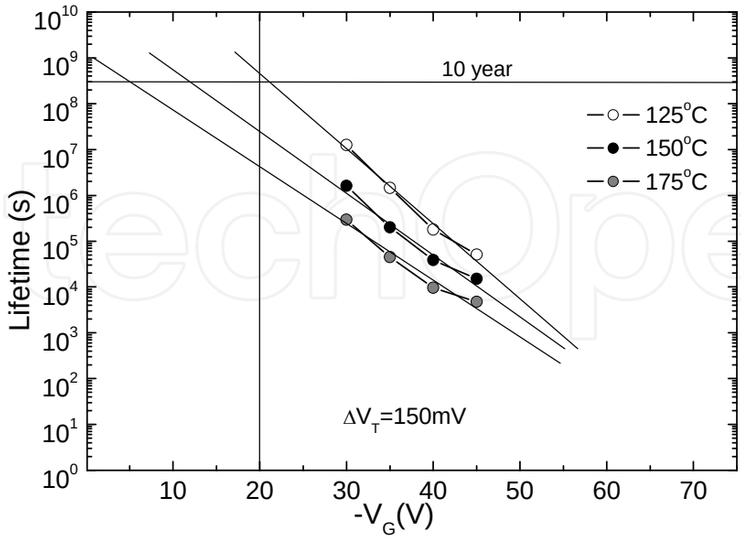
As indicated in Fig. 5, we have defined two different failure criteria as the threshold voltage shifts of 100 mV and 150 mV, respectively, which are now used to project the device lifetime under normal gate bias conditions. Lifetime estimation at three different temperatures for both failure criteria, done by a standard linear extrapolation assuming a maximum normal operating gate voltage to be V_G = - 20 V, is illustrated in Fig. 6, whereas the resulting values of extrapolated lifetime are listed in Table 2. It is quite obvious that lifetime projection strongly depends on the choice of failure criterion.

The saturation tendency of the stress-induced threshold voltage shift gives contribution to a rise of the device lifetime, especially for higher failure criterion (150 mV). It can be seen in Fig. 5 that, in the case of the lower stress voltage, the 150 mV FC line only intersects with the stretched exponential fitting curve but not with experimental data, which means the duration of experiment was shorter than the lifetime at given temperature. However, lower stress voltages are closer to actual operating voltages and are expected to provide more realistic lifetime projection. In this case, the fact that stretched exponential fit successfully predicts threshold voltage shift in saturation enabled us to estimate the lifetime by using the results obtained by fitting instead of the missing experimental ones. If the failure criterion was too high (e.g. 700 mV), its value would fall far above both experimental and fitting curves in Fig. 5, which would result into device lifetime tending infinity. Alternatively, too low failure criterion (below 30 mV) could lead to rather significant underestimation of device lifetime as the value of failure criterion would fall in the early phase of stressing.

Following the above considerations, it appears that most reliable lifetime projections can be obtained by choosing the FC value within the range of threshold voltage shifts observed in the second and saturation phases of device stressing. The correct choice of FC could be verified by considering the values of ten year operation voltage, V_{G10Y}, which is defined as the maximum gate voltage that allows ten years of device operation with V_T shift below the given FC. As can be seen in Table 3, which shows the V_{G10Y} data taken from Fig. 6, the values of ten year operation voltage in most cases fall below the assumed value of maximum operating gate bias voltage of - 20 V, except in the case of 150 mV FC at 125°C. Alternatively, table indicates that in the case of 100 mV FC the devices at 175°C cannot



(a)



(b)

Fig. 6. Linear extrapolation of the device lifetime at different temperatures for two different values of failure criteria: *a*) ΔV_T =100 mV; *b*) ΔV_T =150 mV.

Lifetime (days)	ΔV_T = 100 mV	ΔV_T = 150 mV
125°C	391.07	5792.10
150°C	30.67	289.86
175°C	9.25	48.06

Table 2. Lifetime projections for operating voltage V_G = - 20 V under two different FC values

approach ten years of operation even without any gate bias, which does not make sense. Thus, the realistic failure criterion for the devices and experimental conditions used in our study appears to fall in the 100 - 150 mV range, which yields the ten year operation voltage within the range of normal gate operation voltages between 0 and - 20 V.

V_{G10Y} (V)	ΔV_T = 100 mV	ΔV_T = 150 mV
125°C	-13	-21
150°C	-3	-12
175°C		-5

Table 3. Estimated values of ten year operation voltage under two different failure criteria

3.2.2 Stress voltage range

Another factor that may affect the value of lifetime estimate is the range of stress voltages used in data extrapolation (Aono et al., 2005). The effects of stress voltage range on uncertainties of both lifetime projection and ten year operation voltage in the case of VDMOS devices stressed at 150°C are illustrated in Fig. 7, where the solid line shows extrapolation over the full range of four different stress voltages applied, whereas the dotted and dashed lines represent extrapolation over the higher and lower voltage ranges, respectively (in these cases the data corresponding to the lowest and highest voltages, respectively, have not been used in extrapolation). As can be noticed in the figure, the uncertainties associated with the choice of stress voltage range may cause the lifetime projection to vary for almost one order of magnitude, while the ten year operation voltage, i.e. maximum allowed V_G, varies for about 8 V.

A schematic drawing shown in Fig. 8 provides further evidence that the lifetime obtained by extrapolating the experimental data to normal operating conditions may strongly depend on the choice of both stress voltage range and failure criterion. As can be seen, experimental lifetime values determined for a given FC in the cases of devices stressed with the highest and lowest voltages fall in the early and in saturation phases, respectively. As a result, both these experimental values are higher, for Δt_2 and Δt_1, respectively, than those the lifetime would assume if found in the second phase, leading to a deviation from linearity in the extrapolation plot shown as an inset graph in Fig. 8. As a consequence, the use of higher stress voltage range for extrapolation to normal bias conditions tends to underestimate the lifetime, whereas the use of lower stress voltage range appears to overestimate it, both contributing to uncertainties shown in Fig. 7. More realistic lifetime estimates could be

expected if the lower stress voltage range, closer to normal operating voltage, was used in extrapolation, but in that case the experiment could take too much time, so the most appropriate solution is to use an expression, such as the one given by stretched exponential function, that provides good fit to experimental data in the low stress voltage range.

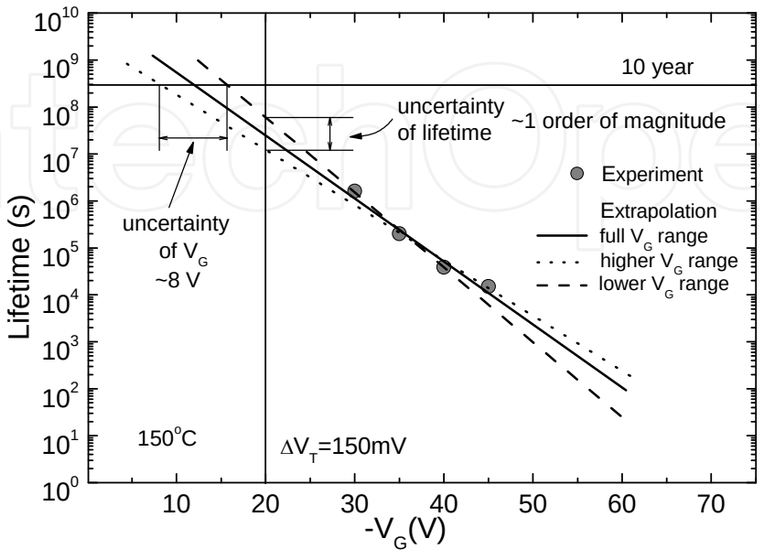


Fig. 7. Uncertainties of the lifetime and ten year operation voltage due to different ranges of stress voltages used in data extrapolation.

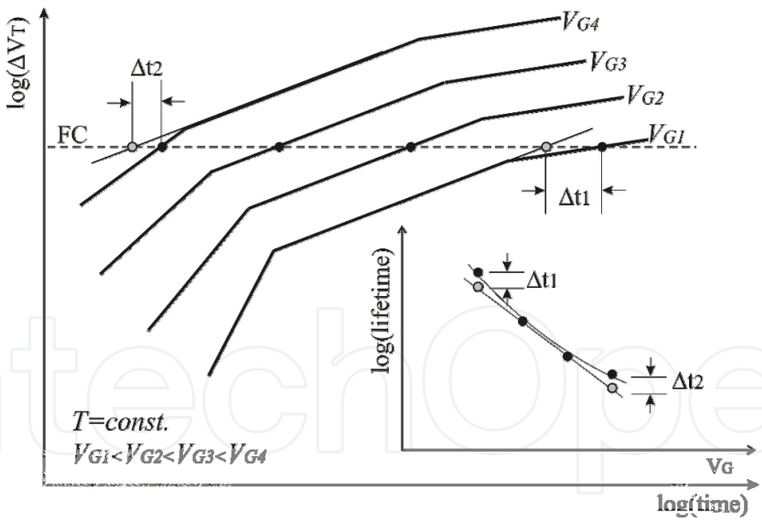


Fig. 8. Schematic illustration to explain the effects of FC and stress voltage range on lifetime projection.

3.2.3 Extrapolation models

In the above analyses of the failure criterion and stress voltage range effects on the lifetime projection we have only applied the standard model, which was based on linear extrapolation function. However, it can be seen in Figs. 6 and 7 that this model in some cases may not provide good fit to experimental data. For this reason, there are several other

commonly used models, such as the so-called V_G and $1/V_G$ models for extrapolation along the voltage axis, which are given by following expressions, respectively:

$$\tau = A \cdot \exp(-B \cdot V_G), \tag{9}$$

$$\tau = A \cdot \exp(B / V_G), \tag{10}$$

as well as the power-law model for extrapolation along the electric field axis:

$$\tau = C \cdot E^{-p}. \tag{11}$$

In the expressions above, τ is the lifetime, V_G and E are the stress voltage and corresponding electric field, respectively, whereas A, B, C, and p are the fitting parameters. These models are based on the experience of different researchers, and it is simple to show, for example, that power-law model can be derived by rearranging the empirical Eq. (5) as follows:

$$t = A^{1/n} E^{-m/n} \Delta V_T^{1/n} \exp(E_a / nkT), \tag{12}$$

and introducing the new parameters, C and p, in Eq. (12) defined as:

$$C = A^{1/n} \Delta V_T^{1/n} \exp(E_a / nkT), \tag{13}$$

$$p = m / n, \tag{14}$$

where t becomes the lifetime, τ, when ΔV_T takes the value of failure criterion.
The uncertainties of both device lifetime and ten year operation voltage in the case of p-channel VDMOSFETs stressed at 150°C, as obtained by the use of four different models for extrapolation, are shown in Fig. 9. As can be seen, each model yields different result, so the

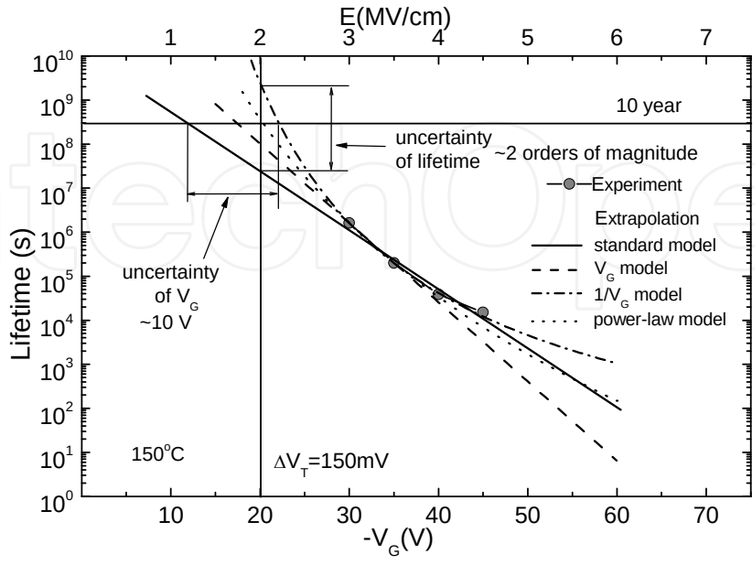


Fig. 9. Device lifetime and ten year operation voltage uncertainties due to different models used for extrapolation.

lifetime estimates obtained using different models may vary for more than two orders of magnitude, while the ten year operation voltage varies for about 10 V. The V_G and especially standard model yield lower values of both lifetime and ten year operation voltage, and both these models do not seem to provide good fit to our experimental data. The V_G model curve shows disagreement with experimental data obtained at higher stress voltages, which is in line with expectation on more realistic estimates if the lower stress voltage range, closer to actual operating voltage, was used for extrapolation. Alternatively, the power-law model provides better fit to our experimental data, but still shows certain disagreement at the higher voltage range, whereas only the $1/V_G$ model appears to fit our experimental results almost perfectly over the full range of stress voltages applied. Thus, the lifetime and ten year operation voltage estimates obtained by the $1/V_G$ model appear to be the least affected by the choice of stress voltage range.

The above considerations may have important consequences on investigations of NBTI related degradation and lifetime prediction not only in power VDMOSFETs but also in other devices exhibiting saturation in the stress-induced threshold voltage shifts over an extended period of NBT stressing. Namely, it appears that lifetime estimates obtained by the power-law, V_G and standard models would approach those obtained by $1/V_G$ model if lower voltages are used for device stressing. However, this could require very long time to perform the experiment. On the other hand, the $1/V_G$ model could provide much faster output since it appears to allow the use of higher stress voltages while still being capable to yield rather accurate lifetime estimates.

3.3 Effects of intermittent annealing

The recovery and annealing of NBTI have received an increased attention recently (Ershov et al., 2003; Tsujikawa et al., 2003; Ershov et al., 2005; Rangan et al., 2005; Huard et al., 2006), so we also have tried to get new insight into the NBTI phenomena by subjecting the devices to a sequence of NBT stress and bias annealing steps. Detailed experiments, with different stress and recovery conditions, have been performed to assess the impact of annealing phase (Danković et al., 2007; Manić et al., 2009), and here we will only present the results obtained on a set of IRF9520 devices subjected to a sequence of three interchanging NBT stress and bias annealing steps as follows: one week of NBT stressing with three different gate voltages (- 35, - 40, and - 45 V) at T = 150°C was followed by one week of positive gate bias annealing with V_G = +10 V also at 150°C, and then the devices were NBT stressed again for one week.

As can be seen in Fig. 10, the initial stress-induced increase of the threshold voltage was most significant in devices stressed with V_G = - 45 V. Initial shifts decreased in all devices during the subsequent annealing, but increased again on repeated NBT stressing. Most rapid decrease on positive bias annealing was observed in devices stressed previously with V_G = - 45 V, and highest increase during the next stressing was found in these devices again.

To assess the impact of intermittent annealing on lifetime projection more closely, Fig. 11 shows the motion of V_T shift over the full 3-step stress/anneal/stress sequence in the case of devices stressed with – 40 V. As can be seen, significant recovery of threshold voltage occurs only in an early stage of the annealing step, so the initial stress-induced ΔV_T did not fall below 100 mV. So, we can conclude that there was a non-reversible component of threshold voltage shift, which resulted from the portion of stress-induced oxide-trapped charge and interface traps that could not have been annealed.

Judging from the data shown in Figs. 10 and 11, the failure criterion that would yield reasonable lifetime projection appears to fall in the range 100-200 mV. Lifetime estimates for

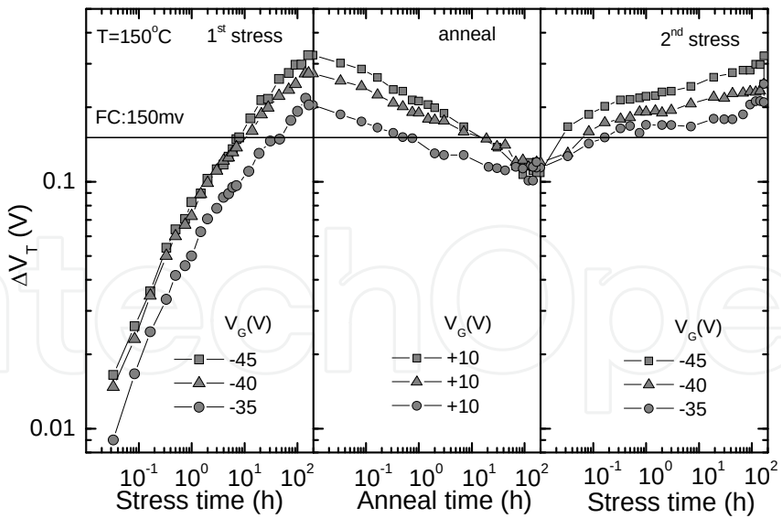


Fig. 10. Threshold voltage shifts during the full sequence of NBT stresses and positive gate bias annealing at 150°C in devices stressed with three different gate voltages.

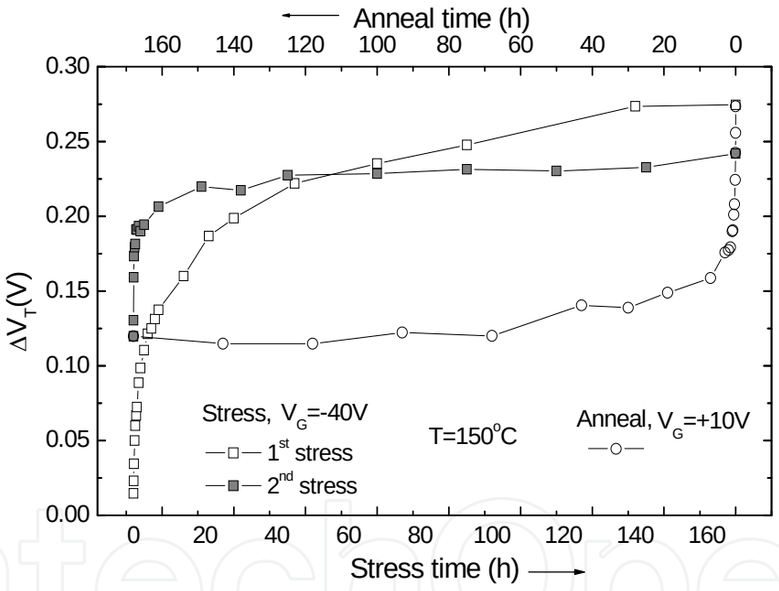


Fig. 11. Threshold voltage shift during the sequence of NBT stresses and positive gate bias annealing at 150°C in devices stressed with – 40 V.

both continuously stressed devices and those subjected to above 3-step stress/anneal/stress sequence, obtained by using the power-law model, are shown in Fig. 12. As can be seen, the two curves overlap in the semi-log plot, yielding practically the same lifetime estimates. The dashed line shows estimation of the difference between the two lifetime projections, $\Delta\tau$. It can be seen that $\Delta\tau < 10^5$ s, i.e. $\Delta\tau$ is less than 2 days, which is negligible in comparison with 10-year lifetime expectation. Therefore, intermittent annealing did not have any apparent impact on device lifetime, which could have been expected since the comparison of data shown in Figs. 3 and 10 indicated that ΔV_T at the end of the above stress/anneal/stress sequence approached ΔV_T observed in continuously stressed devices.

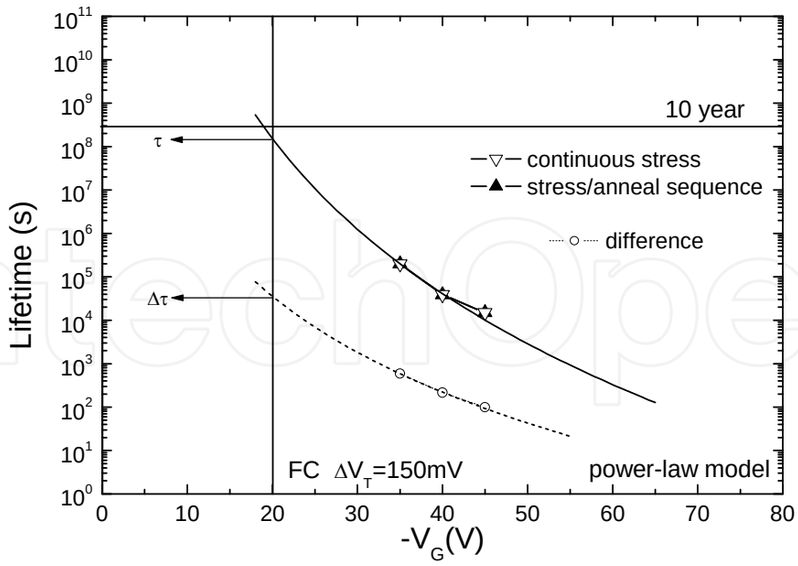


Fig. 12. Lifetime in continuously stressed and sequentially stressed & annealed devices.

4. New approach in estimating the lifetime

As already mentioned, the goal of our study was to estimate the lifetime of investigated VDMOSFETs under normal operating conditions (V_{Go}, T_o) using the results obtained by accelerated NBT stressing (V_G, T). These are the power devices, so we could assume maximum normal bias and temperature to be, for example V_{Go} = - 20 V and T_o = 100°C. In the previous section we have used the accelerated NBT stress data to estimate the lifetime our devices would have if operated under the above gate voltage by means of several models for extrapolation along the voltage axis. Further illustration is provided in Fig. 13, which shows the lifetime estimation in IRF9520 devices by power-law model for three different temperatures applied during the NBT stress. Only extrapolation to V_{Go} = -20 V is

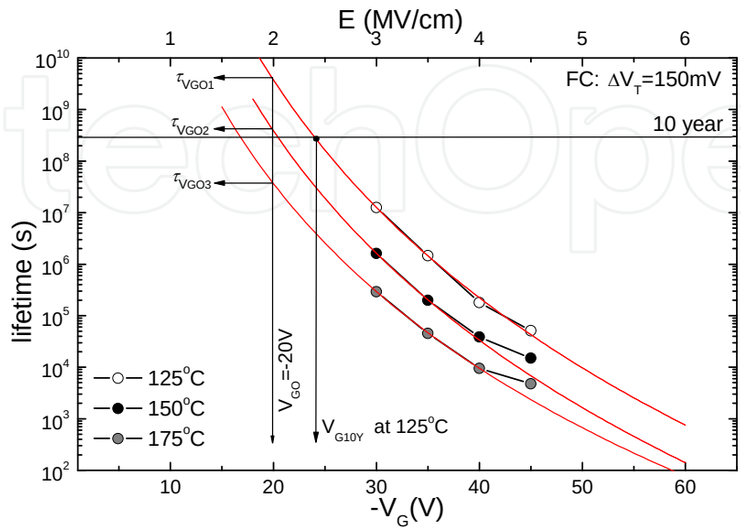


Fig. 13. Estimation of the lifetime and ten year operation voltage by power-law model.

shown, but the same procedure can be used to estimate the lifetime, τ_{VGo}, by extrapolation to any other reasonable operation voltage. In addition, the procedure allows to estimate the ten year operation voltage (V_{G10Y}), which represents the maximum gate voltage that allows 10 years of device operation with stress-induced ΔV_T below FC. However, this procedure yields the τ_{VGoj} and V_{G10Yj} values (j = 1 - 3) only for the temperatures applied during the accelerated stressing, which are generally higher than those actually found in device normal operation mode. So, this approach does not offer the possibility to estimate the lifetime at any temperature other than those used in the accelerated stress experiments, which generally applies to all the models discussed in previous section.

4.1 Extrapolation along the temperature axis

Trying to resolve the above issue, we note that all the empirical expressions for the threshold voltage shifts found during the NBT stressing, which were given by Eqs. (3) – (5), include the temperature dependence of stress-induced degradation by incorporating the Arrhenius temperature acceleration term. It is simple to show that any of these expressions can be used to derive a mathematical function that could be suitable as a model for extrapolation along the temperature axis. For example, Eq. (5) can be rearranged to be written as:

$$t = C_3^{-1/n} E^{-m/n} \Delta V_T{}^{1/n} \exp(E_a / nkT) \cdot \tag{15}$$

Now we introduce the parameters A_2 and B_2 in Eq. (15) as follows:

$$A_2 = C_3^{-1/n} \Delta V_T{}^{1/n} E^{-m/n}, \tag{16}$$

$$B_2 = E_a / nk\ , \tag{17}$$

so the Eq. (15) can be rewritten as follows:

$$\tau = A_2 \cdot \exp(B_2 / T), \tag{18}$$

where the stress time, t, has been replaced with the device lifetime, τ, which is correct if ΔV_T takes the value of failure criterion. Here we note the form of Eq. (18) to be the same as that of the $1/V_G$ model given by Eq. (10). This leads to the idea of using Eq. (18), which in analogy with the $1/V_G$ model could be called a 1/T model, for extrapolation along the temperature axis so we could get the lifetime for the temperatures expected in device normal operation mode. The first step again is to extract the experimental lifetime values from the ΔV_T vs. stress time plots, but in this case we cannot use the data plots for a fixed temperature shown in Fig. 4; instead, we have to use the plots for a fixed stress voltage, such as those shown in Fig. 14. The extracted values t_j (j = 1 – 3) are then used for extrapolation along the temperature axis by means of the model given by Eq. (18). The extrapolation to T_o = 100°C in IRF9520 devices by means of the proposed model, for four different stress voltages, is illustrated in Fig. 15. As can be seen, the current procedure allows to extrapolate the lifetime to any reasonable operating temperature, as well as to estimate a new reliability parameter, which we call a ten year operation temperature, T_{10Y}, (in analogy with well-established parameter, ten year operation voltage, V_{G10Y}) and define it as a maximum temperature that allows 10 years of device operation with stress-induced ΔV_T below FC.

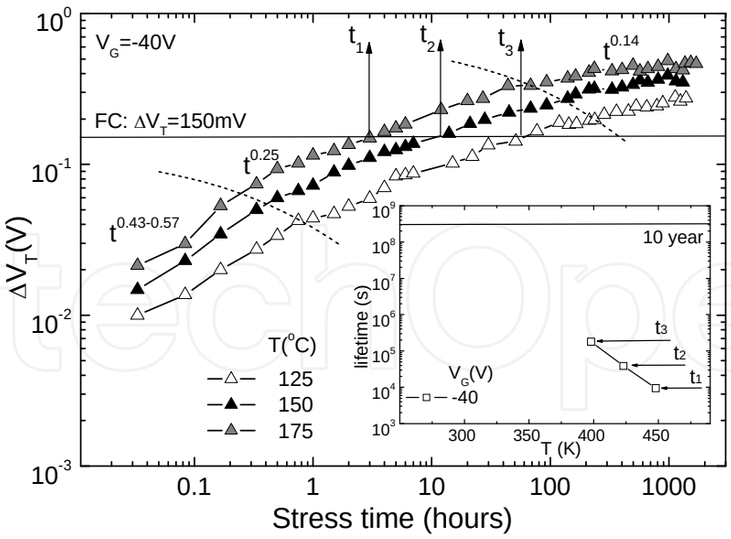


Fig. 14. Threshold voltage shifts in p-channel VDMOSFETs during the NBT stressing with V_G = - 40 V at different temperatures.

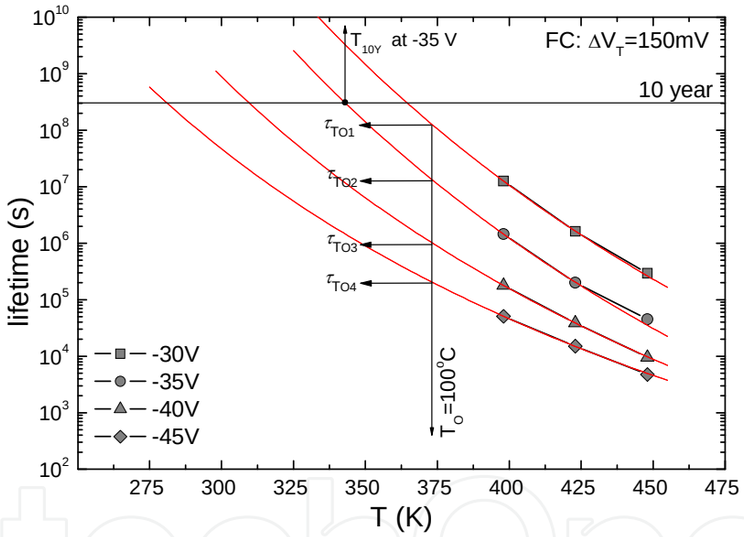


Fig. 15. Estimation of the lifetime and ten year operation temperature by 1/T model.

Thus, the proposed 1/T model offers the possibility of extrapolation to any reasonable operating temperature, but it also has a major drawback of similar nature as that of the models for extrapolation along the voltage axis. Namely, it can be seen in Fig. 15 that the above procedure yields the values of both device lifetime, τ_{Toi}, and ten year operation temperature, T_{10Yi}, (i = 1 - 4) only for the gate voltages applied during accelerated stressing, which are definitely higher than those actually found in device normal operation mode.

4.2 Double extrapolation along the voltage and temperature axes

Each of the two extrapolation procedures considered so far disregards one of the stress acceleration factors, either temperature or voltage, so both procedures may underestimate the device reliability parameters. A reasonable solution could be found by combining the

two procedures, i.e. by performing two successive extrapolations along the gate voltage (or corresponding electric field) and temperature axes, where the latter extrapolation uses the results of the former one as the input data (Danković et al, 2008a). As an example, Fig. 16 illustrates extrapolation along the temperature axis by the proposed 1/T model, where the values of τ_{VGoj} (j = 1 – 3) from Fig. 13, obtained by extrapolation along the voltage axis using the power-law model, have been taken as the input data. As can be seen, the two successive extrapolations yield a single lifetime projection, τ_o, which can be associated with devices operated under the normal conditions, both voltage, V_{Go}, and temperature, T_o. The two extrapolations can be done in reverse order as well: the τ_{Toi} (i = 1 – 4) data from Fig. 15 obtained by extrapolation to a normal operation temperature can be used for extrapolation to a normal operation voltage by power-law model, which is illustrated in Fig. 17. The two τ_o values obtained in Figs. 16 and 17 are almost identical, so the order in performing the two extrapolations does not seem to be of importance.

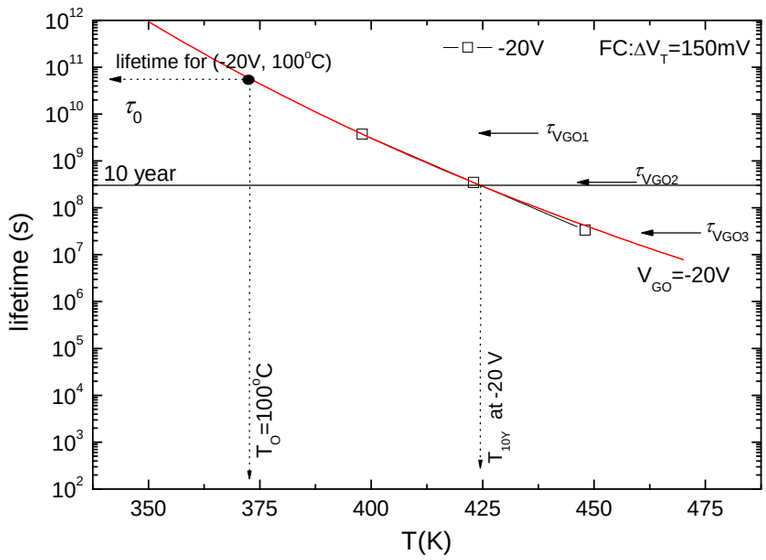


Fig. 16. Lifetime extrapolation to normal operating conditions by 1/T model with input data taken from Fig. 13.

It should be noted that power-law model has been chosen for the above consideration only to explain the proposed procedure requiring double extrapolation along both voltage and temperature axes. In practice, 1/T model for extrapolation along the temperature axis could be combined with any of the other models available for extrapolation along the voltage axis (standard linear model, V_G model, $1/V_G$ model), where the best choice should be the model that provides the best fit to the data. It is also important to note that a double extrapolation approach can be used to estimate the device lifetime for any realistic combination of operating voltages and temperatures, which is schematically illustrated by a drawing shown in Fig. 18. The drawing illustrates both extrapolation routes explained above (extrapolation along the voltage axis followed by the one along the temperature axis and vice versa) and shows the uncertainties in the estimated value of the device lifetime, which have earlier been discussed to originate from the varieties in stress conditions applied, failure criteria chosen, and models used for extrapolation to normal operating conditions. The uncertainties could be reduced if both extrapolation routes were applied in parallel, so the average of the

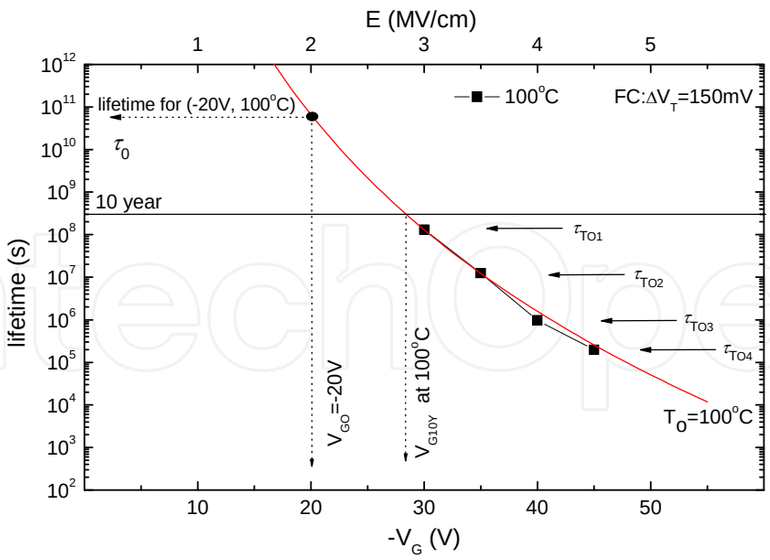


Fig. 17. Lifetime extrapolation to normal operating conditions by power-law model with input data taken from Fig. 15.

Fig. 18. Schematic drawing illustrating lifetime estimation by double extrapolation to a random combination of operating voltage, V_{GO}, and operating temperature, T_O.

two estimated lifetime values could be used. The procedure of double extrapolation, similar to that illustrated in Fig. 18, can be applied to estimate the other reliability parameters, such as the ten year operation voltage at normal operation temperature, $V_{G10Y}(T_o)$, and the ten year operation temperature under normal operation voltage, $T_{10Y}(V_{Go})$.

Finally, we will demonstrate a possibility of constructing the surface representing the lifetime values projected to a full range of operating voltages and temperatures. As already mentioned, the above double extrapolation approach can be applied to estimate the lifetime for any reasonable combination of operating voltages and temperatures (V_{Go}, T_o), which means the procedure can be re-done for each combination falling within the entire range of operating voltages and temperatures. The set of results obtained in this way can be used to construct the surface representing the lifetime values corresponding to a full range of device

operating conditions. The approach has been applied to our experimental results, and Fig. 19 shows such a surface representing lifetime projections to a full range of operation in the case of NBT stressed p-channel power VDMOS devices IRF9520, where the threshold voltage shift of 150 mV has been taken as the failure criterion. Similar surfaces can be created for different failure criteria, and can be of help in estimating either the lifetime or maximum allowed voltage and temperature for every single device in the operation environment.

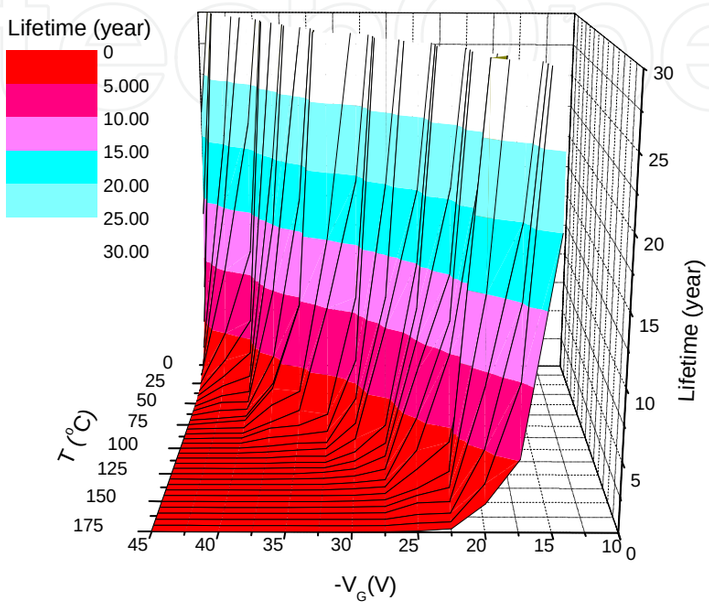


Fig. 19. Surface representing the lifetime estimates in NBT stressed devices for a full range of operating voltages and temperatures with ΔV_T = 150 mV taken as a failure criterion.

5. Conclusion

The NBT stress-induced threshold voltage instabilities in commercial p-channel power VDMOSFETs, as well as the implications of related degradation on device lifetime have been reviewed. The stress-induced threshold voltage shifts have been fitted using different models to estimate the device lifetime and to discuss the impacts of stress conditions, failure criteria, extrapolation models, and intermittent annealing on lifetime projection. Excellent agreement between the stretched exponential fit and experimental data found in later stress phases allowed for an accurate estimation of device lifetime for the lowest stress voltage applied, justifying the need for using the stretched exponential or some other suitable fitting function. The realistic failure criterion for devices and experimental conditions used in our study was found to fall in the 100 - 150 mV range. Estimated values of device lifetime were found to strongly depend on the model used for extrapolation to normal operating conditions, whereas intermittent annealing did not have any apparent impact on device lifetime. The $1/V_G$ model appeared most suited to our experimental results and allowed the use of higher stress voltages while still being capable to yield rather reliable lifetime estimates. However, $1/V_G$ and other models available in the literature offer only extrapolation along the voltage axis, so they are able to provide lifetime estimates only for

the temperatures applied during the accelerated stressing, which are generally above the temperature range observed by normally operated devices. To alleviate this issue, a new approach in estimating the device lifetime, which assumes double extrapolation along both voltage and temperature axes, was proposed. The proposed approach was shown to yield the device lifetime for any reasonable combination of operating voltages and temperatures, including those falling within the ranges normally found in usual device applications.

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This book discusses key aspects of MEMS technology areas, organized in twenty-seven chapters that present the latest research developments in micro electronic and mechanical systems. The book addresses a wide range of fundamental and practical issues related to MEMS, advanced metal-oxide-semiconductor (MOS) and complementary MOS (CMOS) devices, SoC technology, integrated circuit testing and verification, and other important topics in the field. Several chapters cover state-of-the-art microfabrication techniques and materials as enabling technologies for the microsystems. Reliability issues concerning both electronic and mechanical aspects of these devices and systems are also addressed in various chapters.

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