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Self-Aligned π-Shaped Source/Drain Ultrathin SOI MOSFETs

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1. Introduction

In this chapter, we shall study the short-channel characteristics of **self-aligned π-shaped source/drain ultrathin silicon-on-insulator metal-oxide semiconductor field-effect transistor** (SA-πFET). The only difference between conventional and proposed **ultrathin silicon-on-insulator** (UTSOI) transistors is that a path from the **source/drain** (S/D) to the **silicon** (Si) substrate is created and called the **S/D tie** (SDT). Thus, UTSOI **metal-oxide semiconductor field-effect transistor** (MOSFET) thermal performance can be enhanced drastically by opening up the SDT rather than increasing Si body thickness.

Although the path between S/D and Si substrate has degraded the device properties slightly, the short-channel characteristics of SA-πFET are within acceptable limits due to the existence of **UT body** (UTB). After changing the S/D structure in the proposed SOI transistor, the **n-channel enhancement-type MOSFET** (NMOS) current drive gets improved accordingly. Furthermore, the effects of self-heating on SA-πFET performance can be reduced greatly. This is ascribed to the fact that the forms of additional leakage paths truly help dissipate the heat generated by the thermal vibrations of the crystalline lattice phonons. For these reasons, quasi-SOI devices are strong contenders for future **complementary MOS** (CMOS) technology.

The objectives of this chapter are to describe the physical structure of the **π-shaped S/D** (π-S/D) transistor and its process, to give an understanding of why SDT design must use, and to discuss the short-channel characteristics compared with those of a conventional UTSOI. By the end of this chapter, the reader should be able to know the importance of the design of SDT.

2. Structure and process of the SA-πFET

Figure 1 shows the physical structure of the SA-πFET. Observe that the SDT has a length L_{SDT} and a location which is determined by the length of **Si nitride** (SiN) L_{SP}, two important parameters of the SA-πFET.

A simplified description of the fabrication of a SA-πFET is as follows (see Fig. 2(a)−(f)). The SOI wafer structure is used to make π-S/D transistors, which has a Si layer located on top of the **buried oxide** (BOX) and a **bulk Si** (bulkSi) substrate layer located below the oxide insulating layer. The final Si layer thickness is obtained by thermal oxidation and etching down to 5 nm. A channel implantation process is first performed with **boron difluoride** (BF_2), 2.3 KeV, 1.15×10^{12} cm^{-2}. Following this, device isolation is achieved using a traditional

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shallow trench isolation (STI) approach. A gate insulator of **Si dioxide** (SiO_2) is thermally growth and a **polycrystalline-Si** (poly-Si) layer as a gate electrode deposited by using the **chemical vapor deposition** (CVD) process is then formed. In order to form a Π-S/D scheme, the layer of SiN as hard mask is deposited by CVD. After the patterning of the gate stack (see Fig. 2(a)), a SiN layer for forming the spacer is deposited and etched back, as shown in Fig. 2(b). The sidewall spacer hard mask is used for etching Si and BOX, respectively (see Fig. 2(c)). A layer of poly-Si is deposited as SDT shown in Fig. 2(d). After the deposition and planarization of the SiO_2 layer, the etching process is performed in order to form a BOX layer under the source and drain regions (see Fig. 2(e)). The poly-Si layer is deposited, patterned, and etched to create the active region of the S/D, as shown in Fig. 2(f). Next, the S/D implantation process is carried out by **arsenic** (As), 10 KeV, 2.1×10^{14} cm^{-2}. **Rapid thermal annealing** (RTA) process is followed to activate the dopants and repair the lattice damage that is caused by the implantation process. Finally, a conventional SOI fabrication flow can be used for **back-end-of-line** (BEOL) processing.

The simulation parameters are T_{BOX} = 40 nm, T_{BOI} = 50 nm, $T_{S/D}$ = T_{Si} = 5 nm, and T_{GOX} = 1.4 nm for the Π-S/D. Various gate lengts L_G (L_{CH} – 9 nm) of 10 nm ~ 70 nm were investiaged. Notice that all the parameters of the UTSOI NMOS are equivalent to those of the Π-S/D NMOS, expect that the T_{BOX} is equal to the T_{BOI} (= 50 nm).

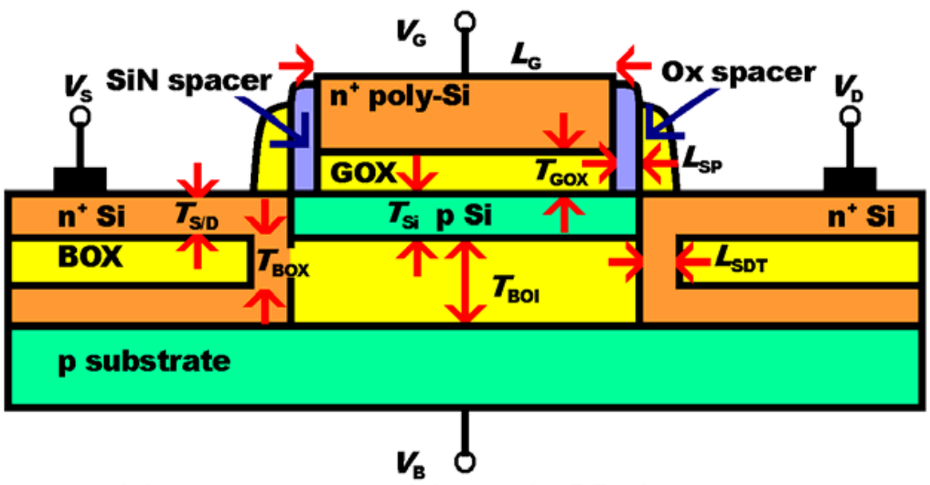
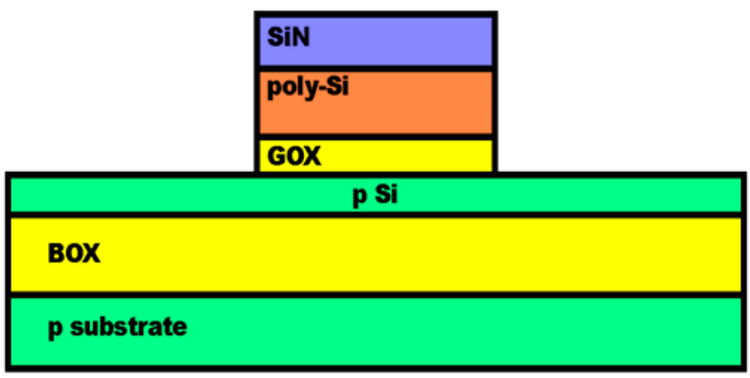
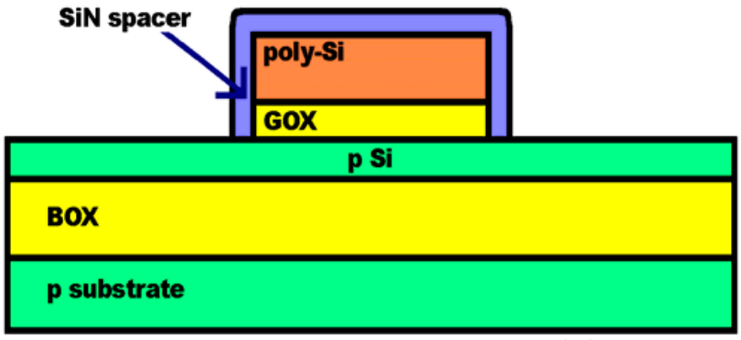


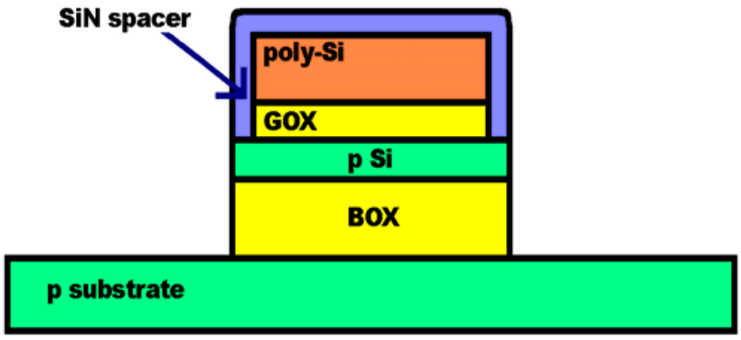
Fig. 1. Schematic cross-sectional view of an n-channel SA-ΠFET. Note that the L_{SDT} and L_{SP} are two important parameters of the SA-ΠFET.



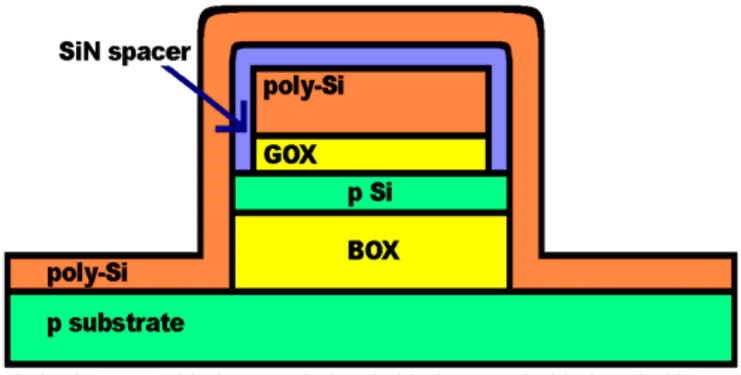
(a)


SiN spacer
poly-Si
GOX
p Si
BOX
p substrate

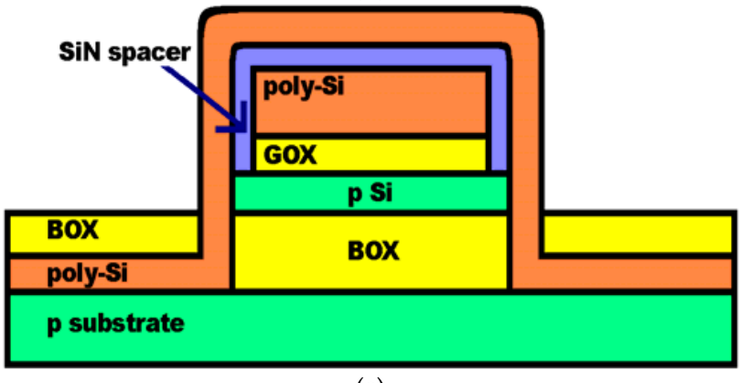
(b)


SiN spacer
poly-Si
GOX
p Si
BOX
p substrate

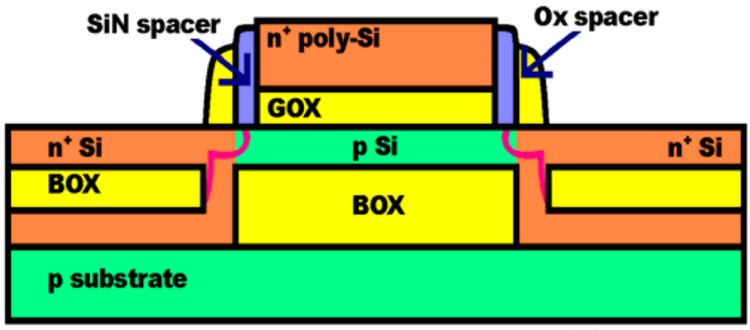
(c)


SiN spacer
poly-Si
GOX
p Si
BOX
poly-Si
p substrate

(d)


SiN spacer
poly-Si
GOX
p Si
BOX
BOX
poly-Si
p substrate

(e)



(f)

Fig. 2. The SA-ΠFET fabrication process [1], [2]; (a) gate patterning, (b) SiN spacer formation, (c) Si/BOX etch with a SiN mask, (d) poly-Si deposition, (e) formation of BOX, and (f) S/D poly-Si deposition and formation by CMP and wet etching.

3. Electrical characteristics of the SA-ΠFET

In this section, we study the physical and electrical characteristics of the SA-ΠFET. It should be clear that the design of SDT is important for scaled Π-S/D transistors. In order to control the **short-channel effects** (SCEs), a conventional UTSOI MOSFET is considered as a strong contender for replacing the position of the bulkSi in near future [3]. However, note that because the SOI family of devices has a BOX layer (which is underneath the active region), the self-heating is undesirable for the performance due to lattice scattering. As device dimensions decrease, the self-heating is more pronounced. Hence the importance of SDT in the conventional UTSOI MOSFET is growing owing to self-heating.

I_{DS}-V_{GS} characteristics of the SA-ΠFET

Figure 3 shows the drain current I_{DS} versus gate voltage V_{GS} characteristic curves of the SA-ΠFET compared with a conventional UTSOI FET. Obviously, the leakage current of a conventional UTSOI FET is lower than that of the SA-ΠFET. This means that an (SDT) additional path appended becomes an encumbrance to the UTSOI NMOS, resulting in increased p-n junction leakage current. However, the short-channel such as **drain-induced barrier lowering** (DIBL) and **subthreshold swing** (S.S.) characteristics of SA-ΠFET are within acceptable limits because of the presence of UTB. Replacing the conventional UTSOI MOSFET S/D structure with an SDT results in the slight performance degradation in the proposed SOI transistor, but the results can get accepted.

Short-channel effects in Π-S/D transistors

As shown in Fig. 4, the dependence of S.S. and **threshold voltage** (V_{TH}) on **gate length** (L_G) for both Π-S/D and UTSOI devices is compared. It is obvious in Fig. 4a that the conventional UTSOI MOSFET having a L_{SDT} = 0 nm exhibits low S.S. values. On the contrary, our proposed UTSOI structure having a L_{SDT} = 10 nm shows how the S.S. is slightly degraded. The reason is that for the Π-S/D NMOS, the SDT provides additional paths for high electric field from the drain side to influence the channel, which leads to S.S. degradation. Fortunately, the results are within acceptable limits (< 100 mV/dec at L_G = 10 nm). Fig. 4b

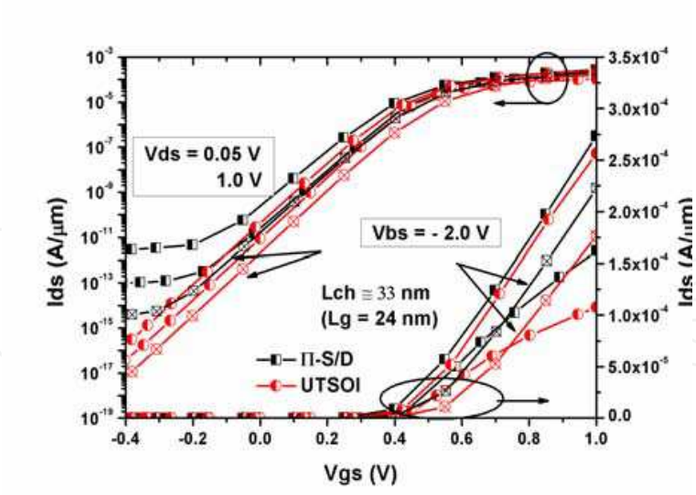


Fig. 3. Comparison of I_{DS}-V_{GS} curves between two transistors Π-S/D and UTSOI.

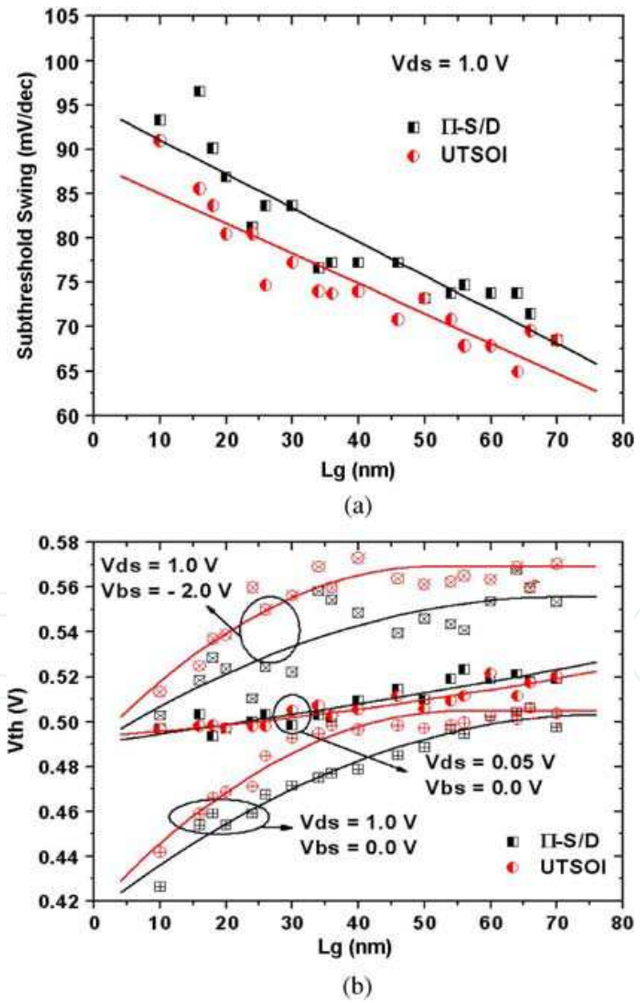


Fig. 4. Effects of the L_G on the (a) S.S. and (b) V_{TH} characteristics of the UTSOI MOSFET w/ and w/o additional SDT.

shows the impact of L_G on V_{TH}. (The intersection of the maximum and minimum slope lines in the log(I_{DS})-V_{GS} characteristic curves was used to extract the V_{TH}.) The V_{TH} is found to decrease with decrease in L_G mainly due to increased charge sharing [4]. It can be seen in figure that the saturation V_{TH} roll-off is worse than linear V_{TH}. When a **substrate bias** (V_{BS}) of – 2.0 V is applied, the V_{TH} is increased, in comparison with V_{BS} equal to 0 V. Apparently, the V_{TH} roll-off behavior of the Π-S/D transistor is quite similar to UTSOI transistor, since both devices have the same Si channel thickness.

Figure 5 shows the impact of L_G on body factor γ and DIBL. The γ was extracted using the method described in [5] ($\gamma = |\Delta V_{TH,SAT}/\Delta V_{BS}|$), which is the shift of the $V_{TH,SAT}$ caused by the change in the V_{BS}, whereas DIBL is the difference between $V_{TH,LIN}$ and $V_{TH,SAT}$. The decrease of the L_G leads to large values of γ and DIBL. This is because the short L_G has less control over the channel region, thereby increasing the **S/D subthreshold off-state leakage current** ($I_{sd,leak}$). For short channel, the V_{BS} has a large effect on $V_{TH,SAT}$. Consequently, the application of V_{BS} in $V_{TH,SAT}$ results in a large γ for short-channel devices. The DIBL of the Π-S/D NMOS is slightly larger than the UTSOI NMOS, as in the case of the S.S. shown in Fig. 4a. The DIBL is similarly impacted by the increased penetration of the fringing fields from the drain region (see Fig. 6).

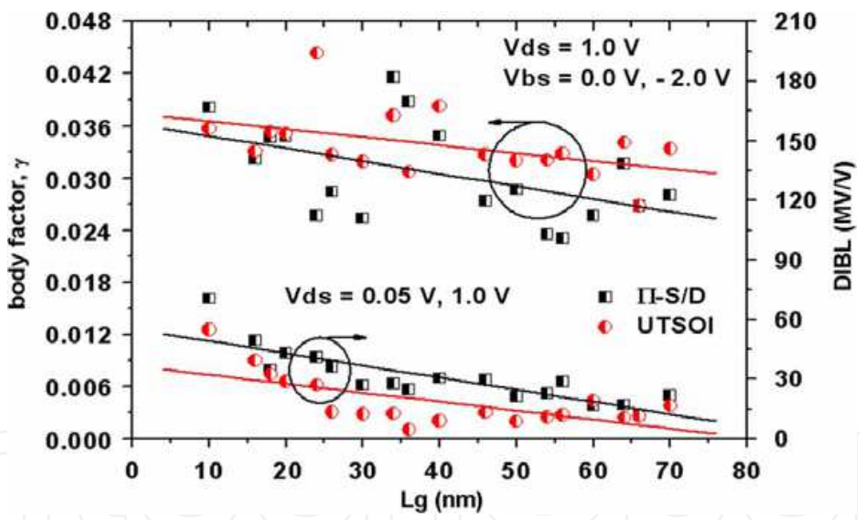


Fig. 5. Effects of the L_G on the γ and DIBL characteristics of the UTSOI MOSFET w/ and w/o additional SDT.

Moreover, we find that the **effective parasitic series S/D resistance** ($R_{S/D}$) for both devices, as shown in Fig. 7 does not decrease dramatically by reducing the L_G. Nevertheless, the Π-S/D transistor has a smaller $R_{S/D}$ compared to a conventional UTSOI transistor, which implies that the SDT added to the UTSOI structure helps increase the drain current. Thus, the additional SDT mainly contributes the $R_{S/D}$ value. Apparently, small $R_{S/D}$ leads to high drain current.

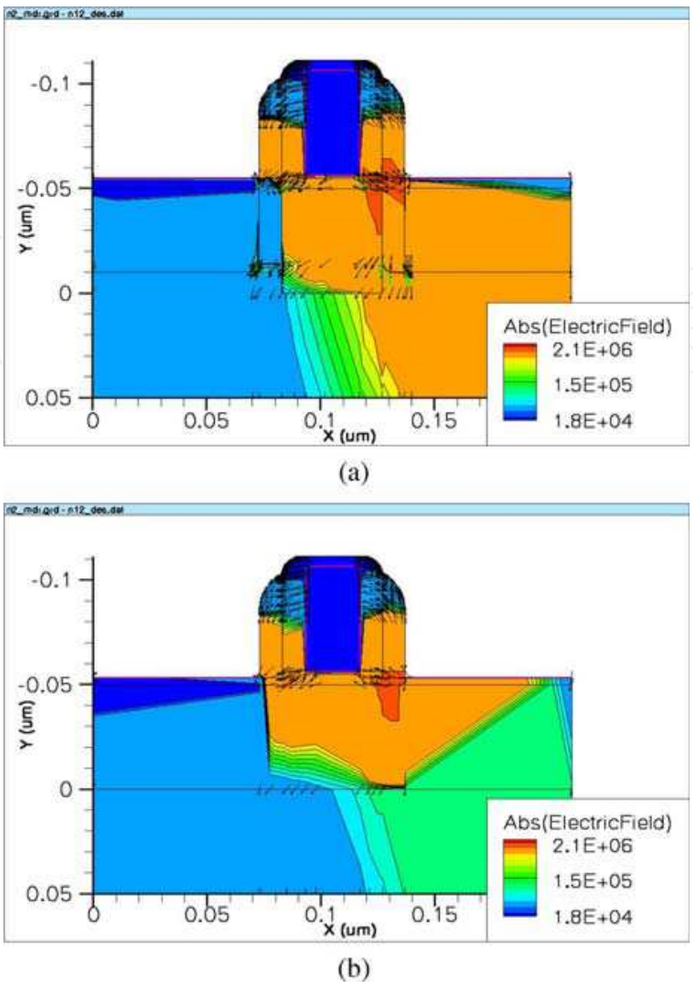


Fig. 6. Contour plot of simulated electric field (in volts per centimeter) at V_{DS} = 4.0 V and V_{GT} (V_{GS}–V_{TH}) = 1.0 V for n-channel UTSOI MOSFET w/ and w/o additional SDT. L_G = 24 nm.

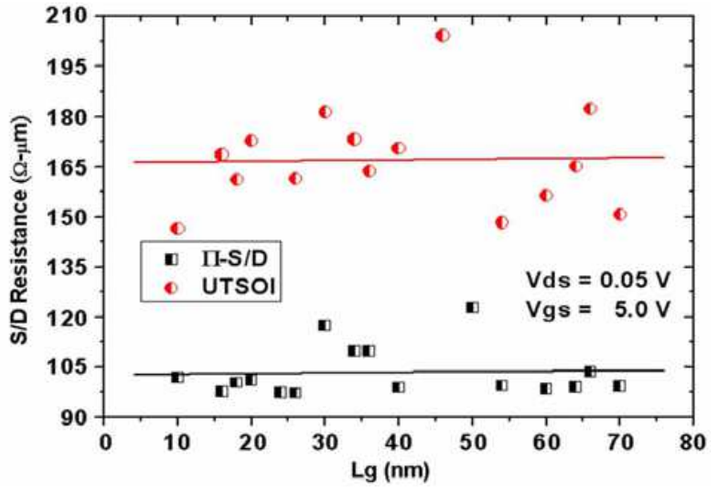


Fig. 7. Effects of the L_G on the $R_{S/D}$ characteristics of the UTSOI MOSFET w/ and w/o additional SDT.

Self-heating effects in π-S/D transistors

In order to investigate the thermal behavior of the π-S/D and UTSOI devices, the curves in Fig. 8 compare the drain current I_{DS} versus drain-to-source voltage V_{DS} for various values of gate overdrive voltage V_{GT}. When the V_{GT} increases from 0.2 V to 1.2 V, the drain-source saturation current I_{DS} also increases in both types of transistors. In addition, a self-heating induced negative differential output conductance is observed for only the UTSOI-FET. The electron mobility decreases when the local lattice temperature increases due to effects of self-heating. The SDT is shown to overcome self-heating issues. The π-S/D structure not only obtains high I_{DS} but also reduces the **self-heating effects** (SHEs). An interesting observation is that the reliability of the UTSOI MOSFET can be improved by the addition of an SDT.

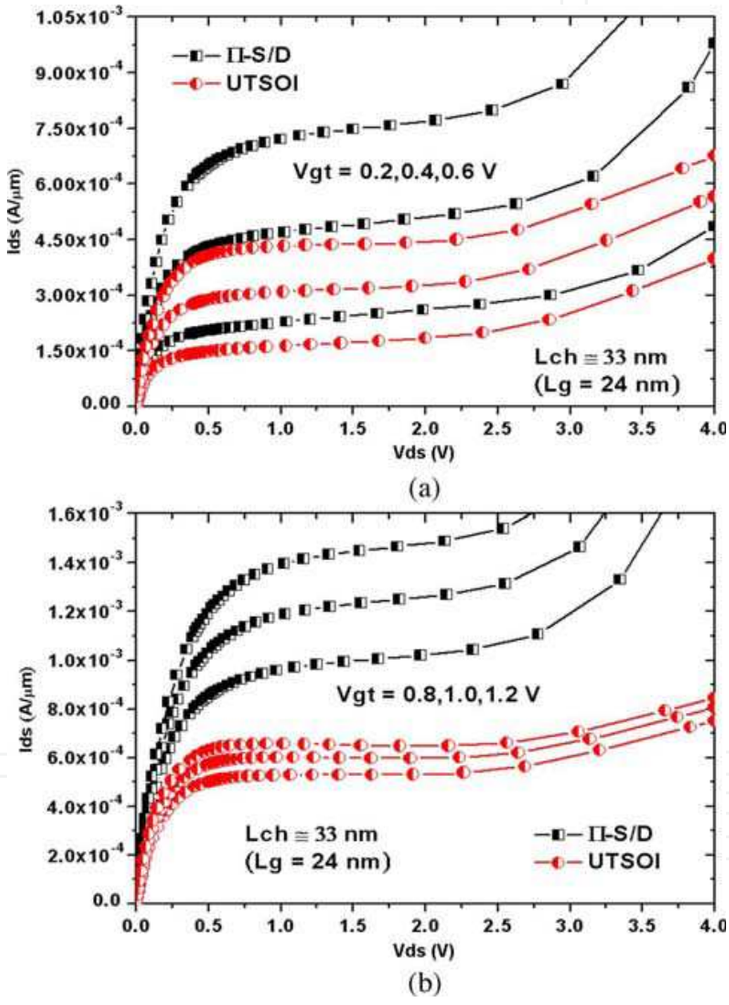


Fig. 8. Comparison of I_{DS}-V_{DS} curves between two transistors π-S/D and UTSOI.

To probe the physical mechanisms involved for improved thermal performance of the π-S/D structure, electron velocity and lattice temperature profiles for the π-S/D and UTSOI are shown in Fig. 9. It should be noticed that the generated electron-hole pair will flow through the SDT, leading to a symmetric lattice temperature near the edges of both the source and drain regions. Moreover, this is due to the fact that the Si channel is thin enough,

the generated hole carriers can flow into the ground terminal only through its source region, resulting in symmetric lattice temperature near the edges of both the source and drain regions. Since the SDT exists only in the Π-S/D NMOS, the SDT is to construct additional pathways to link Si substrate, which helps diminish the SHEs caused by the thermal vibrations. The two additional pathways can quickly disperse the heat generation in Si body, resulting in a higher electron velocity and better G_M-V_{GS} characteristics, as shown in Fig. 10. For a UTSOI MOSFET, the mobility decreases as the lattice temperature increases; this implies that the reduced electron velocity and decreased transconductance are inevitable due to self-heating.

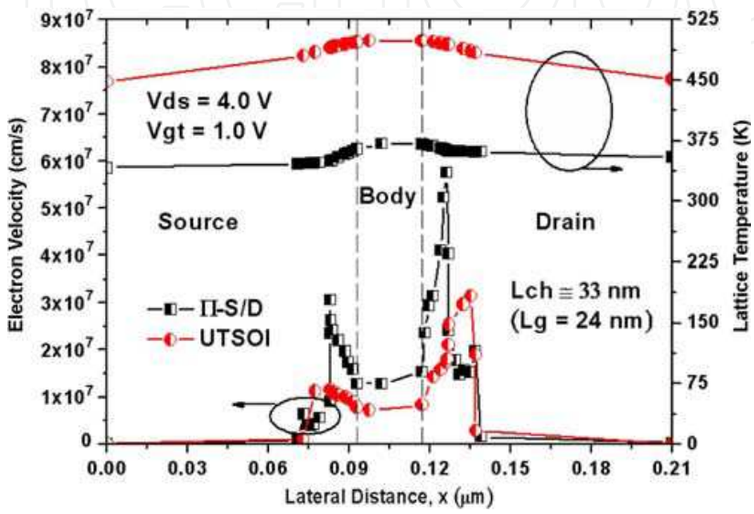


Fig. 9. Comparison of electron velocity and lattice temperature profiles between two transistors Π-S/D and UTSOI.

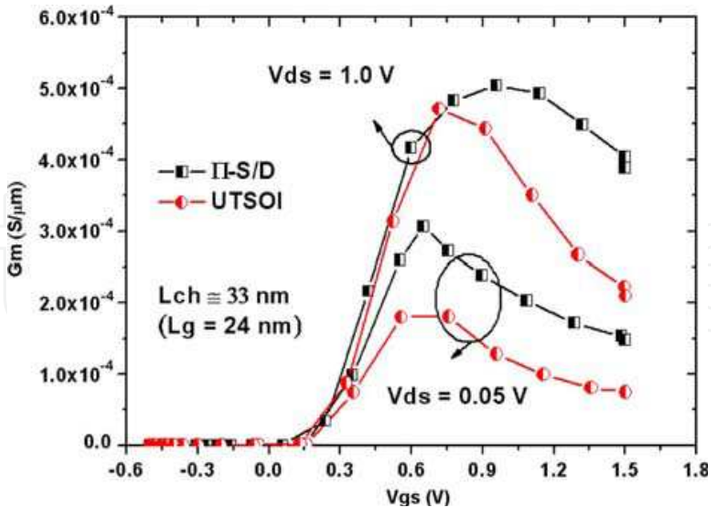


Fig. 10. Comparison of G_M-V_{GS} curves between two transistors Π-S/D and UTSOI.

In this chapter, we demonstrate a new self-aligned Π-shaped S/D UTSOI MOSFET that reduces device self-heating but without losing the desirable electrical characteristics. According to simulation results, we find that although the Π-S/D structure appears to be less advantageous in terms of the charge sharing between the gate and the S/D diffusion

regions, the source-drain current is enhanced. Additionaly, the thermal stability of the π-S/D NMOS are improved because the additional SDT increases the heat conductin area.

4. Summary

A novel UTSOI with SDT MOSFET (π-S/D transistor) is proposed, in order to reduce self-heating errors. A path from the S/D to the Si substrate is created and called SDT that which does not significantly degrade the UTSOI MOSFET characteristics due to UTB usage.
Self-heating can be reduced greatly due to the presence of the SDT. The heat generated by thermal vibration of the atoms can be quickly dissipated via SDT. Furthermore, the short-channel characteristics of **fully depleted** (FD) SOI MOSFET with SDT, such as DIBL and S.S., are not significantly degraded or impacted because the BOX layer is directly under the UTB channel region.

5. References

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