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Introductory Chapter: ASIC Technologies and Design Techniques

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1. Introduction

This chapter aims to introduce the field of application specific integrated circuits (ASICs) and provide a basic reference list of crucial design techniques for the interested student. Modern designs using complementary metal oxide semiconductor (CMOS) technologies are at the forefront of nanoscale mass fabrication with recent CMOS processing nodes pushing towards 7 nm feature sizes. While the fabrication of structures on Silicon, Germanium, Gallium Arsenide and other substrates has advanced, so too have the systems we create [1, 2]. The rapidly increasing complexity inherent in these systems – be they digital or analogue in nature – offers its own challenges for engineers. This book therefore offers a small insight into this exciting field.

Modern silicon design plays a key part in our global, highly interconnected economy and has truly allowed society to advance on several fronts.

- We now have sensors and interfaces to the real world that digitise high-speed analog signals into easily manipulated digital signals at staggeringly high sample rates, well into the GHz range [3]. Modern analog-to-digital converters (ADCs) when combined with precision, low-noise operational amplifiers (op-amps) can accurately measure nano-volt amplitude signals and can separate signals from interfering background noise using a variety of signal processing techniques. The field's prowess in analog ASICs is well exemplified by sensors and actuators that can interface directly with human brain tissue.

- Custom and general use microprocessors [4] have been a shining light of progress on complex integrated digital systems and now offer us continued growth for our increasingly complex computational needs. The improvements in super-computing are a testament to

our ongoing, field-wide interest in increasing the floating-point operations per second, while recent work aims to tackle the energy required per computation. By combining high-performance, low-power ASICs and novel computational architectures (systolic arrays, array processing, graphics processing units, etc.), super-computers and data-centres are now able to provide enough resource for a variety of high-dimensional simulation problems. So powerful are modern central processing units (CPUs) that even embedded processors can run highly-nested (i.e. deep) neural networks of many thousands of complex artificial neurons, which has directly enabled the rise of machine learning (ML), deep learning (DL) and artificial intelligence (AI). Likewise, that same computation with low-energy and high-integration progress allows many of us to have a computer within our pocket that outstrips the military and commercial computers of the 80s.

- Integrated, solid-state memory circuits [5] continue to become smaller, of higher access speed, of higher long-term reliability and of lower power, now replacing traditional hard disk drives in many front-line computing tasks. This has allowed society to store vast quantities of data and has lead – with ease of access and computation – to the rise of big data analytics and an increased interest in statistical and data-guided adaptive signal processing.

- Rapid strides in digital image sensor designs [6] now allow individual pixels of less than 900 nm in width (very close to the diffraction limit), arrays of hundreds of megapixels, sensors able to be used in 645 medium format camera systems and even the counting and timing of single-photons with sub-10 pico-second timing resolutions. Digital image sensors using various semiconductors, substrates and readout methods can image at incredibly high frame rates – well into the millions of frames/s – and over a very large portion of the electromagnetic spectrum. Telescopes such as Hubble and James Webb use these image sensor ASICs to investigate the cosmos, expanding our scientific knowledge, detecting planets orbiting distant stars and showing the innate artistry of nature. And – if this wasn't enough – digital image sensors for machine vision can be coupled with complex digital signal processing ASICs and CPUs/GPUs running neural networks to provide automatic pedestrian detection and avoidance for self-driving cars.

But the progress we have observed in each of the above sub-fields from the 1970s to present has required many difficult issues to be tackled and presents a highly interesting and challenging career for those that are interested in the design details and techniques that are required. In this chapter, Section 2 breaks the ASIC arena down into a set of sub-fields providing some key texts for each. While a little more emphasis is placed on digital circuits and CMOS optical detectors and image sensors, this is a consequence of this author's interests. To this end, Section 3 discusses some of the digital ASIC and programmable logic device hardware description languages (HDLs) that are now routinely used to develop complex systems. Finally, Section 4 discusses three key industry standards – *ISO-9001*, *ISO-26262* and *DO-254* – which emphasise the robustness and design formalism required in the industry. We also discuss the universal design methodology (UDM), which alongside modern ASIC verification standards such as the open verification methodology (OVM) and the universal verification methodology (UVM), introduce some of the key ways in which designers of ASICs can handle increasing design complexity.

2. Suggested references and reading

In this section, a wide selection of texts is references that provide significant context to the design issues inherent within ASIC technologies. The introductory text by Huber [7] provides an insight into how systems were designed during the 1990s. While this does not cover the detail of theory required for design, it introduces us to the manner, methods and tools used within the field. Generally, the below set of resources is split into the overall themes of the field: (i) planar silicon processes and solid-state physics, (ii) analogue transistors and systems, (iii) digital circuit design, and finally, (iv) sensors and interfaces to the real macro world in which we utilise these devices.

2.1. Planar silicon processes and solid-state physics

A crucial text for understanding the nature of electronics using nano-fabrication and doping of semiconductors is the work of Simon Sze [8]. This text not only discusses the way designs can be fabricated in a planar fashion using crystals of semiconductors such as Silicon, but it also introduces many of the microelectronic device structures. For example, bipolar junction transistors (BJTs) and metal-oxide-semiconductor field-effect transistors (MOSFETs) are discussed in detail. Sze undertook much of his research at Bell Telephone laboratories working alongside Walter Brattain, John Bardeen and William Shockley (the inventors of solid-state BJT and MOS transistors). His texts are crucial reading for those interested in the way electrons and holes within semiconductors can be used for analog amplification, digital switching and how semiconductors can be used as sensors.

2.2. Analog transistors, systems, sensors and interfaces

The development of integrated circuits, in particular ASICs and the field of very large-scale integration (VLSI) arguably started with the design and integration of analog circuitry within planar semiconductor manufacturing processes. The theory behind analog systems is well covered by the industry standard texts of Allen and Holberg [9] and Weste and Eshraghian [10]. While for the most part analog designs operate in terms of voltage amplitudes and the amplification, addition, subtraction, filtering and manipulation thereof, it should be noted that a current-mode approach can also be taken [11]. For the case of data communications using currents rather than voltages, authors such as Yuan [12] note that current-mode designs have advantages over their voltage-mode counterparts. As silicon also responds to light, CMOS analogue circuits have found application for many optical sensing methods [13] and of course image sensors [14]. Likewise, many other quantities such as temperature, magnetic fields (via the Hall effect) or ion-concentrations can be measured using CMOS technologies.

2.3. Digital circuit design theory

While modern ASICs – in an effort to increase the levels of system integration – often combine analog and digital circuitry, there has been significant emphasis on digital systems. Of importance for digital ASIC design, the texts by Kaeslin [15], Wakerly [16], and Weste and

Harris [17] can be considered worthwhile purchases for students. Of note, Kaeslin's book [15] covers much of the setup, hold and propagation timing issues that need to be considered during the design of circuits near the upper end of the possible clock speeds for a particular CMOS process node.

Much of the push within the digital ASIC sector has been the rapid development of high-speed digital signal processing (DSP), memory and of course microcontroller and computer architectures. Students interested in the field of DSP are suggested to read the introductory text by Lynn and Fuerst [18]. Likewise, many of the concepts discussed in the context of field-programmable gate arrays (FPGAs) by Hauck and De Hon [19], and Mayer-Baese [20], can be transferred into the digital ASIC domain. The advantage, of course, being that FPGAs offer a method of prototyping or deploying a digital circuit without the high costs associated with CMOS ASIC designs [21]. While computer architecture quickly takes steps away from the low-level details of digital computation, storage and manipulation, the de-facto references for the field are the books by Hennessy and Patterson [22]. The crucial point here is that incredibly complex systems can be created by the prudent use of modular digital designs and a suitable hierarchical design and abstraction strategy.

The languages and tools typical of the digital ASIC design industry are discussed in detail in Section 3. Suffice to say that the hardware description languages (HDLs) of Verilog [23] and VHDL [24] are crucial additions to the digital ASIC designer's repertoire of designs tools.

3. Suggested hardware description languages

While the ASICs of the past were typically drawn by hand – a highly laborious task with a high-risk factor – modern ASICs are almost exclusively developed using complex computer aided design (CAD) packages. The advantages of this are clear, first, that designs can become significantly more complex in a scalable, well maintainable and modular manner and secondly that transient, temporal, thermal, frequency domain, power, parasitic circuit elements and complex second and third order effects can be added in a manner that would not be possible from a hand calculation perspective. CAD packages allow designs to be verified against multiple specifications. Likewise, simulations based upon reliable fitted models can be used to provide such a wide range of correct and erroneous stimuli that we can obtain 99.9% test coverage and a very high expectation of full functionality prior to silicon prototyping. It is possible to run a design against multiple design corners such as low/high power, low/high temperature and fast/slow transistors, allowing simulation to capture a high proportion of likely external factors and combinations thereof.

For analog, MEMs and photonic ICs, the user typically defines the lengths and widths of transistors, silicon features (resonant beams, masses, etc.) or waveguide structures using established theoretical techniques and formulae, and then iterates around this design as the tools iteratively increase the complexities added to the base models.

Digital design now exclusively uses hardware description languages. These were initially used to describe and model digital circuits, however modern ASIC design houses use a HDL

to silicon synthesis process whereby the language describes a set of logical gates and sequential (clocked) registers that are synthesised – often via complex optimisation processes – into physical logic gates, registers and interconnections that are provided as standard cells by the CMOS foundry. This type of design entry is often called the register transfer level (RTL). The standard cells are themselves designed using the analog design flows and complex models to provide known digital performance (setup, hold and propagation times, etc.). There are two crucial HDLs used within the field. The first is Verilog [23], while the second is a very high speed integrated circuit (VHSIC) HDL, called VHDL [24]. Typically, Verilog is used for hardware descriptions that are synthesised to Silicon, while VHDL is typically synthesised to programmable devices such as FPGAs [21] and complex programmable logic devices (CPLDs). This split is however a rather grey area with a great deal of company preference. These description languages should therefore be treated as complementary.

While Verilog and VHDL have structures that comprehensively cover design concepts and the required complexity, languages such as SystemVerilog [25] and SystemC are used to provide functional verification of digital logic designs. The ASIC field would therefore write a SystemVerilog testbench that simulates a wide variety of stimuli for a digital module written in Verilog or VHDL. By doing so, we can be assured of the block's functional or logical design before we progress to more complex timing verification steps. As designs have become more complex, so have the testbenches upon which we assess a design's verifiable functionality and use case or test coverage. To handle such complexity, the digital ASIC field has shifted to a higher-level abstraction. It is here we have introduced the universal verification methodology (UVM) [26] which treats the verification of a block using a transaction-based system. The block or design-under-test (DUT) is provided with transactions that are monitored using a secondary process, with the DUT then being given a score based upon the successful completion of that transaction. For example, a two-input 16-bit adder could be given two series of random values. These would be passed through the DUT, while the monitor would compare the DUT output values with the deterministic, design-independent addition.

4. Standards and the universal design methodology (UDM)

As part of any introduction to design methods, practices and theory, we as designers must also pay attention to industry standards. While this is perhaps not given sufficient emphasis within academia, certain aspects of commercial engineering practice need to be used independent of a student's career goals. We should emphasise that students should read up on industry standards such as *ISO9001*, *ISO-26262* or *DO-254* as these will be used by the clear majority of technology companies and do in fact benefit academic projects.

4.1. Standards

Control of a design project allows us to manage both complexity and risk, while giving customers (or the generalised concept of a project's stakeholder) an assurance as to the robustness of a design. ISO-9001 "*Quality Management Systems - Requirements*" [27] defines a process model whereby tasks are suitably defined, documented and allocated based upon the

requirements of a design. The top-down flow of requirements – in complement to a top-down flow of documentation – allows the project to be traceable in terms of decisions taken and/or risk management. Likewise, it also allows design stages to be signed off after they have been demonstrated to capture all requirements and provide verification as to a design's fitness for purpose. A theme within such project management methods is the use of abstraction levels – a concept in common with electrical system design.

- During the design process, it may be necessary to modify or feedback into the previously agreed requirements of a block. While project managers may not need to know the bit-level detail as to the change, it would be crucial to discuss the changes to a project's costs or timeline to ensure that all involved in the project are clear of the implications.

- ISO-9001 [27] is routinely used throughout engineering to ensure clear communication and the management of expectations of all involved within a design. In industry, this would be hardware engineers, project managers, product marketing executives, the board of directors and of course the assurance for the end-user that their problem has been provided with a suitable solution.

For complex electrical systems, the application – for example, military/aviation, automotive or biomedical – often includes end-use standards that impact the bit-level or electrical system design process. As an example, ISO-26262 "*Road Vehicles – Functional Safety*" [28] defines – in a higher-level manner – the levels of fault and error tolerance that are required when engineers design safety critical systems. In effect, such standards seek to verify and provide assurance that no harm can be caused through poor design or to ensure that under random external fault-causes that the system behaves in a defined and predicable manner.

- One well known implication of this standard is that of redundancy within a system. For example, a set of three redundant control blocks may be created with a voting system passing the control signal to an actuator. A fault in any of the three caused by a timing or power glitch is prevented from causing erroneous action.

- Likewise, a processor responsible for the car's breaks should default to a passenger-safe state or shutdown sequence if a fault is detected within its registers via the use of bit-level parity.

- When data is transmitted – but has implications for safety – error correction codes can be used to ensure that within 99% of cases the message is interpreted correctly at the receiver. The same method also allows compliance by providing a default or shut down for the remaining cases where a message cannot be guaranteed.

DO-254 "*Design Assurance Guidance for Airborne Electronic Hardware*" [29] defines a further, stringent and often mandatory set of design directives for what it states as complex electronic systems. These are defined to be PLDs, FPGAs and ASICs. The standard sets out five (A to E) levels of compliance each related to a risk level, where the assurance is provided by verification and validation steps that fundamentally demonstrate that the quantified risk factors have been suitably mitigated and handled within the design itself. Depending on the ASIC product, these – alongside other such standards – must be met.

4.2. Universal design methodology

While the universal design methodology (UDM) [30] is often applied to FPGA-based hardware design, it is applicable to a wide range of electronics projects including both analog and digital ASIC designs. The power of the UDM model is its ability to fit well with the existing structures and processes of ISO-9001, while also enforcing a robust formalism in the design process. The pathway within UDM, shown in **Figure 1**, includes multiple opportunities for the design to be specified and constrained in a top down manner, while also providing suitable feedback loops to ensure designs meet all specifications without undue over-engineering. UDM also includes multiple signing off and review processes, each with the purpose of finalising, verifying and capturing issues as early as possible as the design moves towards implementation and shipping. In this way, once the design is passed to physical (gate-level) implementation, i.e. synthesis to Silicon or even custom analog layout, designers should never encounter a new requirement to add a separate reset line, a new state within an initialisation or control state machine or modify the block's frequency domain specification.

UDM contains a significant emphasis on design verification at all stages. For example, the functional simulation of a HDL coded design is used with the design specification to ensure the design both captures all design intent within the specifications and is verifiably functionally correct and in agreement with the agreed (via review) list of specifications. Likewise, once the HDL design is synthesised to Silicon, it is formally verified via gate-level simulation or emulation on a programmable logic platform, to ensure that it meets all timing requirements and that no issues are present using a constrained random approach to testing. Part of the verification task is to demonstrate functional equivalence between the design simulated, verified and agreed upon in previous stages with the computer optimised design that was synthesised. The final review within UDM is crucial as it is at this point that all involved in the design, from marketing and product management right down to hardware and software engineers sign-off the design and prepare for manufacture and final testing of the product. UDM can therefore be instrumental in achieving agreement between professionals of highly
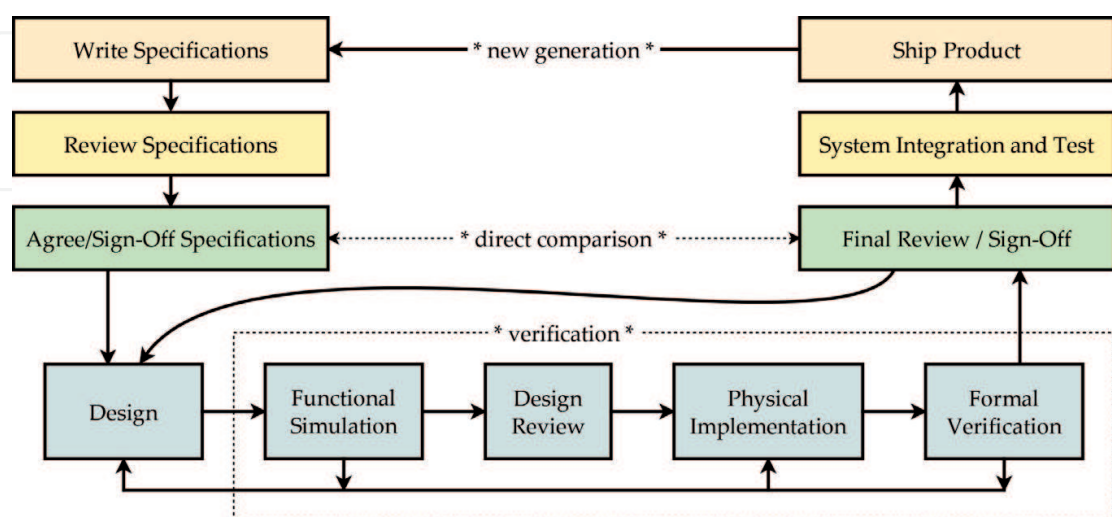
Figure 1. The universal design methodology (UDM), with an emphasis on multiple sign-off processes within the design flow and functional and final design verification against agreed specifications.

disparate backgrounds and provides a mechanism whereby a bit-level hardware design has a proven track record and verifiable performance against a set of high-level requirements.

It should be noted that ASIC design tool vendors such as Cadence and Synopsis include many sign-off checks that complement the sign-off and review steps in UDM. For example, design rule checks (DRC) and layout-versus-schematic (LVS) checks were developed such that a design is not passed to manufacture or any other stage until verifiably passed and the "green light" given. Many CMOS foundries will not fabricate a design or require extensive waivers before allowing the tape-out of an IC with known DRC errors.

5. Conclusions

The design of digital, analog, and sensing ASICs is an exciting but complex field. The references and texts provided are intended as an introductory reading list. Of course, once a student has an idea of a sub-specialty they wish to pursue, they can delve far more deeply. Alongside introducing the different areas within ASIC design, some key industry standards are discussed. Students are encouraged to engage with ISO-9001 as early as possible. This is simply prudent planning for a career within robustly managed engineering projects. Finally, a design flow called the universal design methodology was briefly covered, which emphases the need for agreement as to requirements and scope, along with verification of the design throughout the lifecycle of a complex design.

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References

[1] Daly D, Fujino L, Smith K. Through the looking glass—The 2017 edition: Trends in solid-state circuits from ISSCC. IEEE Solid-State Circuits Magazine. 2017;**9**(1. Winter):12-22

[2] Daly D, Fujino L, Smith K. Through the looking glass—The 2018 edition: Trends in solid-state circuits from the 65th ISSCC. IEEE Solid-State Circuits Magazine. 2018;**10**(1. Winter):30-46

[3] Harpe P. Successive approximation analog-to-digital converters: Improving power efficiency and conversion speed. IEEE Solid-State Circuits Magazine. 2016;**8**(4. Fall):64-73

[4] Faggin F. The making of the first microprocessor. IEEE Solid-State Circuits Magazine. 2009;**1**(1. Winter):8-21

[5] Klein D. The history of semiconductor memory: From magnetic tape to NAND flash memory. IEEE Solid-State Circuits Magazine. 2016;**8**(2. Spring):16-22

[6] Theuwissen A. Better pictures through physics. IEEE Solid-State Circuits Magazine. 2010;**2**(2. Spring):2-28

[7] Huber J, Successful ASIC. Design the First Time Through. New York, United States: Springer. 1991. ISBN-13: 978-1468478877

[8] Sze S. Semiconductor Devices: Physics and Technology. 2nd ed. New Jersey, United States: John Wiley & Sons; 2001. ISBN-10: 0-471-33372-7

[9] Allen P, Holberg D. CMOS Analog Circuit Design. 3rd ed. Oxford, United Kingdom: Oxford University Press; 2012. ISBN-13: 978-0199937424

[10] Weste N, Eshraghian K. Principles of CMOS VLSI Design: A Systems Perspective. 2nd ed. London, United Kingdom: Pearson; 1993. ISBN-13: 978-0201533767

[11] Toumazou C, Lidgey F, Haigh D, editors. Analogue IC Design: The Current-Mode Approach. London, United Kingdom: Institution of Engineering and Technology (IET); 1990. ISBN-13: 978-0863412158

[12] Yuan F. CMOS Current-Mode Circuits for Data Communications. New York, United States: Springer; 2007. ISBN-13: 978-1441939999

[13] Fisher E. Principles and early historical development of silicon avalanche and Geiger-mode photodiodes. In: Britun N, Nikiforov A, editors. Photon Counting. 1st ed. Rijeka: InTechOpen; 2018. ISBN-13: 978-9535157755

[14] Durini D, editor. High Performance Silicon Imaging: Fundamentals and Applications of CMOS and CCD Sensors. 1st ed. Sawston, United Kingdom: Woodhead; 2014. ISBN-13: 978-0857095985

[15] Kaeslin H. Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication. Cambridge, United Kingdom: Cambridge University Press; 2008. ISBN-13: 978-0521882675

[16] Wakerly J. Digital Design: Principles and Practices. 5th ed. London, United Kingdom: Pearson; 2018. ISBN-13: 978-0134460093

[17] Weste N, Harris D. CMOS VLSI Design: A Circuits and Systems Perspective. London, United Kingdom: Pearson. ISBN-13: 978-0321269775; 2004

[18] Lynn P, Fuerst W. Introductory Digital Singnal Processing with Computer Applications (Revised Edition). Chichester, United Kingdom: John Wiley & Sons; 1998. ISBN-13: 978-0471976318

[19] Hauck S, DeHon A, editors. Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation (Systems on Silicon). 1st ed. Burlington, United States: Morgan Kaufmann Publishing; 2010. ISBN-13: 978-9380931869

[20] Mayer-Baese U. Digital Signal Processing with Field Programmable Gate Arrays. 4th ed. New York, United States: Springer; 2014. ISBN-13: 978-3642453083

[21] Trimberger S. Three ages of FPGAs: A retrospective on the first thirty years of FPGA technology. IEEE Solid-State Circuits Magazine. 2018;**10**(2. Spring):16-29

[22] Hennessy J, Patterson D. Computer Architecture: A Quantitative Approach. Burlington, United States: Morgan Kaufmann Publishing; 2017. ISBN-13: 978-0128119051

[23] Ranachandran S, Digital VLSI. System Design: A Design Manual for Implementation of Projects and ASICs Using Verilog. New York, United States: Springer; 2007. ISBN-13: 978-1402058288

[24] Rajan S. Essential VHDL: RTL synthesis done right. F. E. Chicago, United States: Compton Co; 1998. ISBN-13: 978-0966959000.

[25] Thomas D. Logic Design and Verification Using SystemVerilog (Revised). CreateSpace Independent Publishing. ISBN-13: 978-1523364022; 2016

[26] Salemi R. The UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology. 1st ed. Boston, United States: Boston Light Press. ISBN-13: 978-0974164939; 2013

[27] International Organization for Standards. ISO-9001: Quality Management Systems: Requirements [Internet]. 2015. Available from: https://www.iso.org/iso-9001-quality-management.html [Accessed: 30-12-2018]

[28] International Organization for Standards. ISO26262: Road Vehicles—Functional Safety [Internet]. 2018. Available from: https://www.iso.org/standard/68383.html [Accessed: 02-01-19]

[29] Radio Technical Commission for Aeronautics (RTCA). DO-254: Design Assurance Guidance for Airborne Electronic Hardware [Internet]. 2000. Available from: https://www.rtca.org/content/about-us-overview [Accessed: 30-12-18]

[30] Zeidman B. Chapter 4: Universal design methodology for programmable devices (UDM-PD). In: Designing with FPGAs and CPLDs. 1st ed. Florida, United States: CRC Press; 2017. ISBN-13: 978-1138436442