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# Porous Low-Dielectric-Constant Material for Semiconductor Microelectronics

*Yi-Lung Cheng and Chih-Yen Lee*

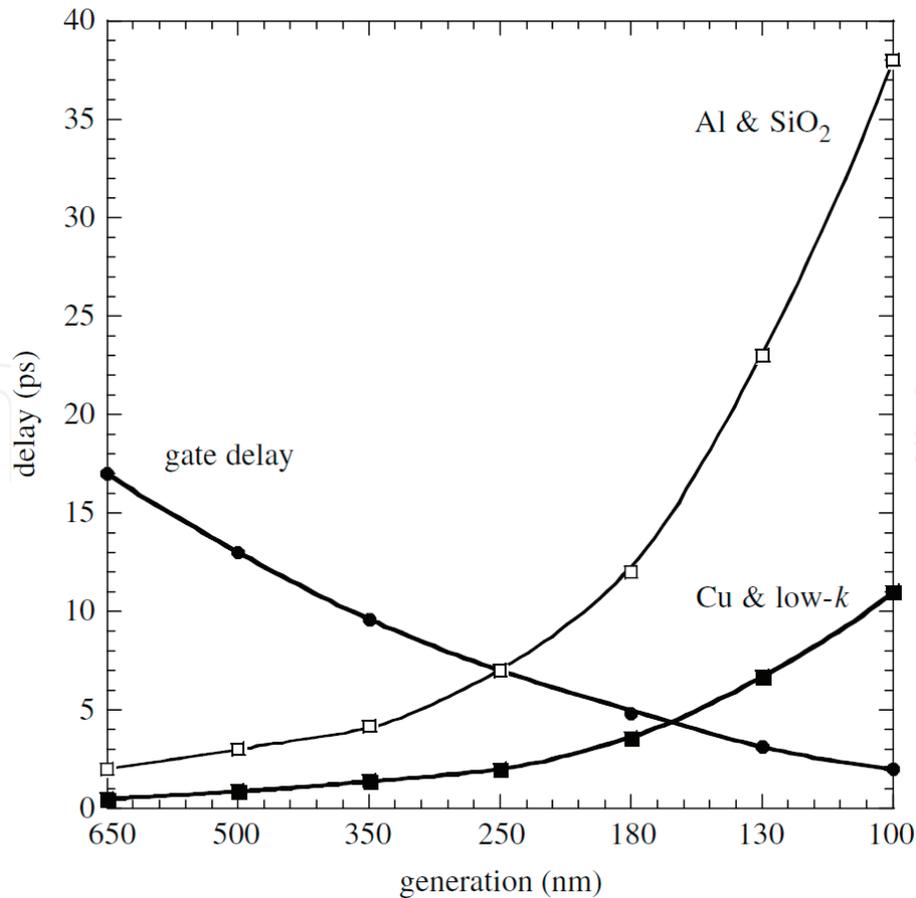
## Abstract

To provide high speed, low dynamic power dissipation, and low cross-talk noise for microelectronic circuits, low-dielectric-constant (low- $k$ ) materials are required as the inter- and intra-level dielectric (ILD) insulator of the back-end-of-line interconnects. Porous low- $k$  materials have low-polarizability chemical compositions and the introducing porosity in the film. Integration of porous low- $k$  materials into microelectronic circuits, however, poses a number of challenges because the composition and porosity affected the resistance to damage during integration processing and reduced the mechanical strength, thereby degrading the properties and reliability. These issues arising from porous low- $k$  materials are the subject of the present chapter.

**Keywords:** porous low- $k$ , porosity, Cu interconnects, BEOL, integration, plasma damage, Cu drift, TDDB, reliability

## 1. Introduction

To obtain a high operation performance and to pack more chips in microelectronics, the semiconductor industry spent a lot of efforts to accomplish successful integration of the integrated circuits (ICs). As the dimensions of the device are continuously shrinking with the advance of technology node, the carrier's transit time across the length of a transistor channel (called gate delay) decreases, while the signal propagation through the interconnects [called resistance-capacitance (RC) delay] increases, as shown in **Figure 1**. As a result, the effective speed of the device is limited by the RC delay since 0.25  $\mu\text{m}$  technology node [2–4]. The RC delay can be reduced by using metals with low resistivity and dielectric materials with low dielectric constant ( $k$ ). Therefore, copper (Cu) and low-dielectric-constant (low- $k$ ) materials have been introduced in back-end-of-line (BEOL) interconnects of ICs to replace the conventional Al/SiO<sub>2</sub> interconnects [4–7]. Cu with a resistivity of 1.7  $\mu\Omega\text{-cm}$  (2.7  $\mu\Omega\text{-cm}$  for Al) is becoming the common metallization material. Low- $k$  materials with  $k$  values lower than 4.0 ( $k$  value of SiO<sub>2</sub>) provide lower capacitance between wires. To effectively reduce the  $k$  value of a dielectric film, low-polar bonds and porosity are introduced into the film. The produced dielectric materials are called porous low- $k$  materials [8–10]. To provide a further low- $k$  value, more porosity is introduced into the low- $k$  material; however, more integration challenges arise.



**Figure 1.** Gate and interconnect delay with technological generation (International Technology Roadmap for Semiconductors [1]).

This chapter is an attempt to provide an overview of porous low- $k$  materials. The resulting issues and reliability during the integration of porous low- $k$  material in Cu interconnects are discussed.

## 2. Low- $k$ dielectric materials and deposition method

### 2.1 Low- $k$ dielectric materials

The dielectric constant ( $k$ ) of a dielectric material is generally described by Clausius-Mossotti Eq. (1):

$$\frac{k - 1}{k + 2} = \frac{4\pi N}{3} \alpha \quad (1)$$

where  $k = \epsilon/\epsilon_0$ ,  $\epsilon$ , and  $\epsilon_0$  are the permittivity of the material and vacuum,  $N$  is the number of molecules per unit volume (density), and  $\alpha$  is the total polarizability, including electronic ( $\alpha_e$ ), distortion ( $\alpha_d$ ), and orientation ( $\alpha_o$ ) polarizabilities. According to Eq. (1), decreasing the total polarizability ( $\alpha$ ) and/or density ( $N$ ) is the feasible method to effectively reduce the  $k$  value of a dielectric material. Reducing the polarizability can be achieved by the use of low-polar bonds (like C-C, C-H, Si-F, Si-CH<sub>3</sub>, etc.). Based on the used type of the low-polar bond, the produced low- $k$  dielectric material can be divided into two types: One type is organic polymer that contains saturated and unsaturated and conjugated and aromatic hydrocarbons [11]. However, this type low- $k$  dielectric material is thermally unstable and has poor

mechanical strength and relatively high coefficient of thermal expansion (CTE). As a result, the successful integration into the BEOL interconnects is still not achieved.

The other type is hybrid silica-based low- $k$  dielectric material, which is the mainstream inter-layer-dielectric (ILD) insulator used in BEOL interconnects. This type of low- $k$  dielectric material can be produced by doping fluorine or/and carbon into the traditional SiO<sub>2</sub> film. The formation of low- $k$  dielectric materials are fluorinated silicon glass (FSG) [11, 12] or carbon-doped silicon glass [SiCOH or called organosilicate glass (OSG)] [11, 13]. Fluorine or carbon substitution lowers the  $k$  value by decreasing the polarizability and increasing the free volume.

The minimum  $k$  value of the hybrid silica-based low- $k$  dielectric material is limited to be 2.6–2.7. To prevent a huge increase in the parasitic capacitance of BEOL interconnects in the 45 nm or below technology nodes, a new low- $k$  dielectric material with  $k$  value less than 2.6 is required. The air has a minimum  $k$  value of  $\sim 1.0$  in the world; as a result, the introduction of air pores in the existing low- $k$  dielectric film is the possible strategy to further reduce the  $k$  value. The produced low- $k$  dielectrics are porous, which are called “porous low- $k$  dielectrics” [14, 15]. The  $k$  value of porous low- $k$  dielectrics depends on the porosity and dielectric constant of the film skeleton ( $k_2$ ) [16]:

$$\frac{k-1}{k+2} = V \frac{k_1-1}{k_1+2} + (1-V) \frac{k_2-1}{k_2+2} \quad (2)$$

where  $k_1$  is the dielectric constant of the material inside the pores and  $V$  is the average pore volume. The first term in the right side of Eq. (2) equals to zero if the air is inside the pore ( $k_1 \sim 1.0$ ). As a result, porous low- $k$  dielectrics with relatively small  $k_2$  value and higher porosity can provide much lower  $k$  value. Currently, porous low- $k$  dielectrics have been successfully integrated into Cu interconnects since 45 nm technology node. The widely used method to produce the porous low- $k$  dielectrics is co-deposition of a silica-like matrix together with a sacrificial organic polymer (porogen) using plasma-enhanced chemical vapor deposition (PECVD). Following, the sacrificial organic polymer in the deposited low- $k$  dielectric material is removed by ultraviolet (UV)-assisted thermal curing at a temperature range of 300–450°C in order to form the pores in the film. The precise composition and porosity depend on the type of precursor molecules, the matrix/porogen ratio used during deposition, and the curing conditions [17, 18].

## 2.2 Deposition method for porous low- $k$ materials

Porous low- $k$  dielectric materials can be produced by either spin-on technology or chemical vapor deposition (CVD) method [14, 15, 17–20]. In the CVD method, the deposition rate of CVD method is strongly dependent of the deposition temperature. To obtain a suitable deposition rate, increasing the deposition temperature is required to deposit the porous low- $k$  dielectric material. However, the temperature of BEOL interconnects is limited to be less than 450°C because of melting concern for metal conductors. With an assistant of plasma technology, the deposition precursors are dissociated to form the active radicals under the electron collision in the cold plasma. The generated active radicals with high reactivity accelerate the deposition process, thus reducing the deposition temperature.

### 2.2.1 Spin-on technology

Spin-on technology has been used in semiconductor processing for photoresist coating. It can also use to deposit the low- $k$  dielectric material. The used dispensing

liquid contains the deposition precursors for low- $k$  materials, which is dropping into the center of the substrate. The created centrifugal forces by rotating of the substrate help to distribute the material on the surface. After the spinning step, a heating (or bake) is required to remove solvent. The temperature is typically below 250°C. Finally, a curing at temperatures varying from 350 to 600°C is required to obtain a stable film.

There are two methods to introduce the porosity into the film to produce porous low- $k$  dielectric materials by spin-on technology. One is through sol-gel process, and the other is formed through the use of sacrificial particles (porogens) that are desorbed during the curing process. In the sol-gel process, the formation of subtractive porosity can be achieved by two approaches: the aging process and the hierarchical organization of the primary particles in the sol (self-assembly) [21, 22]. The other method is the use of sacrificial porogens, in which molecular or supra-molecular particles are added in the low- $k$  dielectric precursor with the purpose of tailoring the thermal stability. In the final curing process, these added molecular particles are removed by pyrolysis effect. The detailed description about spin-on technology to form porous low- $k$  materials can be found elsewhere [23].

### *2.2.2 PECVD technology*

PECVD is a complex process, involving a wide variety of scientific and technical principles, including gas-phase reaction chemistry, thermodynamics, heat and material transfer, fluid mechanics, surface and plasma reactions, thin film growth mechanism, and reactors engineering. During the deposition process, the active intermediates and structural units are formed in the gas phase and then absorbed in the solid substrate. Finally, they migrate and react to form the matrix of the growing layer [11].

In the current semiconductor industry, the production of the porous low- $k$  dielectric material is relied on PECVD technology because the formation material is more thermally stable and the  $k$  value can be lower than 2.0. The subtractive porosity approach is the widely accepted method. In this method, a low- $k$  (generally is SiCOH) skeleton precursor mixed with a porogen precursor is introduced into the reactor during the deposition. After the deposition, a dual-phase SiCOH-CH<sub>x</sub> material is formed after the deposition. Tetramethylcyclotetrasiloxane (TMCTS), octamethylcyclotetrasiloxane (OMCTS), decamethylcyclopentasiloxane (DMCPS), and diethoxymethylsilane (DEMS) are the widely used skeleton precursors [24–27]. These skeleton precursors have a common property with a sufficiently low dissociation level under rf power in order to keep the sufficient hardness for the produced porous low- $k$  dielectric material. The porogen precursor is organic molecule with sufficient volatility. Unsaturated cyclic hydrocarbons like terpinenes or norbornenes, linear alkenes, or molecules with strained rings like cycloalkene oxides or butadiene monoxide are the commonly used porogen precursors [11, 28].

Following, it is necessary to remove the labile organic fraction C<sub>x</sub>H<sub>y</sub> from the as-deposited SiCOH-C<sub>x</sub>H<sub>y</sub> film to form pores in the film. Thermal annealing, electron beam, or ultraviolet (UV) irradiation methods are provided to remove the labile organic fraction C<sub>x</sub>H<sub>y</sub> [29–31]. To reach better removal efficiency, it can be done by UV-assisted curing. However, the temperature of the curing has to be limited at ~400°C. The mechanical strength (elastic modulus and hardness) of the porous low- $k$  dielectric material can also be improved by UV-assisted curing because the UV curing can rearrange and enhance the cross-linking of the skeleton of the low- $k$

material by breaking a fraction of mainly the Si-CH<sub>3</sub> (Si-Me) bonds. The improvement effect is associated to the used wavelength, temperature, and time of the UV curing [32, 33].

Currently, a promising method to deposition of the porous low-*k* dielectric film is using a single precursor molecule consisting of skeleton with embedded (or grafted) porogen precursor. An example of such a porous SiCOH material is Applied Materials' Black Diamond 3 (BD3) dielectric film. The UV curing is also modified to create more uniform porosity and improve the mechanical properties [8, 33].

### 2.3 Characterizations of porous low-*k* dielectric materials

In order to successfully integrate the porous low-*k* dielectric material into Cu interconnects, their physical, chemical, mechanical, and electric properties are important consideration factors. **Table 1** lists the main characterization techniques for porous low-*k* dielectric materials. Detailed principles and operation procedures can be found elsewhere [34, 35].

**Table 2** lists the main properties of porous low-*k* dielectric materials and compares to other generations of ILD materials (including SiO<sub>2</sub>, FSG, and OSG) [36–38]. In addition to providing a lower *k* value, porous low-*k* dielectric materials possess the degrading material properties. The degradation is more pronounced with increasing porosity (for the reduction of *k* value) for porous low-*k* dielectric materials. Therefore, the use of porous low-*k* dielectric materials in the ICs is becoming more challenging.

Characteristics	Characterization techniques	Properties
Physical	Spectroscopic ellipsometry (SE)	Thickness, Refractive index
	X-ray reflectivity (XRR)	Density, Thickness
	transmission electron microscopy (TEM)	Microstrurure, Thickness
	Atomic force microscopy (AFM)	Surface roughness
Chemical	X-Ray Photoelectron Spectroscopy (XPS)	Composition, Chemical bonding
	Rutherford backscattering spectroscopy (RBS)	Composition
	Fourier transform infrared spectroscopy (FTIR)	Composition, Chemical bonding
	electron energy loss spectroscopy (EELS)	composition, Chemical bonding
	Nuclear magnetic resonance (NMR)	Composition, Bonding structure
Mechanical	Nanoindentation.	Hardness, Elastic modulus
	sandwich structure four-point bending (SS4PB)	Adhesion
	modified-edge liftoff test (m-ELT)	Adhesion
	Ccross-section nanoindentation (CSN)	Adhesion
Pore structure	Positron annihilation lifetime spectroscopy (PALS, PAS)	Pore size
	Scattering techniques (SANS, SAXS)	Pore size, Porosity
	Adsorption techniques (BJH, EP)	Pore size, Porosity
Electrical	Mercury probe measurements	Dielectric constant
	Metal/dielectric/metal (MIM) or metal/dielectric/Si (MIS)	Dielectric constant, Leakage, TDDB
	Comb-comb or Comb-serpentine structures	Leakage, TDDB

**Table 1.**  
 Characterization techniques for porous low-*k* dielectric materials.

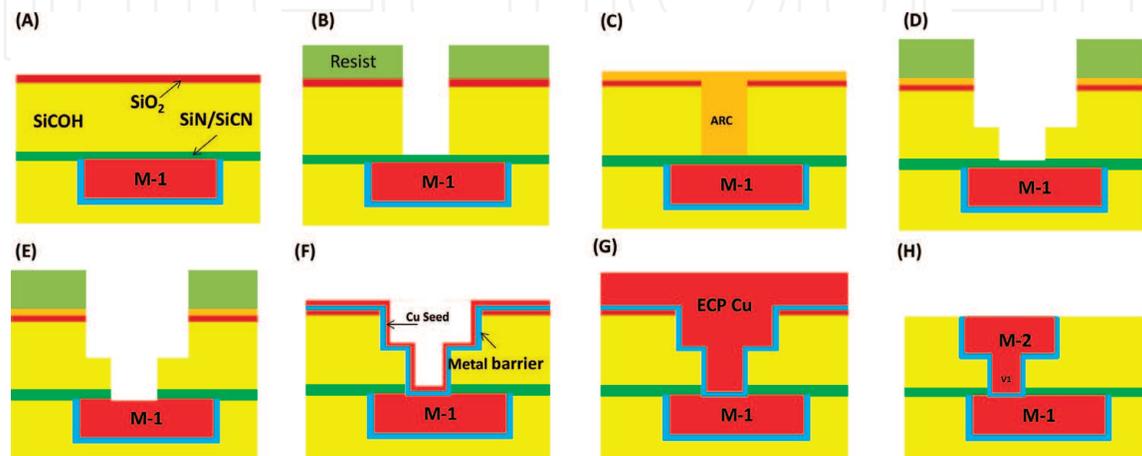
Properties	SiO <sub>2</sub>	FSG	Dense low-k (OSG)	Porous low-k
Density (g/cm <sup>3</sup> )	2.2	2.2	1.8~1.2	1.2~1.0
Dielectric constant (k)	4	3.5~3.8	2.8~3.2	1.9~2.7
Modulus (Gpa)	55~70	~50	10~20	3~10
Hardness (GPa)	3.5	3.36	2.5~1.2	0.3~1.0
CTE (ppm/K)	0.6	~0.6	1~5	10~18
Thermal Conductivity (W/mK)	1.0	1.0	~0.8	0.26
Porosity (%)	NA	NA	<10	25~50
Average Pore Size (nm)	NA	NA	<1.0	2.0~10
Breakdown Filed (MV/cm)	>10	>10	8~10	<8

**Table 2.**  
Properties of various dielectric materials.

### 3. Integration of porous low-k dielectric materials in Cu interconnects

As Cu metallization replaced Al metallization in BEOL interconnects, the fabrication process was also switched to damascene approach from metal etching approach because the Cu etching formation compounds are hardly volatile at low temperature or the etch rate is relatively slow [39]. In the damascene patterning process, a dielectric is firstly etched, and then a Cu metallization is filled and polished. To prevent Cu diffusion and improve the adhesion with the dielectric layer, a barrier is required to surround the Cu wire [40, 41].

Dual-damascene patterning process is widely used to fabricate BEOL interconnects. In this method, both trench and via are patterned in a dielectric film simultaneously, and Cu metallization is filled into both trench and via. Compared to single-damascene patterning process, this method can reduce the processing step of Cu metallization. According to the order of via and trench patterning, dual-damascene patterning process has two types: “Via first” and “Trench first” processes [42, 43]. Generally, “Via first” dual-damascene process is widely used, plotted in Figure 2.

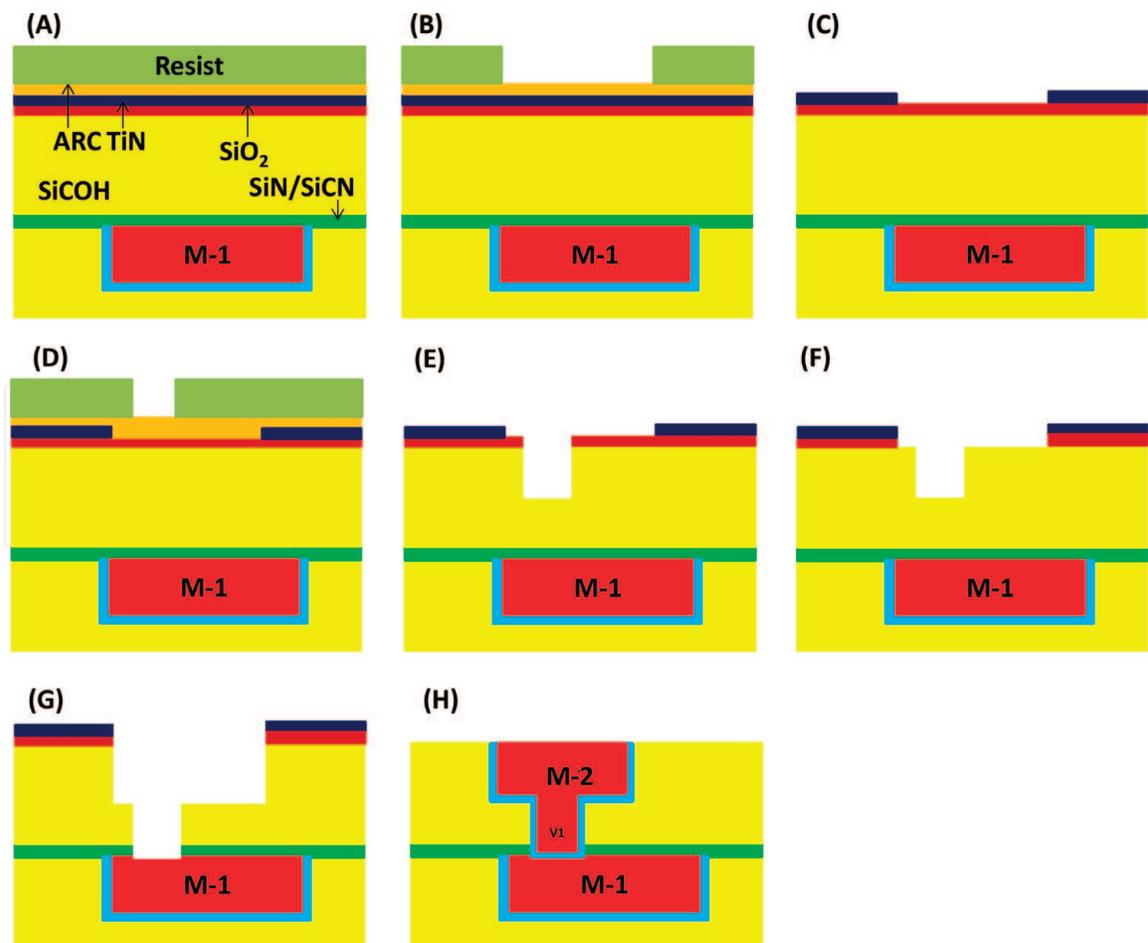


**Figure 2.**  
Via first dual-damascene patterning process: (A) Dielectrics (SiN/SiCN, SiCOH, SiO<sub>2</sub>) deposition. (B) Via-1 lithography and RIE. (C) ARC plug. (D) M-2 trench lithography and RIE. (E) Etching stop layer opening. (F) Metal barrier and Cu seed deposition. (G) Electroplating Cu deposition. (H) Cu CMP.

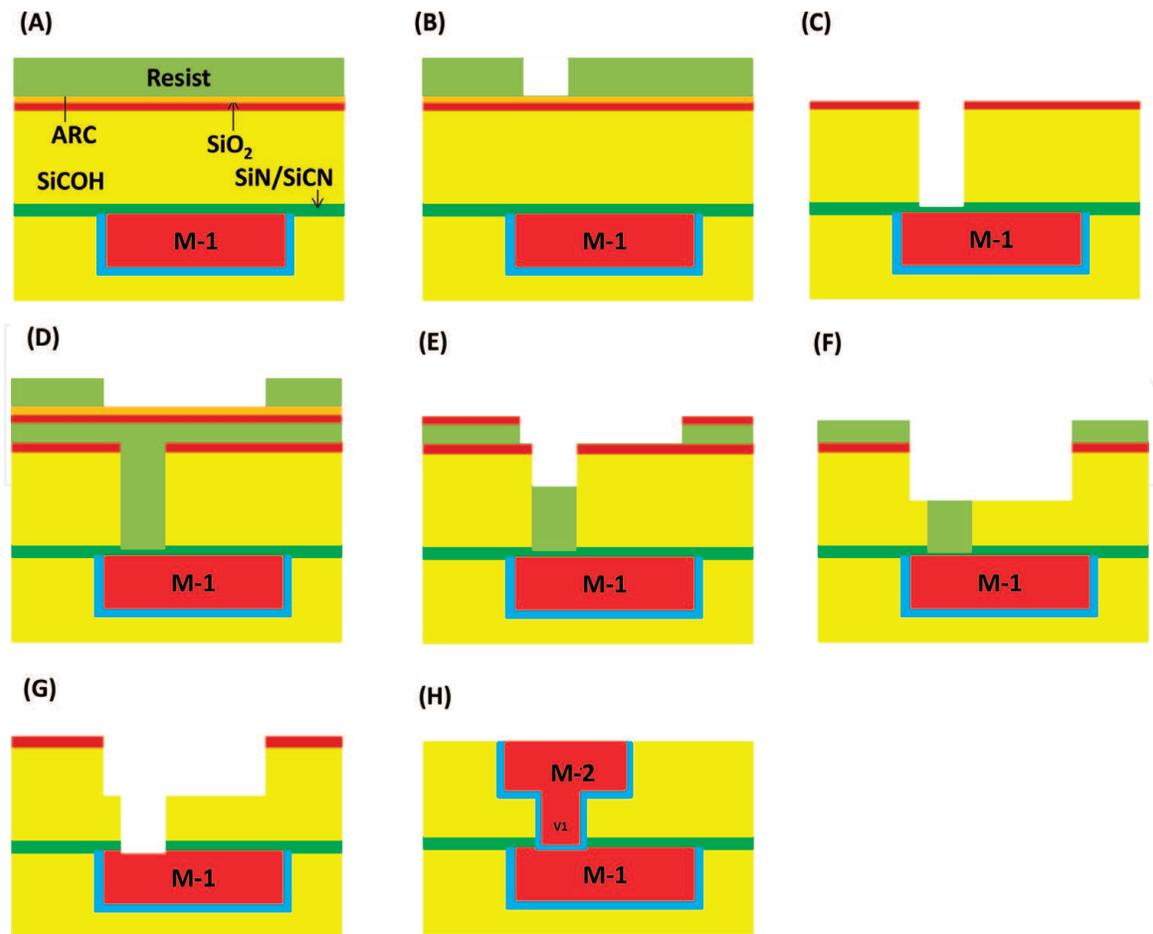
During the fabrication of BEOL interconnects, the used porous low- $k$  dielectric material as an interconnecting insulator undergoes dielectric deposition, photoresist, etching, stripping, Cu metallization deposition, and chemical mechanical polishing (CMP) processes. Plasma damage, moisture/chemicals adsorption, Cu diffusion, and mechanical stress occurred on the porous low- $k$  dielectric materials. These issues would reduce the electrical characteristics and reliability of the porous low- $k$  dielectric materials. The mechanism and the resulting effect will be discussed in the following section.

In order to reduce the plasma-induced damage and pattern small features, the metal hardmask method and the multilayer resist method, as plotted in **Figures 3** and **4**, respectively, are proposed since 32 nm technology node [44–46]. In the metal hardmask process, the resist is stripped prior to the trench and via etching into the porous low- $k$  ILD; therefore, resist-stripping process-induced damage can be minimal. However, the polymer may remain on the sidewalls of the trenches during the trench etching step. The remaining polymer must be removed without damaging the porous low- $k$  dielectric material. Additionally, the stress in the metal layer must be minimized to avoid pattern deformation after the etching process. Metal residues can form on the etched surfaces and block etching of the porous low- $k$  dielectric material.

In the advanced technology nodes, the multilayer resist method is preferred because it has an advantage to pattern small features. However, the porous low- $k$  dielectric material is fully exposed to the resist strips. In order to avoid



**Figure 3.** Metal hardmask dual-damascene patterning process: (A) TiN, ARC, and resist deposition. (B) M-2 metal hardmask RIE. (C) M-2 trench lithography. (D) Via-1 lithography. (E) Via-1 RIE. (F) M-2 oxide hardmask RIE. (G) M-2/Via-1 RIE and M-1 capping layer RIE. (H) M-2/Via-1 Cu metallization.



**Figure 4.** Multilayer resist dual-damascene process: (A) ARC and resist coating. (B) Via-1 lithography. (C) Via-1 RIE. (D) Multilayer resist coating and M-2 trench lithography. (E) LTO and OPL RIE. (F) M-2 trench RIE. (G) OPL strip and M-1 capping layer RIE. (H) M-2/Via-1 Cu metallization.

plasma-induced damage on the porous low- $k$  dielectric material, low-plasma-damage resist-stripping process is required for the multilayer resist method.

## 4. Electrical and reliability characteristics of porous low- $k$ dielectric materials

As porous low- $k$  dielectric materials are used in the BEOL interconnects, the change in the  $k$  value during the integration must be minimal. Additionally, the electrical properties and reliability are the most important concerns. As a result, the leakage current of the porous low- $k$  dielectric between metal lines should be maintained low. The time-dependent dielectric breakdown (TDDB) failure time of the integrated BEOL structure at operating conditions should meet the specifications.

### 4.1 Conduction mechanisms in porous low- $k$ dielectrics

In a crystalline solid, as the electrons overcome the bandgap (or called energy gap), the resulting current is detected. The bandgap is defined as the difference between the energy of the lowest conduction band and that of the highest valence band. For thermally deposited SiO<sub>2</sub> dielectric film, the bandgap is around 8.9 eV [47]. As carbon is doped into SiO<sub>2</sub> dielectric film to form SiOCH low- $k$  dielectric

material, the bandgap was determined to be between 8.0 and 10.0 eV, depending on the low- $k$  dielectric types and the characterization techniques [48–50]. If the carbon content in the low- $k$  dielectric film is not incorporated in the matrix network but primarily exists as terminal methyl groups, its bandgap is similar to that of SiO<sub>2</sub> film. However, if the carbon content is present in the network bonds by forming Si-C-Si bridging structure, the bandgap value would drop dramatically. As porosity is introduced into the SiOCH low- $k$  dielectric material, the bandgap of porous SiOCH low- $k$  dielectrics ( $k = 2.0$ – $3.3$ ) is in the range between 7.5 and 10 eV [51]. The effect of porosity on the bandgap of porous SiOCH low- $k$  dielectrics is not pronounced. More investigation about bandgap determination for porous low- $k$  dielectric materials is required.

The conduction mechanisms of low- $k$  dielectric materials are commonly described by Schottky emission (SE), Poole-Frenkel (PF) emission, and Fowler-Nordheim (FN) tunneling [52–54], as shown in the following Eqs. (3)–(5):

- Schottky emission (SE)

$$J_{SE} = A^*T^2 \exp \left[ -q \left( \frac{\phi_{SE} - \sqrt{qE/4\pi\epsilon_0\epsilon_r}}{kT} \right) \right] \quad (3)$$

- Poole-Frenkel (PF) emission

$$J_{SE} \sim E \exp \left[ -q \left( \frac{\phi_{PF} - \sqrt{qE/4\pi\epsilon_0\epsilon_r}}{kT} \right) \right] \quad (4)$$

- Fowler-Nordheim (FN) tunneling

$$J_{FN} \sim E^2 \exp \left[ \frac{-8\pi\sqrt{2m^*}(q\phi_{FN})^{3/2}}{3qhE} \right] \quad (5)$$

where  $J$  is current density,  $A^*$  is Richardson constant,  $T$  is temperature,  $q$  is the elementary charge,  $\phi$  is barrier height,  $E$  is electric field,  $\epsilon_0$  is permittivity of free space,  $\epsilon_r$  is dielectric constant,  $m^*$  is effective electron mass, and  $h$  is Planck's constant.

SE and PF emissions are field-enhanced thermal excitation conduction models. The excited electrons enter the conduction band from the low- $k$  interface and the trap states with coulomb potentials for SE and PF emissions, respectively. FN tunneling conduction is caused by electrons tunneling from the metal Fermi energy or trapping sites in the material itself into the low- $k$  dielectric conduction band. SE and PF emission currents are associated with the field and temperature. The former exhibits a strong temperature dependency. However, FN tunneling current exhibits a strong field dependency and is independent of temperature. Generally, PF emission is more likely the dominant conduction mechanism in low- $k$  dielectric materials, especially at low fields. At high field, the dominant conduction mechanism transfers to FN tunneling [55, 56].

In the integrated interconnects, the barrier height at both the low- $k$ /metal and the low- $k$ /Si interfaces is around 4 eV, and the barrier height at the etching-stop layer/metal interface is less than 2.0 eV [57]. Therefore, the interface-controlled SE emission occurs.

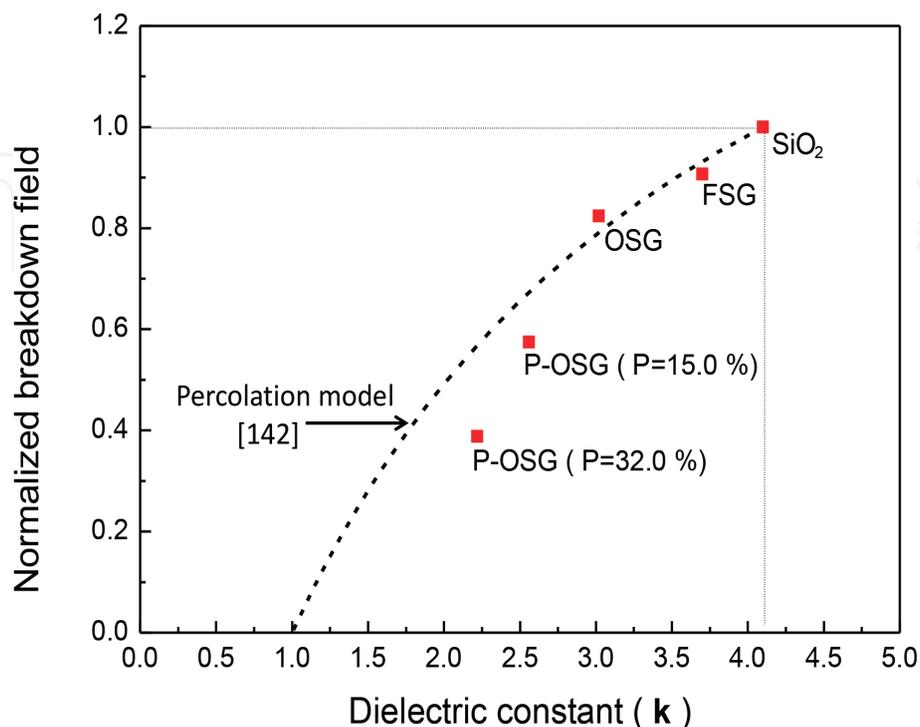
## 4.2 Reliability of porous low- $k$ dielectric materials

The breakdown field and TDDB failure time are the main reliability items for a dielectric material [58, 59]. **Figure 5** plots the relatively breakdown field of various dielectric materials used as BEOL ILDs. Compared to other dielectric materials, the porous low- $k$  dielectrics have relatively weak breakdown field, and the decreasing magnitude is amplified with increasing the porosity [60]. The pores in the porous low- $k$  dielectrics are treated as defective cells, shortening the percolation path. Additionally, porous low- $k$  dielectrics have weaker bonds, higher trap densities, or lower barrier heights at the metal–insulator interface.

TDDB testing is performed by applying an electric stress on a tested dielectric material for a period of time. The stressing field is lower than the breakdown field of the tested dielectric material. The leakage current is monitored with the stressing time. During the electric stress, electric damage occurs in a dielectric material, converting the resistance state of a dielectric material from high to low. This leads to the loss of the insulating properties for a dielectric material. As a conducting path between a dielectric is formed, the leakage sharply increases. Therefore, the dielectric breakdown occurs. This stressing time is defined as the breakdown time of a dielectric material.

TDDB is strongly related to the property of a tested dielectric film and the applied electric field. As a result, as the technology node advances to 45 nm or below technology nodes, TDDB is becoming a critical reliability issue. In addition to using porous low- $k$  dielectrics with a lower breakdown field, the interconnect dimensions are reduced which increases the lateral electric field across the BEOL dielectric. However, in real Cu damascene interconnects, the integration performance strongly dominates TDDB results. The interface of Cu/capping layer, line-edge-roughness line-to-line overlay errors, and via-to-line misalignment are the dominated TDDB failure mechanisms [61–65].

Typically, TDDB testing is done at high fields (voltages) to accelerate the test. To predict lifetime from high voltage/field conditions to operating conditions,



**Figure 5.**  
*Relative breakdown field of various dielectric films.*

Model	Life-time	Mechanism
E	$A \exp(-\gamma E)$	Field-assisted bond breakage
1/E	$A \exp(\gamma/E)$	Fowler-Nordheim injection
$E^{1/2}$	$A \exp(-\gamma E^{1/2})$	Poole-Frenkel or Schottky
Power-law	$AV^{-n}$	Very thin dielectric (<3 nm)

A: Pre-exponential factor.  
 E: Applied electric field.  
 $\gamma$ : Field acceleration factor.  
 n: Power law exponent.

**Table 3.**  
 TDDB lifetime models for dielectric materials.

TDDB lifetime model is required and critical for prediction. The commonly used TDDB lifetime models are summarized in **Table 3** [66–68]. Each TDDB lifetime model has its theoretical fundamentals, but cannot explain all observed TDDB phenomenon. Moreover, for the choice of TDDB lifetime model, it is necessary to consider that the breakdown mechanism under testing conditions is also the dominant mechanism under operating conditions.

In these used TDDB lifetime models, E, 1/E, and power-law models are field-driven models, while  $E^{1/2}$  model is a current-driven model. Moreover, E model is the most conservative model because it gives the shortest dielectric lifetime in the lower-field conditions, and 1/E model is the optimistic model providing the longest predicted lifetime. The  $E^{1/2}$  mode is widely accepted TDDB lifetime model for porous low-*k* dielectrics.

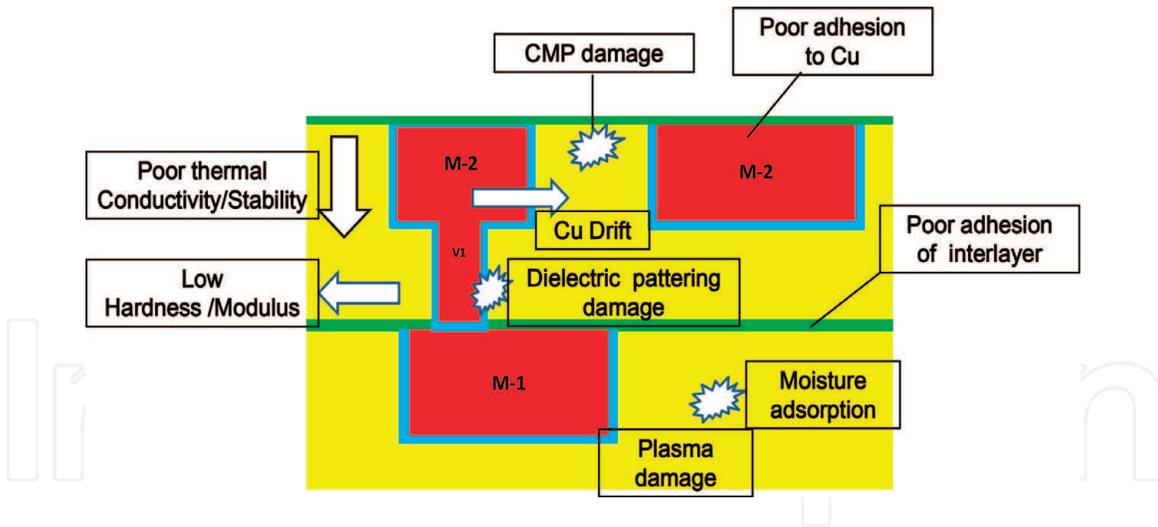
## 5. Integration issues of porous low-*k* dielectric materials

During the integration of porous low-*k* dielectrics into Cu interconnects, the fabricating processes can seriously degrade material properties, electrical characteristics, and reliability. Moreover, the porosity can act as a fast penetration media for reactive species or contamination during the integration, accelerating degradations.

The main key issues associated with porous low-*k* dielectrics are schematically shown in **Figure 6**. The key issues will be discussed and the improvement actions will be provided in this section.

### 5.1 Plasma-induced damage

Plasma is an aggressive medium which produces vacuum ultraviolet (VUV) and ultraviolet (UV) photons, energetic ions, electrons, and highly reactive radicals [69]. Exposure to plasma causes physical damage and chemical modifications on porous low-*k* dielectric materials [70, 71]. Under plasma irradiation, Si-CH<sub>3</sub> and Si-H groups in the porous SiCOH low-*k* dielectric material are extracted from the network and then converted into the Si-O or Si-OH groups, leading to densification

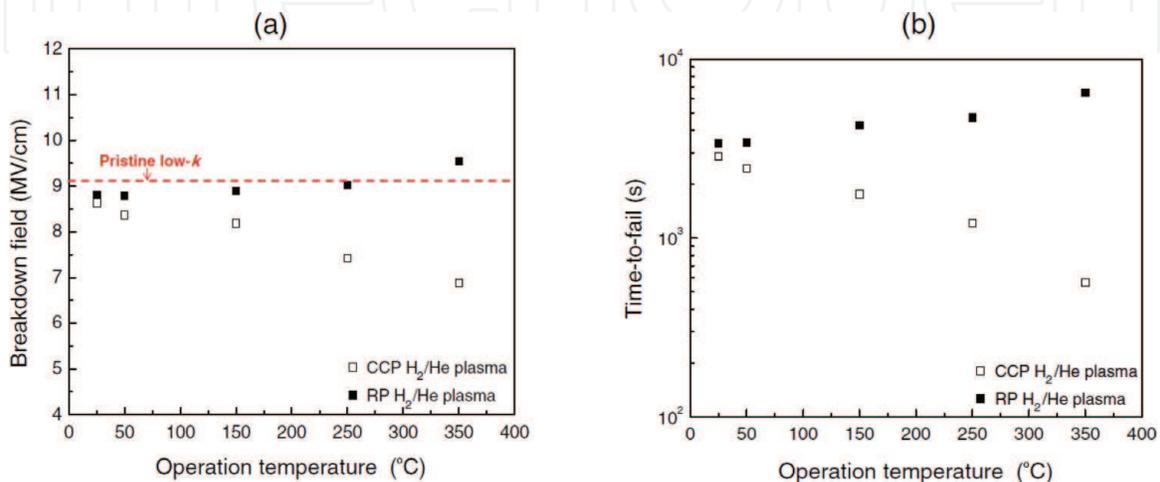


**Figure 6.**  
Main integration issues of porous low- $k$  dielectrics in BEOL interconnects.

and  $k$ -value increase. Moreover, plasma-induced damage makes porous low- $k$  dielectric materials hydrophilic from hydrophobic, facilitating moisture uptake.

Plasma-induced damage on the porous low- $k$  dielectric materials depends on the porosity, the used plasma reactors, power, and gas [72–76]. Therefore, for porous low- $k$  dielectric materials that are irradiated under a plasma with higher density, inductively coupling plasma (ICP) reactor, or  $O_2$  plasma, more damage on low- $k$  dielectrics is expected.

To minimize the plasma-induced damage on the porous low- $k$  dielectric materials,  $H_2$ -based plasma in remote-plasma (RP) system is an alternative for resist-stripping process. [77–81]. **Figure 7(a)** and **(b)** exhibits the breakdown field and TDDB failure time (TTF) of the porous low- $k$  dielectric film after  $H_2/He$  plasma treatment [80, 81]. For porous low- $k$  dielectric films operated in RP system, a higher breakdown field and a longer TTF were observed as compared to those operated in capacitance coupling plasma (CCP) system. In the RP system, neither deep UV light radiation nor ion bombardment is acted on the porous low- $k$  dielectric film, mitigating plasma-induced damage. Additionally, the trends of temperature dependence of reliability characteristics are different for  $H_2/He$  plasma treatments in the CCP and RP systems. The breakdown field and TTF of  $H_2/He$  plasma-treated porous low- $k$  dielectric film in CCP system decrease, while those in CCP system improve with increasing of the operation temperature. Moreover, as



**Figure 7.**  
(a) Breakdown field. (b) Time-to-fail of  $H_2/He$  plasma-treated porous low- $k$  dielectric films operated in CCP and RP systems as a function of operation temperature [81].

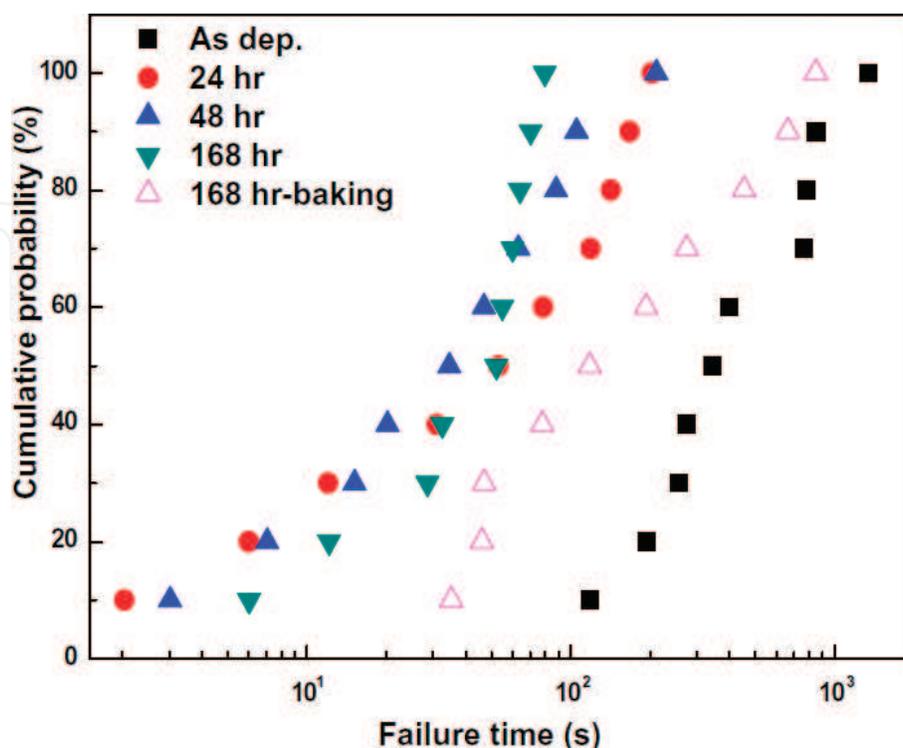
the operation temperature of H<sub>2</sub>/He plasma treatment in RP system is increased to 350°C, the plasma-treated porous low-*k* dielectric films have better reliability than the pristine samples. The improvement mechanism is attributed to the removal of carbon-based porogen residues from the porous low-*k* dielectric film by H<sub>2</sub>/He plasma treatment at 350°C [82].

The dielectric property of the plasma-damaged low-*k* dielectrics can be recovered by applying silylation agents such as hexamethyldisilazane (HMDS), trimethylchlorosilane (TMCS), and dichlorodimethylsilane (DMDCS), depositing hydrophobic agents from hydrocarbon plasma and using a thermal treatment to eliminate the adsorbed hydroxyl (OH) groups and the physisorbed water [83–86].

## 5.2 Moisture uptake

During the integration processing, the porous low-*k* dielectric films are damaged and are transferred to be hydrophilic. The hydrophilic surface tends to uptake moisture in subsequent process steps. Due to a high *k* value of water (~80), only a small amount of moisture adsorption in the low-*k* dielectric film increases the effective *k* value significantly [87]. As the porosity increases in the porous low-*k* dielectric film, the pores connect each other to form “open pores,” which serve as the fast diffusion path for moisture. The adsorbed moisture degrades reliability performance of porous low-*k* dielectric films, as shown in **Figure 8** [88]. The TDDB failure time is reduced by a factor of approximately 10 for the moisture-uptake low-*k* dielectric film and slightly decreases as the moisture immersion time increases. An annealing step is demonstrated to remove moisture and improve the film reliability, as also presented in **Figure 8**. However, even with thermal annealing at 400 C for 1 h, TDDB performance was only partially restored, being poorer than that of the fresh sample.

As the moisture is adsorbed in the low-*k* dielectric film, there are two types: physisorbed and chemisorbed moisture [89]. The physisorbed moisture starts to be



**Figure 8.** Cumulative probability of TDDB failure times of porous low-*k* dielectric films as functions of the moisture immersion time [88].

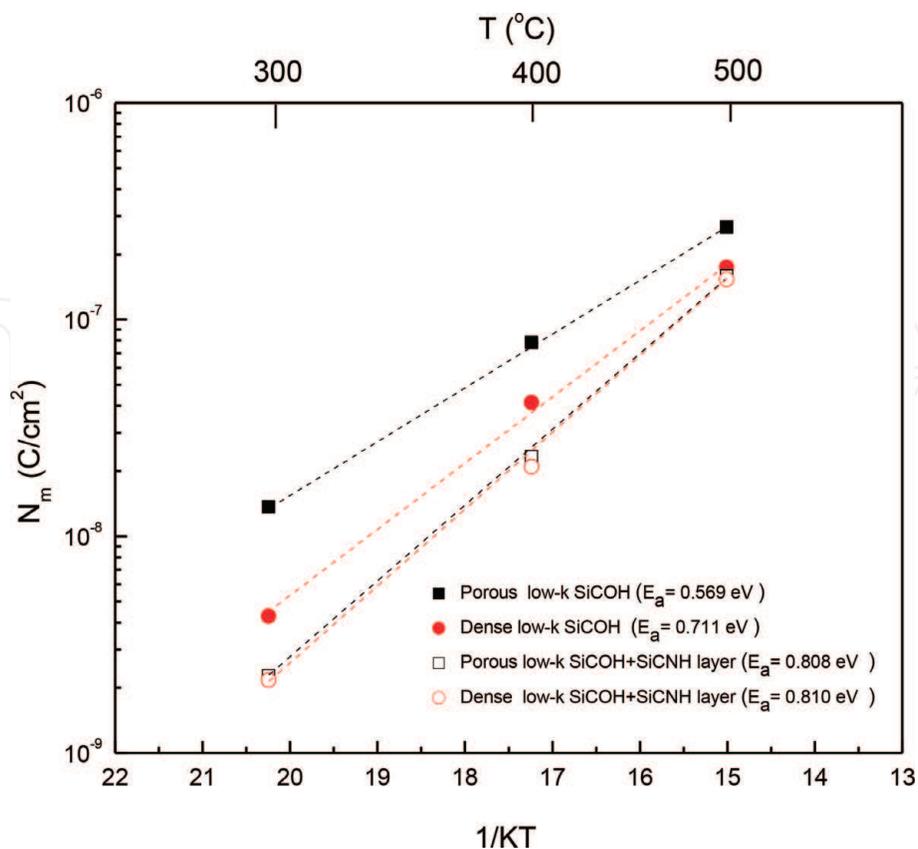
desorbed at 190°C. After the 400°C annealing, most physically adsorbed moisture is desorbed. The chemisorbed moisture has the higher bonding energy; thus, it can be desorbed by a thermal annealing with the temperature above 600°C. As a result, the temperature of annealing is required to be elevated to 600–1000°C in order to remove the adsorbed water from porous low- $k$  dielectric films. However, this temperature is not suitable to use in the BEOL interconnects because porous low- $k$  dielectric films become unstable at temperature above 600°C.

To reach a better recovery for moisturized low- $k$  dielectric films, a combination of UV curing and silylation process has been provided. UV curing and silylation processes can be done in the same chamber to save the processing step. The UV-assisted restoration is performed at elevated temperatures using a gaseous hydrocarbon in the curing ambient. The efficiency of recovery can be optimized with the process parameters, including UV wavelength and intensity, substrate temperature, UV curing time, chamber pressure, and reactant gas mixture [90, 91].

### 5.3 Cu drift

Due to a high diffusivity, Cu is easily oxidized to Cu mobile ion and then diffuses into ILDs under thermal and/or electrical bias [92, 93]. The diffused Cu ions could generate shallow energy levels in the bandgap of the porous low- $k$  dielectric film [94]. These generated states act as defect centers, facilitating PF type conduction. Additionally, the penetration of Cu atoms or ions contributes to field enhancement locally inside the dielectric or at the electrode of electron injection [95]. These effects result in the significant degradation in the electric characteristics and reliability for the porous low- $k$  dielectric films.

To prevent or minimize the diffusion of Cu ions and Cu barriers, including metal and dielectric barriers, are required for Cu metallization. **Figure 9** plots the Cu ion



**Figure 9.** Cu ion concentration in dense and porous low- $k$  SiOCH films with and without capping SiCNH layer after annealing as function of temperature [96].

concentration  $N_m(T)$  in the various low- $k$  dielectric films after thermal stress as a function of annealing temperature [96]. The Cu penetration is enhanced at increased temperatures. The larger Cu ion concentration in the porous low- $k$  dielectric film after annealing indicates that the pores in the low- $k$  dielectric film induced the rapid migration of Cu ions. Additionally, the porous low- $k$  dielectric film had the lowest activation energy (0.57 eV) with a value close to those reported elsewhere (0.42–0.60 eV) [97, 98]. The SiCNH capping layers on the low- $k$  dielectric films increased the activation energy to  $\sim 0.81$  eV for both dense and porous low- $k$  films, suggesting that the SiCNH capping layer acts as a Cu barrier and prevents possible Cu migration. The use of SiCNH capping layer as a Cu barrier increases the effective  $k$  value of BEOL ILD, being a main concern.

The deposition of metal barrier can also prevent Cu migration. However, due to a high resistivity of metal barrier, the overall resistivity of the metal line significantly increases in the scaling interconnect pitch. Additionally, barrier metals like tantalum (Ta) deposited by physical vapor deposition penetrate into low- $k$  dielectric in a way similar to Cu, causing low- $k$  dielectric degradation. Moreover, the metal barrier-induced damage increases as the porosity of the low- $k$  dielectric increases [99, 100].

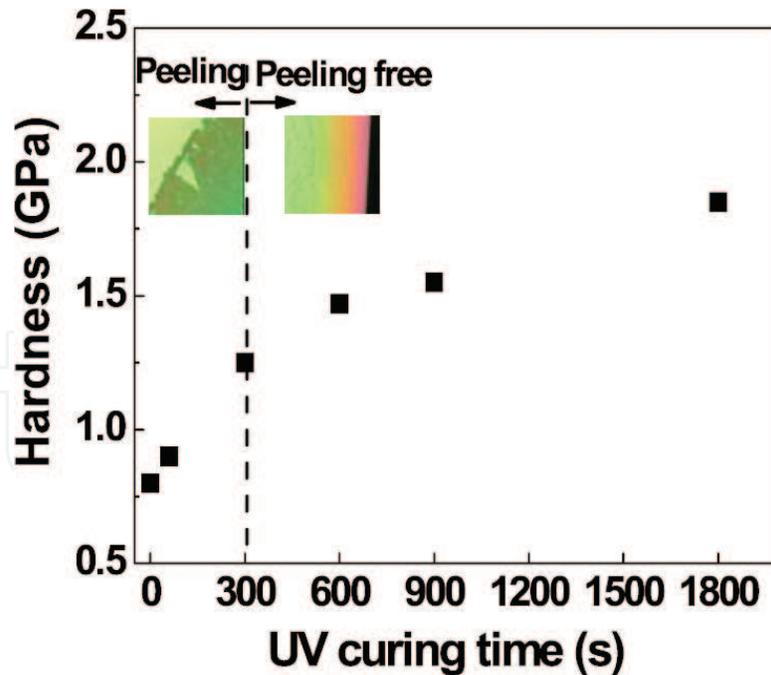
Currently, self-forming barrier [101], atomic layer deposition (ALD) barrier [102], and self-assembled monolayer (SAM) [103, 104] processes are promising methods to prevent metal penetration. However, the integration with the porous low- $k$  dielectric must be controlled precisely to meet all requirements.

#### 5.4 CMP-induced damage

The purpose of chemical mechanical polishing (CMP) is to produce planarization topography by means of both mechanical polishing and chemical reaction. A simultaneous interaction between polishing slurry, a semiconductor wafer, and a polyurethane pad occurred. Thus, the chemical, mechanical, and material properties of the pad, wafer surface, and slurry determine the controllability and quality of CMP process.

In Cu metallization, CMP process is used to remove the excess Cu film and the barrier metal. There are three main steps in Cu CMP process. Firstly, the excess Cu film is polished. Then, as reaching the interface, both metal barrier and Cu film are polished. Finally, to ensure that all metals are removed from the field regions in all parts of the wafer, over-polishing in the last step is necessary. Thus, the used dielectric insulator is polished simultaneously. To reach high degree of planarization and avoid Cu dishing, dielectric erosion, and interface quality degradation (dangling bonds, generation, metal contaminants, and moisture presence), precise control CMP process is required [105, 106].

As the porous low- $k$  dielectric film is used as an interconnecting insulator, peeling, delamination, and cracking may occur under CMP process because it has not enough mechanical strength to survive the large mechanical stress process. Therefore, improving the elastic modulus or hardness of the porous low- $k$  dielectric film is required. **Figure 10** shows the change in the hardness of porous low- $k$  dielectric materials as a function of UV curing time [107, 108]. By increasing UV curing time after the porous low- $k$  dielectric film deposition, the hardness (H) can be improved. Moreover, CMP-induced peeling was checked to determine the minimum hardness for integration of the porous low- $k$  dielectric film into BEOL interconnects. At a UV curing time of less than 300 s for the porous low- $k$  dielectric films, peeling was observed. Peeling was worse at shorter UV curing times. As UV curing time is greater than 300 s, the wafer exhibited peeling-free for the porous



**Figure 10.**  
Hardness of porous low- $k$  dielectric materials as a function of UV curing time [107].

low- $k$  dielectric films, indicating that the minimum hardness for integration of the porous low- $k$  dielectric film into BEOL interconnects is 1.2 GPa.

The other problem of Cu CMP problem is that the V-shape corners in the porous low- $k$  trenches are formed due to the higher mechanical force. This would become a potential critical path for porous low- $k$  dielectric breakdown owing to field enhancement along the CMP interface.

## 6. Conclusions

To improve the performance of ICs, porous low- $k$  dielectric materials have been used as an interconnecting insulator for providing lower parasitic capacitance between the wires to reduce RC time delay. Porous low- $k$  dielectric materials can be achieved by introducing low-polarizability chemical bonds and porosity into the film. During the integration, the semiconductor processing induces damage on the porous low- $k$  dielectric material, making the dielectric material densification hydrophilic, facilitating moisture uptake, and inducing Cu and barrier metal penetration. These lead to  $k$  value increase and reliability degradation for the porous low- $k$  dielectric material. Moreover, high porosity and large pore size in the porous low- $k$  dielectric materials make them sensitive to integration-induced damages. Moreover, porosity in the low- $k$  dielectric material weakens the hardness and enhances the local field of the film, resulting in CMP damage and reliability challenges. Therefore, in order to achieve a successful implementation of advanced porous low- $k$  dielectric films in the future BEOL interconnects, optimization and innovation of material science and integration processing are needed.

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### **Author details**

Yi-Lung Cheng\* and Chih-Yen Lee  
Department of Electrical Engineering, National Chi-Nan University, Taiwan, ROC

\*Address all correspondence to: [yjcheng@ncnu.edu.tw](mailto:yjcheng@ncnu.edu.tw)

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