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Avalanche Photodiode Focal Plane Arrays and Their Application to Laser Detection and Ranging

Hai-Zhi Song

Abstract

Focal-plane avalanche photodiodes (APDs) are being more and more widely and deeply studied to satisfy the requirement in weak light and single photon imaging. The progresses of this worldwide study, especially the distinctive researches and achievements in Southwest Institute of Technical Physics and University of Electronic Science and Technology of China are reviewed in this chapter. We successfully fabricated up to 64 × 1 linear-mode Si APD arrays, and 32 × 32–64 × 64 Si single-photon avalanche detector (SPAD) arrays, and applied them in Laser Detection and Ranging (LADAR) platforms like driverless vehicles. Also, we developed 32 × 32–64 × 64 InGaAsP/InP SPAD arrays, and constructed three-dimensional imaging LADAR using them. Together with the progresses of other groups and other materials, we see a prospective future for the development and application of focal-plane APDs.

Keywords: avalanche photodiode, focus plane, laser detection and ranging

1. Introduction

Avalanche photodiodes (APDs) have been widely studied and effectively applied in commercial, military, and academic fields [1] for a few decades. Compared with p-i-n photodiodes, APDs provide higher gain, higher sensitivity and lower detection limit [2], so they are mostly well applied in optical communications [3], imaging [4, 5], and single photon detection [6, 7] in recent years. As all-solid-state optoelectronic devices operating at room-temperature or under thermoelectrically-cooled conditions, APDs are scalable to numerous pixels so that they are taking more and more important roles in focal-plane processing and imaging [8]. Owing to the advantages such as internal photoelectric gain, small size, low driving voltages, high

efficiency, and fast response, focal-plane APD arrays bring about new three-dimensional (3D) imaging techniques which provide much wealthier and more accurate information for object recognition and identification [9]. Advanced 3D imaging technologies are strongly required in radar systems including laser detection and ranging (LADAR), so the focal-plane APDs and their LADAR applications were widely and deeply studied in recent years [10–20]. For the purpose of more progress in the future, it is necessary to take an overview on the present research and production of APD arrays. Briefly, the most significant progress is made by MIT Lincoln Laboratory. They developed state-of-the art products of Si and InP/InGaAs Geiger-mode focal-plane arrays [10], which have been successfully applied in a few LADAR systems. Princeton Lightwave also succeed in producing focal-plane single photon avalanche detector (SPAD) arrays and commercializing their single-photon camera based on the SPADs [11]. The research and production of other groups [12–14] may also be valuable as references for future developments. In this chapter, we review the research and application of the focal-plane APDs in Southwest Institute of Technical Physics and University of Electronic Science and Technology of China [15–20]. It includes linear mode Si APD arrays, Si SPAD arrays and InGaAsP/InP SPAD arrays, which have been applied in LADAR systems.

2. Linear-mode Si APDs

The detection of weak light is technically significant in many application fields such as single molecule fluorescence, high-speed quantum cryptography, and infrared detection [21–23]. In all the application fields, APD devices are strongly required to perform photon-counting with high quantum efficiencies, quick optoelectronic response, and low dark counting rates (noise). LADAR imaging systems work in the way of sampling the spatial and/or temporal information of the optical radiation to an array of detectors. Linear-mode (applied bias slightly lower than the breakdown voltage) APDs are often desired by LADAR systems because their dead-time is normally much shorter than that of Geiger-mode (applied bias slightly higher than the breakdown voltage) APDs so that they can measure sequential pulse returns from closely spaced multiple objects. In extreme cases, linear-mode APDs can even detect a few photons or a single photon, which adds an extra dimension to LADAR scene data [21]. Generally, in the near-infrared spectral band, especially at 905 nm, Si APDs might be applied for ultra-weak light detection, and can be used in linear-mode at gains up to about 500 or greater [23]. Therefore, linear-mode Si APD arrays were developed and applied in LADAR systems.

2.1. Fabrication of the linear-mode Si APD chips

A basic linear-mode APD detector, as shown schematically in **Figure 1**, consists of the APD element and the readout integrated circuit (ROIC) [24, 25]. The ROIC is composed of a trans-impedance amplifier (TIA), a stabilivolt source circuit and a comparer. The APD element converts incident light signal into primary photo-generated carriers and photocurrent, then amplifies the resulting photocurrent through internal avalanche gain, i.e. the impact ionization. The TIA converts the amplified APD current into a voltage signal, which is proportional to the total multiplied charge delivered by the APD.

The design and simulation of an APD device were carried out using a full-band Monte Carlo (MC) device model. For each APD geometry, the MC model incorporates realistic band structures [26, 27]. The basic reach-through APD model with separate layers of absorption, charge and multiplication (SACM) is shown in **Figure 2(a)**. In particular, it is important to know that, in general, electrons can be much more ionized than holes in silicon. Electrons rather than holes should be swept by the electric field into the high field region where the multiplication takes place. Thus, there should be a π-type absorbing region of suitable width for absorbing the incident radiation, and the radiation should be able to enter this region with no loss in any n^+-type layer.

The basic design of a reach-through APD consists of a narrow high-field region where the multiplication takes place, with a much wider low field region in which the incoming radiation is absorbed. As schematically shown in **Figure 2(b)**, an avalanche process occurs as the electric field in a p-n junction is higher than the critical field (E_{cr}) at which impact ionization of carrier starts. The electric field in the p-n junction of a Si APD should be some 2–5×10^5 V/cm. It should not be more than 10^6 V/cm at which the Zener effect may take place [28–30].

For satisfactory operation of the APD, the high resistivity π-type substrate must be fully depleted by the applied bias voltage. Generally, it works well provided the substrate wafer is not too thick and the required response times are not less than ~10 ns. However, fabrication
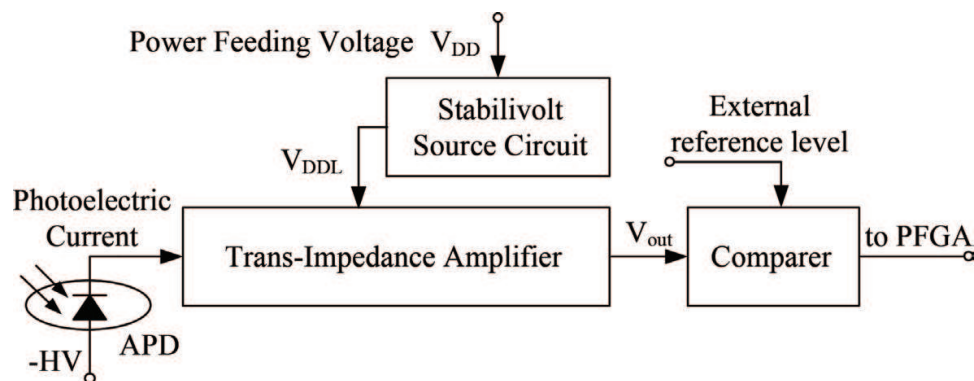

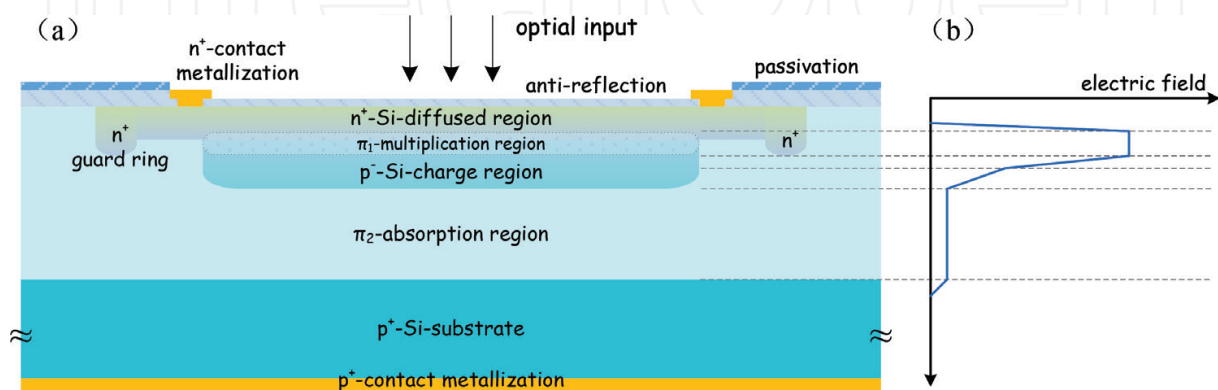**Figure 1.** Schematic of the linear-mode Si APD.

Figure 2. (a) Schematic cross section (not to scale), and (b) schematic profile of electric field of a typical APD structure.

of Si APDs on 6-inch or 8-inch wafers, as is now usually the case, will often mean that the absorption region is thick (~700 μm), operating voltages are high, and response times are slow. These problems can be avoided with the use of an epitaxial version of the design in **Figure 2(a)**. In this approach, a high-resistivity π-type layer is epitaxially grown on the surface of a low resistivity p-type Si substrate. The absorption region (epitaxial layer) may be of any thickness (typically chosen to be in the range of 30–50 μm), and its resistivity is chosen to be low enough so that it does not introduce a significant series resistance. When bias voltage is applied, the depletion layer stops at the interface between the substrate and the epitaxial layer [31–34]. While fast response is a requirement, the narrow active region of this APD is normally the best option.

Linear-mode Si APD arrays are fabricated by adopting Si planar manufacturing process on a high-resistivity π-type layer, which is grown epitaxially on the top of a low resistivity p-type Si substrate. The initial material developed is the Si layer 35–40 μm thick, a highly-resistive epitaxial layer on a p⁺-type Si <111> substrate.

2.2. Design of the TIA

As mentioned above, the ROIC chips consist of a voltage-stabilized source and a TIA. The voltage-stabilized source effectively reduces external noise jamming and increases voltage suppression ratio of the power source. Here we have the structure of a new-type regulated cascode circuit configuration which is compatible with the APD chips. The bandwidth, the parallel negative feedback and the trans-impedance gain of the TIA are improved by using regulated cascode circuit [35, 36].

Figure 3 schematically illustrates the TIA with the regulated cascode circuit configuration. The regulated cascode circuit consists of common gate amplifier input stage (including R_1, R_2
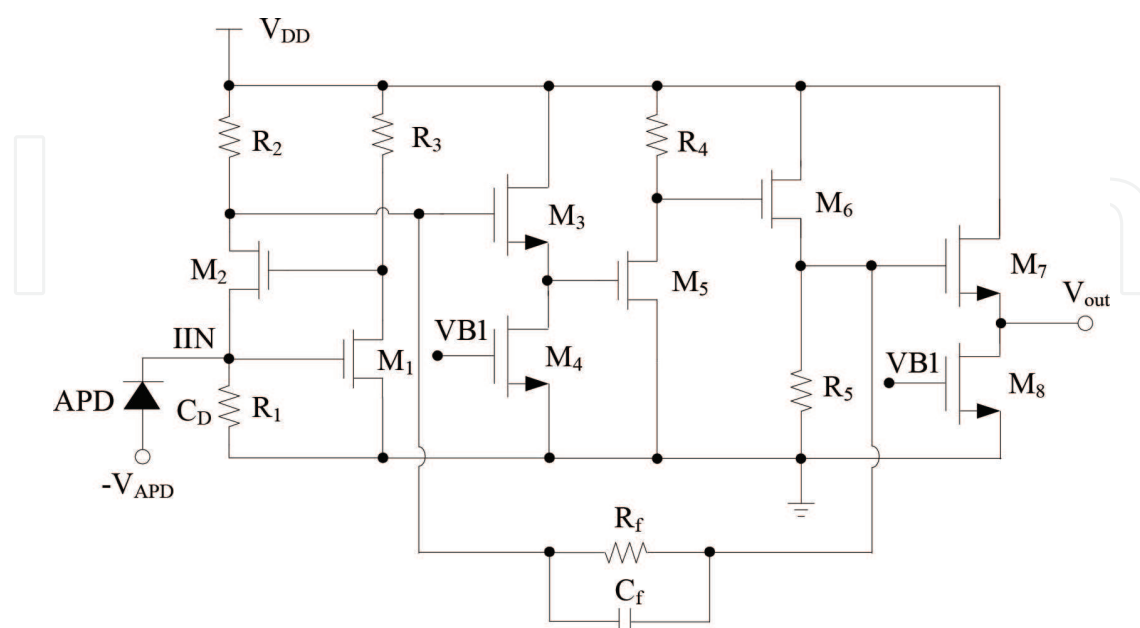

Figure 3. The TIA with the regulated cascode circuit configuration.

and M_2) and common source amplifier stage (including M_1 and R_3), forming partial current parallel negative feedback. The primary photocurrent generated by APD is imported to the source electrode of the cathode-input amplifier. Then the APD's current signal is converted into a voltage signal. The source follower, consisting of M_3 and M_4, is used for isolation. The secondary common-source amplifier is composed of M_3 and R_4, which play a part role in amplifying signal again. To improve the output drive capability, the output stage contains two-stage source followers, made up of $M_6 + R_5$ and $M_7 + M_8$ respectively.

2.3. Properties of the Si APD array

Developed at SITP, Si APD arrays were characterized at UESTC. The fabricated devices exhibit high primary photoelectric sensitivity (about 0.5 A/W @905 nm at gain M = 1) and high speed of operation (about 10 ns). **Figure 4** shows an example of typical dependences of the gain on the reverse bias. As the bias arises up to the reach-through voltage V_{rt}, it depletes the π-type avalanche region. For the APDs, V_{rt} attains values of 60–70 V, over which not much more regions are depleted. Further increasing the bias voltage mainly leads to higher electric fields in the structure. As the highest electric field reaches the critical value E_{cr}, multiplication of carriers starts to occur. More rising in the reverse voltage makes the steady current density go up to in principle infinity, where actually the avalanche breakdown takes place [37–39]. The corresponding voltage here is thus named avalanche breakdown voltage V_{br}, about 110 V for Si APDs.

At operating voltage ($V_{br} \times 98\%$), the multiplication region of a Si APD has an electric field as high as about 3.7×10^5 V/cm and an impact generation rate as high as about 2.8×10^{25} s^{-1} cm^{-3}. As a result, the avalanche gain (M) and the sensibility (S) of the linear-mode Si APDs are observed to be up to about 600 and 300 A/W @905 nm respectively.
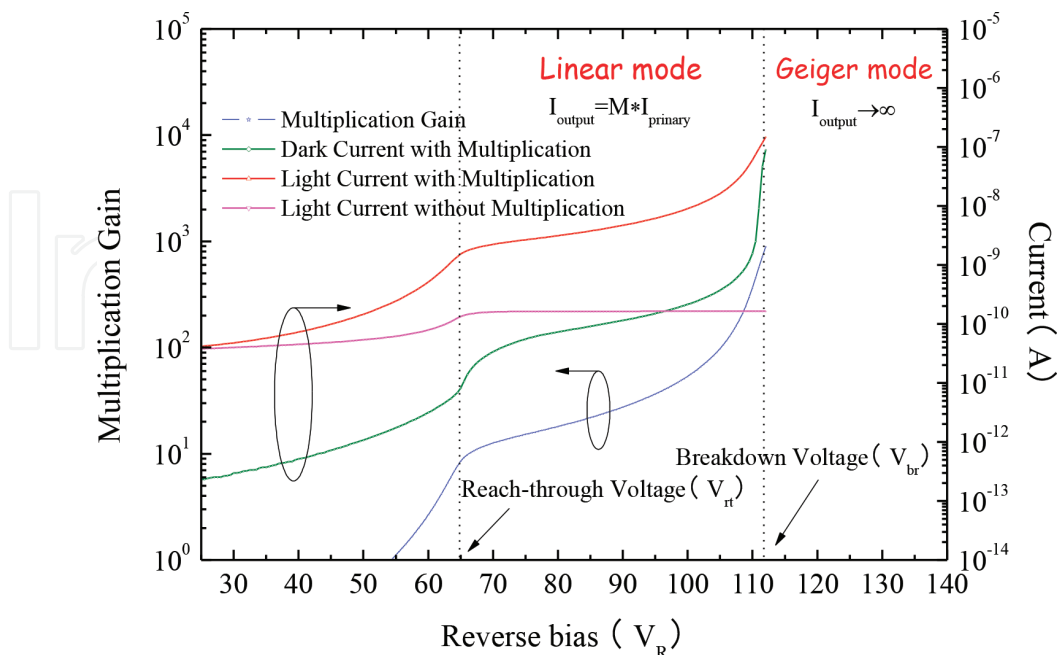

Figure 4. Dependence of dark current, photocurrent (with/without multiplication) and multiplication gain on reverse bias voltage of the designed SACM Si APD.

The ROIC chips were developed on the 0.18-µm CMOS platform of SMIC, Shanghai. The voltage-stabilized source effectively reduces external noise jamming and increases voltage suppression ratio of the power source. TIA shows trans-impedance of 120 dBΩ, the equivalent input noise is about 6 pA/Hz$^{1/2}$, the rise time is 7.3 ns, and the bandwidth is $BW \geq 35$ MHz.

Arrays of 64 × 1 Si APDs and ROIC chips were integrated to form the photodetector device by performing bonder-leading welding techniques. Together with packaging processing, the devices of 64 × 1 Si APD focal-plane arrays were successfully fabricated, one of which is shown in **Figure 5**. The power of input signal light is 0.9 nW (the duty cycle is 1/1000), and the maximum output voltage amplitude is 1.04 V. The devices present pulse responsivity $R \geq 1 \times 10^6$ V/W, noise equivalent power $NEP \leq 5$ pW/Hz$^{1/2}$, rise time $t_r \leq 3$ ns, and inhomogeneity of responsivity of each pixel ≤10%, under 905 nm, 100 ns and 10 kHz of laser irradiation.

2.4. Application of the linear mode Si APD array

As we constructed linear-mode Si APD focal-plane detectors, the 64 × 1 array devices are tested for possible applications. One example is that, the device is effective in running a driverless platform. Using this APD array, an obstacle-avoidance LADAR, as shown in **Figure 6(a)**, is successful with detection distance of 110 m, distance resolution of 5 cm and angle resolution of 0.5°. This LADAR can effectively detect the obstacles on the way, as shown in **Figure 6(b)**. Compared with traditional technique, in which a single detector was used, the image is much clearer (10 times of pixels) and the imaging speed is much faster (35 versus 15 Hz), so this newly developed obstacle-avoidance LADAR is more accurate and better to be used in driverless vehicles.
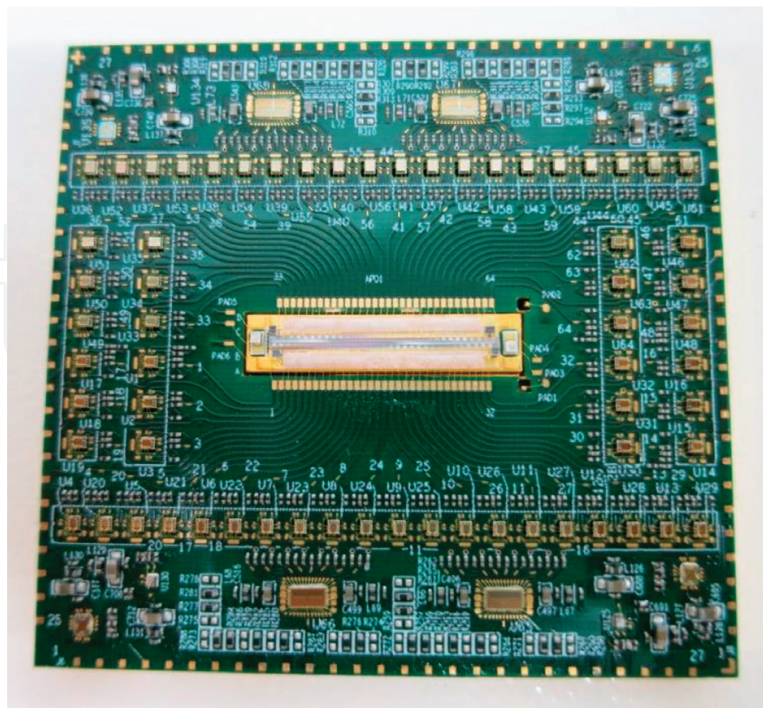

Figure 5. The device of 64 × 1 linear-mode Si APD focal-plane array.

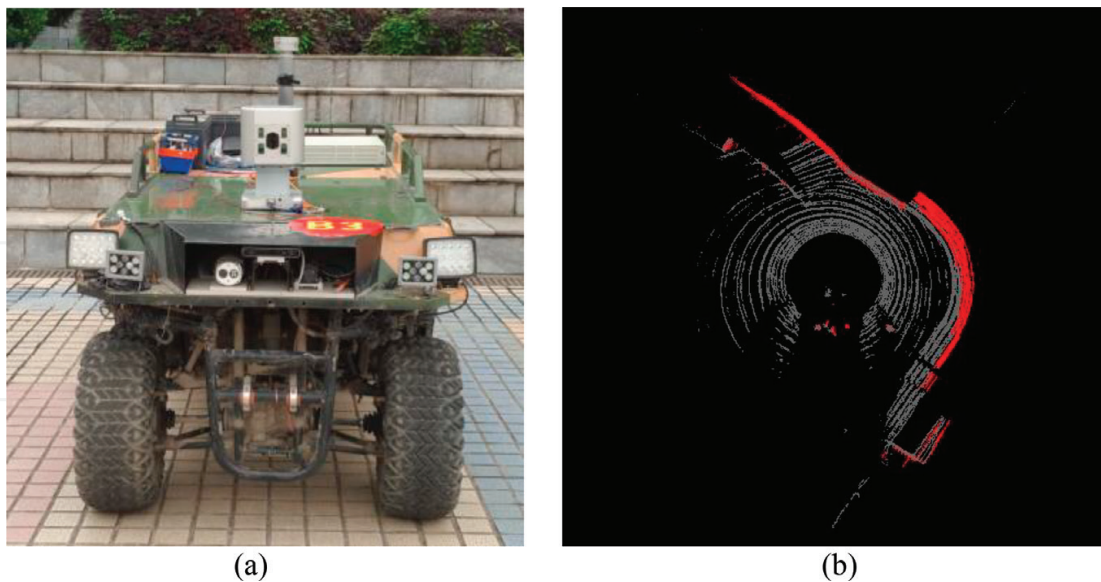(a)   (b)

Figure 6. (a) An obstacle-avoidance LADAR, using 64 × 1 linear-mode Si APD array as the focal-plane detector, is installed on a driverless vehicle. (b) The imaging effect of the LADAR, where the red pattern shows the existence of obstacles.

3. Si SPAD focal-plane arrays

A Geiger-mode APD can detect a signal as weak as a single photon. In recent years, it is very active and effective as a single-photon detector and usually termed SPAD. Organized into arrays, SPAD can be used in many systems such as LADAR, mobile laser imaging and viewing instrument. By using some special processing, we developed typical Si-based SPAD arrays working at 905 nm. The key techniques are described as follows.

3.1. Fabrication of Si SPAD array chip

3.1.1. Design

According to the requirement of a Si SPAD, there would be a depletion region as thick as 30 μm. Using usual single-sided abrupt p-n junction, to get such a large depletion while remaining avalanche gain, one need to apply a voltage as high as 500 V, which is not realistic enough. We design a reach-through structure, containing n^+-π-p-π-p^+ layers, as shown in **Figure 7**. The electric field distribution under bias near breakdown is similar to that in **Figure 2(b)**. The light-generated carriers is multiplied in the region with highest electric field, so called multiplication region. This region is very thin compared to the whole depletion region. The other parts in the depletion region can have electric field as weak as possible but sufficient to ensure carrier drifting at the saturated speed. As a result, the operating voltage can be greatly decreased.

There could be two types of host materials. One is high-resistive Si wafer (p-type with 10^{14} cm^{-3} boron doped), the other is epitaxial lowly-doped p-type Si on a p^+-doped Si wafer. To fabricate the reach-through structure on bulk Si, the whole wafer has to be depleted as the
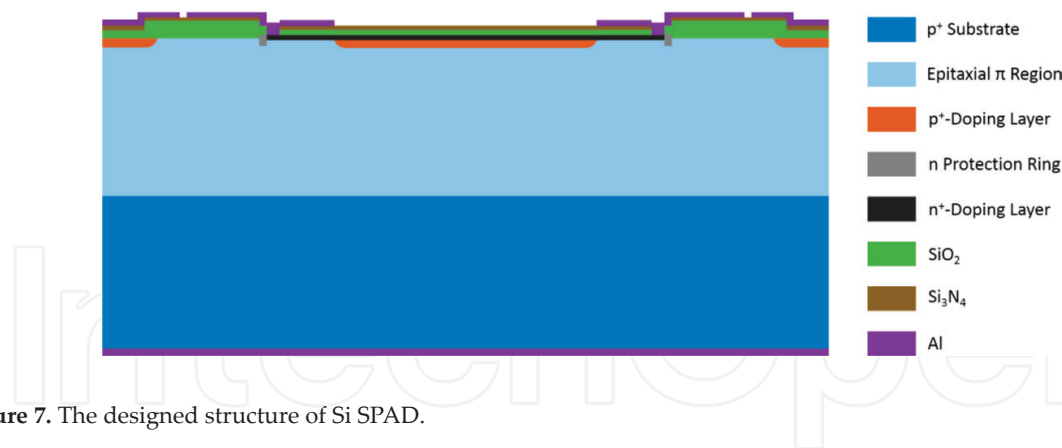
Figure 7. The designed structure of Si SPAD.

device works. To get low breakdown voltage of 150 V or so, we must polish the wafer down to a thickness of 50 μm, which is difficult and brings a lot of unstable features to the devices. Therefore, we use epitaxial wafer as the material for fabricating Si SPAD arrays.

Decreasing the dark count rate (DCR) is conflicting with choosing lower avalanche electric field E_{max} and lower operating voltage. There should be tradeoff between these two to get optimized structure parameters. Our previous product has DCR of several 10 kHz with light receiving area of Φ500 μm. Here we try making a device area of Φ50 μm to get much lower DCR. By further well designing and optimizing the internal structure, improving the pixel uniformity and surface passivation effect, we succeeded in controlling the DCR under 10 kHz.

3.1.2. Precise control and uniformity

Precise control of the device structure is a decisive step. The multiplication layer and charge layer are most important because they greatly influence the key parameters such as quantum efficiency, response time and gain. To precisely control the charge quantity and multiplication length, we adopt the following process. Boron ion-implantation is firstly performed to accurately control the dopant amount. Due to smaller diffusion coefficient of boron in Si, the broadening of boron distribution after thermal treatment is weaker. Then, second epitaxy is carried out to grow n-type layer. This is the way to precisely control the multiplication length.

It is the critical process of a Si SPAD array to make all the pixels controllably consistent in characteristics, e.g. the avalanche gain, the response time, and the breakdown behavior. The pixels uniformity is influenced by four factors: epitaxial structure, ion-implantation of the charge layer, diffusion of the p-n junction, heat-induced doping redistribution in the device process. The most important is that, the epitaxial layers should be grown as uniform as possible. Usually, a 50-μm thick epitaxial layer should have thickness uncertainty of less than 50 nm.

In an SPAD array, one of the critical structures is the guard-ring. The designed SPAD structure shows that, the n⁺ contact and light-incident layer is so small that the p-n junction depth is about 0.5 μm. In order to prevent the device from being lowly broken down, a guard-ring around the device can be fabricated by doping at the edge of the n⁺-doped area. It uses more deeply diffused n-doping (Phosphorus has big diffusion coefficient in silicon) to decrease the curvature rate of the edge of the p-n junction with the π-region, to reduce the electric-field

of the junction edge, to improve the breakdown voltage at the edge of the device. Properly controlling diffusion depth, doping level and ring width, the edge breakdown voltage can be improved to be about 1.5 times that in the avalanche region. As an example, usually, 2–3 μm wide guard-ring is suitable for the above purpose.

3.1.3. Isolation process

In the avalanche procedure, there come photons at wavelength shorter than 1 μm while creating multiplication carriers. These photons may enter other pixels nearby to generate unintentional count. In order to suppress cross-talk between pixels, design of the SPAD structure is optimized. Further by processing the light-hiding belt and with the aid of decreasing the reflectivity at the interface, the optical cross-talk is well controlled. In the Si SPAD array, there exist big shunt capacitances in between the adjacent pixels, so the electric cross-talk could be of high possibility. This is resolved by decreasing capacitances related to the wires in the later interconnection process.

With a long absorption region (~30 μm), it needs to keep background doping level being lower than 10^{14} cm^{-3} in order to remain lower electric field in this layer. In the meantime, the inversion layer near the surface is a major factor causing device failure. Thus, it is necessary to set a p$^+$-doped area around the surfical active region, i.e. the channel-resisting region. It can cut the inversion layer at the SiO$_2$-p-Si interface and stop the surfical expansion of the depletion region. Its final role is to suppress the surfical leakage current and to prevent the device from being broken down by a low bias. By calculation and experience, a doping level higher than 10^{16} cm^{-3} in the surface layer is sufficient to form the channel-resisting effect.

By performing the above processes, chips of 32 × 32–64 × 64 Si SPAD arrays are fabricated. One sample is shown in **Figure 8**.
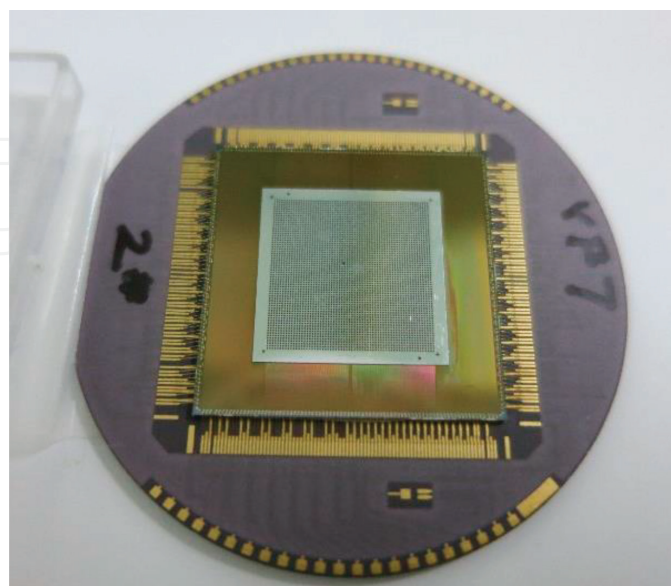

Figure 8. One chip of Si SPAD array.

3.2. ROIC optimization

To realize highly accurate timing of the photon arrival, we use a time-digit-conversion (TDC) circuit with the aid of phase-shifting technique. This approach satisfies the requirements of 2 ns in the time resolution and 20 kHz in frame frequency while decreasing the power consumption of the whole chip. An active-quenching design is used to reach an extinction time of less than 50 ns.

High precision timing and time-reading circuit is composed of TDC and memory readout unit, as shown in **Figure 9**. After gate/signal conversion circuit transforms the high voltage output of SPAD into low voltage signal, it firstly needs to read the photon flying time of every pixel through TDC, to change times into digits, and to read out the digits through the memory readout circuit. For the purpose of 2 ns of time resolution, highly frequent, highly stable main clock is supplied to the 12-digits counter. Frequency more than 500 MHz is not easy to be realized at every pixel at the same time. Due to the processing limit, shunt resistors and capacitors may significantly contribute to the power consumption (To an 32 × 32 array, the power consumed in clock lines would be 100 mW). Without using phase-locking loop (PLL), here we design TDC circuit with the aid of phase-shifting technique, to satisfy the requirement of high time resolution while decreasing the requirement for clock frequency. The TDC consists of counter and time-delay chain. When the external timing signal (a rising edge) comes, the counter starts to work; when a photon is detected, the circuit generates a signal to stop the counter and remain the present count data. Via the time-delay chain composed of 8 units, the external clock creates 8 clock signals with different phases. As the starting signal comes, every clock signal is sampled and the time-delay chain outputs an 8-digit signal, which will be coded and saved into the data process module. A similar process happens when a stop signal comes. Difference calculation between the start and stop data gives a 4-digit signal, constructing a 12-digit information together with the data from the counter. Then, the time interval
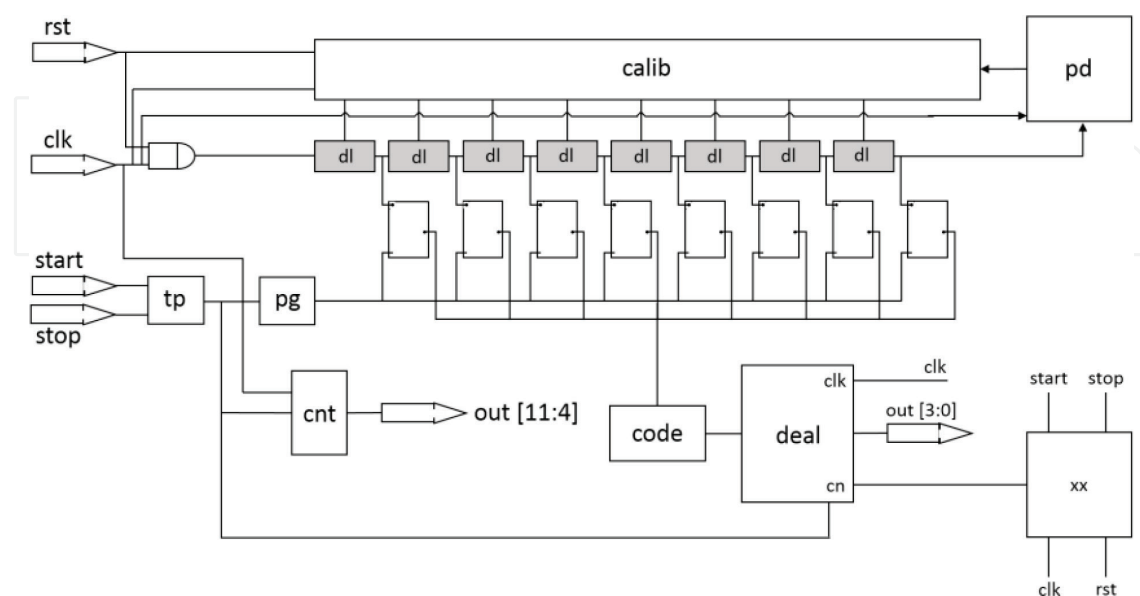

Figure 9. Structure of the high precision time-digit conversion circuit designed for Si SPAD array.

between start and stop is converted into a 12-bit digital signal. When the counter output clock is effective, its locked state is transferred bit by bit into a 12-digit register. Controlled by a 25 MHz clock, the register transfers its digits into the register of the neighboring pixel. This serial transform mode gives at last a frame frequency of 25 kHz.

Avalanche-quenching circuit is another important aspect in SPAD array. To realize a dead-time less than 50 ns, we design actively-quenching circuit as shown in **Figure 10**. When avalanche photocurrent is detected, the voltage at point a jumps down and forces the quenching circuit run. After a while, the voltage at point b comes higher, switching on the transistor M1 via the feedback branch, and quickly pulling down the voltage at point V_{apd} to make the APD bias lower than breakdown voltage (quenching the APD). After more a while, the charge–discharge circuit gradually decreases the voltage at point b, M1 is turned off via feedback circuit, and V_{dd} charges the APD through R_0 and parasitic capacitances to restore the Geiger mode.

The above designs are realized by performing CMOS processing, and thus the ROIC chips are produced.

3.3. Interconnection and package

The next key processing is interconnecting the SPAD chip and the ROIC chip. The fabrication is as follows. After some degree of thinning processing, the backside of the wafer is treated to have a light-incident window for every pixel. As shown in **Figure 11**, the window area is formed by etching off the p-type substrate, and the layer under the etched window is made to be ~35 μm thick. Dry etching such as $SF_6 + O_2$ ICP is used to fabricate windows with straight sidewalls. In addition, the uniformity of this processing must remain ≤ ±2% in the window depth and ≤ ±0.5 μm in the window diameter. Then, it is realized that negligible light is absorbed by the p-type substrate. Using standard Indium-shot interconnection processing, the SPAD chip is connected exactly with the ROIC, as shown in **Figure 11**. Integrating the interconnected chip with TEC cooling cells, and packing these all into a vacuum can, a Si SPAD focal-plane device is developed.
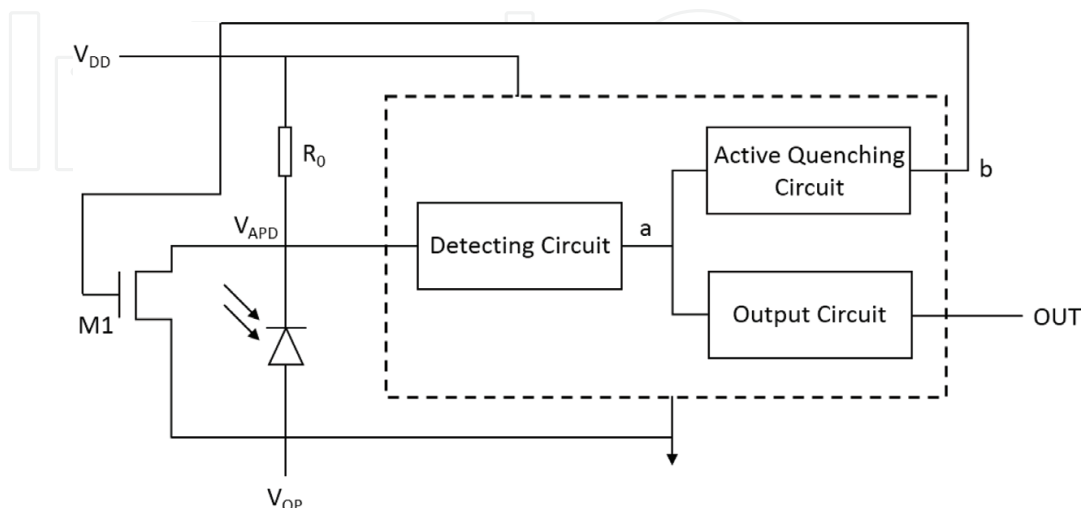

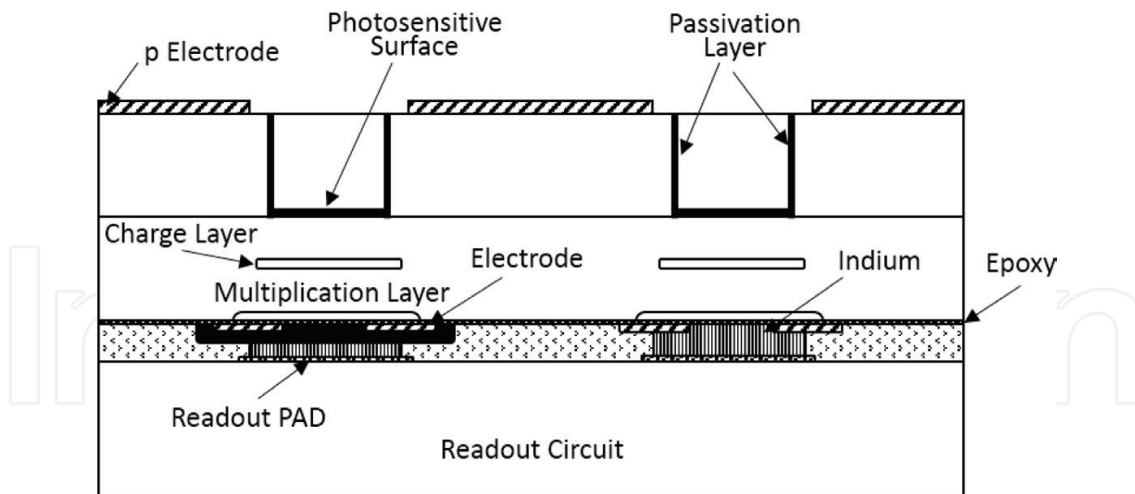**Figure 10.** Structure of the quenching circuit for Si SPAD array.

Figure 11. Schematic of the interconnection process for fabricating Si SPAD arrays.

3.4. Application of Si SPAD focal-plane arrays

Measurements show that the developed SPAD array have DCR lower than 5 kHz, average photon detection efficiency (PDE) ~25%, time resolution <1 ns, and frame speed ~25 kHz. The 32 × 32 SPAD array exhibits pixel uniformity < ±5% (e.g. in counting rate). It can thus be applied in a practical imaging system. The above fabricated SPAD array device is installed in a LADAR 3D imaging instrument. The instrument can three-dimensionally detect and recognize multi-hided objects in forests and mountains, and be of small size, light weight, high resolution and rapid imaging.

4. InGaAsP/InP SPAD focal-plane arrays

Like InGaAs/InP SPADs [40], InGaAsP/InP SPADs are also extensively studied and practically explored for their utility in many fields including single photon imaging [41] and quantum information processing [42, 43] in the near-infrared wavelength range. Thanks to the advanced epitaxial techniques, this kind of SPADs has been well developed and applied in, e.g., LADAR in recent years [41, 44]. Nevertheless, many critical problems are still open to be resolved. One of them is the device homogeneity, such as the reproducibility and uniformity of the SPAD performance [45], which are strongly required to be precisely controlled by refining the structure parameters in epitaxial growing and device processing. One can, of course, estimate the effects of some individual physical parameters on the performance homogeneity using some analytical method [46], but it is not easy to obtain the knowledge of many parameters at the same time. It is even unlikely to make clear the collective influence of multiple parameters and to quantitatively take a balance between various parameters. The quantitative association between the device inhomogeneity and structure uncertainty should thus be necessarily established. Therefore, we firstly carry out a statistical analysis on InGaAsP/InP SPAD characteristics by randomizing the structure parameters, and then figure out the

necessary control accuracies in a few significant structure parameters, which are required for nice device homogeneity. Accordingly, we fabricate InGaAsP/InP SPAD focal-plane arrays and demonstrate their applications.

4.1. SPAD array homogeneity versus material controllability

An InGaAsP/InP APD structure is designed as an example SPAD object. It is of a hetero-structure comprising SACM layers, as can be seen schematically in **Figure 12(a)**. By using conventional APD theory [28, 47] and lately advanced approaches [48–50], citing material parameters from previous reports [49, 51, 52], and neglecting the dead-space effect [53], the device characteristics of this structure was calculated.

Figure 12(b) illustrates the calculated current–voltage (*I-V*) characteristics in dark. Here the breakdown voltage V_b is principally the applied reverse bias V at infinite avalanche current. The simulated DCR r_d versus PDE η is shown in **Figure 12(c)**. Both of them are dependent on the applied excess bias $V_{ex} = V - V_b$. As the SPAD is running under a middle excess bias $V_{ex0} = 5$ V, r_d is found below 10 kHz and η appears some 0.50. It suggests that 5 V of V_{ex} is an optimal operating condition at 230 K, so $V_{ex} = 5$ V will be the reference point in this study.

As a SPAD array is used, there is usually a common bias V_0 generally applied to more than thousands of pixels [44]. Provided structure fluctuations exist among the numerous pixels, the
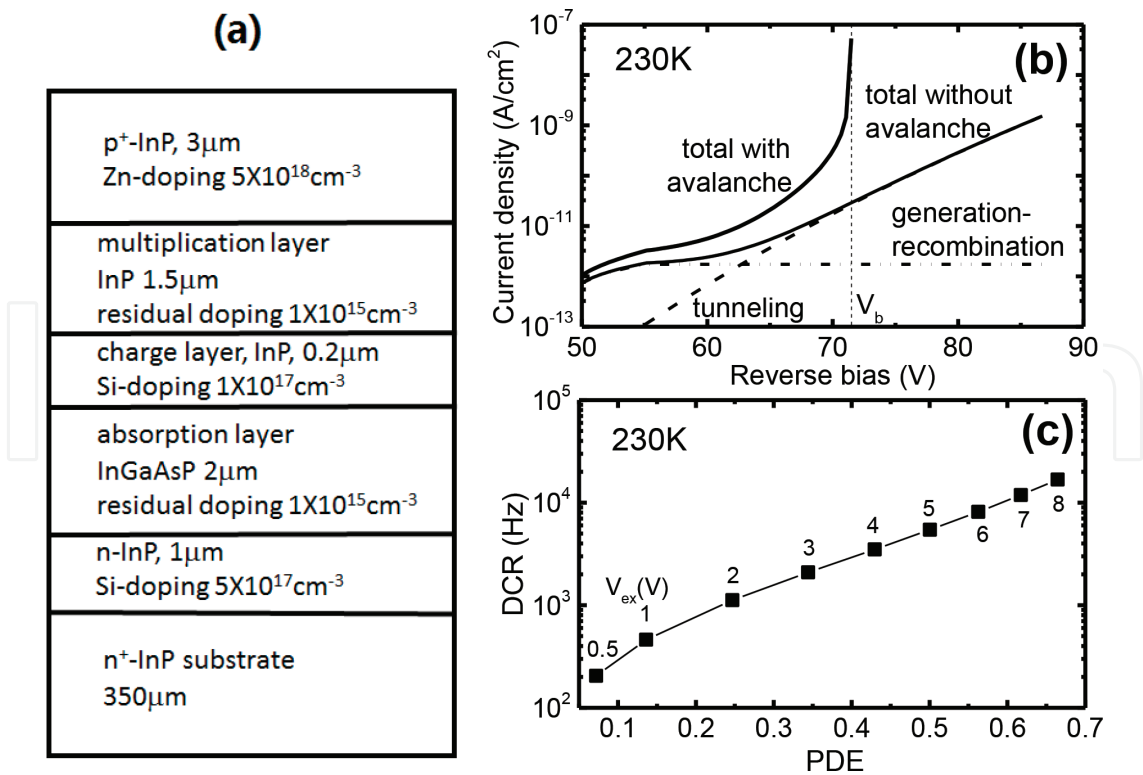

Figure 12. (a) The structure diagram of a designed InGaAsP/InP Geiger-mode APD (or SPAD) studied in this work; (b) calculated *I-V* relationship in dark and (c) calculated DCR versus PDE for the InGaAsP/InP SPAD device at 230 K.

effective V_{ex} will vary from this to that pixel so that device performance exhibits inhomogeneity. To clarify this effect, we first set any structure parameter t randomly changing in a way as

$$t_i = t_0(1 + W\sigma_i),\tag{1}$$

where the subscription $i = 1, 2, 3$ is the calculation sequence number in a series of simulations, t_i is the ith value of parameter t, t_0 is the designed value of t, W is the fluctuation degree of t relative to t_0, and σ_i is the ith value of the random variable σ, distributed in a normal mode with full width at half maximum (FWHM) of unity. Similarly we can set

$$n_{ci} = n_{c0}(1 + W_{nc}\sigma_{nci}),$$
$$t_{mi} = t_{m0}(1 + W_{tm}\sigma_{tmi}),\tag{2}$$

and so forth, where $n_{ci}(t_{mi})$ is the ith value of charge density n_c (multiplication width t_m), $n_{c0}(t_{m0})$ is the designed value of $n_c(t_m)$, $W_{nc}(W_{tm})$ is the relative FWHM of $n_c(t_m)$ with respect to $n_{c0}(t_{m0})$, and $\sigma_{nci}(\sigma_{tmi})$ is the ith value of σ for changing $n_c(t_m)$. All the variables are defined in a similar way to the above. The structure parameters are changing independently because each has its own FWHM and σ values. With a set of structure parameters (n_{ci}, t_{mi},...), one set of device performance data is calculated. With thousand sets of device performance data, distributions of V_b, V_{ex}, r_d, and η are obtained through statistics, and then the correlation between the performance fluctuations and device structures is figured out.

Our simulations show that n_c, t_m and t_c (charge layer thickness) have strong effects, while absorption layer doping level n_a, thickness t_a and multiplication layer doping level n_m have weak effects on V_{ex}. The strong t_m effect can be easily understood since the width of the multiplication region is crucial to determine the characteristics of a SPAD [48, 54]. It means that the charge quantity should be controlled most precisely in design and epitaxy process. In addition, we see that every single structure parameter leads to V_{ex} fluctuation in a linear manner.

Extending the above simulation to more structure parameters, the homogeneity of device performance can be obtained in terms of varying parameter numbers. The result of V_{ex} is displayed in **Figure 13(a)**, where a sublinear change of V_{ex} fluctuation is seen to happen with increasing parameter number. Taking all of the six parameters into account, we get that V_{ex} varies with a FWHM of 24%, far less than a simple summation of the effects of individual parameters. The V_{ex} distribution arisen by six independently varying parameters is demonstrated in **Figure 13(b)**. With the referred excess bias $V_{ex0} = 5$ V, the practical value of V_{ex} varies mainly in the range of 4.4–5.6 V, quite good for many applications. It may be also worthy to get the effects on other performance characters. **Figure 13(c)** presents the variation of DCR r_d, which exhibits a roughly normal distribution with a wide relative FWHM (54%). In detail, the worst DCR is some 30% higher than the designed value, which is acceptable in applications. **Figure 13(d)** displays the distribution of PDE η, normal with a narrow relative width (17%). It suggests a PDE change within 0.46–0.54, which is homogeneous enough in many applications.

The reason why the DCR fluctuation is much larger than PDE is that DCR depends almost exponentially on V_{ex} and PDE, as **Figure 12(c)** shows.

In realistic epitaxial growth, controlling the thickness or the doping level may usually have a common precision in different layers, although a non-dope layer would have worse carrier density fluctuation than the intentionally doped regions. The following thus shows a way more effective to investigate the uncertainty correlation between the epitaxy growth and the device performance. Let us study the device characteristics varying with common fluctuation width W_{nd} of the residual carrier densities in the absorption layer and the
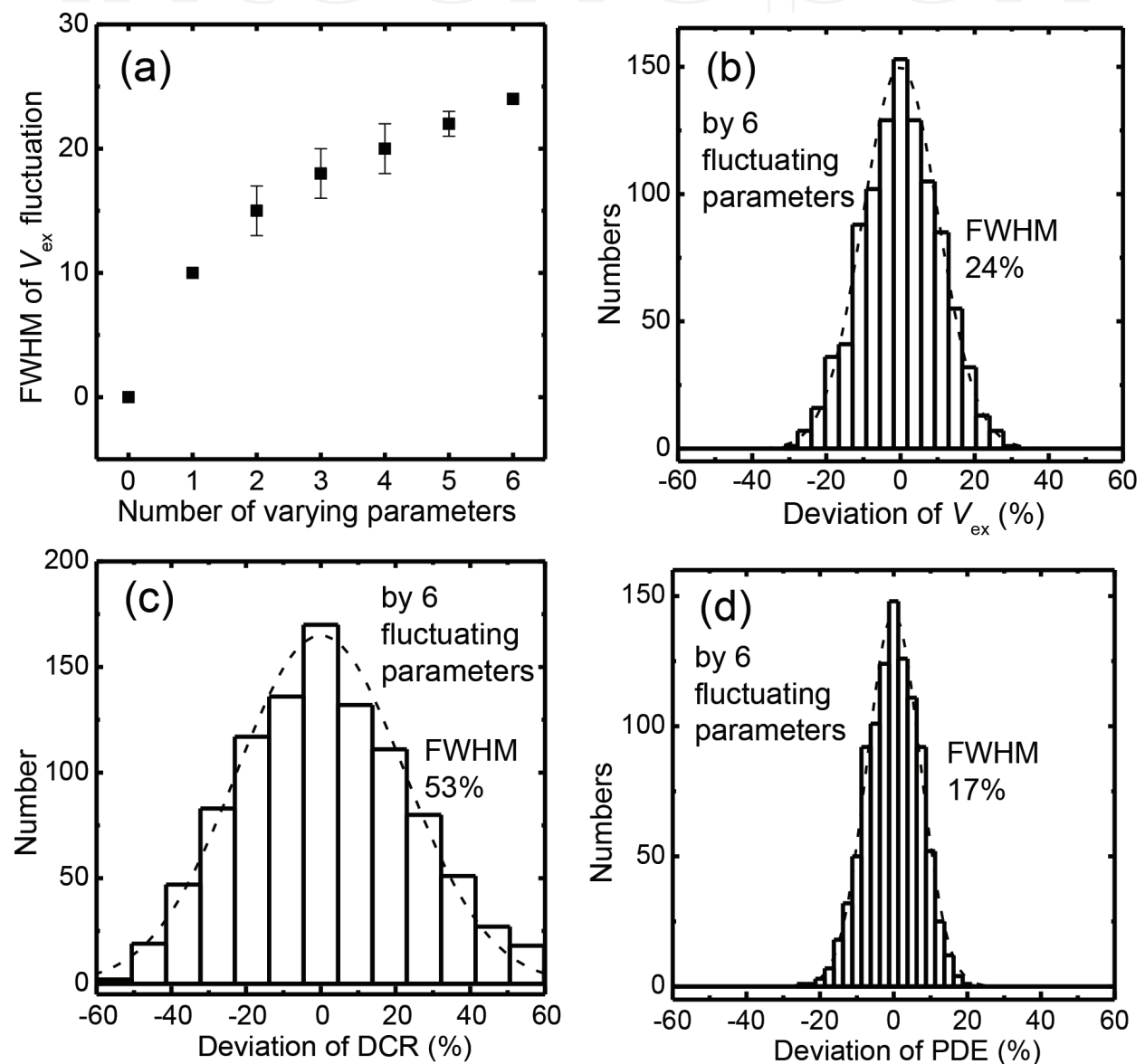

Figure 13. (a) Simulated distribution FWHM of the excess bias V_{ex} dependent of the number of simultaneously varying parameters; distribution histograms of (b) V_{ex}, (c) DCR and (d) PDE brought about by six simultaneously varying parameters including the doping level and the width of the absorption region n_a and t_a, of the charge layer n_c and t_c, and of the multiplication region n_m and t_m, respectively. The dashed lines on the histograms indicate the fitted results to normal distributions.

multiplication layer, common fluctuation width W_t of the widths of the absorption, charge and multiplication regions, and fluctuation width W_n of the doping level in the charge layer, that reads

$$
\begin{aligned}
n_{ai} &= n_{a0}(1 + W_{nd}\,\sigma_{nai}),\\
n_{mi} &= n_{m0}(1 + W_{nd}\,\sigma_{nmi}),\\
n_{ci} &= n_{c0}(1 + W_{n}\,\sigma_{nci}),\\
t_{ai} &= t_{a0}(1 + W_{t}\,\sigma_{tai}),\\
t_{mi} &= t_{m0}(1 + W_{t}\,\sigma_{tmi}),\\
t_{ci} &= t_{c0}(1 + W_{t}\,\sigma_{tci}).
\end{aligned}
\tag{3}
$$

One typical trial is to examine the dependence on two fluctuating parameters while remaining the others fixed. With W_{nd} fixed, **Figure 14** shows the V_{ex} contours as functions of W_n and W_t. From these data, the precision range of epitaxy growth required for definite performance homogeneity can be clearly seen. At first, two conditions with 10 and 20% of W_{nd} appear close to each other, especially for high V_{ex} variations, owing to the weak effect of the carrier density in non-dope layer. The relationship between W_n and W_t is far away from a linear curve but more like a circle for a finite V_{ex} fluctuation. To constraint V_{ex} fluctuation below a certain value, the fluctuations in thickness and charge control should roughly follow

$$
W_n^2 + W_t^2 < W_x^2,
\tag{4}
$$

where W_x is a certain precision control value of thickness and charge. Quantitatively speaking, V_{ex} relative fluctuations below 50, 40, 30 and 20% need W_x values of about 4, 3, 2 and 1%, respectively.
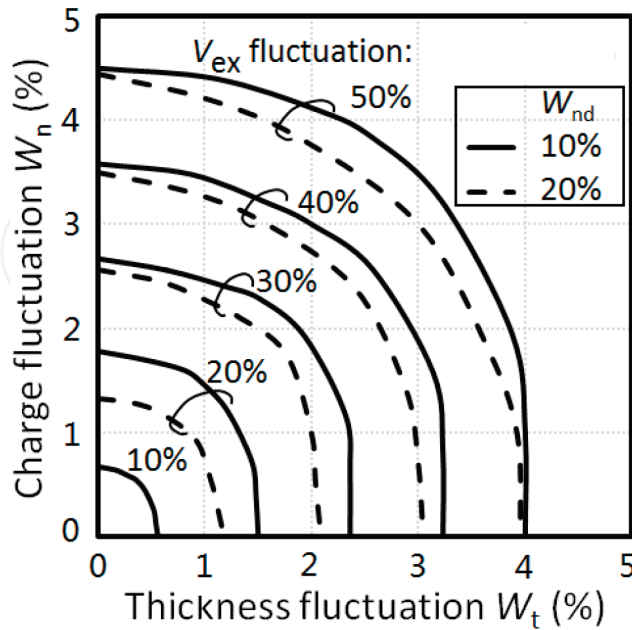

Figure 14. Contours of V_{ex} fluctuation width as a function of the thickness and doping level fluctuation widths W_t and W_n, under different fixed fluctuation widths of the residual carrier density in the non-dope layers W_{nd}.

In conventional growth, it is more difficult to control doping than thickness. Based on the result of **Figure 14**, as the thickness control can be better than 1–2%, V_{ex} homogeneity of 50, 40 and 30% could be realized by constraining the charge precision within 4–4.5, 3–3.6 and 2–2.7%, respectively. Viewed from another angle, the result is suggestive of a large space to tradeoff between the controls in thickness and charge. The example of V_{ex} fluctuating below 50% with $W_{nd} = 10\%$ suggests that the thickness (charge) precision $W_t(W_n)$ is better to be as small as 1% if $W_n(W_t)$ just satisfies 4.5%(4%), while $W_t(W_n)$ could be roughened to 3%(3.5%) if $W_n(W_t)$ weakly decreases to be about 3.5%(3%). In general, limiting the device inhomogeneity (in term of V_{ex}) below 50, 40, 30, and 20% needs the thickness and charge be controlled to a precision degree better than 3–3.2, 2.4–2.6, 1.7–1.9, and 0.9–1.2%, respectively. Since these degrees of control accuracies are easy or possible in epitaxy growth, InGaAsP/InP SPAD arrays are now producible in many laboratories [55–57] including our group, as will be described below. In order to finely limiting the device homogeneity, such as with V_{ex} fluctuation less than 10%, the thickness and charge should be controlled better than 0.5% in fluctuation, together with non-dope carrier density controlling within 10%. This degree of epitaxy precision is quite a challenging technique. It is possibly one of the reasons why it is presently still difficult to prepare 512 × 512 or larger scale SPAD arrays. Obviously, the above method is very helpful and effective to quantitatively correlate the controllability of multiple structure parameters with the SPAD device homogeneity.

4.2. Fabrication of InGaAsP/InP SPAD arrays

InP based APDs must use epitaxial materials. Firstly, we prepared APD materials with the main structure as shown in **Figure 12(a)** by using metal organic chemical vapor deposition (MOCVD). MOCVD growth is performed to satisfy the material uniformity requirements described above. On this epitaxial wafer, SPAD device structure as shown by **Figure 15** will be fabricated. As an array, there are isolating grooves (channels) between the pixels, Indium shots on the front side for interconnection and micro-lenses on the backside for light collection.

The key processes to fabricate the InGaAsP/InP SPAD arrays are as follows. First the active p-n junction is formed by selective diffusion. The diffusion process includes, thermally
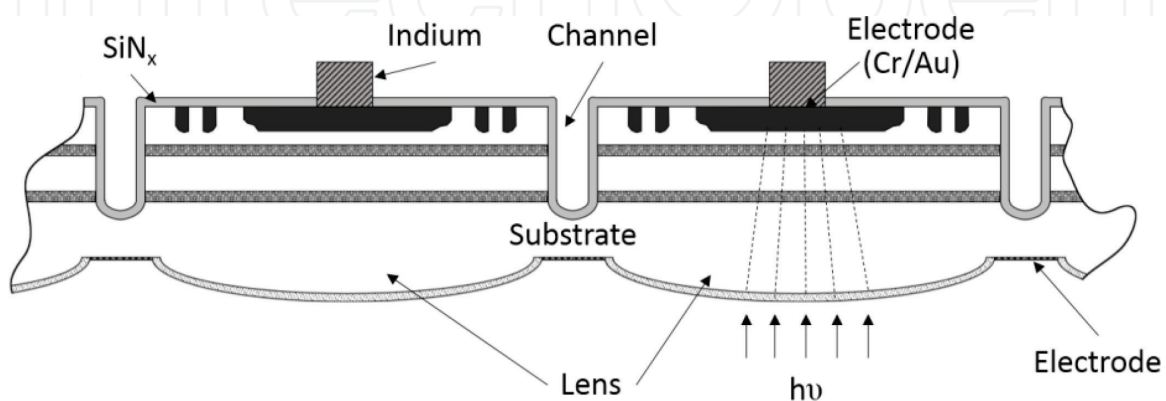

Figure 15. Structure of InGaAsP/InP SPAD array chip.

evaporating one layer of solid Zn_3P_2, depositing one layer of SiN_x to thoroughly cover Zn_3P_2, rapid thermal annealing to diffuse Zn into the chip, and etching off the SiN_x and the resident Zn_3P_2. To make the response time of a SPAD device shorter than 5 ns, the active area (the p-n junction area) of a pixel is made to be less than ϕ100 μm. Considering the guard-rings, the lateral depletion width and the diffusion length of electrons and holes, the distance between neighboring pixel centers is taken to be 300 μm. To suppress the cross-talk between pixels, the isolation between pixels is, besides the deep grooves, aided by highly resistive p-n junction. To increase the filling factor, light is incident on the backside, where there fabricated micro-lenses for each pixel. The microlenses here are not bonded onto the backside, but directly fabricated on the backside by specific dry-etching.

The fabricated SPAD array is characterized as shown in **Figure 16**. Measurements on material properties show that residual carrier density, layer thickness, and doping level fluctuations in a 10×10 mm^2 area appear about 8, 0.8 and 1.5%. On such a chip, 32×32–64×64 arrays of SPADs were developed and characterized at low temperatures. Under gated mode with gate repetition rate of 500 kHz and gate width of 10 ns, DCR and PDE were measured using a single-photon laser at 1.06 μm. The afterpulsing probability is controlled below 2% by setting the dead time to be ~2 μs. As presented by the inset in **Figure 16**, various pixels have dark I-V curves with V_b (defined to be the bias at 10 μA) weakly changing but around 75 V. **Figure 16** shows that, the fluctuation in the excess bias distributes in a normal way with FWHM of 14%, which is consistent with the simulated value 18%, and compatible with an estimation based on **Figure 16**. The DCR and PDE vary normally with FWHM of 31 and 10%, and this is also consistent with the simulated values 37 and 12%, respectively.

The ROIC is designed in a way similar to that of Si SPAD arrays. The interconnection is a standard indium-shot inversion-bonding process. After packaging into a vacuum can with
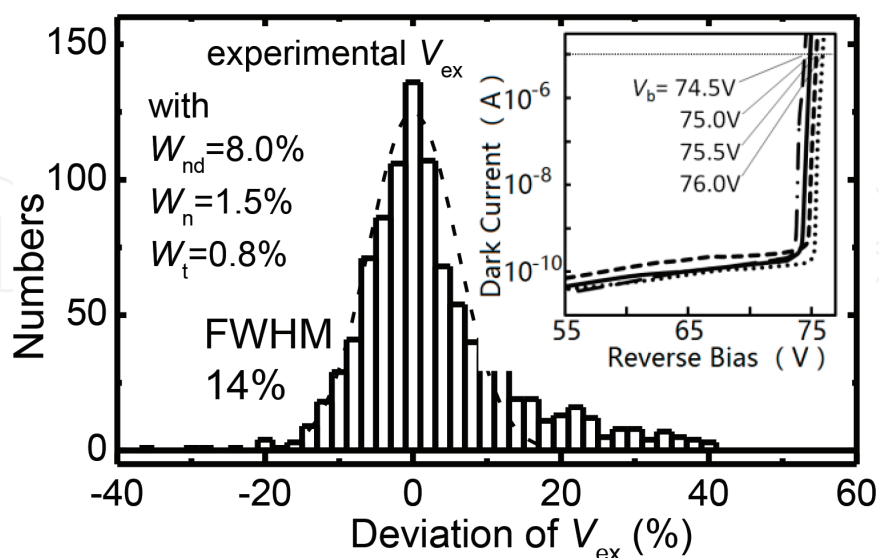

Figure 16. An experimental result of V_{ex} fluctuation distribution of InGaAsP/InP SPAD array. The dashed line represents the fitting to a normal distribution. The inset exhibits the I-V curves in dark of a few typical InGaAsP/InP SPAD devices.

Figure 17. Imaging by a LADAR instrument with 64 × 64 InGaAsP/InP SPAD focal-plane array detectors.

a transparent window, the InGaAsP/InP SPAD array is developed and can be used in an imaging system.

4.3. Application of the InGaAsP/InP SPAD arrays

A 64 × 64 InGaAsP/InP SPAD array device is installed onto the focal plane of a LADAR system. Under 1.06 μm laser irradiation, the scence 1–3 km away was successfully imaged with 3D information, as shown in **Figure 17**.

5. Summary

APDs are being more and more widely and deeply studied to satisfy the requirement in weak light and single photon imaging. The progresses of this worldwide study, especially the distinctive researches and achievements in SITP and UESTC are reviewed. We successfully fabricated up to 64 × 1 linear-mode Si APD array, and 32 × 32–64 × 64 Si SPAD arrays, and applied them in LADAR platforms like driverless vehicles. Also, we developed 32 × 32-64 × 64 InGaAsP/InP SPAD arrays, and constructed 3D imaging LADAR using them. Together with the progresses of other groups and other materials, we see a prospective future for the development and application of focal-plane APDs.

Acknowledgements

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