Chapter 4

Analysis for Higher Voltage at Downstream Node, Negative Line Loss and Active and Reactive Components of Capacitor Current, and Impact of Harmonic Resonance

Sushanta Paul

Additional information is available at the end of the chapter

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Abstract

In a study, it was found that the voltage at the downstream node is higher than the voltage at the upstream node, even though all the current flows from the upstream node to the downstream node. In IEEE's load flow simulation results for the 13-bus system, 34-bus system, and 123-bus system, it was also found that line losses in some feeders are negative. In this chapter, it has been analyzed how higher voltage at the downstream node and negative line losses in a phase appear in an AC power system. It has also been demonstrated that even though a capacitor generates only reactive power, its current has both active and reactive components with respect to the system reference. Finally the impact of harmonic resonance on capacitor has been discussed.

Keywords: capacitors, line loss, load flow, power system simulation, reactive power

1. Introduction

We generally know that current flows from high voltage to low voltage and this is true for a DC system but that does not apply to an AC system, because it can be seen that even though current is flowing from upstream node to downstream node, voltage at downstream node is higher than the voltage at upstream node. The reason of having higher voltage at downstream node in an AC system is that voltage drop in a single phase depends on mutual impedance and current in other phases besides self-impedance and current of its own phase. In [1], Vienna

rectifier (three-phase/three-switch converter) and Z-source inverter (ZSI) have been proposed with fewer number switches to boost the DC voltage and reduce the voltage sag.

Load flow simulation results for 13-bus system, 34-bus system, and 123-bus system show that line losses in some feeders are negative. Negative line losses may appear in the lighted loaded phase in unbalanced system. Distribution system is practically unbalanced system because of unbalanced loads and having single-phase and two-phase lines. From the operational standpoint, unbalanced conditions typically occur in the normal operation of aggregated loads or during short periods of abnormal operation with unbalanced faults or with one/two phases out of service [2].

Generally there are two approaches to measure the line losses. One is classical approach where line losses are computed as the difference between input power at upstream node and output power at downstream node; in this approach, losses in neutral and dirt are included in each single phase of a three-phase line. In other approaches, line losses are computed as (I^2R), phase resistance multiplied by current squared. In this second approach, losses in neutral and dirt need to be calculated separately to determine the total three-phase losses. In the study, for example, the IEEE 13-bus system, it is seen that some single-phase lines have negative line losses and that negative line losses show up in the classical approach. It needs to be mentioned that, although single-phase line losses may appear as negative in the first approach, total three-phase losses are the same as total three-phase losses determined in the second approach and these have been shown in [3]. Even though negative line losses appear in classical approach-based line loss computation, there is no physical explanation of negative line losses where positive line losses are considered as electrical energy that dissipates as heat energy when electric current flows through the line. In [2], Carpaneto et al. proposed a resistive component-based loss partitioning (RCLP) method. Their results show that even though single-phase line losses obtained by RCLP method differ from line losses obtained by classical approach, three-phase line losses obtained by RCLP method are the same as three-phase line losses obtained by classical approach. In our previous work [4], it has been shown that line losses increase or decrease at reduced voltage, depending on the types of the loads. In [5], it was demonstrated how temperature, depending on the type of the load, influences the variations in line losses.

A capacitor has huge application in the power system for reactive power compensation. It can provide several benefits such as voltage profile improvement, line loss reduction, and power factor correction. We know capacitor provides the reactive power, but its current has both active and reactive components with respect to the system reference. Capacitive reactance can cause resonance with the system inductance resulting in high harmonic voltage or current depending on the parallel or series resonance.

In this paper, in Section 2, it was analyzed how downstream node voltage can be higher than the voltage at upstream node. Section 3 demonstrates how negative line losses appear in a single phase in classical approach of line loss calculation. In Section 4, it was presented that capacitor current has both active and reactive components with respect to the system reference, even though a capacitor generates only reactive power. In Section 5, the impact of harmonic resonance on the capacitor, series and parallel resonances, and harmonic mitigation technique has been discussed.

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2. Analogy on higher voltage at downstream node

For a DC system, current flows from high voltage to low voltage, but that does not apply to an AC system shown in **Figure 1**, because in the study, it was seen that even though current flows from upstream node to downstream node, voltage at downstream node is higher than the voltage at upstream node. The reason of having higher voltage at downstream node in an AC system is that voltage drop in a single phase depends on mutual impedance and current in other phases besides self-impedance and current of its own phase as shown in Eq. (1).

$$\begin{bmatrix} V_{agm} \\ V_{bgm} \\ V_{cgm} \end{bmatrix} = \begin{bmatrix} V_{agn} \\ V_{bgn} \\ V_{cgn} \end{bmatrix} - \begin{bmatrix} Z_{aa} & Z_{ab} & Z_{ac} \\ Z_{ba} & Z_{bb} & Z_{bc} \\ Z_{ca} & Zcb & Z_{cc} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{1}$$

$$V_{igm} = V_{ign} - \Delta V_i \tag{2}$$

Now,

$$|V_{ign}| = \sqrt{\left(\Re e\left[V_{ign}\right]\right)^2 + \left(\mathrm{Im}\, g\left[V_{ign}\right]\right)^2} \tag{3}$$

$$|V_{igm}| = \sqrt{\left(\Re e\left[V_{ign}\right] - \Re e[\Delta V_i]\right)^2 + \left(\mathrm{Im}\, g\left[V_{ign}\right] - \mathrm{Im}\, g[\Delta V_i]\right)^2} \tag{4}$$

where V_{ign} and V_{igm} are the voltages of phase $i(i = a, b, c)$ at the upstream node and downstream node, respectively; ΔV_i is voltage drop in phase i; $\Re e\left[V_{ign}\right]$ and $\mathrm{Im}\, g\left[V_{ign}\right]$ are, respectively, real and imaginary components of V_{ign}; $\Re e[\Delta V_i]$ and $\mathrm{Im}\, g[\Delta V_i]$ are, respectively, real and imaginary components of ΔV_i.

Phase voltage at the downstream will be higher than the phase voltage at the upstream node if

$$\begin{aligned} &|V_{igm}| > |V_{ign}| \\ &\Rightarrow \sqrt{\left(\Re e\left[V_{ign}\right] - \Re e[\Delta V_i]\right)^2 + \left(\mathrm{Im}\, g\left[V_{ign}\right] - \mathrm{Im}\, g[\Delta V_i]\right)^2} > \sqrt{\left(\Re e\left[V_{ign}\right]\right)^2 + \left(\mathrm{Im}\, g\left[V_{ign}\right]\right)^2} \\ &\Rightarrow (\Re e[\Delta V_i])^2 + (\mathrm{Im}\, g\Delta V_i)^2 - 2^*\Re e\left[V_{ign}\right] * \Re e[\Delta V_i] - 2^*\mathrm{Im}\, g\left[V_{ign}\right] * \mathrm{Im}\, g[\Delta V_i] > 0 \end{aligned} \tag{5}$$

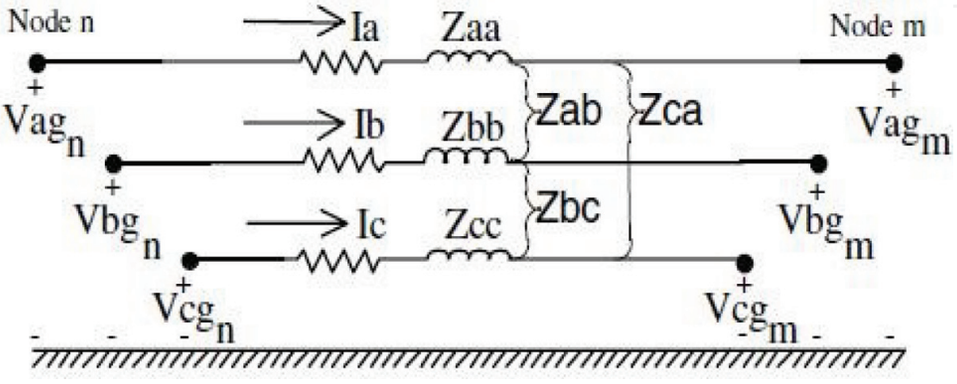

Figure 1. Three-phase line.

Similarly, phase voltage at downstream will be lower than the voltage at upstream node if

$$\begin{gathered} |V_{igm}| < |V_{ign}| \\ \sqrt{\left(\Re e\left[V_{ign}\right] - \Re e[\Delta V_i]\right)^2 + \left(\operatorname{Im} g\left[V_{ign}\right] - \operatorname{Im} g[\Delta V_i]\right)^2} < \sqrt{\left(\Re e\left[V_{ign}\right]\right)^2 + \left(\operatorname{Im} g\left[V_{ign}\right]\right)^2} \\ \Rightarrow (\Re e[\Delta V_i])^2 + (\operatorname{Im} g \Delta V_i)^2 - 2^* \Re e\left[V_{ign}\right] * \Re e[\Delta V_i] - 2^* \operatorname{Im} g\left[V_{ign}\right] * \operatorname{Im} g[\Delta V_i] < 0 \end{gathered} \tag{6}$$

Now, in Eq. (4), if real components of upstream node voltage (V_{ign}) and voltage drop (ΔV_i) have the same sign and imaginary components of upstream node voltage (V_{ign}) and voltage drop (ΔV_i) also have the same sign, then upstream node voltage must be higher than downstream node voltage. Similarly, in Eq. (4), if real components of upstream node voltage $\left(V_{ign}\right)$ and voltage drop (ΔV_i) have opposite sign and imaginary components of upstream node voltage $\left(V_{ign}\right)$ and voltage drop (ΔV_i) also have opposite sign, then upstream node voltage must be lower than downstream node voltage. Again, in Eq. (4), if real components of upstream node voltage $\left(V_{ign}\right)$ and voltage drop (ΔV_i) have the same sign, but imaginary components of upstream node voltage $\left(V_{ign}\right)$ and voltage drop (ΔV_i) have the opposite sign or if real components of upstream node voltage $\left(V_{ign}\right)$ and voltage drop (ΔV_i) have the opposite sign, but imaginary components of upstream node voltage Vig_n and voltage drop (ΔV_i) have the same sign, then the upstream node voltage can be higher or lower than the downstream bus voltage. **Figure 2** shows how (+ and −) signs of real and imaginary components of upstream node voltage $\left(V_{ign}\right)$ and voltage drop (ΔV_i) change for their locations in four quadrants.

If upstream node's voltage phasor $\left(V_{ign}\right)$ and voltage drop phasor (ΔV_i) lie in the same quadrant, then real components of upstream node voltage $\left(V_{ign}\right)$ and voltage drop (ΔV_i) will have the same sign, and imaginary components of V_{ign} and ΔV_i will also have the same sign; in this case, upstream node voltage must be higher than downstream node voltage.

If upstream node's voltage phasor $\left(V_{ign}\right)$ and voltage drop phasor (ΔV_i) lie in two different quadrants which are exactly opposite (first and third quadrants or second and fourth quadrants), then real components of voltage $\left(V_{ign}\right)$ and voltage drop (ΔV_i) will have opposite sign, and imaginary components of V_{ign} and ΔV_i will also have opposite sign; in this case, voltage at the

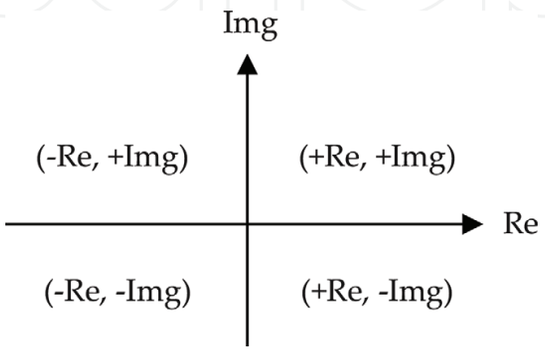

Figure 2. (+ and −) signs in four quadrants.

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upstream node must be lower than the voltage at the downstream node. Again, if upstream node's voltage phasor (V_{ign}) and voltage drop phasor (ΔV_i) lie in two different quadrants which are adjacent (first and second quadrants or second and third quadrants or third and fourth quadrants or fourth and first quadrants), then real components of V_{ign} and ΔV_i can have the same sign or opposite sign; if they have the same sign, then imaginary components of V_{ign} and ΔV_i will have the opposite sign; if they have opposite sign, then imaginary components of V_{ign} and ΔV_i will have the same sign; in these both cases, upstream node voltage can be higher or lower than the downstream node voltage. **Table 1** summarizes the conditions that cause the upstream node voltage to be higher or lower than the downstream node voltage.

How the downstream node voltage and voltage drop vary with loads in an AC system is tested on a two-bus system in **Figure 3**, and results are shown in **Table 2**.

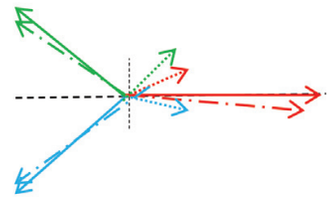
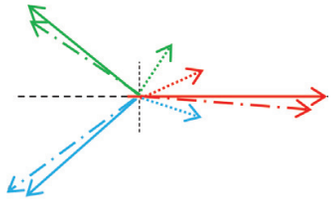
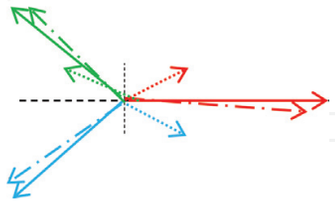
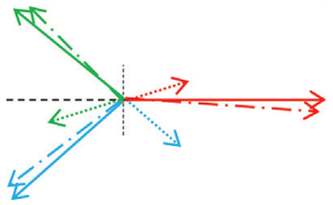
In **Table 2**, the phasor diagrams show how voltage drop and downstream node voltage change their locations into the quadrants as load varies. For example, when a three-phase load at node 2 changes from 1000 kW+ j500 kVAr, 500 kW+ j200 kVAr, and 300 kW+ j100 kVAr to 200 kW+ j100 kVAr, 500 kW+ j200 kVAr, and 300 kW+ j100 kVAr, respectively, in phase a, phase b, and phase c, it is seen that voltage drop phasor ΔV_a changes its location from first quadrant to fourth quadrant and voltage drop phasor ΔV_c changes its location from first quadrant to third quadrant.

When a three-phase load, 600 kW + j300kVAr, 500 kW + j200kVAr, and 300 kW + j100kVAr, is connected at the downstream node 2 in phase a, phase b, and phase c, respectively, it is seen that phase c voltage (2394.8 V) at the downstream node 2 is lower than the phase c voltage (2400 V) at the upstream node 1, where voltage phasor V_{cgn} at the upstream node 1 and voltage drop phasor ΔV_c lie in the same quadrant (second). Again, when the three-phase load changes

Location of upstream node voltage (Vig_n) and voltage drop (ΔVi) phasors into the quadrants		**Upstream node voltage level with respect to downstream node voltage level**
Same quadrant		$\lvert V_{ign}\rvert > \lvert V_{igm}\rvert$
Different quadrants	Exactly opposite quadrants	$\lvert V_{ign}\rvert < \lvert V_{igm}\rvert$
	Adjacent quadrants	$\lvert V_{ign}\rvert > \lvert V_{igm}\rvert$ or $\lvert V_{ign}\rvert < \lvert V_{igm}\rvert$

Table 1. Conditions for the upstream node voltage to be higher or lower than downstream node voltage.

Figure 3. Two-bus system.

	Bus voltage (V)	Voltage drop (V)	Phasor diagram of bus voltages and voltage drop	Load (kW, kVAr)
Bus 1	2400∠0 (2400 + j0) 2400∠-120 (−1200−j 2078.5) 2400∠120 (−1200 + j2078.5)			
Bus 2	2261.0∠−2.4 (2259−j 95.4) 2426.4∠−121.8 (−1280.2−j2061.2) 2386.9∠120.7 (−1218.8 + j2052.2)	140.98 + j95.44(170.2∠34.09) 80.22–j17.26(82.1∠−12.14) 18.75 + j26.22 (32.23∠54.4)		1000 + j500 500 + j200 300 + j100
	2292.4∠−1.7148 (2291.4−j68.6) 2406.7∠−121.7 (−1265.1−j2047.3) 2389.1∠120.28 (−1205 + j2063)	108.59 + j68.61 (128.4∠32.3) 65.12−j31.13 (72.2∠-25.55) 4.97 + j15.5 (16.27∠72.22)		800 + j400 500 + j200 300 + j100
	2351.7∠−1.03 (2322.1−j41.6) 2368.1∠−121.6 (−1250.9−j2033.4) 2394.8∠119.9 (−1191.9 + j2073.8)	77.89 + j 41.56 (88.3∠28.08) 50.86−j 45.1 (67.97∠−41.56) −8.103 + j 4.64 (9.3∠150.17)		600 + j300 500 + j200 300 + j100
	2351.7∠−0.358 (2351.6−j14.7) 2368.1∠−121.48 (−1236.9−j2019.5) 2394.8∠119.5 (−1179.3 + j2084.3)	48.37 + j 14.7 (50.5∠16.89) 36.88−j 58.9 (69.5∠−57.98) −20.67−j 5.84 (21.5∠−164.2)		400 + j200 500 + j200 300 + j100

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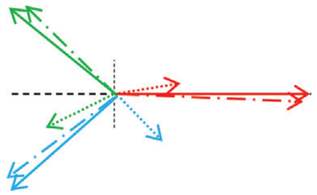
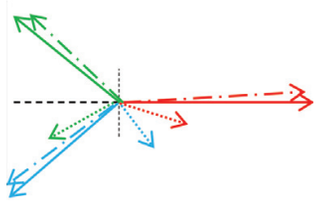
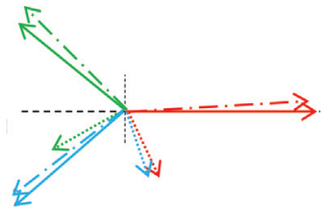
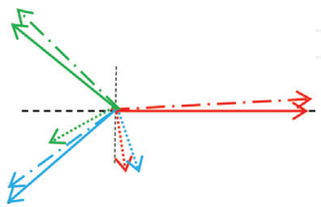
Bus voltage (V)	Voltage drop (V)	Phasor diagram of bus voltages and voltage drop	Load (kW, kVAr)
2365.90∠−0.029 (2365.9−j1.2) 2358.7∠−121.4 (−1230.3−j2012.5) 2396.7∠119.3 (−1173.2 + j2089.9)	34.13 + j 1.15 (34.15∠1.94) 30.284−j 65.99 (∠−65.35) −26.78−j11.4 (72.6∠−156.8)		300 + j150 500 + j200 300 + j100
2379.9∠0.29 (2379.9 + j12.1) 2349.6∠−121.4 (−1223.8−j2005.7) 2398.3∠119.1 (−1167.3 + j2095.0)	20.14−j 12.1 (23.5∠−30.9) 23.84−j 72.78 (76.5∠−71.8) −32.7−j 16.58 (36.6∠−153.1)		200 + j100 500 + j200 300 + j100
2394.0∠0.62 (2393.8 + j25.9) 2339.6∠−121.33 (−1216.7−j1998.3) 2400.4∠118.9 (−1161.2 + j2100.9)	6.15−j25.86 (26.58∠−76.6) 16.7−j80.12 (81.8∠−78.2) −38.8−j22.4 (44.8∠-150.02)		100 + j50 500 + j200 300 + j100
2400.1∠0.776 (2399.9 + j 0.032.5) 2335.8∠−121.3 (−1214.6−j1995.2) 2401.3∠118.8 (−1158.8 + j2103.2)	0.1−j32.52 (32.52∠−89.8) 14.6−j83.26 (84.5∠−80.04) −41.2−j24.76 (48.06∠−149)		50 + j25 500 + j200 300 + j100

Bus 1 phase a voltage: Bus 2 phase a voltage: Voltage drop in phase a:
Bus 1 phase b voltage: Bus 2 phase b voltage: Voltage drop in phase b:
Bus 1 phase c voltage: Bus 2 phase c voltage: Voltage drop in phase c:

Table 2. Variation in the location of node voltage phasors and voltage drop phasors with loads.

to 100 kW + j50kVAr, 500 kW + j200kVAr, and 300 kW + j100kVAr in respective phases, it is seen that phase c voltage (2400.4 V) at the downstream node 2 is higher than phase c voltage (2400 V) at the upstream node 1, where voltage phasor V_{cgn} at the upstream node 1 lies in second quadrant but voltage drop phasor ΔV_c lies in third quadrant.

3. Analogy on negative line loss

A classical approach of line loss calculation was presented here. In this approach, line loss was computed as the difference between input power at upstream node and output power at downstream node. The formulation of line loss equation and condition for negative line loss has been demonstrated using a two-bus system shown in **Figure 4**.

Line loss = input power – output power

$$\begin{aligned} P_{Loss} + jQ_{Loss} &= V_n I^* + V_m I^* \\ &= |V_n|\angle\alpha_n{}^*|I|\angle -\beta - |V_m|\angle\alpha_m{}^*|I|\angle -\beta \\ &= |V_n||I|\angle(\alpha_n - \beta) - |V_m||I|\angle(\alpha_m - \beta) \\ &= |V_n||I|\angle\theta_n - |V_m||I|\angle\theta_m \end{aligned} \tag{7}$$

Active power loss,

$$P_{Loss} = |V_n||I|\cos\theta_n - |V_m||I|\cos\theta_m \tag{8}$$

where input power is the power leaving the upstream node and output power is the power entering into the downstream node. $|V_n|\angle\alpha_n$ is the voltage at the upstream node n; $|V_m|\angle\alpha_m$ is the voltage at the downstream node m; $|I|\angle\beta$ is the current in the line between the node n and m; and $\theta_n = (\alpha_n - \beta)$ and $\theta_m = (\alpha_m - \beta)$ are the power factor angles at node n and m, respectively.

From Eq. (8), we can see that active line loss will be negative, if

$$\begin{aligned} & P_{Loss} < 0 \\ \Rightarrow\ & if, |V_n||I|\cos\theta_n - |V_m||I|\cos\theta_m < 0 \\ \Rightarrow\ & if, |V_n|\cos\theta_n < |V_m|\cos\theta_m \end{aligned} \tag{9}$$

Here, four cases are considered to demonstrate the conditions of occurrence of negative line losses:

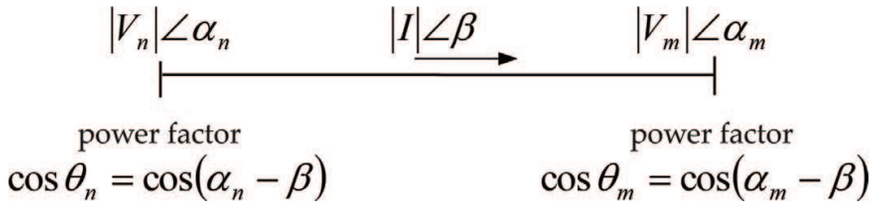


Figure 4. A line segment between upstream node n and downstream node m.

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Case 1: Downstream node voltage lags behind the upstream node voltage and leads the line current in **Figure 5**.

As voltage $|V_n|\angle\alpha_n$ leads voltage $|V_m|\angle\alpha_m$, we have

$$\begin{aligned} &\alpha_n > \alpha_m \\ \Rightarrow\ &(\alpha_n - \beta) > (\alpha_m - \beta) \\ \Rightarrow\ &\cos(\alpha_n - \beta) < \cos(\alpha_m - \beta) \\ \Rightarrow\ &\cos(\theta_n) < \cos(\theta_m) \end{aligned} \tag{10}$$

Since by Eq. (10), $\cos\theta_n < \cos\theta_m$ in Eq. (9), there is a possibility of $|V_n|\cos\theta_n < |V_m|\cos\theta_m$, i.e., $P_{Loss} < 0$, even though $|V_n| > |V_m|$. If upstream node voltage is lower than the downstream node voltage ($|V_n| < |V_m|$) that may happen in an AC system as shown in Section 2, then it confirms that $|V_n|\cos\theta_n < |V_m|\cos\theta_m$ (i.e., active line loss) must be negative.

Case 2: Downstream node voltage leads both the upstream node voltage and the line current as shown in **Figure 6**.

As voltage $|V_n|\angle\alpha_n$ lags the voltage $|V_m|\angle\alpha_m$, we have

$$\begin{aligned} &\alpha_n < \alpha_m \\ \Rightarrow\ &(\alpha_n - \beta) < (\alpha_m - \beta) \\ \Rightarrow\ &\cos(\alpha_n - \beta) > \cos(\alpha_m - \beta) \\ \Rightarrow\ &\cos(\theta_n) > \cos(\theta_m) \end{aligned} \tag{11}$$

Even though, by Eq. (11), $\cos\theta_n > \cos\theta_m$ in Eq. (9), there is still a possibility of $|V_n|\cos\theta_n < |V_m|\cos\theta_m$ (i.e., $P_{Loss} < 0$) if upstream node voltage is lower than the downstream node voltage $|V_n| < |V_m|$ which could happen very rarely. If the upstream node voltage is higher than the

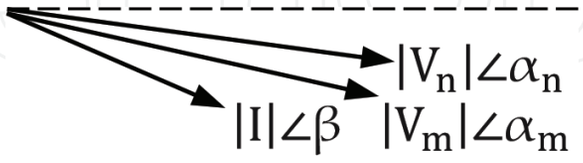

Figure 5. Phasor diagram for upstream and downstream node voltage and line current for Case 1.

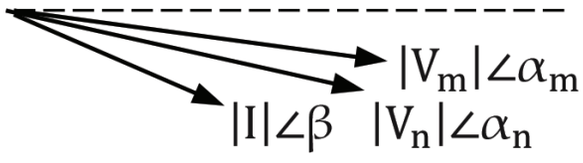

Figure 6. Phasor diagram for upstream and downstream node voltage and line current for Case 2.

downstream node voltage, $|V_n| > |V_m|$, then it is guaranteed that active line loss cannot be negative.

Case 3: Downstream node voltage lags behind both the upstream node voltage and the line current, as shown in **Figure 7**.

As voltage $|V_n|\angle\alpha_n$ leads voltage $|V_m|\angle\alpha_m$, we have

$$\alpha_n > \alpha_m$$
$$\Rightarrow (\alpha_n - \beta) > (\alpha_m - \beta)$$

[Since $(\alpha_n - \beta) < 0$ and $(\alpha_m - \beta) < 0$, multiply both sides by -1]

$$\Rightarrow -(\alpha_n - \beta) < -(\alpha_m - \beta)$$
$$\Rightarrow \cos(-(\alpha_n - \beta)) > \cos(-(\alpha_m - {}^{m}\beta))$$

$$[\text{Since } \cos(-(\alpha_n - \beta)) = \cos(\alpha_n - \beta) \text{ and } \cos(-(\alpha_m - \beta)) = \cos(\alpha_m - \beta)$$
$$\Rightarrow \cos(\theta_n - \beta) > \cos(\theta_m - \beta)$$
$$\Rightarrow \cos(\theta_n) > \cos(\theta_m) \quad (12)$$

Even though, by Eq. (12), $\cos\theta_n > \cos\theta_m$ in Eq. (9), there is still a chance of $|V_n| \cos\theta_n < |V_m| \cos\theta_m$, i.e., $P_{Loss} < 0$, if downstream node voltage is higher than the upstream node voltage ($|V_n| < |V_m|$). If downstream node voltage is lower than the upstream node voltage, ($|V_n| > |V_m|$), then it confirms that active line loss cannot be negative.

Case 4: Downstream node voltage leads the upstream voltage and lags behind the line current, as shown in **Figure 8**.

As voltage $|V_n|\angle\alpha_n$ lags voltage $|V_m|\angle\alpha_m$, we have

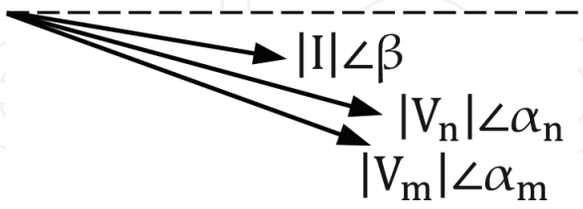

Figure 7. Phasor diagram for upstream and downstream node voltage and line current for Case 3.

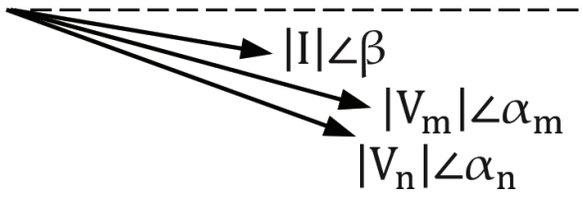

Figure 8. Phasor diagram for upstream and downstream node voltage and line current for Case 4.

$$\alpha_n < \alpha_m$$

$$\Rightarrow (\alpha_n - \beta) < (\alpha_m - \beta)$$

[Since $(\alpha_n - \beta) < 0$ and $(\alpha_m - \beta) < 0$, multiply both sides by -1]

$$\Rightarrow -(\alpha_n - \beta) > -(\alpha_m - \beta)$$

$$\Rightarrow \cos(-(\alpha_n - \beta)) < \cos(-(\alpha_m - {}^{m}\beta))$$

[Since $\cos(-(\alpha_n - \beta)) = \cos(\alpha_n - \beta)$ and $\cos(-(\alpha_m - \beta)) = \cos(\alpha_m - \beta)$]

$$\Rightarrow \cos(\theta_n - \beta) < \cos(\theta_m - \beta)$$

$$\Rightarrow \cos(\theta_n) < \cos(\theta_m) \tag{13}$$

Since, by Eq. (13), $\cos\theta_n < \cos\theta_m$ in Eq. (9), there is a possibility of $|V_n|\cos\theta_n < |V_m|\cos\theta_m$, i.e., $P_{Loss} < 0$, even though $(|V_n| > |V_m|)$. If downstream node voltage is higher than the upstream node voltage $|V_n| < |V_m|$, then it is confirmed that $|V_n|\cos\theta_n < |V_m|\cos\theta_m$, i.e., active line loss must be negative.

By and large, downstream node's power factor will be greater than upstream node's power factor if downstream node voltage lags behind the upstream node voltage and leads the line current or downstream node voltage leads the upstream voltage and lags behind the line current. In this case, if upstream node voltage is lower than downstream node voltage, then output power at downstream node will be higher than input power at upstream node, i.e., line loss must be negative.

Downstream node's power factor will be lower than upstream node's power factor, if downstream node voltage leads both the upstream node voltage and the line current or downstream node voltage lags behind both the upstream node voltage and the line current. In this case, there is a chance of getting a negative line loss, only if upstream node voltage is lower than downstream node voltage. **Table 3** summarizes the chances of occurrence of negative line loss in the classical approach-based line loss calculation.

Generally, transmission and distribution lines are inductive by nature; therefore, downstream node voltage leads the line current and lags behind the upstream node voltage. Downstream node voltage may lead the upstream node voltage in a lightly loaded phase in an unbalanced system. Both upstream and downstream node voltages can lag behind the line current for a system with too many capacitor banks for voltage profile improvements and/or line loss reduction.

Example 1: IEEE's load flow results in [6] show that, for 13-bus system shown in **Figure 9**, line loss in phase b feeder between substation voltage regulator's secondary side and node 632 is negative (−3.25 kW), which can be explained by Eq. (9). From IEEE's load flow results, phase b voltage at substation voltage regulator's secondary is $V_{bRG60} = 2521.86\angle -120$; phase b voltage at node 632 is $V_{b632} = 2502.65\angle -121.72$; and phase b current in that feeder is $I = 414.37\angle -140.91$.

Phasor diagram of V_{bRG60}, V_{b632}, and I is shown in **Figure 10**.

Lagging/leading status	Power factor (Pf)	Voltage level status	Occurrence of negative line loss
Downstream node voltage lags the upstream node voltage and leads the line current or downstream node voltage leads the upstream node voltage and lags the line current	Pf at downstream node > Pf at upstream node	If downstream node voltage < upstream node voltage	Possibility of occurrence of negative line loss
		If downstream node voltage > upstream node voltage	Guarantee of occurrence of negative line loss
Downstream node voltage leads both the upstream node voltage and the line current or downstream node voltage lags behind both the upstream node voltage and the line current	Pf at downstream node < Pf at upstream node	If downstream node voltage < upstream node voltage	No possibility of occurrence of negative line loss
		If downstream node voltage > upstream node voltage	Possibility of occurrence of negative line loss

Table 3. Conditions of occurrence of negative line loss.

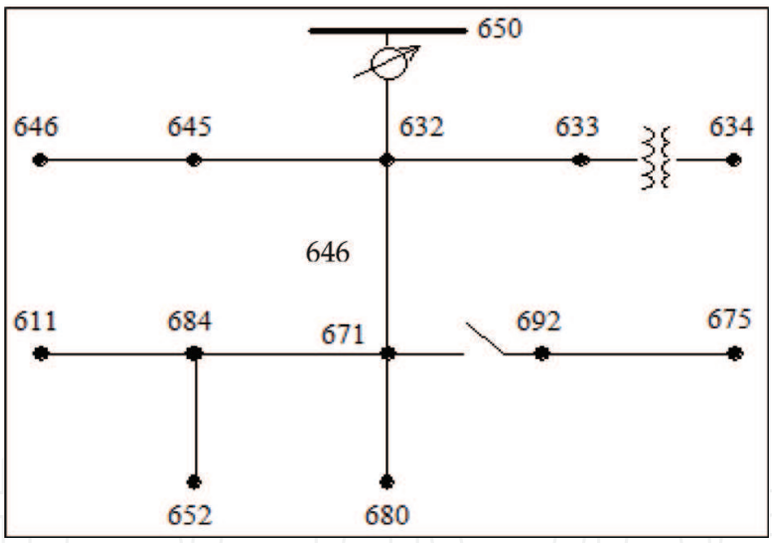

Figure 9. IEEE 13-bus system.

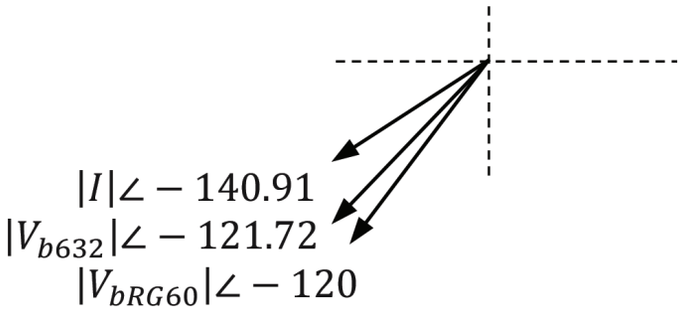

Figure 10. Phasor diagram of voltages and line current for the feeder between substation regulator and node 632.

By Eq. (8), active power loss is

$$P_{Loss} = |V_{bRG60}||I| \cos\theta_{bRG60} - |V_{b632}||I| \cos\theta_{b632}$$

$$= 2521.86*414.37*\cos(20.91) - 2502.65*414.37*\cos(19.19)$$

$$= 2521.86*414.37*0.93414 - 2502.65*414.37*0.9444$$

$$= 1044.985*0.93414 - 1037.023*0.9444 \text{ kW}$$

↓ ↓

The upstream node's power factor is less than the downstream node's power factor

$$= 976.16 - 979.36 \text{ kW}$$

$$= -3.2 \text{ kW}$$

The above power loss calculation shows that, although downstream node voltage (2502.65 V) is lower than upstream node voltage (2521.86 V), downstream node's power factor (0.9444) is higher than upstream node's power factor (0.93414). The upstream node's lower power factor makes the input power (976.16 kW = 2521.86*414.37*0.93414) lower than the output power (979.36 kW = 2502.65*414.37*0.9444) at the downstream node, even though all the active power at the downstream node comes from the upstream node. The reason of higher power factor at the downstream node is that downstream node lags behind the upstream node voltage and leads the line current as shown in **Figure 10**.

Example 2: IEEE's load flow results in [6] also show that, for 123-bus system shown in **Figure 11**, line loss in phase b feeder between node 101 and node 105 is negative (−0.019 kW), which can also be explained by Eq. (9). From IEEE's load flow results, phase b voltage at node

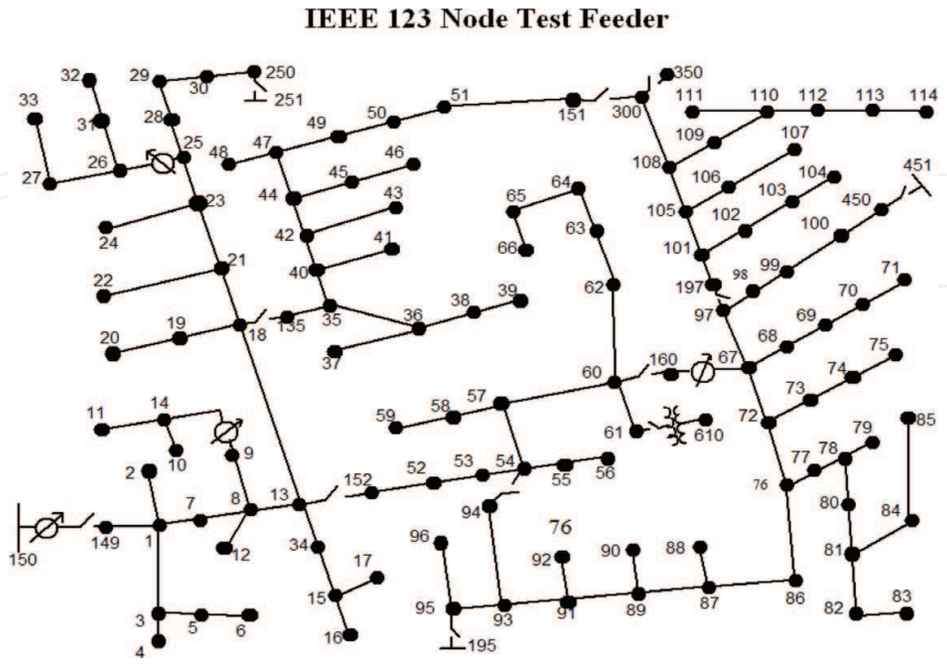

Figure 11. IEEE 123-bus system.

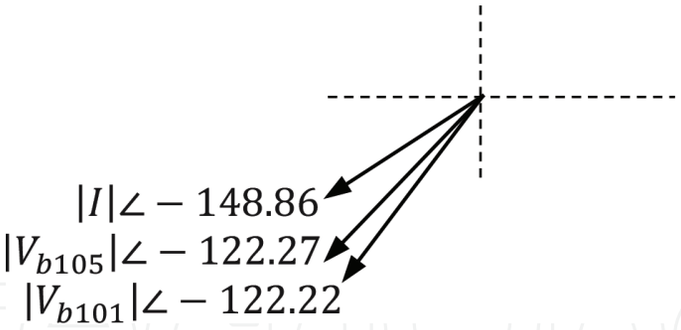

Figure 12. Phasor diagram of voltages and line current for the line between node 101 and node 105.

101 is $V_{b101} = 2474.55\angle -122.22 V_{b101} = 2474.55\angle -122.22$; phase b voltage at node 105 is $V_{b105} = 2474.07\angle -122.27 V_{b105} = 2474.07\angle -122.27$; and phase b current in that feeder is $I = 36.21 \angle -148.86 I = 36.21\angle -148.86$.

Phasor diagram of V_{b101}, V_{b105}, and I is shown in **Figure 12**.

By Eq. (8), active power loss is

$$P_{Loss} = |V_{b101}||I| \cos\theta_{b101} - |V_{b105}||I| \cos\theta_{b105}$$

$$= 2474.55*36.21*\cos(26.64) - 2474.07*36.21*\cos(26.59)$$

$$= 2474.55*36.21*0.893841424 - 2474.07*36.21*0.894232372$$

$$= 89603.455*0.893841424 - 89586.0747*0.894232372 \text{ kW}$$

↓ ↓

The upstream node's power factor is less than the downstream node's power factor

$$= 80.09128026 - 80.11076808 \text{ kW}$$

$$= -0.019487 \text{ kW}$$

In the line loss calculation above, it is seen that, although voltage (2474.55 V) at the upstream node is higher than the voltage (2474.07 V) at the downstream node, power factor (0.893841424) at the upstream node is less than the power factor (0.894232372) at the downstream node. The higher power factor at the downstream node makes the output power (80.11076808 kW = 2474.07*36.21*0.894232372*10^{-3}) at the downstream node greater than the input power (80.09128026 kW = 2474.55*36.21*0.893841424*10^{-3}) at the upstream node, even though all the active power at the downstream node comes from the upstream node. Greater output power at downstream node with respect to input power at upstream node is the reason of having a negative line loss.

4. Active and reactive components of capacitor current

Although a capacitor delivers reactive power, its current has both active and reactive components with respect to the system reference. The reason of having both active and reactive current components with respect to the system reference is that capacitor current leads the

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capacitor bus voltage by 90°, with bus voltage angle represented with respect to the system reference. Now the angle of a capacitor current with respect to the system reference is equal to the capacitor bus voltage angle plus 90°; the cosine and sine value of that angle of capacitor current make, respectively, the active and reactive current component of the capacitor current, where capacitor's current is only reactive with respect to capacitor bus voltage. Here it needs to be mentioned that if Kirchhoff's current law is applied at the capacitor bus, considering capacitor current is only reactive, then it does not satisfy the Kirchhoff's current law. If the angle of capacitor current is presented with respect to the system reference which results in both real and imaginary components of capacitor current, then it satisfies Kirchhoff's current law. These have been demonstrated with the load flow results of 13-bus system. Load flow results [6] of 13-bus system are given below for phase a of node 675 and line 692–675:

Voltage at node 675 is V_{675} = 0.9835∠−5.56°; current in line 692–675 is I_{Line} = 205.33∠−5.15°; load that is constant power load at node 675 is $P_{Load} + jQ_{Load}$ = 485 + j190; and output power of the capacitor is jQ_{Load} = j193.4.

Now, line current: $I_{Line} = 205.33\angle - 5.15^{\circ} = 204.501 - j18.43$

Load current: $|I_{Load}|^2 = \frac{P_{Load}^2 + Q_{Load}^2}{|V|^2}$

$$= \frac{485^2 + 190^2}{|0.9835^{*}2.40177|^2} = 48626.8$$

$$\Rightarrow |I_{Load}| = 205.33$$

If θ is the power factor angle, i.e., angle between voltage and current, then

$$\cos\theta = \frac{485}{\sqrt{485^2 + 190^2}} = 0.931,$$

$$\Rightarrow \theta = 21.39$$

Since the load current lags the voltage, we have

$$I_{Load} = 220.5148\angle\left(-5.56^{\circ} - 21.39^{\circ}\right) = 196.56 - j99.95$$

Capacitor current: $I_{Cap} = \frac{Q_{Cap}}{|V|}$

$$= \frac{193.44}{0.9835^{*}2.40177} = 81.8915$$

Here, if the capacitor current is assumed to be only reactive current, i.e., I_{Cap} = 81.89∠90°, then it does not satisfy Kirchhoff's current law ($\sum linecurrent + loadcurrent + capacitorcurrent = 0$) at the bus 675. Capacitor current I_{Cap} leads bus voltage V_{675} (0.9835∠−5.56°) by 90°; therefore, the angle between the system reference and capacitor current I_{Cap} is −5.56° + 90° = 84.44°, and I_{Cap} should be presented as I_{Cap} = 81.89∠84.44° = 7.93 + j81.51. It is seen that capacitor current I_{Cap} does not make a 90° angle with the system reference which is the phase a voltage of substation regulator. Therefore, capacitor current has both real and imaginary current components with

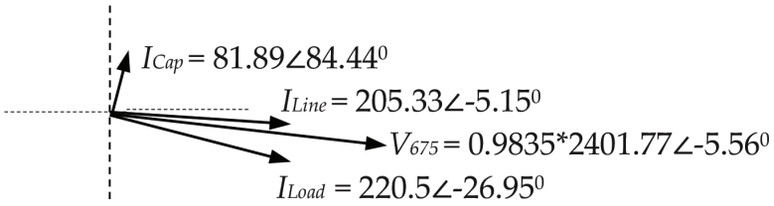

Figure 13. Phasor diagram of bus voltage, line current, and capacitor current.

respect to the system reference, whereas the output power of a capacitor is reactive. It needs to be mentioned that capacitor current is also only reactive with respect to capacitor bus voltage. **Figure 13** depicts the phasor diagram of I_{Line}, I_{Load}, I_{Cap}, and V_{675}.

Kirchhoff's current law is satisfied with the capacitor current, $I_{Cap} = 81.89\angle 84.44°$. It is seen at bus 675 in phase a:

$$P_{Line} + jQ_{Line} = V_{675} I^*_{Line}$$

$$= 0.9835^* 2.4017\angle - 5.56^* 205.3\angle - 5.15$$

$$= 485 + j3.47$$

If we apply the law of conservation of power at node 675 in phase a, we can see

$$\left(P_{Line} + jQ_{Line}\right) + \left(jQ_{cap}\right) = \left(P_{Load} + jQ_{\underset{=}{Load}}\right)$$

$$\Rightarrow (485 - j3.4) + (j193.44) = (485 + j190)$$

Here we can see that power consumed by the load is equal to the capacitor's output power plus power injected through the line, whereas line current is equal to capacitor current plus load current.

5. Impact of harmonic resonance on capacitor

Shunt capacitors are used for voltage profile improvement and power factor correction. A capacitor can cause resonance frequency which results in high voltage across the capacitor and severe voltage distortion. Therefore, it needs to verify if the shunt capacitive reactance will resonate with the system inductive reactance. A harmonic resonance will occur if

$$X_L h = X_C h$$

$$2\pi f h L = \frac{1}{2\pi f h C}$$

$$f h = \frac{1}{2\pi\sqrt{LC}}$$

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where X_L is the system reactance at fundamental frequency, X_C is the capacitive reactance at fundamental frequency, h is the harmonic order, and f is the fundamental frequency. L is the system inductance, and C is the capacitance of the shunt capacitor.

Formulation of relationship among harmonic order, capacitor-rated MVAR, and system fault MVA at the capacitor location:

At resonant condition,

$$2\pi fhL = \frac{1}{2\pi fhC}$$

$$h^2 = \frac{1}{2\pi fL} * \frac{1}{2\pi fC}$$

$$= \frac{1}{X_L} * X_C$$

$$= \frac{V * V * 10^6}{X_L} * \frac{X_C}{V * V * 10^6}$$

$$= I_{sc} * V * 10^6 * \frac{1}{I_C * V * 10^6}$$

$$= \frac{MVA_{SC}}{MVAR_C}$$

$$h = \frac{\sqrt{MVA_{SC}}}{\sqrt{MVAR_C}}$$

where V is the system voltage, I_{sc} is the available short circuit current at the capacitor location, and I_c is the rated current of the capacitor. MVA_{SC} is the available fault capacity at the capacitor location, and $MVAR_C$ is the rated reactive power of capacitor.

Harmonic current can have an adverse effect on the capacitor resulting in overloading, overheating, and voltage stress. As per IEEE 18-2000, capacitor shall deliver a maximum of 135% of its rated reactive power (kVAR). It also withstands a maximum continuous RMS overvoltage of 110%, peak overvoltage of 120%, and an overcurrent of 180% of rated value.

5.1. Series and parallel resonance

Whether a series or parallel resonance will occur or not depends on the system configuration. Nowadays the distribution system is a radial system. Motor loads in the system make the equivalent impedance lower at the capacitor location because at the short circuit, motor loads inject the current back to the system adding parallel circuits. Equivalent impedance of the system with dominant non-motor load is higher than the system with dominant motor load. Series and parallel resonance circuits are shown below (**Figures 14** and **15**).

5.1.1. Series resonance

$$\mathrm{I}\angle\Theta = \frac{\mathrm{V}\angle 0}{\mathrm{R} + \mathrm{j}2\pi fL - \frac{\mathrm{j}}{2\pi fC}}$$

$$|I| = \frac{|\mathrm{V}|}{\sqrt{R^2 + \left(2\pi fL - \frac{1}{2\pi fC}\right)^2}}, \angle\Theta = -\tan^{-1}\left(\frac{2\pi fL - \frac{1}{2\pi fC}}{R}\right)$$

|I| and ∠Θ vary with f. When $2\pi fL = \frac{1}{2\pi fC}$, |I| is maximum and ∠Θ = 0, i.e., current and voltage are in phase.

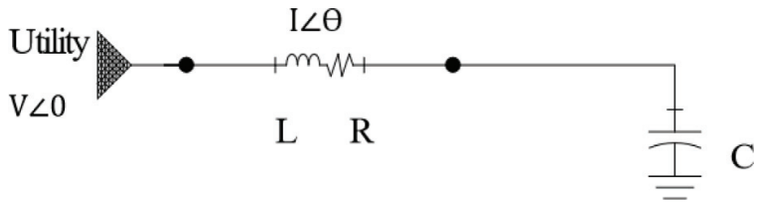

Figure 14. Series resonance circuit.

5.1.2. Parallel resonance

$$\mathrm{V}\angle\Theta = \frac{I\angle 0}{Y}$$

where

$$Y = \frac{1}{R} + j2\pi fC + \frac{1}{j2\pi fL}$$

$$|V| = \frac{|\mathrm{I}|}{\sqrt{\left(\frac{1}{R}\right)^2 + \left(2\pi fC - \frac{1}{2\pi fL}\right)^2}}, \angle\Theta = -\tan^{-1}\left(\frac{2\pi fC - \frac{1}{2\pi fL}}{\frac{1}{R}}\right)$$

|V| and ∠Θ vary with f. When $2\pi fC = \frac{1}{2\pi fL}$, |V| is maximum and ∠Θ = 0, i.e., current and voltage are in the same phase.

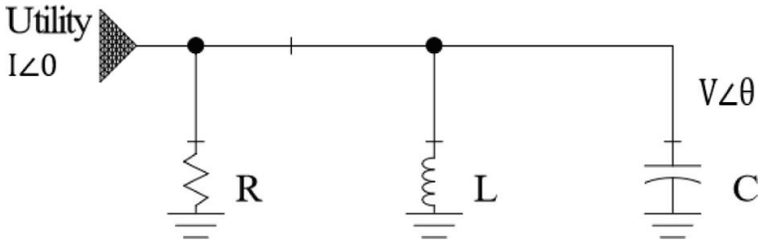

Figure 15. Series resonance circuit.

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5.2. Harmonic mitigation methods

There are several techniques to mitigate harmonic distortions. The following are the prevailing methods for mitigating the harmonic distortions:

(i) Reactor**:** Reactor is a simple and cost-effective technique to reduce the harmonics injected by nonlinear loads. Reactors are usually used to the nonlinear loads such as variable speed drives. The changing current through a reactor induces voltage across its terminals in the opposite direction of the applied voltage which consequently opposes the rate of change of current. This characteristic of a reactor helps in reducing the harmonic currents produced by variable speed drives and other nonlinear loads.

(ii) Delta–delta and delta-wye transformers: In this technique, two separate utility transformers with equal nonlinear loads are used. The phase relationship to various six-pulse converters is shifted through cancelation techniques that help in reducing the harmonics. This technique is also used in a 12-pulse front end of the drive.

(iii) Isolation transformers: In this technique, system voltage is stepped up or stepped down for voltage match. A neutral ground reference for nuisance ground faults is also provided in this technique. This is the best solution when SCRs are used as bridge rectifiers in AC and DC drive.

(iv) Passive harmonic filters or line harmonic filters: Passive or line harmonic filters (LHF) are used to mitigate lower order harmonics such as fifth, seventh, eleventh, and thirteenth. This also known as harmonic trap filters. In a six-pulse drive, it is used as a stand-alone part. It is also used for multiple single-phase nonlinear loads. In line harmonic filters, LCR circuit is tuned to a particular harmonic frequency that needs to be mitigated. Their operation is based on the resonance phenomena.

6. Conclusion

In this paper, it was presented how higher voltage at downstream node and negative line losses appear in an AC power system. It was also demonstrated that capacitor current has both active and reactive components with respect to the system reference.

If the upstream bus voltage and voltage drop phasors lie in the different quadrants that are exactly opposite to each other, then downstream node voltage will be higher than upstream bus voltage; if the upstream bus voltage and voltage drop phasors lie in the same quadrant, then upstream node voltage will be higher than downstream node voltage.

Transmission and distribution lines are generally inductive by nature; therefore, downstream node voltage leads the line current and lags behind the upstream node voltage, and that results in downstream node's power factor to be greater than the upstream node's power factor. Downstream node's higher power factor can cause the output power to be greater than the input power at upstream node, although all the power comes from the upstream node. If input power at upstream node is lower than output power at downstream node, then line loss will be negative in classical approach-based line loss calculation, where line losses are calculated as the difference between input power at upstream node and output power at downstream node. If the upstream node's

power factor is higher than the downstream node's power factor and upstream node voltage is lower than downstream node voltage, then there is still a chance of having a negative line loss.

A capacitor supplies only reactive power, but its current has both real and imaginary components with respect to the system reference. With respect to the capacitor bus voltage, all the current of a capacitor is reactive. Therefore, real and imaginary current components are reference relative.

Shunt capacitor used for power factor correction and voltage profile improvement can cause resonance at a harmonic frequency with system inductive reactance. At series resonance capacitor, current is very high, and at parallel resonance, voltage across the capacitor is very high which can rupture the capacitor. Therefore, the size of the capacitor should be checked if resonant condition can occur. There are several methods to mitigate the harmonic distortion—the use of reactor, delta–delta and delta-wye transformer, isolation transformers, and passive harmonic filters or line harmonic filters. A reactor is the simple and cost-effective method to reduce the harmonic distortion.

Author details

Sushanta Paul

Address all correspondence to: sxpaul@shockers.wichita.edu

Wichita State University, Wichita, USA

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