Chapter 4

High-Performance Packaging Technology for Wide Bandgap Semiconductor Modules

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Additional information is available at the end of the chapter

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Abstract

The properties of wide band gap (WBG) semiconductors are beneficial to power electronics applications ranging from consumer electronics and renewable energy to electric vehicles and high-power traction applications like high-speed trains. WBG devices, properly integrated, will allow power electronics systems to be smaller, lighter, operate at higher temperatures, and at higher frequencies than previous generations of Si-based systems. These will contribute to higher efficiency, and therefore, lower lifecycle costs and lower CO_2 emissions. Over 20 years have been spent developing WBG materials, low-defect-density wafers, epitaxy, and device fabrication and processing technology. In power electronics applications, devices are normally packaged into large integrated modules with electrical, mechanical and thermal connection to the system and control circuit. The first generations of WBG device have used conventional or existing module designs to allow drop-in replacement of Si devices; this approach limits the potential benefit. To realize the full potential of WBG devices, especially the higher operating temperatures and faster switching frequency, a new generation of packaging design and technology concepts must be widely implemented.

Keywords: reliability, solder, wirebonding, inductance, thermal impedance, sintering, high-frequency

1. Introduction

Semiconductor packaging provides the interface between semiconductor devices and the outside world. All semiconductor devices need packaging of some sort, whether they are the integrated circuits of a computer's central processing unit, an amplifier, diode, transistor or

any other kind of device. This chapter focuses on power modules: a subsection of the field of semiconductor packaging. A power module normally contains several power electronics devices such as MOSFETs or IGBTs, diodes, and often the associated passive components like gate resistors and DC link capacitors. The package provides a mechanical interface with the rest of the system, since most semiconductor components produce heat that must be managed in order to keep the device below its maximum allowable junction temperate (T_{jmax}), the package is almost always mechanically connected to a heatsink. The packaging is also the primary thermal interface between the heat-generating devices and the heat sink. The operating temperature of the devices defines their performance and long-term reliability, if devices operate at higher temperatures their reliability will decrease exponentially as temperature increases [1]. As a result, the thermal interface provided by the packaging is crucially important, and many of the properties of the processes and materials are optimized to provide the best possible heat sink with the lowest achievable thermo-mechanical stress. Electrical interfaces between the devices and the system are also features of the package, with signal pins and power terminals being internally connected to the devices, and emerging through the packaging to allow external connections. Depending on the design, it is also common for electrical insulation to be a feature of the package, normally to ensure that the high-voltage part of the circuit inside is suitably isolated from the heatsink to which the package is attached. The outer surface of the package must also meet the requirements of creepage and clearance to ensure that the terminals are properly insulated from each other. The packaging also provides environmental protection for the modules to some degree. The simplest arrangements have a plastic housing filled with a potting compound, normally a silicone gel. The plastic case makes the module a robust component which can easily be handled during testing, installation, and operation while protecting the devices inside. The case and potting provide protection from dirt, contamination and foreign objects which could damage them or their interconnections. The package can provide reasonable protection from liquid water, but most packages do not provide thorough protection from water vapor. For special applications such as some aerospace systems, hermetically sealed packages are required to provide complete isolation from the environment.

A simplified diagram of a typical power electronics module is shown in **Figure 1** which has the main design elements outlined above. There is a broad range of shapes and sizes of power modules, but the structure of many of the most commercially successful ones can be described as having similar construction to this. The semiconductor devices are attached, normally using solder, to a ceramic tile metallized with copper on each side. The tile, or substrate, provides a thermal path to extract heat from the device and has a circuit outline etched into the top to provide.

Isolation between contact pads for the various terminals of the device: anode and cathode in the case of a diode; emitter, gate and collector in the case of an IGBT; or gate, drain and source in the case of a MOSFET for example. Connections between these pads and the device are made using wirebonds, aluminum being a widely used metal in power electronics which is compatible with the aluminum surface of the device. With this combination of soldering and wirebonding, the device is connected to the package, and these connections are some of the most crucial for ensuring the long-term reliability of the entire package under real-world

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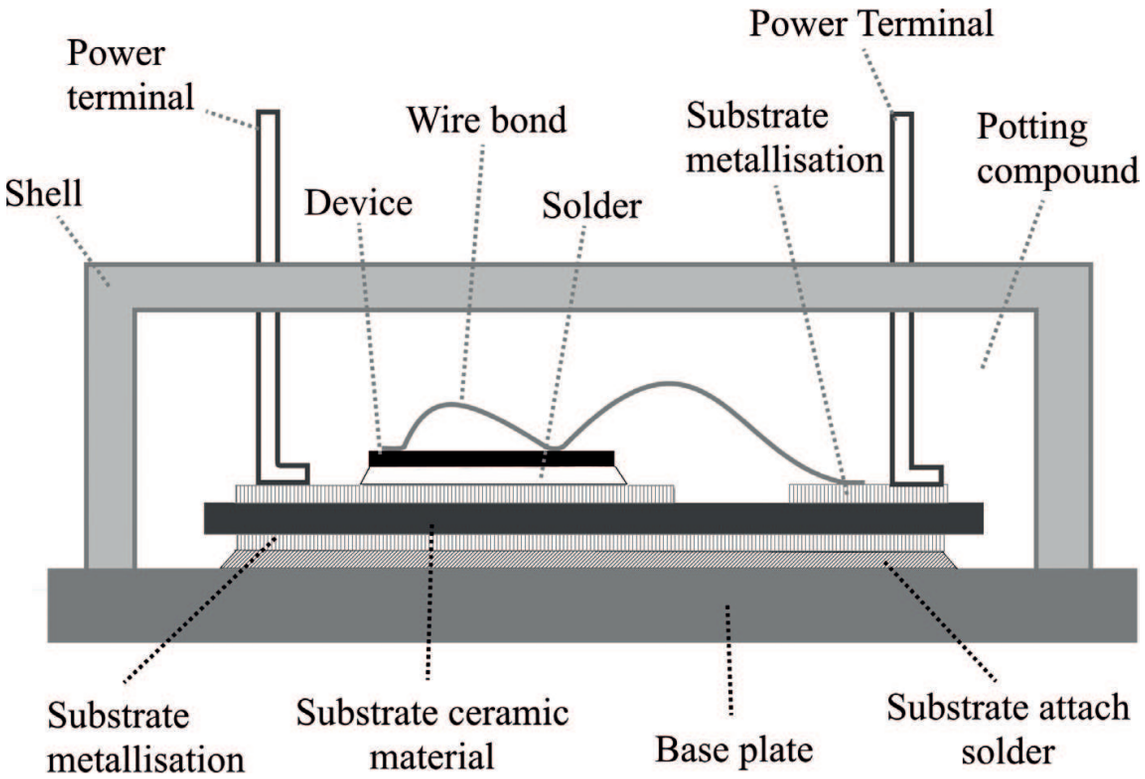

Figure 1. A simplified diagram of conventional power module packaging structure. Key to structure is the insulating ceramic tile which is soldered to a base plate. The semiconductors are soldered to the topside of the tile along with the power and signal terminals. The topside interconnection to the devices is achieved with wire bonding. The structure is then encapsulated in silicone gel and a plastic housing.

conditions [2]. The entire substrate is then soldered to the base plate, providing a thermal path from the device to the outside world. In many packages, multiple substrate tiles are soldered into one module. Terminals also need to be connected to the contact pads on the substrate tile to allow current flow into and out of the package, and auxiliary signal pins are connected for the device gates and other connections needed to control the devices. The entire arrangement is then surrounded by a plastic case and potted with dielectric gel to provide some protection and electrical insulation (**Figure 2**).

Power module packages based on the principles shown in **Figure 1** have been successful for decades but are not capable of exploiting the benefits of WBG devices such as higher junction temperatures and faster switching speeds. Every part of the package needs to be reconsidered if it is to become a high-performance part suitable for housing WBG semiconductors: the backside die attach material must be able to operate reliably for years at junction temperatures over 200°C; the topside attachment must be suitable for high power density and high reliability. The ceramic substrate and the base plate must have excellent thermal conductivity to keep the devices as cool as possible. The current density of SiC devices is higher than Si which is an advantage for reducing the volume of components, but it also makes it more difficult to cool them. The encapsulating gel must be able to sustain high temperatures without degrading especially since they are normally in intimate contact with the devices themselves, and therefore will be subject to some of the highest temperatures in the package. Further from the

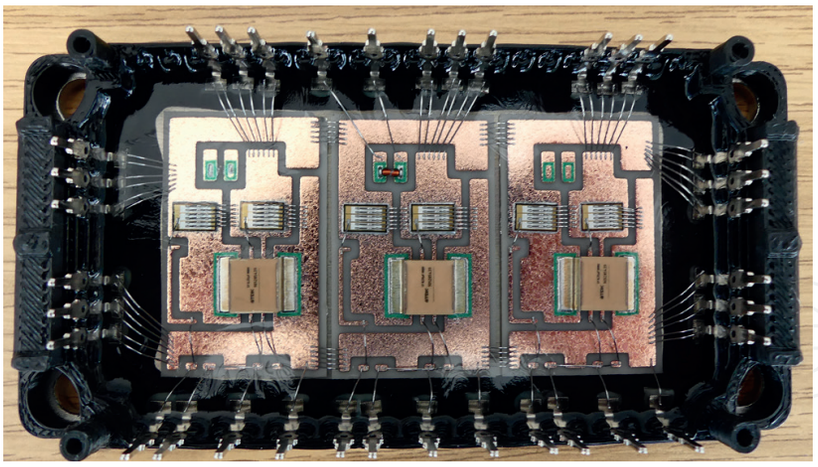

Figure 2. An example of a three-phase power module with one SiC MOSFET per switch, negative temperature coefficient resistor for temperature sensing, and a DC link capacitor on each substrate. The package concept is similar to that shown in **Figure 1**. Image courtesy of Dynex Semiconductor Ltd.

junction, temperatures will be lower but the capabilities of materials still need to improve, including the plastic housings, and glue used to connect the housing to the baseplate.

These shortcomings in packaging technology have been recognized and described thoroughly for example in [3], and Section 2 presents a summary of some of the solutions that have been investigated.

2. Materials and processes

SiC has a higher thermal conductivity than Si which is one of the properties that makes it an excellent material for power electronics devices. To take advantage of this, all the other materials in the module must have compatible high performance. Alumina or Al_2O_3 is the most widely used ceramic used for insulating substrates in power modules primarily due to its low cost and large numbers of suppliers across the world. The properties of Al_2O_3 are not ideal, having a relatively large thermal impedance and high coefficient of thermal expansion. AlN is commonly used in modules where higher reliability and lower thermal impedance are more important requirements, in applications such as rail traction and renewable energy, where system failures can be costly in terms of maintenance and operational losses. AlN has a thermal conductivity around six times greater than $Al_2O_{3,}$ and CTE around half as much, making it a much more efficient heat sink which is a better thermal match to the semiconductor devices and therefore reduces thermomechanical stress, which is the main cause of fatigue and wear-out failure in power electronics modules. Silicon nitride, Si_3N_4, is being increasingly used because it has an even lower CTE than AlN and high mechanical strength [4]. The bond between the ceramic material and the metal layer of the substrate is a common wear-out failure mode caused by long time-constant (minutes and hours rather than seconds) temperature cycling of the module. Therefore, the reliability of the overall system is dependent on the reliability of the substrate material, and improving substrates is an intense area of R&D for the

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manufacturers. Active metal brazing for bonding the metallization to the ceramic has shown to be more reliable to peeling off then direct copper bonding (DBC), and also aluminum direct bonding (DBA) has been shown to excellent reliability. For these reasons, Si_3N_4 is likely to be an ideal substrate candidate material for WBG devices. Conventionally substrates have been formed of a single layer of ceramic with metallization on either side, but double layer ceramics are becoming more common for WBG applications: Two ceramic layers are bonded together with a metallization layer between them, with metallization on the top and bottom sides also, giving an overall sandwich structure of three layers of metal and two ceramic [5]. Typically, the top and middle metal layers are used for conducting current, and the bottom layer is used to connect to a heatsink. Electrical connections are made using through the ceramics, thus allowing a very low profile package with a large degree of overlap between conducting surfaces. This allows designers to create very low inductance and low thermal impedance packages.

The module baseplate in silicon power module has normally been made from Cu in less-expensive modules and AlSiC in high-reliability modules. AlSiC is required for achieving the maximum benefit from AlN ceramic tiles, as the large CTE mismatch between AlN and Cu causes excessive stress, despite the high thermal conductivity of the system. High reliability baseplates are normally the largest single component of a module and the most expensive after the semiconductors. The trend in baseplate material is toward higher thermal conductivity, lower CTE, and higher mechanical strength. Base plates must also be finished to a high quality to give excellent bonding and interconnection with the other components. Enhanced cooling can be provided to the module by incorporating metal pin fins on the underside which can be used to directly liquid-cool the material, and these solutions have been widely used in automotive and traction applications to give low Z_{th} from junction to case in the module [6]. Recently, MgSiC has emerged as a promising new baseplate material, which offers marginally higher thermal conductivity (up to around 210 W/mK compared with 170–180 for AlSiC) but which could be simpler to manufacture, and hence help to reduce cost [7].

For high-power modules, thick copper bus bars are needed to handle high current loads without overheating. Solder interconnects have been very common as they are easily manufacturable and can be made in the same process as die attach soldering or substrate attach. As these other processes are becoming solder free, a new attach process for bus bars is beneficial, otherwise one soldering process will remain. Ultrasonic bonding is a mature process for bus-bar attach, which is already widely used in power electronics modules [8].

2.1. Die attach

The most widespread interconnection process for the backside of vertical power semiconductor devices is soldering, either using a solder paste which is mixture of flux and solder alloy; or using a solder preform which is a pre-fabricated foil of solder alloy, usually with the same surface area as the device to be soldered. The choice of alloy to be used for the die attach depends on several factors, such as whether or not the application has a requirement to be Pb free; the maximum processing temperature of other components in the module (such as passive SMT components); and cost. If there is no requirement to be Pb-free, this

allows a wide choice of relatively inexpensive Pb-based alloys with melting points up to 300°C, albeit alloys which are far from being eutectic and could have a pasty phase 10°C wide or more between solidus and liquidus. High-melting point lead-bearing alloys are common in high-power, high-reliability power modules in which maximum T_j of the current generation of Si devices is 150°C and while it is theoretically possible to operate Si devices of around 200 V blocking voltage up to 200°C [9], is unlikely to increase above 175°C in high-power modules with blocking voltages greater than 3.3 kV due to device-physics limitations. This gives a temperature range of more than 100°C between the absolute maximum junction temperature of the devices and the melting point of the solder. When considering the suitability of an interconnection material, a useful parameter to define is the homologous temperature, T_H, where

$$T_H = \frac{T}{T_M}$$

T (K) is the temperature of interest, which could be the mean operational temperature or the maximum junction temperature in this case, and T_M (K) is the melting point of the material. In general, smaller homologous temperatures will give longer lifetimes in electronics packages either by operating as far as possible from the melting point of the solder, or by using a higher melting point solder; however, creep deformation can still occur at relatively low temperatures [10]. If T_H is <0.4 this is considered mechanically stable, $0.4 < T_M < 0.6$ is considered to be the creep range, sensitive to strain, and $T_M > 0.6$ is unable to bear engineering loads [9]. If we take 473 K (200°C) to be a useful operating temperature for SiC devices, the melting point of 1234 K (961°C) for pure silver gives a T_H value of 0.38. In comparison, a Pb-rich solder with a melting point of 573 K (300°C) has a T_H value of 0.82.

The wide band gap of SiC or GaN allows devices to have a maximum junction temperature of around 300°C, this rules out any solder with a melting point close that figure. Solders with even higher melting points could be too costly, so there has been a great deal of effort in packaging R&D to find an alternative interconnection technology for Si and WBG devices. At the same time that WBG power devices are becoming mature, along with the associated demands on power electronics packaging, there is also the external pressure of environmental policy to eliminate hazardous substances from manufacturing. As mentioned earlier, Pb and its use in solder have been specifically targeted in legislation worldwide as a material which could be eliminated from consumer and industrial products. The European End of Life Vehicle (ELV) Directive sets targets for the reuse, recycling, and recovery of ELVs and their components [11] and the European Reduction of Hazardous Substances (RoHS) Directive Restriction of the Use of Certain Hazardous Substances in Electronic and Electrical Equipment specifically restricts the use of Pb. As of 2018, alloys with a Pb content of more than 85% are exempt from the RoHS restrictions but are subject to periodic exemption review.

In 2010, a consortium of Bosch, Infineon Technologies, NXP, Freescale Semiconductor and STMicroelectronics formed with the aim of developing alternative processes for die attach in semiconductor packages to replace Pb solders, specifically high-melting point solders. The

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consortium is known as the Die Attach 5 (DA5) [12]. The DA5 are focusing on four potential replacements to high-Pb solder: Ag sintering; high electrical and thermal conductivity adhesives; alternative solders; and transient liquid phase soldering (TLPS) [13]. Alternative solders with appropriate properties are available, such as Au80Sn20, AuGe, and AuSi, but the high gold content makes them too expensive to be viable for most applications. Even the best conductive adhesives have poor electrical and thermal properties compared with solder. Ag sintering or transient liquid phase bonding provides a more promising alternative.

2.2. Silver sintering

Sintering is the process of forming a solid mass of material from smaller particles or flakes using temperature, pressure, or both, while remaining below the melting point of the sinter material. It is widely used in manufacturing of metallic and ceramic parts. In the context of power-electronics packaging, we refer to sintering as the process of forming interconnection layers by processing a layer of micro or nanoparticles (normally of Ag) by applying a temperature and pressure profile for a controlled period of time. The resulting porous Ag layer has excellent electrical and thermal conductivity and a melting point equal to bulk silver at 961°C, normally with some remaining porosity. The silver particles (also known as the filler) in the paste are combined with a capping agent, binders and solvents. The purpose of these additional materials is to ensure that the silver particles do not begin to sinter themselves together before the actual processing begins, and to make the consistency of the past suitable for screen printing or dispensing. A range of chemicals have been used by the different suppliers of sinter pastes, a useful summary of these was published in 2014 [14]. Sinter pastes are broadly classified as being either 'pressured,' that is they require pressure to be applied during processing, or 'pressureless.' Sintering is an attractive technology for Pb-free and high temperature operations because the processing temperature are similar to those already used for device soldering, and pressureless paste in particular is seen as a potential drop-in solution which would require the minimum of additional manufacturing equipment; however, it is common for even pressureless pastes to benefit from some application of pressure during the manufacturing stage to increase the deformation of the Ag filler particles and increase the diffusion rate of silver atoms. An early patent (1973) for using sintering to join metal parts illustrated the use of the technique in lap, butt, and T-joints [15]. Sintered connections are not a new technology in semiconductor device packaging, with sintered glass beads being used for insulating materials, and sintering ceramic sheets being used as substrates ([16] for example). Only more recently, sintering has been used as a means to connect electronic components themselves [17] and particular power-semiconductor devices [18]. In 2006, a sintered interconnection for semiconductor device interconnection was described [19] which had an electrical conductivity of around 2.6×10^{-5} $(\Omega cm)^{-1}$, thermal conductivity of around 2.4 W/Kcm and apparent elastic modulus of 9 GPa. The high thermal conductivity of a sintered joint can lead to a small reduction in the thermal impedance Z_{th} from junction to case compared with a soldered die, particularly in small modules where there are not many devices which may overlap thermally with one another. One team of researchers [20] observed 12% lower thermal impedance compared to a SAC305 solder connection (**Figures 3** and **4**).

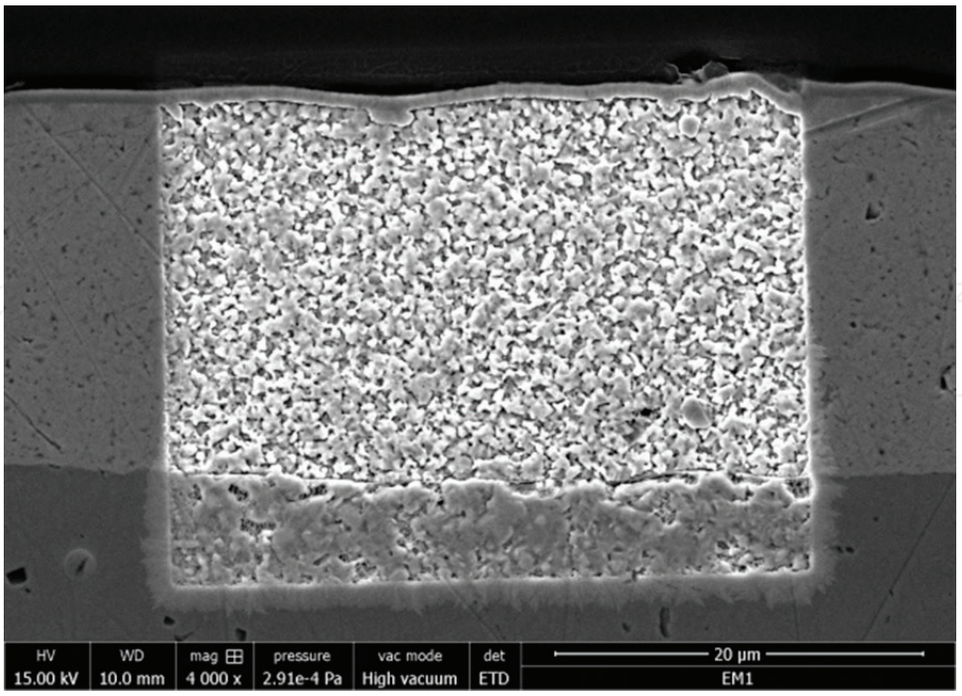

Figure 3. Cross section of a sintered die attach layer captured using scanning electron microscopy. The bright central area shows where the porosity of the layer has been revealed using focused ion beam (FIB) milling. The edges of the image show the apparent porosity after polishing with diamond suspension fluid. Image courtesy of Dynex Semiconductor Ltd.

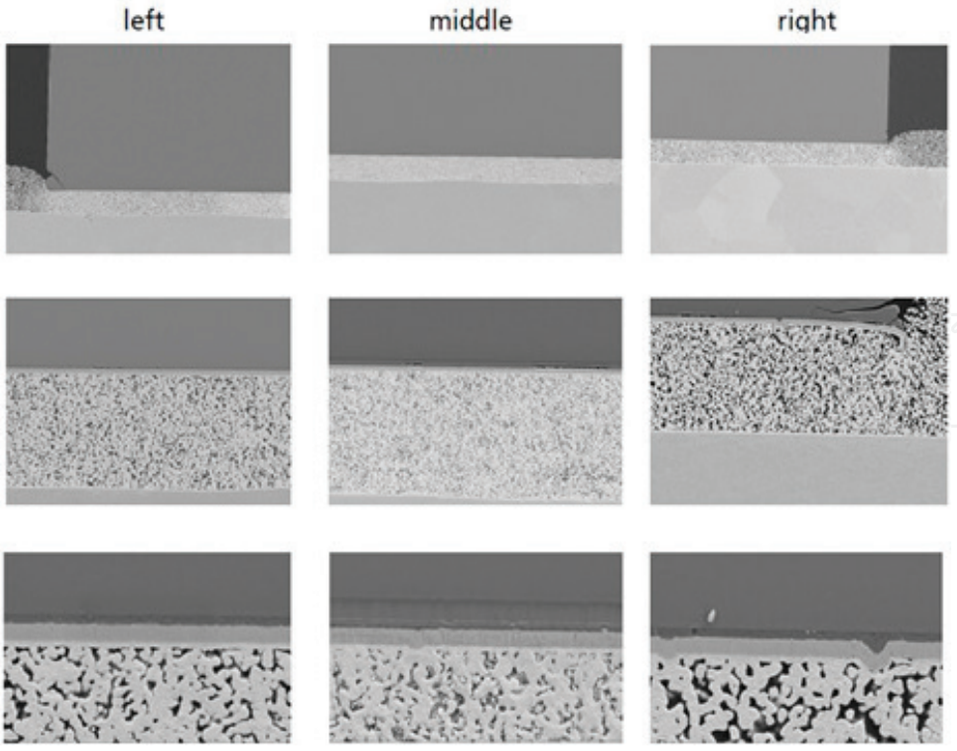

Figure 4. Scanning electron microscope (SEM) images of the sinter layer under a semiconductor die showing the variation in porosity from the edges to the middle. The measured porosity on the left, middle, and right-hand side is 22.6, 19.5 and 26.1%, respectively. Image courtesy of Dynex Semiconductor Ltd.

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Sintering for die attach in power electronics modules has been an area of extensive research and development and a recent consideration of the maturity of the state of the art has been published in [14, 21]. Ag sintering processes are mature enough for some manufacturers to ship power modules with sintered interconnections, for example it has been used by Semikron to produce entirely solder-free modules [9] and has been used successfully in bipolar devices for joining large thyristors to molybdenum plates. The SKiN module went even further and replaced the wirebonds with a PCB which is sintered to the topside of the device [22]. Uncertainty around the potential for widespread use of Ag sintering for die attach centers on a relative lack of data on the long term reliability compared with soldered interfaces, although many laboratory studies of reliability have been carried out that invariably show a large increase in the number of cycles-to-failure, sometimes by a factor of 10 compared to solder.

One reason silver sintering is more challenging to apply to mass production because of the difficulty in carrying out in-line high-volume automated quality control of sintered joints. In IGBT module production lines, there is 100% screening of the solder layers using X-ray imaging to find and measure the presence of voids in the solder caused by contamination, poor wetting or process irregularities. Modern industrial X-ray imaging systems are capable of automatically detecting and measuring the area of voids for statistical process control and comparison against defined pass/fail criteria. Imperfections in sintered bond lines do not appear as voids in the die attach layer, a good sintered joint and a failed sintered joint look identical to most X-ray systems with the exception of an advanced 3D tomography system, but such analysis would take too long per scan and therefore be too expensive to use as a screening technique in large-scale production. Poor bonding during the sintering process which leaves thin planar areas of no contact between the device and sinter layer, or the sinter layer and the substrate, might potentially be identifiable using scanning acoustic microscopy (SAM). The other alternative would be to forgo complete screening and instead carry out destructive tests on samples from each production batch using the mechanical strength measured in a die-shear test for example as a figure of merit. An alternative destructive method used during process development is a bend test in which the die and substrate and bent over a mandrel, of the substrate cracks and deforms before the device adhesion fails, the sintered joint is considered to be good. **Figure 5** shows the result of a bend test of 0.635 mm thick AlN active metal-brazed (AMB) tiles from the FIR3ST project power module. The tiles have been bent over a mandrel almost 90° which has caused the AlN ceramic and the SiC devices to fracture. The devices remain adhered to the surface.

The long-term reliability of Ag-sintered interfaces under thermomechanical cycling conditions is not as well understood as for soldered interconnections, but is an area of ongoing research. Sintered interconnections are vulnerable to the same driving forces of failure as soldered ones because they form a sandwich of materials with different coefficients of thermal expansion and experience temperature cycling with both fast time constants (caused by losses when the devices are switched and conducting current) and slow time constants (caused by heat soak of the overall system and the specific mission profile of the application). This causes thermomechanical stress which leads to cracking and delamination of the layers. Even if the CTE of the materials is closely matched thermomechanical failure modes will take place because power semiconductor modules are, in general, rarely in thermal equilibrium, but always have some temperature gradient across the vertical structure of the module. Studies

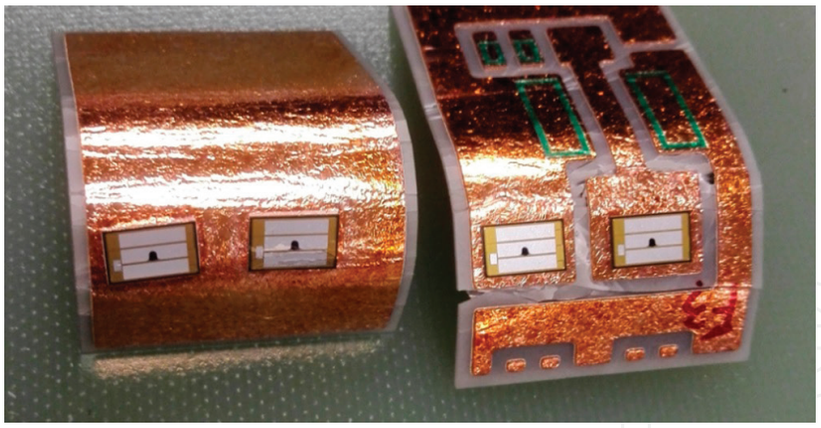

Figure 5. Sintered SiC MOSFETs on direct bonded copper (DBC) ceramic tiles after bend test. The substrate is bent through almost 90° and is cracked beneath the devices, which have remained adhered to the damaged surface. Image courtesy of Dynex Semiconductor Ltd.

have focused on how resilient sintered connections are compared with soldered interconnections under temperature cycling conditions, and on the nature of failure modes unique to sintered interfaces. Mechanical shear strength of nano-silver sintered die has been used as a measure of bond quality in 1.706 × 1.380 mm SiC SBDs [23]. It was found that the die shear strength was strongly related to the process time and temperature, with a 40 minute dwell at 300°C providing shear strength of around 40 MPa. These reduced by around 50% (the failure criteria defined in this study) after 5000 temperature cycles between 50 and 250°C. The reduction in shear strength was attributed to thermal-stress-induced dislocation creep leading to the formation of microcavities and grain boundaries.

The properties of sintered interfaces have been found to be a function of the porosity and porosity is a function of the starting material and the pressure used in the process [24]. Even small changes in the porosity can have a large impact, for example increasing the porosity from 5 to 7% (in other words from 95% dense to 93% dense) decreased the thermal conductivity from 380 to 320 W/mK at 100°C, accompanied by a similar relative change in electrical conductivity. On the other hand, the coefficient of thermal expansion was found to be relatively constant at temperatures less than 250°C and between porosity of 5 and 38% [25]. One study found that an established production process capable of sintering DBC master cards up to 5″ × 7″ in area has a porosity of 5%, but that reducing pressure by a factor of 4, the porosity increases to around 20%. **Figures 3** and **4** show SEM images of a 20 μm thick sinter layer showing the variation in porosity between the central area of the bond and the edges. Focused ion beam (FIB) milling is needed to reveal the true porosity under the polished surface.

A comparison of some properties between solder and silver sinter materials is shown in **Table 1**. Large area sintering has been investigated as a possible alternative to the use of solder for substrate to baseplate attachment [26]. A large ceramic tile (40 cm^2) was sintered to a baseplate and subjected to temperature cycling between −40 and +150°C. The integrity of the sample was measured using scanning acoustic microscopy and the test was stopped after 3000 cycles when it was found that the sinter layer showed no signs of degradation, but the substrate was beginning to delaminate. This is a common trend found in many papers on sintering: practically, all of the research papers report considerable increases in reliability under

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temperature cycling and active cycling conditions, between a factor of 4 and 10 increases in the number of cycles to failure. This large increase in reliability of one specific interface usually means that another interface in the system becomes the first failure mode instead of the die attach layer, or other solder layer. In many cases, the weak point is the ceramic tile, which starts to delaminate and will quickly cause a large rise in the thermal resistance between junction and case once the delamination begins to impinge on the area under the devices.

One negative aspect of sinter layers for both die and substrate attach is that the thin, stiff layers offer less stress relaxation to the structure, and the mechanical stress is transferred to other layers in the module. **Figure 6** shows how from changing from soldering to sintering of substrates on a base plate the convex bow shape is completely reversed to become concave. The convex bow is necessary to ensure good thermal contact during operation as the module tends to flatten out due an effect similar to a bimetallic strip as it heats up, thus ensuring as large as possible contact area between base plate and heat sink. If the base plate has become concave, there will be a large area which is not contacted with the heat sink, so thermal impedance will increase, and as a result, the junction temperature.

2.3. Diffusion soldering

In any fully formed solder joint, there is a layer of intermetallic compounds formed as the metallization of the workpieces is dissolved into the molten solder. Typically, these intermetallic

Parameter	Pb-Sb solder	Pb-free solder	Ag nanopowder
CTE (ppm/K)	28	20	19–21
Thermal Conductivity (W/mK)	70	70 (SnAg3.5)	240–290
Melting Point (°C)	183	220	~961
Electrical Conductivity	14.5	8–12	41

Data have been gathered from [9, 28, 29].

Table 1. Showing a comparison of some important properties of solders and sinter materials used for die attach.

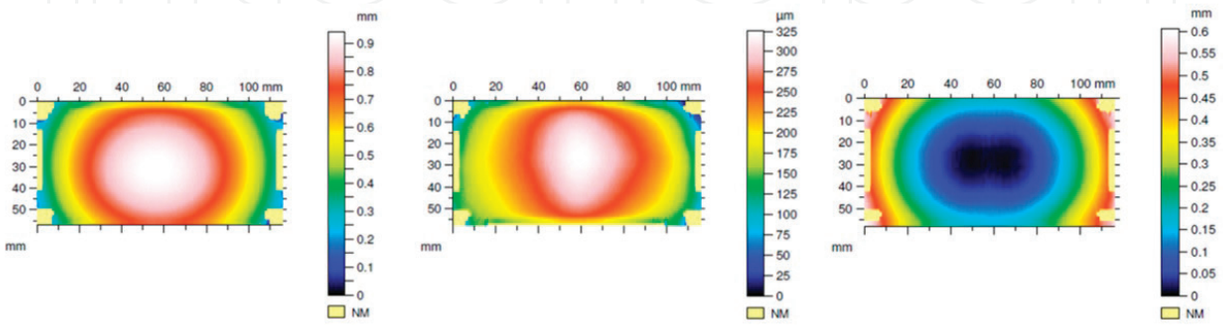

Figure 6. Three profiles of nominally identical baseplates before processing (left), after substrates have been soldered (middle) and after substrates have been attached by sintering (right). The sintering process causes the baseplate to switch from a convex to a concave profile.

layers are of irregular thickness of around several microns. Diffusion soldering promotes the growth of the intermetallics throughout the bulk of the solder joint, so that at the end of the process, the entire solder layer is formed of intermetallics. Sn rich solders and copper metallized substrates are a common combination which give Cu_6Sn_5 and Cu_3Sn intermetallics that have melting points of 416 and 676°C, respectively. A combination of Ag metallized die backside and Sn rich solder can give Ag_3Sn (T_m = 480°C). Studies have shown that diffusion-soldered interconnections can have a factor of 10 higher reliability than conventional solder joints, at least as good as sintered interconnections [27].

2.4. New topside interconnections

Aluminum wedge wirebonding remains the most widely used topside interconnection and has been an area of intense R&D to improve reliability. The most dramatic change is the use of copper wire instead of aluminum [30, 31]. The higher thermal and electrical conductivity of the wire allows increased current density for a given reliability or greater reliability at a given current density. The use of copper wire for die topside interconnection requires a special metallization on the topside of the chip, and some groups have experimented with the use of thick pads on the die topside to enhance the bondability of copper wire [32]. An alternative is the use of aluminum clad copper wire [33–35].

One study introduced the concept of spot sintering braided cable connections to the topside of devices [36]. A power cycling comparison was made between soldered, wirebonded diodes; and sintered diodes with spot sintered braid topside interconnection. A load current of 90A was used with a constant on time and off time of 1 and 5 s respectively. This test method gave a ΔT_j of between 86 and 100 K. The average number of cycles to failure of the soldered/wirebonded interconnection was 50 k cycles, for the sintered die, it was around 300 k cycles.

3. Special design considerations for wide band gap power modules

Advantages of using unipolar wide-band gap devices in power electronics applications also have downsides. High switching speeds when switching inductive loads will cause large voltage overshoots which may exceed the breakdown capability of the device. The ringing of the voltage and current in the circuit caused by fast switching can have implications for EMC and interference at a system level. **Figure 7** shows examples of waveforms from 3.3 kV rated devices.

Packaging design has an important role to play in mitigating these unwanted side effects. Any electronic component always has some unwanted electrical characteristics and these are normally referred to as ‘stray’ or ‘parasitic’ properties. Stray capacitance, inductance, and resistance can all have negative effects in power electronics modules, and the fast switching speeds of WBG devices make it crucial to not only minimize these stray properties, but even to engineer them to specific values in order to optimize performance. Stray inductance causes voltage overshoots during periods of changing electrical current according to the relationship

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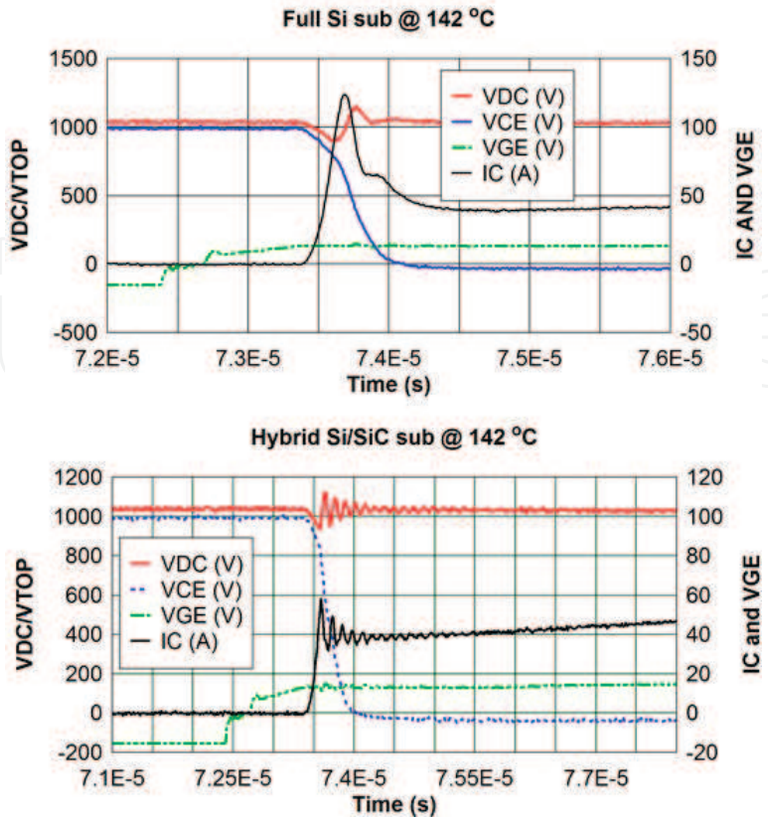

Figure 7. Turn-on waveforms for a 3.3 kV Si IGBT with Si fast recovery diode (top), and the same IGBT but with SiC SBD (bottom). The first turn off of the unipolar SiC diode causes oscillation of the output current compared with the slower bipolar Si diode [37].

$$V = L\frac{di}{dt}$$

where V is the overshoot voltage, L is the inductance, and di/dt is the rate of change of current. Clearly any inductance in the circuit combined with the high di/dt values associated with WBG devices will cause large voltage overshoots which could destroy the devices if the overall voltage exceeds the breakdown voltage of the device. Stray inductance can easily be minimized in principal by making the current carrying components planar, reducing depth, and overlapping terminals with opposite polarity as much as possible. In practice, however, this is more challenging to achieve: the presence of wire bonds for interconnection make it difficult to achieve really low parasitic inductance, say <5 nH per phase leg, and achieving low profile planar modules requires totally different module design concepts.

3.1. Examples of advanced packaging concept implementation

The power module developed by the I²MPECT collaboration [38] achieved low stray inductance by adopting a wirebond free design, instead sintering a flexible PCB directly to the topside of the devices and using a low profile design with ultrasonically bonded bus bars for

a solder free final package. Ag plated Si3N4 substrates are used and a pressure-assisted sintering processing connects SiC MOSFETs to the substrates, and the substrates are also sintered to the baseplate. The module is shown in **Figure 8**.

A 3.3 kV full SiC power module for rail traction applications has been reported [39] and further use of a full SiC 3.3 kV module rated at 450 A has been described in [40] and a similar package type has been used with 3rd generation SiC MOSFETs to give a module with 3.3 kV voltage rating and $R_{DS\,(on)}$ of 5 mΩ at 25°C and 13.8 mΩ at 175°C [41]. This package is becoming widely available from all the principal power module manufacturers, and while it uses relatively conventional packaging technology, for example, it still relies on extensive wire bonding for the topside connections to the devices, it focuses on using a new design approach to reduce the parasitic inductance. In rail traction applications, power modules normally consist of a single switch circuit topology combined together in the inverter to form phase legs. This newer style of package adopts a phase leg topology in a single package, which allows the bus bars to be designed in a way which allows a high degree of overlap between the DC+ and DC− bus bars, thus reducing the inductance while maintaining a module that can be manufactured on existing production lines.

In [42], a packaging concept is presented featuring a modular full SiC design. In each switching element, 1200 V 80 mΩ SiC MOSFETs with solderable top and bottom sides are joined source-to-source with solder and copper bumps in a flipchip type arrangement. This allows a planar, low inductance, double-side cooled switch to be manufactured with a reported inductance [43] of around 12 nH at 10 kHz. V_{ON} of the MOSFETs was monitored during temperature cycling from −55°C to +150°C with 30 min soak at each temperature extreme and 15 min transition time. No sign of degradation was apparent after 500 cycles. Thermal simulation and FLIR camera measurement showed that with 100 W dissipated in each MOSFET, junction temperature could be kept below 80°C [44]. The main elements of this design are shown in **Figure 9**.

In [45], a novel 10 kV, 60 A all SiC power module prototype was manufactured using third Generation Wolfspeed 350 mΩ SiC MOSFETs. Pressure-assisted sintering was used for the

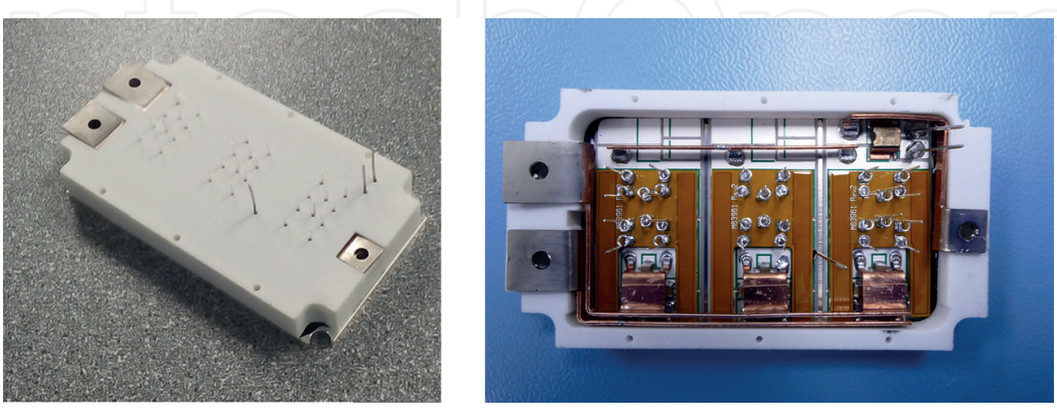

Figure 8. I2MPECT SiC power module. On the left, the complete package with lid. The right-hand side shows package internal solder-free structure, with ultrasonically bonded bus bars, double side sintering, and flexible PCB for topside die attach. Image courtesy of Dynex Semiconductor Ltd.

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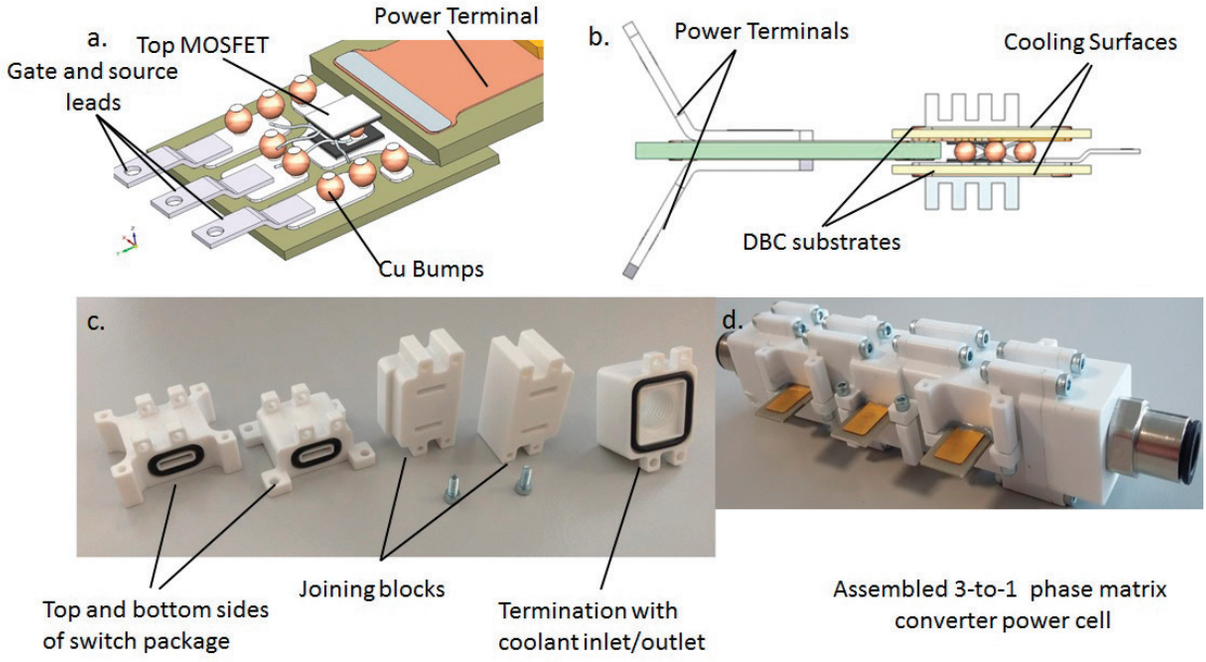

Figure 9. Overview of the module design concept described in [42]. A CAD drawing of the substrate element is shown in (a) revealing the source-to-source soldered MOSFET chips and Cu bumps used for interconnection. (b) Shows the overall sandwich structure allowing double side cooling, (c) and (d) show the real implementation of the building blocks and interconnecting elements. (image credit to Dr. Alberto Castellazzi, Univeristy of Nottingham, and Mr. Philippe Lasserre, deep concept, France).

die attachment in a wirebond free arrangement which gave an overall thermal resistance in the range 0.11 to 0.14 K/W. This design allowed the low power-loop inductance of 4.4 nH to be achieved, while a direct impingement liquid cooled heat sink allows power densities up to 18.1 W/mm$^{3.}$

4. Conclusions

Market forces and technology trends push semiconductor power modules requirements to higher power density, higher operating temperature, higher efficiency, lower cost and higher reliability. Wide band gap power semiconductor devices and Si devices are placing new demands on packaging technology in order to realize the potential of the latest generation of devices to meet these requirements. Silicon devices still have a much larger market share across all applications in which the ever increasing demands outlined above are already providing challenges. As a result, it is often Si power modules that lead the way with the most advanced packaging technology because of the high demand for these devices and competitive market for high reliability products. Sintering, copper wire bonding, wirebond free, planar modules with low inductance have all been introduced with Si devices. It is almost counter intuitive that the first generations of SiC power devices have been brought to market using less advanced packaging technology, often simply being used as drop in replacements for Si devices in conventional packaging, so the full capability of the devices cannot be

utilized. However, it seems certain that the time is near when the combination of advanced packaging and the latest generation of WBG devices is realized in mass production of power electronics modules.

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