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Chapter 4

Interface Control Processes for Ni/Ge and Pd/Ge Schottky and Ohmic Contact Fabrication: Part One

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Abstract

Metal-semiconductor interfaces are an essential part of any nano-electronic device. One of the concerns in germanium based technology is the presence of Fermi-level pinning (FLP) which leads to large Schottky barrier heights (SBH) for electrons. Details of the factors that pin the Fermi level will be discussed in this chapter. In an Ohmic contact there is an almost unimpeded transfer of majority carriers across the interface. One way to achieve such a contact is by doping the semiconductor heavily enough so that tunneling is possible. Heavy doping is not always advantageous or possible, depending on the type of device being fabricated. Other ways are to locally incorporate dopant atoms at the metal-germanium interface or to insert an interlayer into the interface. In practice, however, the contact resistivity is very sensitive to the interlayer thickness and the temperature of annealing used during the fabrication process. The latter two ways of achieving an Ohmic contact are interface control processes as opposed to the first way which is a bulk process. In this chapter we present the essential theoretical and experimental details required for the examination of some of the novel interface control processes developed for the fabrication of NiGe/*n*-Ge and PdGe/*n*-Ge Schottky and Ohmic contacts.

Keywords: thin film, Schottky barrier, Ohmic contact

1. Introduction

Germanium based nano-electronic technology suffers from two major limitations. In order to produce high speed devices, *n*-type germanium is preferred over *p*-type germanium because electrons have a higher mobility than holes. However, the doping levels in *n*-type germanium are low [1]. The second major limitation is that it is difficult to produce Ohmic contacts on *n*-type germanium [2–7] because of Femi-level pinning. One way to achieve Ohmic contacts is by

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doping the semiconductor heavily enough so that tunneling is possible, this will be explained further in Section 1.1.2. However, heavy doping is a bulk process which is not always possible in *n*-type Ge. Other ways of producing Ohmic contacts are interface control processes like the local incorporation of dopant atoms at the metal-germanium interface or the insertion of an interlayer into the interface. The contact resistivity is very sensitive to the interlayer thickness and the temperature of annealing used during the fabrication process.

It has been demonstrated, in earlier studies [8], that NiGe/Ge and PdGe/Ge Schottky contacts have some of the lowest values of sheet resistivity in Ge-based technology. These contacts were also observed to remain stable over a wide temperature range during annealing [8, 9]. In this chapter we present the essential theoretical and experimental details required in order to make a comprehensive review of some of the interface control processes developed for the fabrication of NiGe/*n*-Ge and PdGe/*n*-Ge Schottky and Ohmic contacts; the review is presented in the next chapter.

1.1. Theory

Electrons in solids obey Fermi-Dirac statistics. At low temperatures, the distribution of electrons over a range of allowed energy levels at thermal equilibrium is given by,

$$f(E) = \frac{1}{1 + e^{(E-E_F)/k_B T}} \tag{1}$$

where, k_B is the Boltzmann constant. The function, $f(E)$ is the Fermi-Dirac distribution function which gives the probability that an available energy state, E will be occupied by an electron at temperature, T on the Kelvin scale. The quantity, E_F is the Fermi level. **Figure 1** shows a schematic illustration of the dependence of the Fermi-Dirac distribution function on electron energy at various temperatures.

At $T = 0$ K, $f(E) = 1$ for $E \leq E_F$ and $f(E) = 0$ for $E > E_F$. This means that there is a 100% probability that all available energy states, up to the energy, E_F, will be occupied at absolute zero, i.e., all energy levels up to E_F are occupied at 0 K. As the temperature is increased to T_1 and T_2 some energy levels which were occupied will become vacant and some energy levels, above the Fermi energy, which were vacant at absolute zero will become occupied. The probability, $f(E)$ at all temperature, T is equal to 0.5 when the energy E is equal to a quantity, μ called the chemical potential. At $T \approx 0$ K, $\mu = E_F$ and therefore $f(E_F) = 0.5$.

In applying the Fermi-Dirac distribution to semiconductors, we must recall that $f(E)$ is the probability of occupancy of an available state of energy, E. Thus, if there is no available electron state at the energy, E (e.g., if E is in the band gap of the semiconductor), there is no possibility of an electron having that energy. We can best visualize the relationship between $f(E)$ and the band structure of a semiconductor by turning the $f(E)$ versus E diagram on its side so that the E scale corresponds to the energies of the energy band diagram as shown in **Figure 2**.

Figure 2 represents intrinsic materials where the concentration of holes in the valence band is equal to the concentration of electrons in the conduction band and therefore the Fermi level E_F

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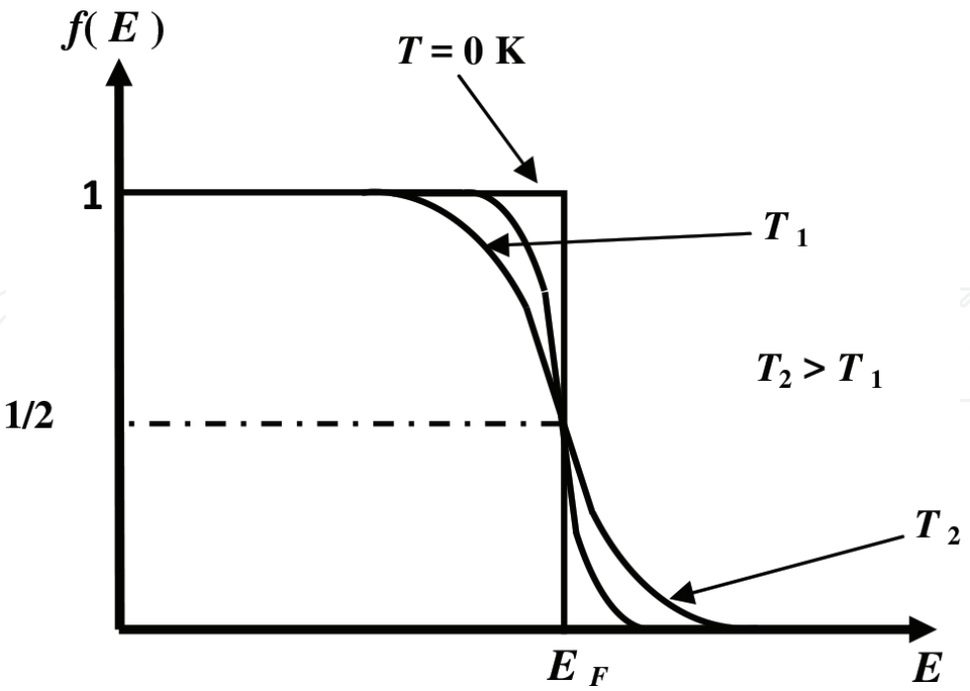

Figure 1. Schematic illustration of the dependence of the Fermi-Dirac distribution function on electron energy at various temperatures.

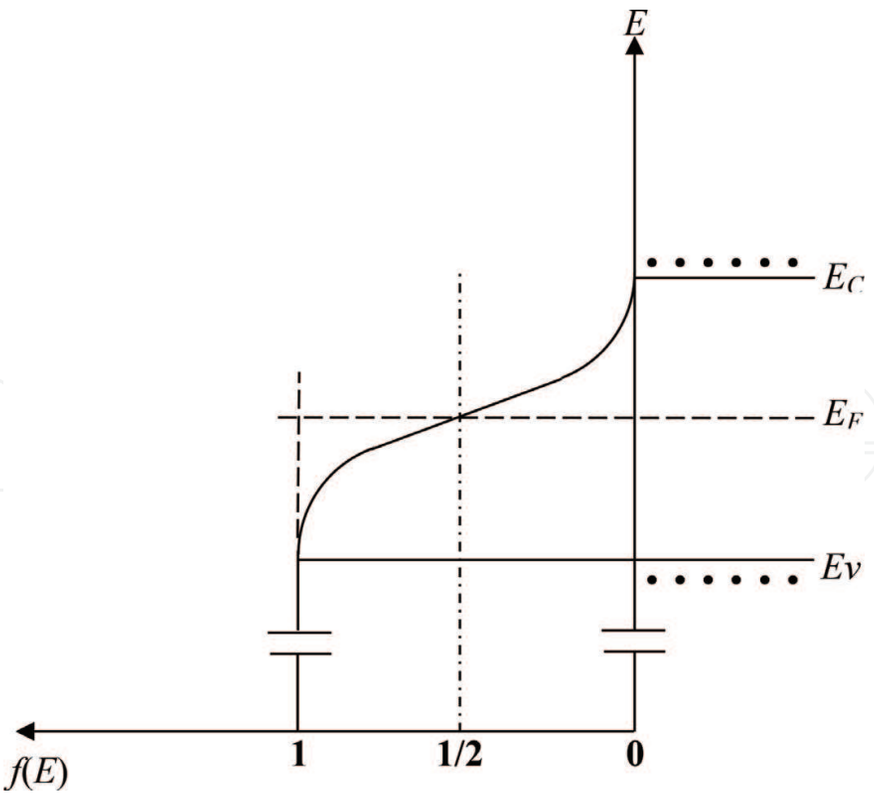

Figure 2. Visualization of the relationship between *f*(*E*) and a semiconductor band structure by turning the *f*(*E*) versus *E* diagram on its side so that the *E* scale corresponds to the energies of the energy band diagram.

lies near the middle of the band gap. In reality the effective densities of states, N_C and N_V in the conduction and valence bands respectively are slightly different because they depend on the effective inertial masses of the electrons and holes respectively, which are not the same. This causes the intrinsic Fermi level to be slightly displaced from the middle of the gap.

In *n*-type materials, there is a higher concentration of electrons in the conduction band than the hole concentration in the valence band. Thus, the Fermi level lies nearer the conduction band than the valence band, as shown in **Figure 3**.

In *p*-type materials there is a higher concentration of holes in the valence band compared with the electrons in the conduction band. The Fermi level therefore lies nearer the valence band than the conduction band, as seen in **Figure 4**.

In metals the valence and conduction bands overlap and there is not band gap. The Fermi level of a metal therefore lies in its conduction band, this fact will be referred to later on as we analyze **Figure 13** in Section 1.1.3 and **Figures 14** and **15** in Section 1.1.4.

1.1.1. Surface and interface states

Allowed electron energy states can be produced in the forbidden band gap of a semiconductor by the introduction of impurities or defects in the crystal. A metal-semiconductor interface introduces incomplete covalent bonds and other lattice defects at the semiconductor surface, which may result in the creation of interface states in the band gap. To explain a way in which

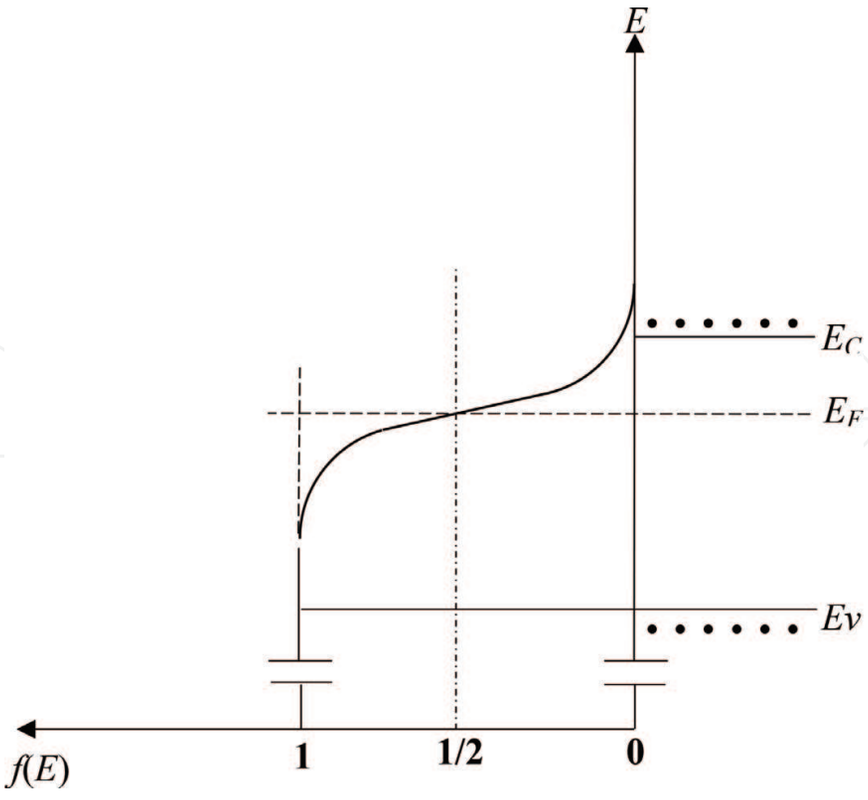

Figure 3. In *n*-type materials the Fermi level lies nearer the conduction band than the valence band.

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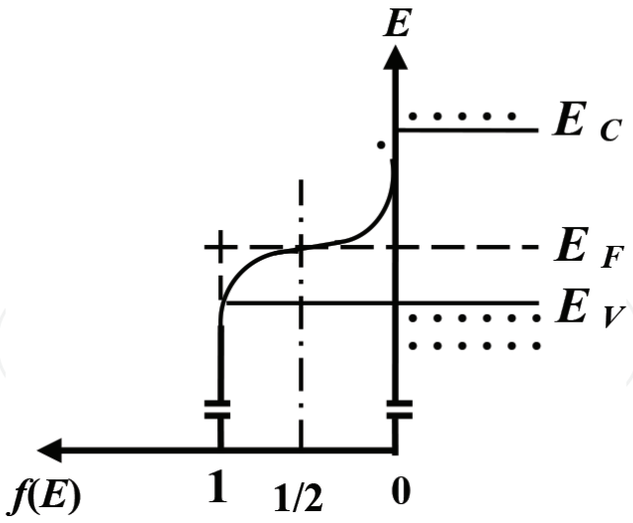

Figure 4. In *p*-type materials, the Fermi level lies nearer the valence band than the conduction band.

states may be created in the band gap, we could take the example of Ge doped with a donor impurity such as phosphorus (P) and an accepter like boron (B), as shown in **Figure 5**.

Phosphorus is in group V of the periodic table and is pentavalent. A P atom in the Ge lattice has the required number of valence electrons to complete the covalent bonding with four neighboring Ge atoms. The fifth valence electron of P does not fit into the bonding matrix of the Ge lattice and is therefore loosely bound to the P atom. Such electrons introduce energy levels very near the conduction band in the Ge band gap. These levels are occupied with electrons at 0 K and very little thermal energy is required to free them from the P atom, i.e., to excite them to the conduction band. At a temperature between 50 and 100 K, virtually all of the electrons in the impurity P levels are "donated" to the conduction band as shown in **Figure 6**.

Atoms like B from group III of the periodic table introduce accepter impurity levels in the Ge band gap near the valence band. B has only three valence electrons to contribute to the

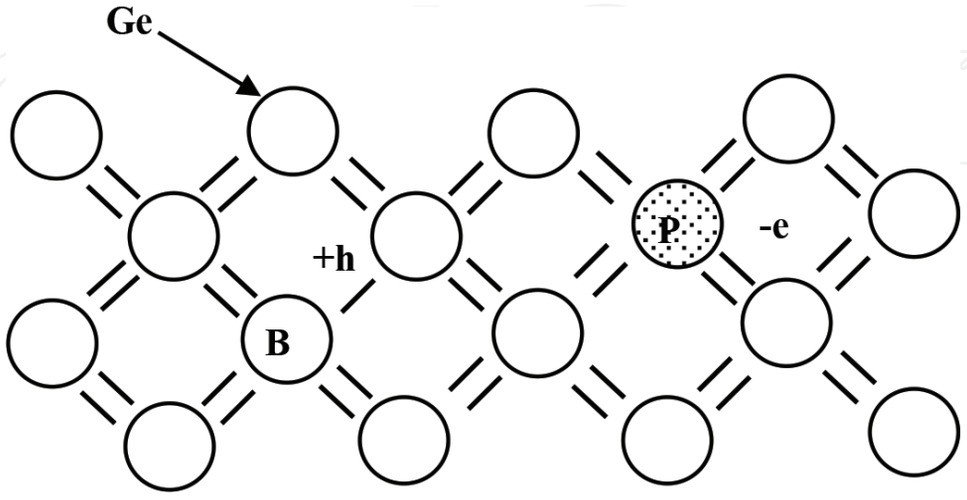

Figure 5. Schematic illustration of Ge doped with a donor impurity such as phosphorus (P) and an accepter like boron (B).

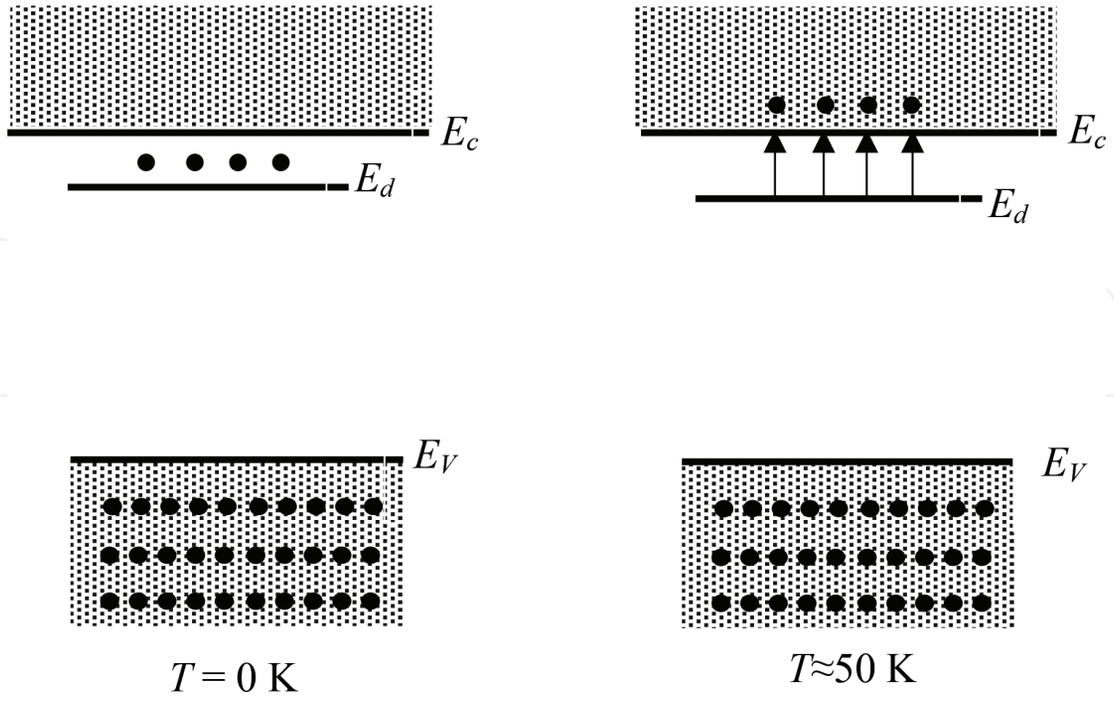

Figure 6. A donor level, E_d is occupied with electrons at 0 K and very little thermal energy is required to excite these electrons to the conduction band. Between 50 and100 K, virtually all of the electrons in the impurity level are "donated" to the conduction band.

covalent bonding thereby leaving one incomplete bond. Such levels are not occupied by any electrons at 0 K. As the temperature is increased the thermal energy increases enough to excite electrons from the valence band into the impurity levels, leaving holes in the valence band, which become current carriers when an external field is applied, by the continuous "hopping" of electron across adjacent incomplete bonds.

The incomplete bonds at a metal-semiconductor interface introduce energy levels in the band gap in a way similar to those due to accepter impurities. Interface traps, which introduce energy levels in the Ge band gap, can be caused by a sudden termination of a Ge crystal lattice at a metal/germanium interface.

1.1.2. Ideal Schottky barriers

A reference energy, E_0, called the vacuum energy, is the energy that an electron just "free" of a material would have in a vacuum. The work function of a semiconductor, Φ_s is defined as the energy required to move a unit electronic charge from the Fermi level to the vacuum level, i.e.,

$$\Phi_s = \frac{E_0 - E_{FS}}{q}, \tag{2}$$

where q is the electronic charge and E_{FS} represents the Fermi energy of the semiconductor. Similarly the work function of a metal is,

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$$\Phi_m = \frac{E_0 - E_{Fm}}{q}, \tag{3}$$

where E_{Fm} represents the Fermi energy of the metal. The electron affinity, χ_s of a semiconductor is defined as the energy required to move a unit electronic charge from the conduction band edge to the vacuum level, i.e.,

$$\chi_s = \frac{E_0 - E_C}{q}, \tag{4}$$

Figure 7 is a schematic diagram of the band structures of a metal and a semiconductor before contact for the case where $\Phi_m > \Phi_s$, the semiconductor Fermi level, E_{FS} is higher than that of the metal, E_{Fm}.

If $\Phi_m > \Phi_s$, the total energy of a metal/*n*-type semiconductor system could be reduced by moving electrons from the *n*-type semiconductor to the metal. When a metal is placed in contact with the semiconductor, therefore, electrons diffuse from the semiconductor to the metal in order to establish equilibrium. The electron diffusion causes the Fermi levels of the metal and the semiconductor to align at the same level throughout the interface region. Since the electron diffuse from the *n*-type semiconductor into the metal leaves behind uncompensated donor ions, a depletion region, W of an induced resultant positive charge is developed on the semiconductors side of the junction. A corresponding negative resultant charge is therefore induced on the metal

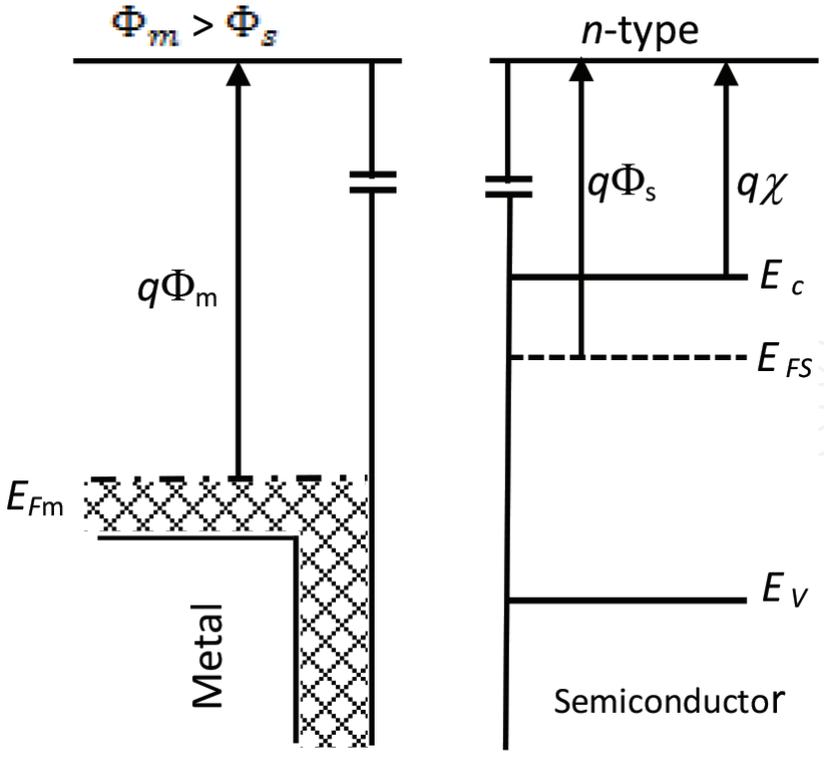

Figure 7. A schematic illustration of the band structures of a metal and a semiconductor before contact for the case where $\Phi_m > \Phi_s$, the semiconductor Fermi level, E_{FS} is higher than that of the metal, E_{Fm}.

side of the junction. The resultant positive charge from uncompensated donor ions in the depletion region matches the resultant negative charge induced on the metal, resulting in an electric field directed from the positive charge in the semiconductor to the negative charge in the metal. This causes the conduction energy band, *E*c and the valence energy band, *E*v of the semiconductor to bend in order to maintain continuity in the semiconductor band structure across the depletion region W, this is shown in **Figure 8**.

The electric field builds up to a magnitude where it eventually stops the electron diffusion across the junction, hence reaching a point of equilibrium. The corresponding induced equilibrium contact potential, V_o, across the junction, which prevents further electron diffusion from the semiconductor into the metal, is the difference in the work function potential energies, $\Phi_m - \Phi_s$, of the metal and the semiconductor, i.e., an energy of, $q(\Phi_m - \Phi_s)$ is required for an electron to cross from the semiconductor to the metal. The barrier V_o can be raised or lowered by the application of a voltage across the junction.

When a forward-bias voltage V is applied to the barrier the contact potential is reduced from V_o to $V_o - V$, as shown in **Figure 9**. As a result, electrons in the semiconductor's conduction

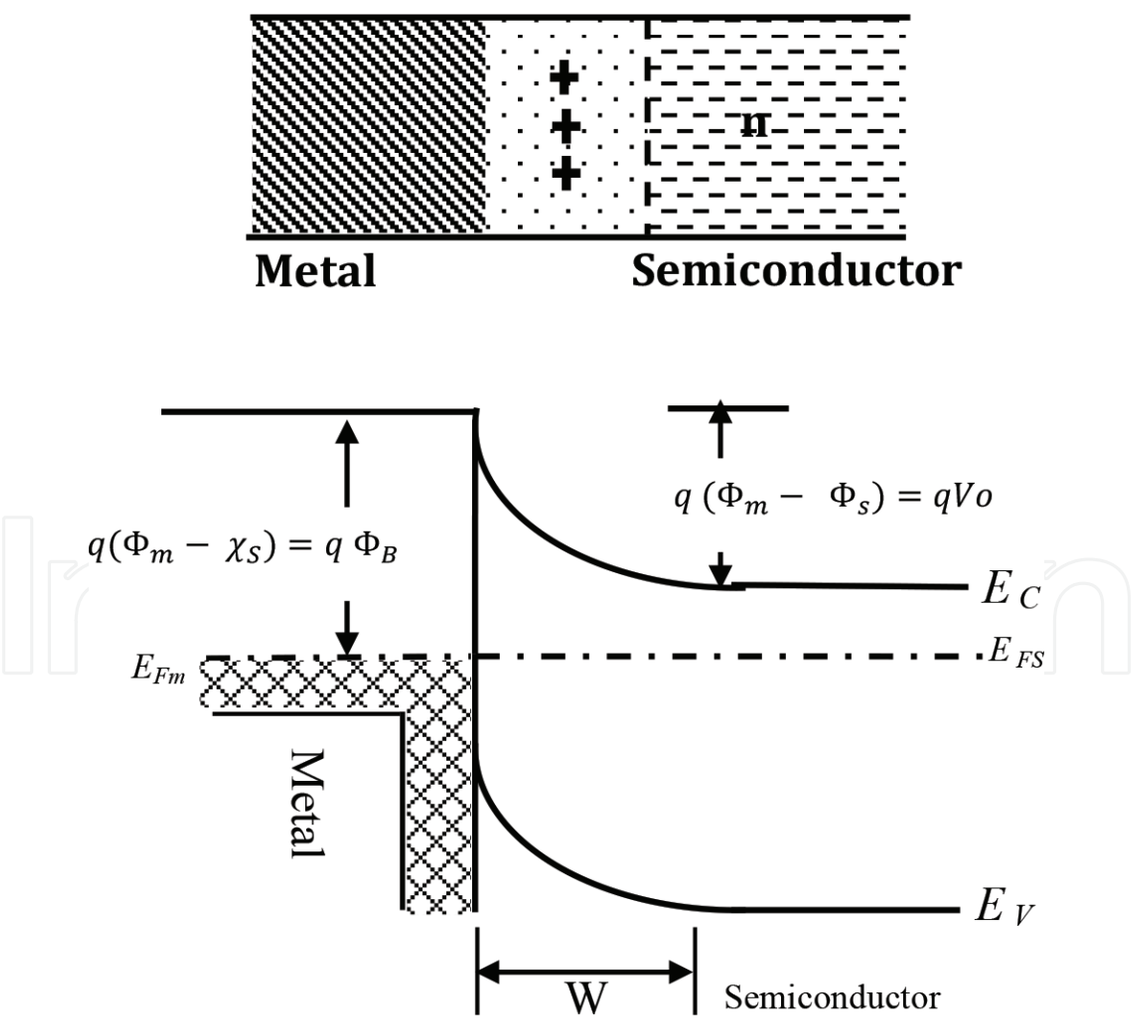

Figure 8. When a metal is placed in contact with a semiconductor the conduction, E_c and valence, E_v energy bands of the semiconductor bend in order to maintain continuity in the semiconductor band structure across the depletion region W.

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band can diffuse across the depletion region to the metal. This gives us the forward current from the metal to the semiconductor, since the direction of electron flow is opposite to the associated current direction.

When a reverse-bias voltage V_r is applied to the metal/*n*-type semiconductor junction, the contact potential is increased from V_o to a large potential barrier for electron flow from the semiconductor to the metal of, $V_o + V_r$ as shown in **Figure 10**. The electron flow from semiconductor to metal becomes negligible.

The reason that Ohmic contacts can be formed by heavy doping of the semiconductor, as mentioned in Section 1, is that even if this large, $V_o + V_r$ barrier exists at the interface, the heavy doping reduces the width of the depletion region, W to an extent that is small enough to allow electrons to tunnel through this barrier.

In both the forward and reverse-bias cases, electrons in the metal need to tunnel through an energy barrier of height,

$$q\Phi_B = q(\Phi_m - \chi_s), \tag{5}$$

in order to get into the semiconductor. The quantity, Φ_B, which will often also be labeled as Φ_{Bn} in this chapter, is referred to as the Schottky potential barrier height. This potential barrier

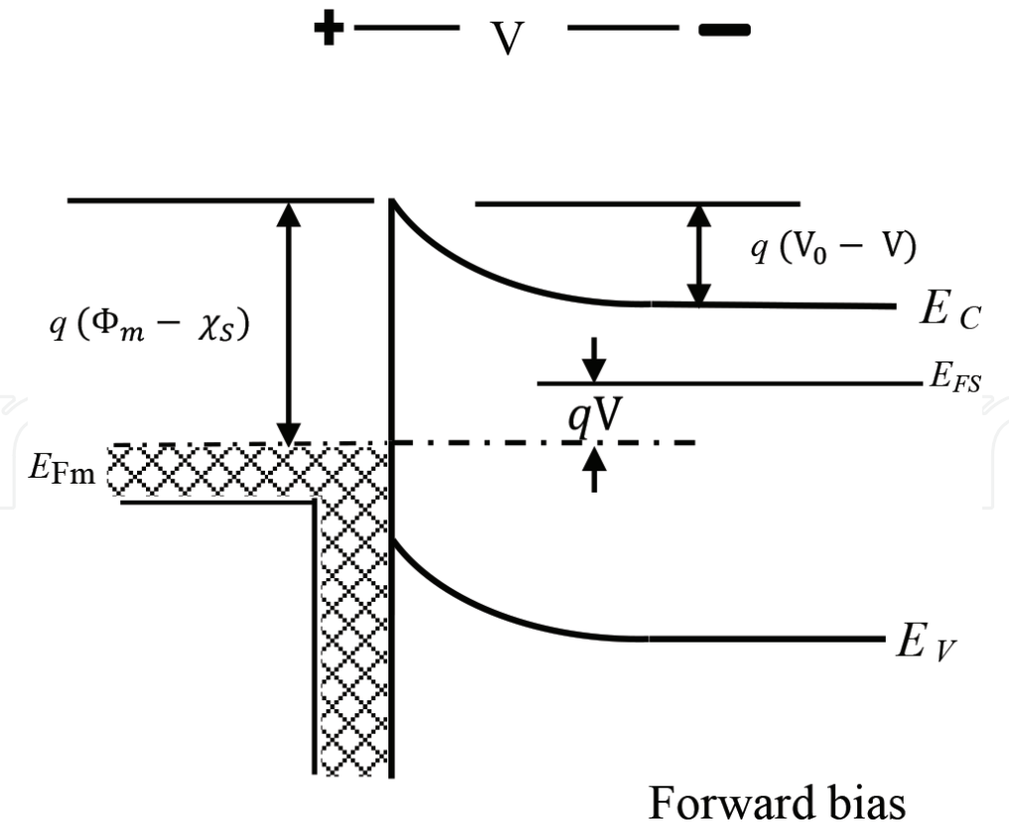

Figure 9. When a forward-bias voltage V is applied, the potential energy barrier from the semiconductor to the metal is reduced from V_o to $V_o - V$. Electrons are therefore able to tunnel across the barrier to give a forward current. Notice that the potential barrier from the metal to the semiconductor, $\Phi_m - \chi_S$ is much larger.

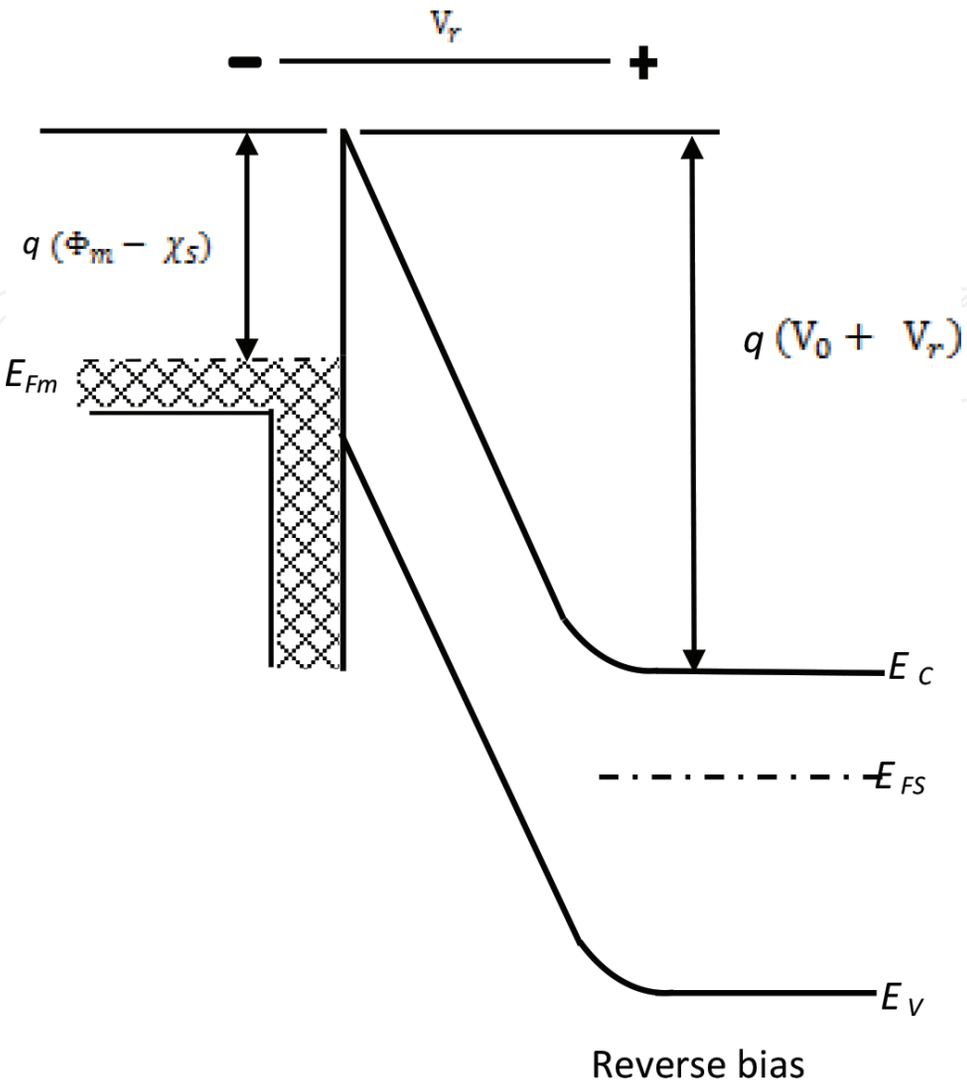

Figure 10. When a reverse-bias voltage V_r is applied, the barrier from the semiconductor to the metal is increased from V_o to $V_o + V_r$ and electron are not able to tunnel across the barrier. Notice that the potential barrier from the metal to the semiconductor remains, $\Phi_m - \chi_S$ as it was in the forward-bias case.

height is unaffected by the bias voltage but any reverse current due to electron injection from the metal into the semiconductor depends on the size of the Schottky potential barrier height, Φ_B. Electrons may flow from the metal to the semiconductor but the flow is retarded by the energy barrier, $q(\Phi_m - \chi_s)$. The contact therefore acts as a diode with I–V characteristics of the form sketched in **Figure 11**.

The resulting, I–V equation is similar in form to that of the *p-n* junction diode,

$$I = I_o\left(e^{qV/kT} - 1\right). \tag{6}$$

The reverse saturation current, I_0 depends on the size of the energy barrier, $q(\Phi_m - \chi_s)$ for electron injection from the metal into the semiconductor. This behavior of a metal/semiconductor contact is referred to as Schottky behavior as opposed to Ohmic behavior.

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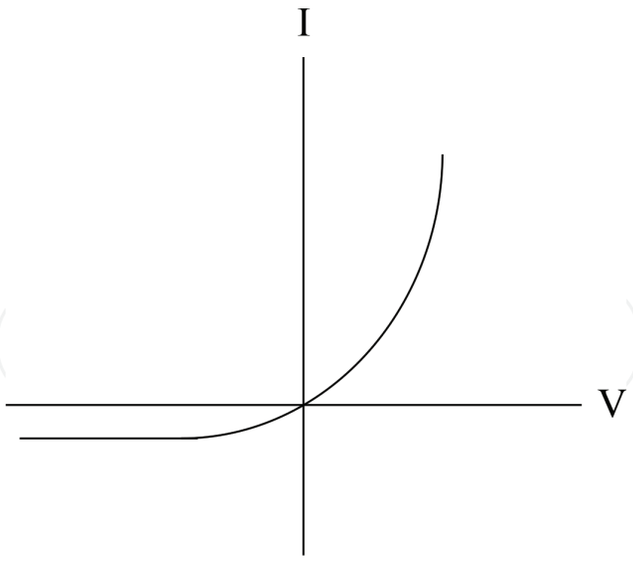

Figure 11. Schottky I–V characteristics where the reverse saturation current depends on the size of the energy barrier, q ($\Phi_m - \chi_s$) for electron injection from the metal into the semiconductor.

1.1.3. Ohmic contacts

In many cases we wish to have an Ohmic metal/semiconductor contact, having linear I-V characteristics in both biasing directions. In *n*-type metal/semiconductor contacts, ideal (without Fermi level pinning) Ohmic behavior is observed if $\Phi_m < \Phi_s$. The separate energy bands for a metal and a semiconductor in this case are shown, before contact, in **Figure 12**.

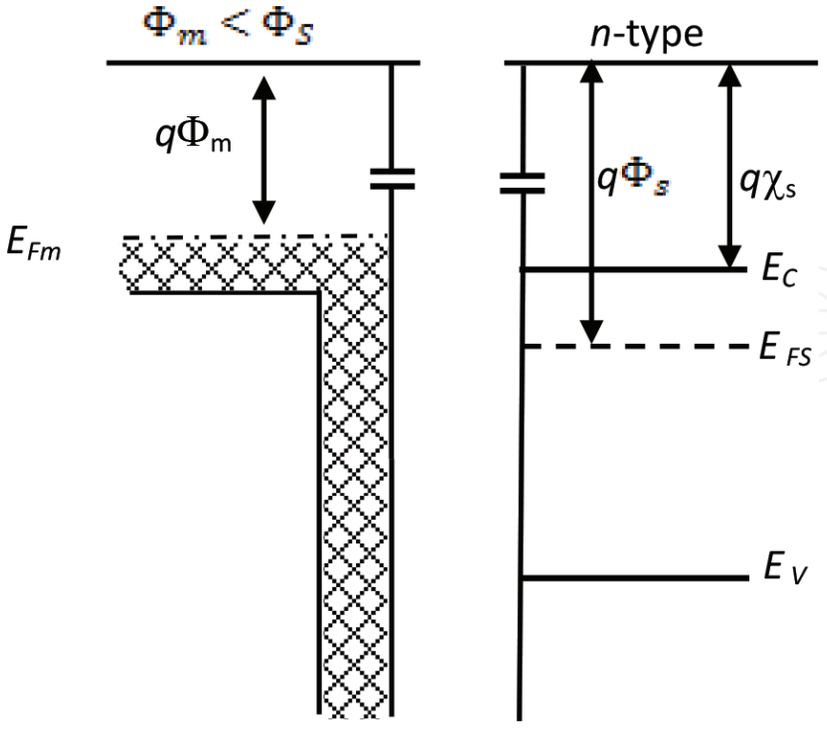

Figure 12. A schematic illustration of the band structures of a metal and a semiconductor, before contact, for the case where $\Phi_m < \Phi_s$. The semiconductor Fermi level, E_{FS} is lower than that of the metal, E_{Fm}.

After contact is made between the semiconductor and the metal, in the $\Phi_m < \Phi_s$ (*n*-type) case, the Fermi levels become aligned at equilibrium by transferring electrons from the metal to the semiconductor and not by the transfer of electrons from the semiconductor to the metal. The energy band structure, at the interface, for this case is illustrated in **Figure 13**.

We see in **Figure 13** that the conduction band of the semiconductor bends downwards towards the Fermi level of the metal at the interface, at equilibrium. What this means is that, since the Fermi level of a metal is in its conduction band as mentioned at the end of Section 1.1, the electrons in the metal are free to cross from their Fermi level straight into the conduction band of the semiconductor, i.e., electrons can flow unimpeded across the two conduction bands in both directions. Unlike in the rectifying contacts discussed earlier, no depletion region, W occurs in the semiconductor in this case.

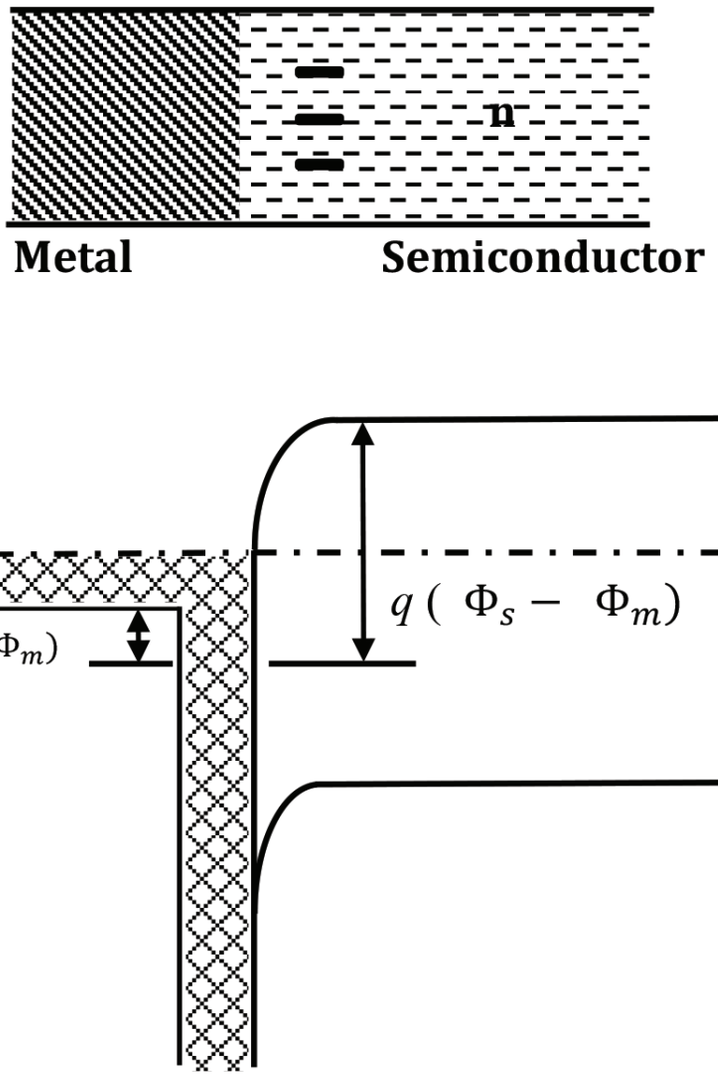

Figure 13. After contact is made between a metal and a semiconductor for the case where, $\Phi_m < \Phi_s$ the conduction band of the semiconductor bends downwards towards the Fermi level of the metal at the interface allowing electrons to flow unimpeded across the two conduction bands in both directions.

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1.1.4. Practical Schottky barriers

The ideal energy band diagram for a metal semiconductor interface has two main limiting factors. Firstly, the ideal contact does not take the surface states into account between a metal and a semiconductor. Secondly, when a practical metal/semiconductor interface is made, a thin interfacial layer is present on the semiconductor surface. This thin layer could potentially be a native oxide or processing residue, which contains a large density of surface states (D_{it}), many with energies distributed within the band gap of the semiconductor. The physics of the junction is then no longer governed by the properties of the metal and semiconductor materials alone but is then largely governed by the properties of the semiconductor surface [10].

The height of the Schottky potential barrier (Φ_B) is, in the ideal case, the difference between the metal work function (Φ_m) and the semiconductor's electron affinity (χ_s). A thin native oxide or processing residue insulating layer at the metal/semiconductor interface causes an additional voltage drop (V_i) over the metal/semiconductor interface, which is determined by the charge (Qs) at the semiconductor surface and the capacitance at the interface layer (C_i). Therefore,

$$\Phi_B = \Phi_m - \chi_s - V_i = \Phi_m - \chi_s - \left(\frac{Q_s}{C_i}\right). \tag{7}$$

It is possible to define a neutral level, Φ_0 in the interface energy band diagram. When the Fermi Level differs from the neutral level Φ_0, a net charge (Q_{it}) will be present at the semiconductor surface. Depending on the position of the surface states relative to Φ_0, the semiconductor surface will either be positive or negatively charged. For a very large density of surface states (D_{it}), the potential barrier height is only dependent on the band gap of the semiconductor and the neutral level of the semiconductor. Fermi level pinning then takes place at the interface making the potential barrier height independent from the metal work function. If the density of surface states is modeled as being infinitely large then the potential barrier height would be pinned at $(2/3)E_g$, which is known as Bardeen's limit [11]. The formation of surface states is dependent on the bonding type of the semiconductor material [10]. Covalent semiconductors such as germanium give rise to a large density of states at the surface due to the unsaturated bonds at the surface. For ionic semiconductors, the potential barrier height is more dependent on the metal work function [12]. In the following section we will define a quantity, n called the ideality factor and the symbol, Φ_{Bn} will be used for the Schottky potential barrier height.

The emission of electrons across a Schottky potential barrier can be described by two mechanisms: thermionic emission (TE) and diffusion. In practice, the transport process is a combination of both. The thermionic emission theory is based on a heat-induced flow of charge carriers from a surface over a potential energy barrier and is derived from the following assumptions [12, 13]:

1. The energy barrier height ($q\Phi_{Bn}$) is greater than the thermal energy of the electrons determined by k_BT, where k_B is Boltzmann's constant and T is the absolute temperature;
2. Thermal equilibrium is achieved at the plane that determines the emission;
3. Thermal equilibrium is not affected by the existence of a current flow. The two current fluxes, from the semiconductor to the metal and vice versa, can be superimposed;

4. The transfer of electrons across the interface of the metal and the semiconductor is the current limiting factor;
5. The electron mean-free-path should be bigger than the width of the region over, which a drop in potential energy, with a value of (k_B T), occurs at the barrier.

The total current density for thermionic emission, with an applied voltage, V across the barrier is given by [12, 14]:

$$J_T = J_{T0}\left[exp\left(\frac{qV}{nkT}\right) - 1\right], \tag{8}$$

where J_{T0} is the saturation current determined by

$$J_{T0} = A^* T^2 exp\left(\frac{-q\Phi_{Bn}}{kT}\right) \tag{9}$$

and

$$A^* = \frac{4\pi q m_n^* k^2}{h^3}. \tag{10}$$

The constant A^* is called the effective Richardson constant, q the electron charge, m_n^* the electron effective mass and h Planck's constant. The saturation current density (J_{T0}) is therefore independent of the applied voltage. Φ_{Bn} is the zero bias effective Schottky potential barrier height which can be obtained using the intercepts of the straight lines obtained by the extrapolation of J_{T0} in the semi-log forward bias ln J–V characteristics according to [15, 16]:

$$\Phi_{Bn} = \frac{kT}{q} ln\left(\frac{A^* T^2}{J_0}\right). \tag{11}$$

The factor n is equal to 1 for an ideal diode which conforms to pure thermionic emission but usually has values between 1 and 2. It determines the departure from the ideal diode characteristics and therefore modifies the diode equation, it is called the ideality factor, as mentioned earlier. The values of n can be calculated from the slopes of the linear regions of the semi-log forward bias ln J–V characteristics. It can be determined assuming pure thermionic emission [15, 16] using:

$$\frac{1}{n} = \frac{kT}{q}\frac{d}{dV}\ln(J). \tag{12}$$

The ideality factor is not a constant as it depends on the bias (V) and can only be specified for a particular point on a current-voltage characteristic curve.

The diffusion theory is based on the transport of charge carriers across a depletion region and is derived from the following assumptions [12]:

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1. The energy barrier height ($q\Phi_{Bn}$) is greater than the thermal energy of the electrons determined by k_BT;
2. The effect of electron collisions taking place in the depletion region is included;
3. The current flow does not affect the carrier concentrations at the interface and in the semiconductor;
4. The impurity concentration of the semiconductor does not degenerate.

The diffusion current-voltage characteristics can be derived from the current density in the depletion region:

$$J_x = q\mu_n n(x)E(x) + qD_n \frac{\delta n}{\delta x}. \tag{13}$$

The diffusion current density in the x-direction depends on the electron charge, q the electron mobility, μ_n the electron concentration, $n(x)$, the electric field at the barrier, $E(x)$ and the diffusion coefficient for electrons, D_n. The current density can only be expressed in this form if the mobility and diffusion coefficient are independent of the electric field [10]. The total current density, J_D with an applied voltage across the barrier, V and temperature, T can be expressed, after applying Einstein's relationship ($Dn/\mu n = kT/q$), in the form:

$$J_D = J_{D0}\left[exp\left(\frac{qV}{kT}\right) - 1\right], \tag{14}$$

where the saturation current is,

$$J_{D0} = \left[\frac{q^2 D_n N_C}{kT}\left(\frac{2q(V_{bi} - V)N_D}{\varepsilon_{rs}\varepsilon_0}\right)^{1/2} exp\left(\frac{-q\Phi_{Bn}}{kT}\right)\right]. \tag{15}$$

The saturation current density, J_{D0} is determined by the effective density of states in the conduction band, N_C, the built in potential, V_{bi}, the donor concentration, N_D, the permittivity of free space, ε_0 and the relative permittivity of the semiconductor material, ε_{rs}.

We can see that the expressions for the current density are similar for the thermionic emission and diffusion theory and are based on the saturation current density. However, the saturation current density for the thermionic emission theory, J_{T0} is more sensitive to the temperature while the saturation current density of the diffusion theory, J_{D0} is more sensitive to the applied voltage [14]. It should be mentioned that a number of the results discussed in this chapter are for I–V as opposed to J–V characteristics, in such cases the equations presented in this section are applied with the incorporation of the perpendicular cross-sectional area of the current's flow.

If a Schottky diode is connected to electrodes which give a maximum electric field, E_m, there is what is referred to as an image-force which is the interaction due to the polarization of the conducting electrodes by the charged atoms of the sample. The image-force effect causes the energy barrier for electron transport across a metal-semiconductor interface to be lowered. The amount of barrier height reduction, $\Delta\Phi_B$ is given by [15, 16],

$$\Delta\Phi_B = \left[\frac{qE_m}{4\pi\varepsilon_{rs}\varepsilon_0}\right]^{1/2}. \tag{16}$$

In Schottky diodes, the depletion layer capacitance, C can be expressed as [15],

$$C^{-2} = \frac{2(V_0 - V)}{q\varepsilon_s A^2 N_D}, \tag{17}$$

where A is the cross-sectional area of the diode, V_0 is obtained from the intercept of the C^{-2}–V plot with the voltage axis and N_D is the donor concentration of the n-type semiconductor substrate. The value of N_D can be determined from the slope of the C^{-2}–V plot using Eq. (17). The maximum electric field E_m can be calculated using,

$$E_m = \left[\frac{2qN_D V_0}{\varepsilon_{rs}\varepsilon_0}\right]^{1/2}. \tag{18}$$

Due to the presence of surface states, an interfacial layer, microscopic clusters of metal-semiconductor phases and other effects, it is difficult to fabricate junctions with barriers near the ideal values predicted from the work functions and electron affinity. Therefore, measured barrier heights are used in device design and fabrication. In some semiconductors like Ge, the metal/semiconductor interface introduces states in the semiconductor band gap that pin the Fermi level at a fixed position, regardless of the metal used.

An example of a semiconductor Fermi level, E_{FS} that is pinned well below the conduction band edge is in n-type GaAs. In this case there is a collection of interface states located at energy position that are 0.7–0.9 eV below the conduction band. These state are responsible for pinning the Fermi level as explained later in the next section. The Fermi level, E_{FS} at the surface of the n-type GaAs is pinned at a position which is 0.8 eV below the conduction band edge, regardless of the choice of metal used, as shown in **Figure 14**. The Schottky barrier height is then determined from this pinning effect rather than by the work function of the metal. This means that electrons at the Fermi level of any metal in contact will always have to overcome the 0.8 eV barrier in order to cross over into the conduction band of the semiconductor.

A somewhat unique case of interest is in n-type InAs were E_{FS} at the interface is not pinned below but above the conduction band edge of the semiconductor, as shown in **Figure 15**. The semiconductor conduction band edge bends downwards at the interface with the metal just as illustrated for Ohmic contacts by **Figure 13** in Section 1.1.3. However, in this case, the bending of the semiconductor conduction energy band edge goes to a position, at the interface, which is below the Fermi levels of both the semiconductor E_{FS} and the metal E_{Fm}. Regardless of the metal in contact, the semiconductor Fermi level, E_{FS} remains in the conduction band (above E_C) of both the semiconductor and the metal. Since the Fermi level is the highest energy level filled with electrons at 0 K, this means that the electrons can freely cross from the metal to the semiconductor and back, at any temperature. Excellent Ohmic contacts to n-type InAs can therefore be produced by the deposition of almost any metal as a contact because of this Fermi level pinning in the conduction band.

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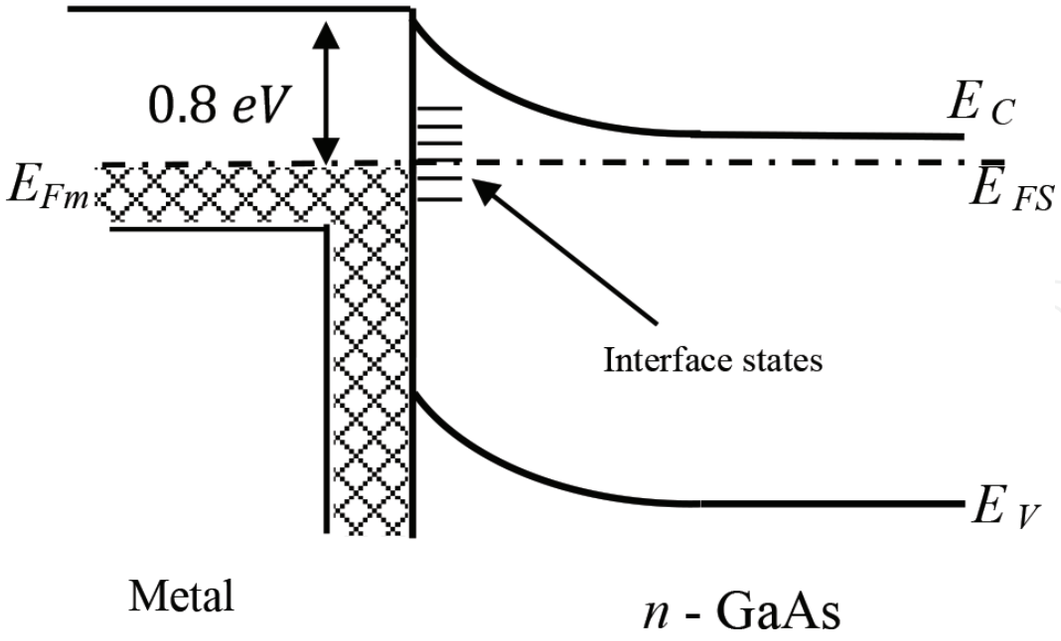

Figure 14. Notice that the semiconductor Fermi level, E_{FS}, lies 0.8 eV below the conduction band edge at the metal-semiconductor interface. This is regardless of the choice of metal used as a contact for GaAs, i.e., the Fermi level is pinned at this position.

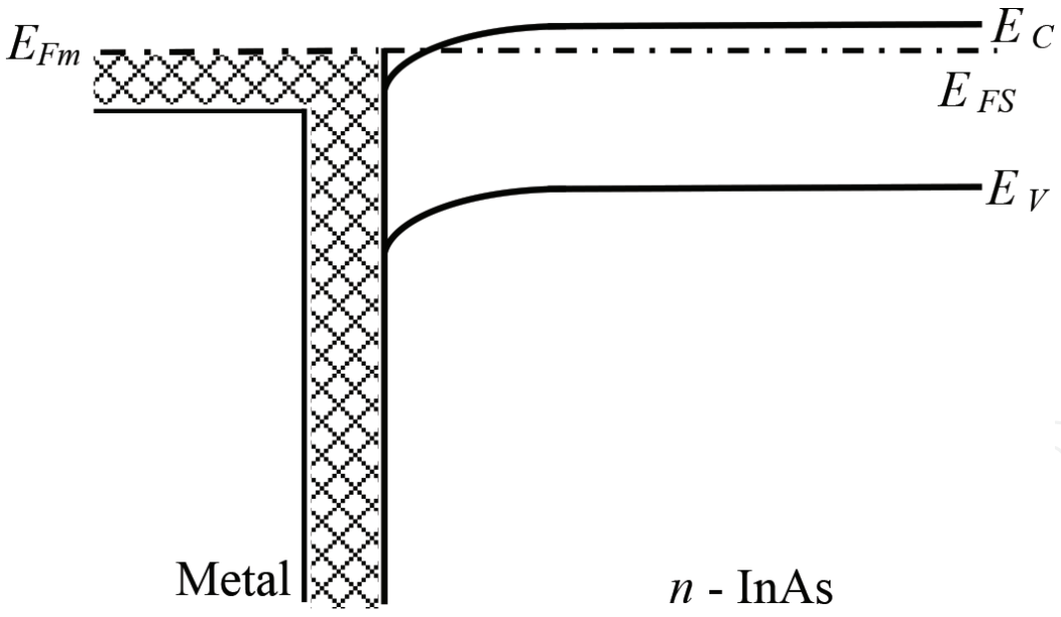

Figure 15. A schematic illustration of the case of *n*-type InAs. The semiconductor conduction band edge bends downwards at the interface with the metal, to a position below the Fermi level of the semiconductor, E_{FS}. This is regardless of the choice of metal used, therefore the Fermi level is pinned at this position above E_C.

1.1.5. Depinning of the interface

Fermi level pinning can be described by the theory of Metal Induced Gap States or MIGS [10]. In a metal/semiconductor junction the free electron wave function can penetrate into the semiconductor band gap. This generates band gap states, which consist of donor and acceptor

like states. As mentioned in Section 1.1.4, there is a charge neutrality level, Φ_0 in the band gap where the gap-state charges are balanced. The Fermi level is pinned close to the charge neutrality level because of dipole formation. To prevent the Fermi level pinning, the free electron wave function penetration has to be reduced. This can be done by introducing a thin dielectric layer. Si_3N_4 [17–19] has low dielectric constant and moderately high band gap to prevent the free electron wave function from penetrating into the semiconductor band gap and hence releasing the Fermi level. Al_2O_3 [19] has also been reported to reduce the Fermi level pinning effects.

2. Experimental techniques

2.1. Metallization

There are principally three different methods of depositing metal on a substrate: plating, metal evaporation and sputtering. Metal plating is generally used to deposit thick layers. Only metal evaporation and sputtering were used in the work reported on in this chapter.

2.1.1. Metal evaporation

Evaporation techniques are based on heating up a source to a temperature where the material starts vaporizing. The vaporized material is then deposited on the sample and cools down forming a thin film. Thermal evaporation can either be achieved by heating the source with a resistive element or by using an electron beam. Resistive heating takes place by passing a current through a heating element, often made out of tungsten, which heats up a crucible containing the source material. Resistive evaporation has the disadvantage of potential contamination from the crucible if the melting temperature of the crucible is close to the melting temperature of the source material, resulting in a poor film quality. Electron beam evaporation uses an electron beam generated from a cathode to heat up the source material locally. The crucibles are water cooled to minimize contamination. The electron beam is generated by a thermionic emission filament and is accelerated towards the crucible using a high accelerating voltage. The beam is then focused into a spot on the surface of the source material and the interaction between the accelerated electrons and the source material will cause the material to start heating up and vaporize. The combination of local heating and water cooled sources prevents crucible metal contamination, resulting in a high purity film deposited on the substrate. The evaporation processes take place under high vacuum (10^{-3}–10^{-4} mTorr) in order to create a mean free path of the evaporating flux, which is greater than the distance between the source and the sample.

2.1.2. Sputtering

While evaporation requires a source to be heated to produce a flux of gas, sputtering targets make use of a physical plasma process rather than heat. The plasma is formed using an inert gas (normally Argon) and is excited by either a direct current (DC) or radio frequency (RF) source. The target source is negatively biased and the plasma sputters neutral atoms of source

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material away from the target towards an anode, where the neutral atoms are deposited on the sample. Since a plasma is required, the working pressures of sputtering systems are relatively high ($\approx 10^{-1}$ mTorr). The sputtering method used for most of the work reported on in this chapter is RF magnetron sputtering. Radio frequency magnetron sputtering is an enhanced sputter method which enables a higher deposition rate at low operating pressure together with the possibility of obtaining high quality films at low as well as high substrate temperatures. A schematic diagram of the experimental setup for this method is shown in **Figure 16**.

In the chamber filled with the Ar gas, a high voltage is applied at high frequency between the target and the sample. The surface atoms of the target material are removed and deposited onto the substrate by bombarding the target with the ionized Ar atoms. The magnet, located behind the target, enhances ionization and effectively directs the sputtered atoms towards the substrate.

2.1.3. Cyclic stacking

To explain the process of cyclic stacked we take the example of the production of an NiGe layer on a Ge substrate. Multi layers of Ni and Ge are formed by RF magnetron sputtering on an *n*-type germanium substrate at room temperature and the average composition of the whole multi-layers is controlled so as to have a stoichiometric equivalence to the atomic ratio of Ni

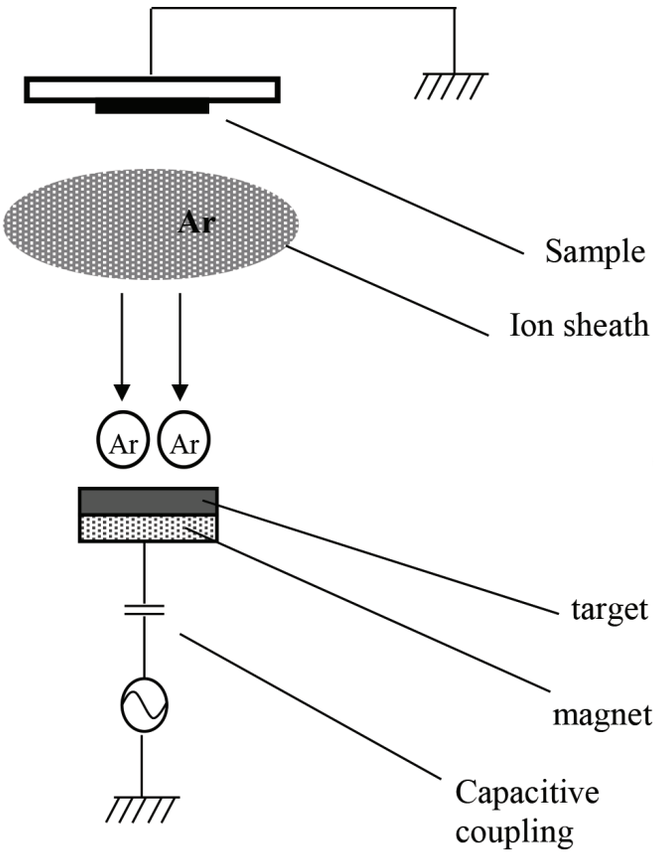

Figure 16. A schematic diagram of an RF magnetron sputtering unit.

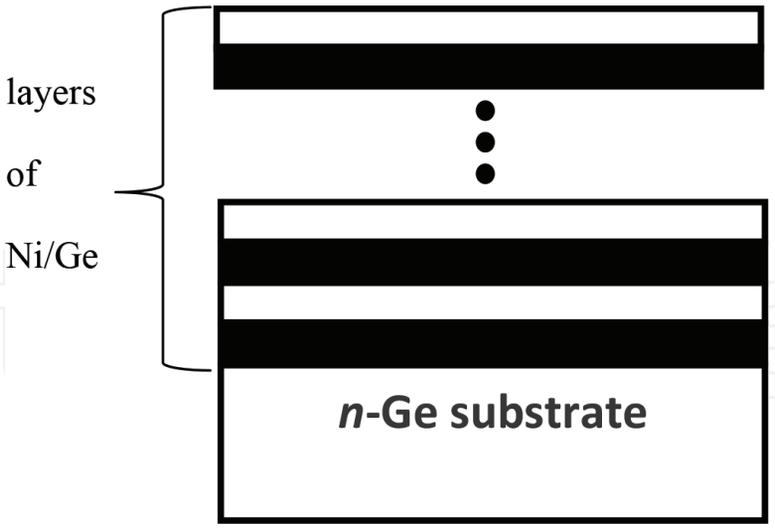

Figure 17. A schematic illustration of the sample configuration in cyclically stacked Ni/Ge films on an *n*-type Ge substrate.

and Ge atoms of 1 to 1 as in the phase, NiGe [20]. **Figure 17** is a schematic diagram showing the sample configuration in a cyclically stacked Ni/Ge film.

The idea behind this stacking of layers is to suppress the reaction between Ni and the Ge substrate upon annealing. In this way it is possible to get a high-quality NiGe film with a smooth interface on the Ge substrate. It is hoped that this smooth interface would reduce the Fermi level pinning effects of the interface electron energy states.

2.2. Donor implantation

Implanting atomic species like selenium (Se) into the surface of *n*-type germanium before metallization helps to reduce the Schottky barrier height by introducing local interfacial doping. In order to achieve a reasonable amount of implantation into the surface of the Ge substrate, the atoms to be implanted need to be energized to around 130 keV. The implantation is usually followed by heating at a high activation temperature to activate the diffusion of the dopant atoms further into the semiconductor surface, before metallization.

2.3. Four-terminal sheet resistivity measurement

The results of sheet resistance measurements presented in this chapter were obtained using a four-terminal resistor structure also known as a Kelvin resistor [21] structure. The structure consists of four contact pads: two pads are connected to the doped bulk semiconductor material and two pads contact to the metal used to form the contact. Current is then passed through two terminals between the semiconductor and the metal and the corresponding voltage drop is measured using the other two terminals between the metal and the semiconductor. In this way a sheet resistivity, ρ_{sh} can be extracted.

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