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The Atomic Layer Deposition Technique for the Fabrication of Memristive Devices: Impact of the Precursor on Pre-deposited Stack Materials

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Abstract

Atomic layer deposition (ALD) is a standard technique employed to grow thin-film oxides for a variety of applications. We describe the technique and demonstrate its use for obtaining memristive devices. The metal/insulator/metal stack is fabricated by means of ALD-grown HfO_2 , deposited on top of a highly doped Si substrate with an SiO_2 film and a Ti electrode. Enhanced device capabilities (forming free, self-limiting current, non-crossing hysteretic current-voltage features) are presented and discussed. Careful analysis of the stack structure by means of X-ray reflectometry, atomic force microscopy, and secondary ion mass spectroscopy revealed a modification of the device stack from the intended sequence, $\text{HfO}_2/\text{Ti}/\text{SiO}_2/\text{Si}$. Analytical studies unravel an oxidation of the Ti layer which is addressed for the use of the ozone precursor in the HfO_2 ALD process. A new deposition process and the model deduced from impedance measurements support our hypothesis: the role played by ozone on the previously deposited Ti layer is found to determine the overall features of the device. Besides, these ALD-tailored multifunctional devices exhibit rectification capability and long enough retention time to deserve their use as memory cells in a crossbar architecture and multibit approach, envisaging other potential applications.

Keywords: atomic layer deposition, nonvolatile memory, forming free memristive device, complementary resistive switching cell, redox-based resistive random access memory, ReRAM

1. Introduction

1.1. The ALD technique

The chemical vapor deposition (CVD) technique is a chemical reaction of a volatile compound with other gases for the deposition of a solid on a substrate. This reaction takes place inside a reactor in which the reactants are inserted as gases. Temperature and pressure are the two main parameters to be controlled. Temperature affects the rate in a predictable manner (Arrhenius behavior). The pressure range, even when it has a lower impact, determines whether the deposition mechanism will be surface-reaction limited or transport limited. During a transport-limited process, the deposition speed is very high, and the growth rate is very sensitive to the temperature. On the contrary, a surface-reaction regime can reach rates as low as an atomic layer per cycle by means of an oversupply of reactants available in the vicinity of the surface. This regime is more conditioned by the boundary layer than by the main flow of reactants, being less dependent on the temperature.

The atomic layer deposition (ALD) technique, though bearing many resemblances to CVD, excludes the gas phase reaction of the precursors. ALD is characterized by chemisorption steps while the physisorbed molecules are purged away during the necessary purge steps [1–3]. ALD relies on the activation of the surface on top of which the resultant layer is placed. This activation insures the growth to be self-limited to the minimum thickness determined by the reaction (usually an atomic layer). The substrate surface exhibits a certain density of surface sites, for example, OH groups, which serve as “anchors” for the metal precursor molecules. ALD requires four steps: I—chemisorption of the metal precursor to surface (OH) groups; II—release of the by-products during the purge; III—the reaction of the oxygen source with the remaining reactive groups at the metal ion; and IV—the purge of the by-products. After steps I–IV, the surface is again covered with (OH) groups, now on the deposited surface layer. The chemisorption of the precursor molecules to the surface, which can happen via different chemical reactions (1), stops suddenly when all surface sites are occupied. As a consequence, the ALD process exhibits extremely low deposition rates and an accurate control of the film thickness. The strict timely separation of the two precursor materials, which is achieved with the purge steps, gives the difference between ALD and CVD.

The key role played by the buffer material in the ALD technique can be identified from the described procedure. Surface preparation consists of the chamber introduction of some precursor that reacts with the former and improves the adhesion of the deposited compound. After that, deposition is performed by cycles in order to grow, layer by layer, the required material in a controlled manner. In the case of binary oxides, each cycle requires an oxygen source and a metal precursor. The oxidant and precursor chemically react, giving rise to a conformal growth layer above the buffered surface. The reaction during each cycle is summarized in Eq. (1):



Before repeating each cycle, purge gases are inserted into the chamber to avoid further reactions with possible remaining products. Once a complete run has occurred (activation, oxidant

and precursor, and purge gases), the process is repeated as many times as required to obtain the desired film thickness. It is worth to point out that the two gas-phase reactants are not in contact in the gas phase since the surface reactions are performed sequentially. The reaction (Eq. (1)) occurs when the second reactant reaches the surface. This sequence avoids possible reactions in the gas phase that could collapse at the surface forming undesired grains. Typical deposition rates are in the order of 0.1 nm per cycle [2].

ALD is a very versatile technique for many reasons. Among them, we emphasize here those that allow large-scale production: suitability to be applied in a wide temperature range, low cost, and easy scalability. Many reviews have addressed the fundamentals of ALD and its applications [1, 4]. Instead, the aim of the present study is to demonstrate how a spurious phase, produced by some inherent details of the technique, could be used to achieve devices with improved characteristics. This chapter highlights exactly such an issue in a concrete example: the deposition of a thin film of HfO_2 by ALD on top of a Ti-buffered Si/SiO₂ substrate. We will show how an unconsidered change, produced by the nature of the oxidant itself, has occurred at the Ti buffer during the ALD cycle, determining the growth of an extra oxide layer of TiO_x and thus providing interesting and useful features to the final device. We will take advantage of several microscopic and macroscopic techniques in order to fully characterize the resulting oxide layer, in order to fully elucidate the effect produced by the surface reaction.

In brief, we report here the structural evidence for the presence of TiO_x below the HfO_2 layer and discuss the key role of the O_3 precursor in its formation during the ALD process. Although it is quite difficult to disentangle the oxidant and/or precursor effect, some signs seem to point to the former as the main responsible one of the produced changes. We also include macroscopic electrical evidence to support that the TiO_x layer determines the occurrence of a very interesting metal-insulator-metal nonvolatile memory device. Besides, an additional deposition process was carried out in order to clarify whether we could be in presence of another unconsidered effect. Finally, we will introduce a phenomenological model to describe the electrical response and microscopic transport properties that support the microscopic picture achieved.

1.2. Details of the ALD technique and the device's fabrication

For ALD-based HfO_2 growth, the oxygen source is typically either H_2O [4] or O_3 [4] while the metal source could be for example Tetrakis(dimethylamino)hafnium (TDMAH) or TEMAH [5]. In our specific case, O_3 and TDMAH were the oxygen and metal source, respectively, although we will also include some comparison with samples grown using H_2O instead of O_3 . The substrate employed was commercial Si (highly doped)/thermally oxidized SiO₂ (120 nm) of 1 cm² size. The Ti layer (20 nm) was sputtered on top. After Ti sputtering, the ALD process—using either ozone as oxygen source and TDMAH as the metal precursor—was carried out to obtain a uniform 20 nm-thick HfO_2 layer. After this deposition process an array of 5 lines by 16 columns was determined by means of optical photolithography, delimiting 80 squared-shaped structures of 200 μm lateral size covered with sputtered Pd (40 nm)/Co (35 nm) acting as the top electrode (TE). To complete these two terminal devices, the access to the bottom contact was achieved by a scratch.

1.3. The ReRAM scenario

As downscaling of storage devices is approaching its physical limits, new strategies based on emergent materials and non-previously explored effects are moving into the focus of intense research as FLASH memory replacement. In particular, the metal-insulator-metal (MIM) structures acting as memory cells are developing as prominent candidates for such replacement. The resistive switching (RS) is the mechanism underlying the memory behavior. Its appealing features (speed, downscaling, retention, endurance) have evolved into a nowadays mature technology, coined as resistive random access memory (ReRAM).

The ability to produce a reversible change of conductance in these technologically simple structures (the RS effect) relies on the extremely large electric field applied to the strategically engineered thin insulating layer (i.e., between the metallic electrodes) but also on the choice of the electrodes' material. Basically, the effect consists of a switching process between a high resistance state (HRS) and a low resistance state (LRS) through a soft dielectric breakdown of the insulating layer(s). The change from HRS to LRS is called the SET process and the opposite one (from LRS to HRS) is referred to as RESET. Thus, memristive cells are resistive switching units, and their unique properties are strongly dependent on the materials used and on the fabrication details. They could need an initial electroforming process or not, and the polarity could be a relevant parameter (bipolar switches) or not (unipolar switches). Comprehensive discussions on the resistive switching phenomena are found in Ref. [6].

The simplicity of the geometrical structure and the absence of transistors make the concept extremely interesting for low-power, high-density, and nonvolatile memory applications. However, a challenge to achieve a technological implementation, using the RS concept, is to be allowed to select a designated cell within a passive crossbar array without interference from neighboring cells (i.e., the sneak currents problem) [7].

A way to overcome the sneak currents problem includes the use of rectifying elements to isolate each nonvolatile memory cell. The integration of a rectifying element, to achieve bipolar operation, would solve the sneak path problem "in situ." But so far no sufficiently scalable material has been found yet [7]. Therefore, simple structures based on nanometer thick oxides are a major topic of work in scientific and industrial research. A detailed knowledge of expected behaviors allows material engineering. In that sense, rectifying metal/oxide junctions, based on TiO_x , ZnO , and on TaO_{2-x} , has been recently described [8, 9], where upon appropriate oxygen vacancy accumulation the interface is switched to a non-rectifying resistive device. In particular, structures based on HfO_2 have shown excellent rectifying capabilities [10, 11]. Besides, hafnium oxide is a preferred high-k material, and therefore it is one of the most promising ReRAM materials since it has been already added to the complementary metal-oxide semiconductor (CMOS). From the industrial point of view, this fact is an enormous advantage and explains why so much effort is being done related with HfO_2 .

In this scenario, and responding to the actual trend on multifunctional components, there is a renewed interest on the mechanisms governing its dielectric behavior. These facts, combined with the observation of perpendicular magnetic anisotropy (which involves another promising low-power memory mechanism [12]) in Co films deposited on high-k materials [13] and FeFETs based on doped HfO_2 [14], put devices based on HfO_2 again in the focus of the attention.

2. Understanding the origin of remarkable electrical properties in simple RS stacks based on ALD-deposited HfO_2

2.1. Electrical characterization

The MIM stack was electrically characterized in a two-terminal configuration (see inset **Figure 1a**). We used a Keithley 4200 unit hooked through coaxial wires to a room-temperature probe station. Applying voltage while recording the current flowing through the stack allowed us to identify the general properties of the devices. In particular, sweeping voltage in a pulsed way is suitable for avoiding heating effects.

Figure 1a shows a typical current-voltage (I-V) dependence of a fabricated stack, obtained by sweeping voltage pulses, as demonstrated in the inset in **Figure 1a**. Four branches can be defined: (a) from 0 to +15 V, (b) from +15 to 0 V, (c) from 0 to -15 V, and (d) from -15 to 0 V. After deposition (pristine state), all devices are found in HRS (branch A in **Figure 1a**). When the positive voltage applied to the top electrode is increased, the device abruptly switches to LRS in a SET operation happening at around +5 V. No additional previous “forming” is required. Upon decreasing the stimulus (branch B), the I-V curve exhibits huge hysteresis (the semi-logarithmic scale in **Figure 1b** highlights the change rate).

Further cycling with positive voltages reproduces the LRS, as shown in the second and fourth sweeps in **Figure 1b**. Thus, the programmed state is nonvolatile with respect to the time scale of the measurement.

When the polarity is reversed, the negative voltage cycle starts in the HRS (branch C in **Figure 1a**), even when the positive cycle finished in a LRS, that is, a rectifying response is found. This behavior is referred to as a non-crossing hysteresis in the literature [15]. From that HRS on, the description of the negative voltage cycle is completely analogous to the positive

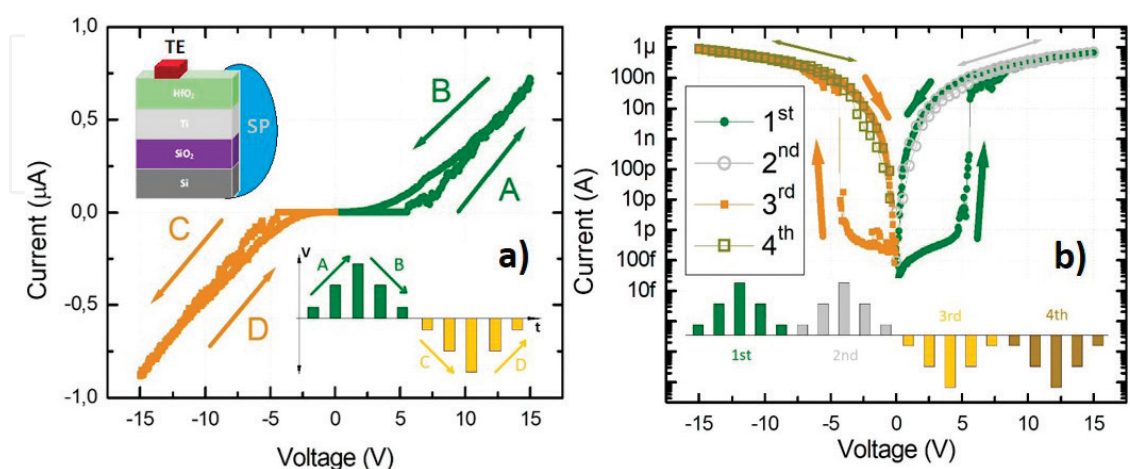


Figure 1. (a) Current as a function of voltage (I-V) measured with a pulsed sweep (see lower right inset). The upper left inset sketches the stack (TE stands for top electrode while SP is the way to access to the bottom contact of the structure). (b) I-V curve displayed in semi-logarithmic scale. As can be seen from the inset, the protocol consists in two repetitions of each polarity sweep in order to test the nonvolatile behavior.

one, and the other SET operation is recorded each time the voltage reaches ~ 5 V. After a negative polarity sweeping loop, the positive HRS is recovered at the positive stimulus.

It is worth to point out that even when no trace of a RESET operation was observed, just upon zero voltage crossing the rectifying capability of these devices rebuilds a high-resistance level.

Memristive cells are classified into bipolar and unipolar behavior. Bipolar cells are those which demonstrate the SET and RESET operations in opposite voltage polarities, for example, SET at positive polarity and RESET at negative voltage. In turn, in unipolar cells the SET and RESET can occur at the same polarity (while other parameters need to be controlled, i.e., current compliance). Whether both polarities are required to operate the memristive cells or not is determined by the mechanism governing the switching. Despite the difference, typical memristive cells (being either bipolar or unipolar) depict crossing I-V curves, a behavior qualitatively different from the one obtained in our Pd/Co/HfO₂/Ti/SiO₂/Si samples. So far samples showing non-crossing I-V curves were referred to as complementary RS [7]. This behavior can be modeled as the response of two coupled bipolar memristive switches in series, in a back-to-back configuration. Within this scheme, one of the two coupled memristive switches (or RS units) shows the SET operation at a positive voltage, while the other one exhibits the SET at a negative voltage. When the stimulus polarity change is produced, instead of maintaining the low-level resistance obtained during the positive excursion, it reveals the high-level resistance corresponding to the second RS unit. The coupling between the two RS units would be responsible for RESET screening. The explanation for apparent RESET absence arises on the fact that alternating the voltage polarity leads us to measure the reversed RS unit. However, if we record the resistance level between consecutive pulses (applying a small pulse of the same polarity even when the sweeping curve goes through zero), we progressively observe the changes from HRS to LRS at certain polarity and from LRS to HRS at the opposite voltage polarity. Interestingly, the back-to-back configuration determines two different pair of states: positive high- and low-resistance states (pHRS and pLRS, respectively) and equivalently for negative polarity (nHRS and nLRS).

By following the resistance level, measured in between every two consecutive pulses during the pulsed voltage sweep (green pulses in **Figure 2b** and **d**), the specific voltage values at which the SET and RESET occur (identified as the changes from HRS to LRS, and from LRS to HRS, respectively) can be identified. If the resistance level is recorded with a positive pulse (green pulses in **Figure 2b**), the pHRS and pLRS will be tested, while if the small pulse consists of a negative voltage value (green pulses in **Figure 2d**), the nHRS and nLRS will be under study. In that way, the two units can be split. By experimentally exploring the voltage required to observe each operation by a unique pulse (positive SET and RESET and negative SET and RESET), reduced protocols were achieved. **Figure 2b** and **d** sketch the protocols used to distinguish the two RS units. Instead of going through the whole sweep as in **Figure 1**, a unique voltage pulse is chosen to reach the LRS. In each case, positive and negative, the highest signal is used to SET the unit while the pulse with the inverted polarity is used to RESET it, and in between two pulses act as the reading voltages to quantify the resistance level. **Figure 2a** (**Figure 2c**) shows the resistance at pHRS and pLRS (nHRS and nLRS) as a function of the elapsed time. **Figure 2a** (**Figure 2c**) corresponds to applied values of +10 V (−10 V)

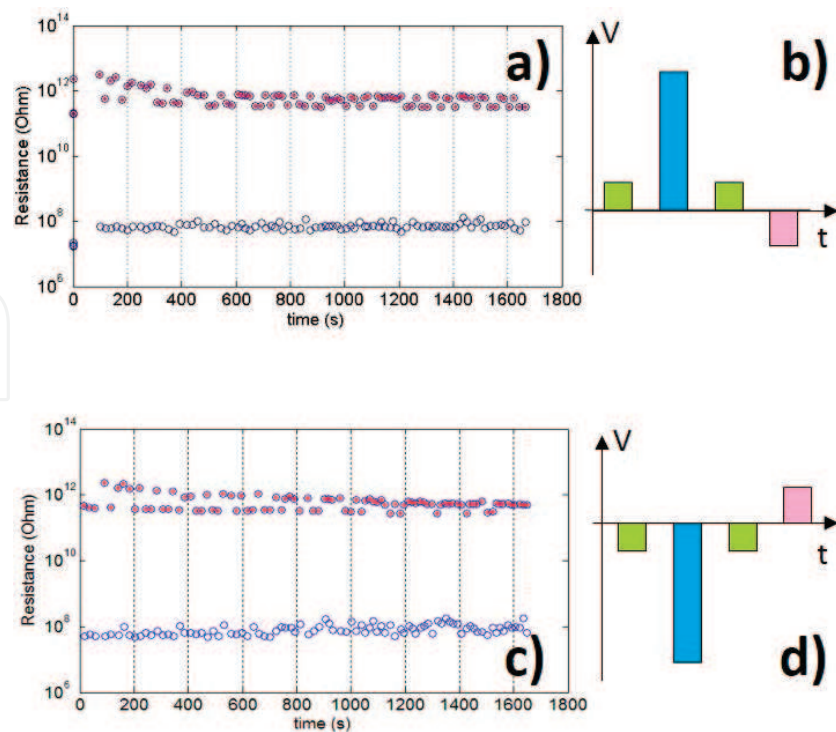


Figure 2. Resistance measured at 3 V after the SET and RESET operations for each RS unit. (a) Corresponds to pHRS and pLRS, with $V_{set} = +10$ V, $V_{read} = +3$ V, $V_{reset} = -3.5$ V (protocol sketched in (b)), while (c) represents nHRS and nLRS, with $V_{set} = -10$ V, $V_{read} = -3$ V, $V_{reset} = +3.5$ V (protocol sketched in d).

for SET operation and -3.5 V ($+3.5$ V) for RESET while the resistance is recorded in between at $+3$ V (-3 V). All applied pulses last for 5 ms. Resistance levels measured at $+3$ V and -3 V can be recognized as the two possible states displayed by the hysteretic curves shown in **Figure 1**. Although some dispersion can be appreciated within each defined state (pHRS, pLRS, nHRS, and nLRS), the rate between each pair of HRS and LRS remains of four orders of magnitude for at least 2000 repetitions.

To gain further insight into the electrical response of the device, we performed capacitance measurements. Capacitance is a differential quantity that has to be recorded applying an AC voltage; frequency and amplitude (levels) are the parameters of such an AC signal. To quantify the capacitive contribution an electrical model is required. Two different models considering a capacitor and a resistor were employed: serially and parallelly connected. In both cases, the capacitive term was equivalent pointing out the predominance of the capacitive over the resistive term. An LCR meter Agilent E4980 parameter analyzer was used to perform the measurements in a two-terminal configuration connected through coaxial wires to a probe station with a heating system.

Figure 3b was obtained applying a 100 kHz–100 mV AC signal while sweeping a superimposed DC voltage. Most relevant conclusions are obtained under different polarization conditions or bias (DC voltage). Remarkably, no change of the capacitance is observed even though the applied DC sweep goes through the values expected to switch the electrical resistance of the device (**Figure 3a**) includes an I-V curve for comparison). Such independence as a function

of DC bias is usually attributed to a parallel-plate capacitor, that is, a MIM stack. Instead, two RS units are supposed to take part in a complex scenario of different states. The measurement of a constant value implies that whatever the involved switching mechanism is, at least the capacitive component will remain unaffected. Moreover, recording C-V at different frequencies and/or temperatures (**Figures 3c** and **4a**, respectively) also exhibits a value independent on the bias.

It is worth pointing out that capacitance appears unaffected by DC stimulus but is strongly dependent on the two additional parameters analyzed: AC frequency and temperature, **Figures 3c** and **4a**, respectively. Since we are using a resistor-capacitor (RC) model and the comparison between the capacitance determined from a parallel array coincides exactly with the one measured considering a series array, the capacitive term seems to indicate an intrinsic feature of the stack. Within this scenario, in a simple RC circuit, capacitances should correspond to the imaginary part of the complex impedance, at the so-called reactance term. The capacitive reactance depends on capacitance and frequency. However, once the capacitance term was identified, the simplified variable should not depend on the frequency. Usually, the dependence of this parameter of frequency is attributed to a wrong determination of the capacitive term and is more notorious in the high-frequency regime [11]. In this case, the full range of available frequencies (from 2 Hz to 1 MHz) was explored, obtaining a monotonous dependence. **Figure 3c** demonstrates the frequency-dependent capacitance by plotting C recorded at four selected fixed frequencies as a function of voltage (each of them, in turn, independent from bias).

Regarding the measurements as a function of temperature, such dependence (**Figure 4a**) reminds us of a semiconductor material since the amount of available carriers increases [16]. However, as we mentioned, the constant capacitance is the signature of a MIM-like stack. How to reconcile an MIM indication, of an invariable capacitance as function of bias, with a semiconductor-like dependence with the frequency? Where does the semiconductor nature

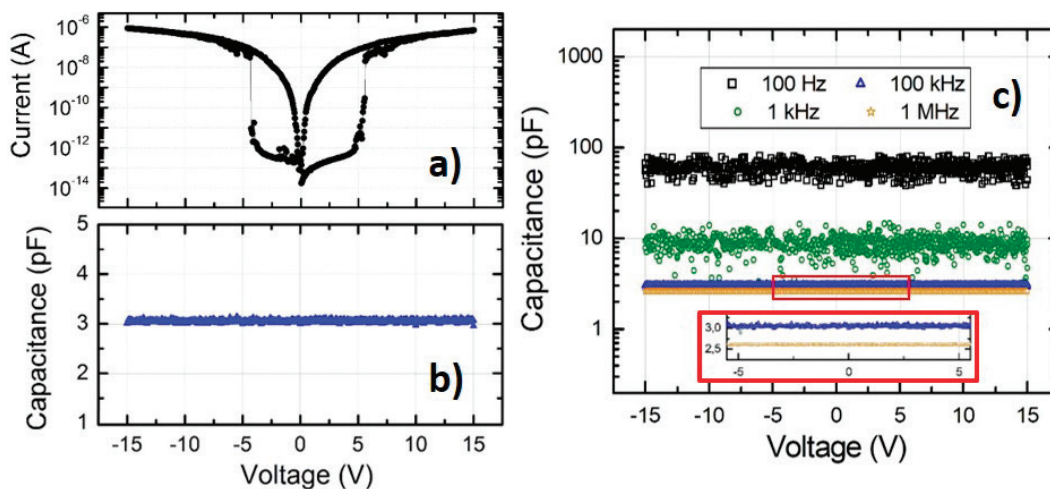


Figure 3. Capacitance as function of bias voltage (C-V) recorded at 100 kHz and room temperature (b). The upper panel (a) offers a reference with the switching observed during an I-V excursion. (c) C-V measured at room T under different AC frequencies.

arise from? Some works report a semiconducting behavior of HfO_2 at HRS [17] but since no change is observed beyond the SET value this cannot be a satisfactory explanation. To have a deep insight on this issue, the LRS was analyzed as a function of the temperature (**Figure 4b**). The current flowing across the stack, measured in a two-terminal connection at +15 V, increases with temperature which evidences a nonmetallic behavior (it could be an insulator or a semiconductor). Moreover, this would be in agreement with the capacitance dependence on the temperature. Nevertheless, it remains unclear as to how to justify the flat C-V observed for the whole bias range.

Beyond the mentioned dependencies, the absolute value of capacitance deserves to be discussed. If we proceed by considering a parallel-plate capacitor (Eq. (2)), as suggested from the C-V flat trend, the dielectric constant of HfO_2 could be found considering the area and thickness as known parameters. Eq. (2) is the capacitance attributed to a parallel-plate capacitor with metal electrodes of area A , a dielectric material characterized by ϵ_r (dielectric constant referred to the vacuum permittivity ϵ_0), and thickness t :

$$C = \frac{\epsilon_0 \epsilon_r A}{t} \quad (2)$$

However, such estimation offers in all the cases (different frequencies and temperatures) extremely low values of ϵ_r compared with the one expected ($\epsilon_r = 0.005$ calculated from experimental data against $\epsilon_r = 20$ which was expected [18]). Even though a certain dispersion could be a reasonable (i.e., related with the particular deposition method), the estimated difference exceeds in orders of magnitude of the spread so far reported. Devices with different areas, HfO_2 thicknesses, and TE materials were also measured supporting the dielectric constant obtained in samples with 20 nm-thick HfO_2 and square ($200 \mu\text{m}^2$) side top electrodes. **Figure 5** includes data from all those devices, showing capacitance scales as expected with area but not with thickness. In fact, three different HfO_2 thicknesses were measured presenting the same absolute value. This independency with the HfO_2 thickness suggests either that the

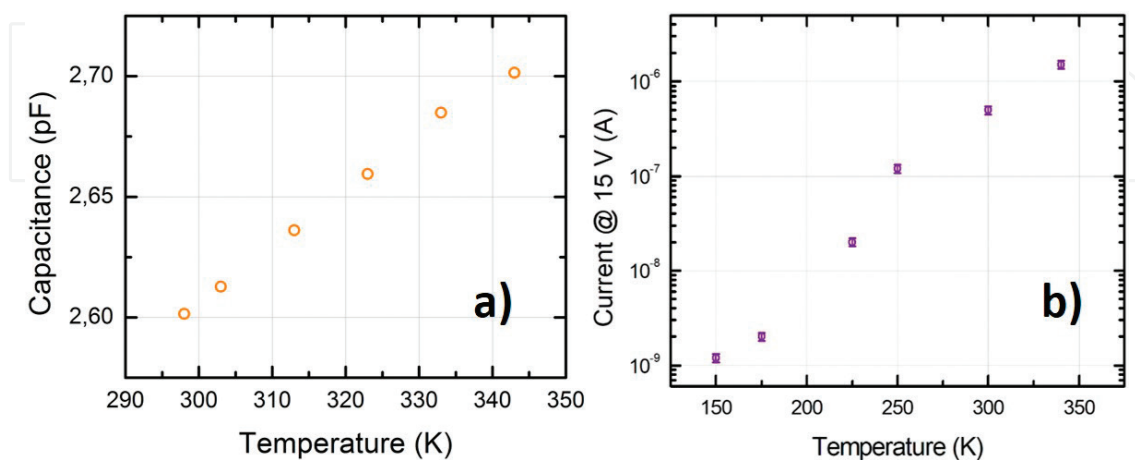


Figure 4. (a) Capacitance as function of temperature. Each point represents the average value obtained within the ± 15 V bias range. (b) Resistance measured at +15 V (pLRS) as function of temperature. The decrease is usually attributed to a nonmetallic behavior.

model is incorrect (capacitance does not originate from the TE/HfO₂/Ti like in a parallel-plate capacitor fashion) or that HfO₂ is not the dielectric of the capacitor that governs the general trend. Importantly, also, Au electrodes were tested without remarkable differences. Although a semiconductor behavior is deduced from the temperature dependence, a capacitive term related with some depletion layer formation is ruled out since the C-V trend should follow the width modulation with bias.

Another interesting issue is extracted from the extrapolated intercept in **Figure 5**. A zero intercept is expected when a pure capacitor is measured. Instead, a nonzero value is related with an extra contribution usually from unconsidered terms, such as interfacial effects. However, if an interfacial effect is suspected, that should not be at the TE interface since the two explored materials seem to converge to the same intercept. The possibility of a nonzero intercept also highlights the need of measuring many areas in order to get the real slope. The upper-left inset demonstrates the difference between point-to-point slope determination and the real one provided by the area dependence.

So far, the capacitance dependence does not follow the expected trend with HfO₂ thickness. In addition, the absolute value of the measured capacitance appears not to be related with the dielectric constant usually attributed to such materials. Something else determines the capacitive behavior, although a depletion layer formation was discarded based on the absence of dependence with bias voltage. Moreover, two different memristive cells were necessary to explain the non-crossing feature and the impossibility of appreciating RESET operations. There is no clue yet about where those RS units, acting as junctions, are located. However, once more if we consider two different elements a plausible picture is obtained. **Figure 5c** sketches two M-I-S (metal-insulator-semiconductor) devices connected in series. As it is well-known the sum of capacitors in series is governed by the smaller term, because the sum

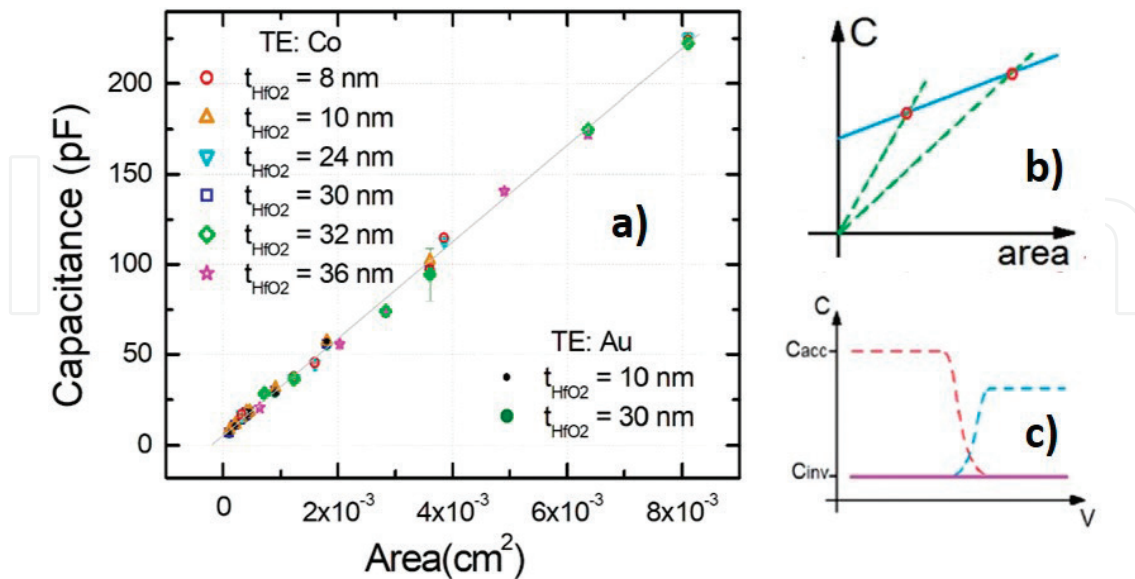


Figure 5. (a) Capacitance as function of area, including many different samples measured at 100 kHz. Capacitance scales as expected with area while no variation is observed for different HfO₂ thicknesses. Considering different TE's material does not reflect changes. (b) Sketch of a proposed explanation for the behavior observed in **Figures 3, 4** and **5a**). (c) Sketch of two M-I-S devices connected in series.

corresponds to the inversion value for each MIS. Since the inversion value of capacitance is not directly related to the dielectric material but to the semiconductor properties, that offers a possible explanation for the independence with HfO_2 thickness. Also, given the fact that the semiconductor rules the absolute capacitance value, the temperature dependence can be satisfactory understood.

Interestingly, the accuracy of such an explanation arises on the fact of considering two MIS stacks with opposite-doped semiconductors but exactly the same flat-band condition, which means the voltage required to exactly compensate the band bending. That voltage is the one at which the change between accumulation and depletion occurs. Now, two new questions appear:

1. Why should the inversion capacitance for both MIS stacks be coincident? and
2. Why they switch from accumulation to inversion and vice versa at the very same voltage?

In the following we will try to identify the origin of these two elements within the stack composition to answer these questions.

2.2. Structural characterization

In order to determine each layer's thickness, roughness, and density within the obtained stack, X-ray reflectivity (XRR) was recorded. Since the top electrodes are patterned, that is, Pd/Co does not constitute a uniform layer, the samples studied by XRR do not have the metal cover. This technique distinguishes materials by their electronic density. A typical measurement consists of the grazing incidence of X-rays, starting with total reflection and followed by a pronounced decrease identified as the critical angle, when the X-rays start penetrating the material. Following oscillations are related to the interference pattern produced by the interference of X-rays reflected by the different interfaces present within the sample under study. The critical angle and the period are directly related to the density of the material on top and the total thickness, respectively. Further estimations require a model and, by fitting it, a deeper comprehension of the stack can be achieved. **Figure 6a** includes XRR experimental data and a fitting. The experimental data are shown normalized by the Fresnel coefficient ($R_F = 16 \pi^2 / Q^4$) and the x-axis uses the propagation vector (Q) instead of 2θ . The good agreement between experiment and fitting provides a reasonable confidence about the conclusions extracted from it. It is worth pointing out that some parameters were previously determined in order to reduce the parameter space and get a physical representative set of values, that is, the HfO_2 roughness was fixed as the value obtained from atomic force microscopy (not shown). Results are summarized in **Table 1**.

As discussed, the contrast in this X-rays technique is related with the electronic density of the materials. This feature makes it impossible to distinguish between Ti and TiO_2 layers. However, an important conclusion has to be highlighted; the Ti-related layer is 50% thicker than what it was supposed to be. Since the accurate control of Ti sputter deposition can be assured, this could consist of an indirect proof of oxidation.

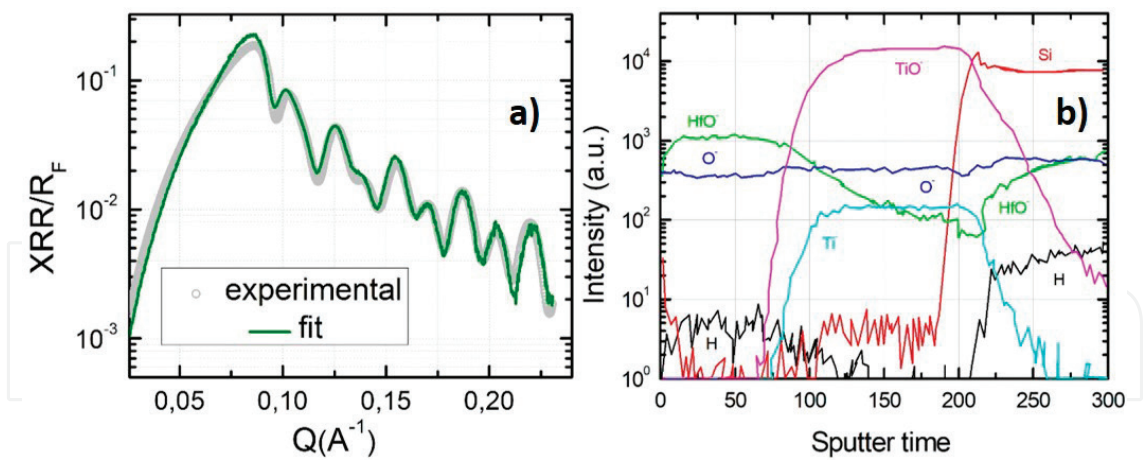


Figure 6. (a) X-ray reflectometry normalized with Fresnel coefficient ($R F = 16 \pi^2 / Q^4$) as a function of the incident propagation vector. A good agreement between experimental and fitting is achieved. (b) Secondary ion mass spectroscopy (SIMS) as a function of elapsed sputtering time. During the etching of the sample the signals of the expected species are recorded. The intensity, in logarithmic scale, relates with the relative presence of each compound while deeper layers are reached as sputter time passes through.

	Parameter	From fitting	Expected
HfO ₂	Thickness [nm]	26.5	20
	Roughness [nm]	Not fitted	1 (AFM determined)
	Density [g/cc]	10.1	10.12
Ti/TiO _x	Thickness [nm]	27.8	20
	Roughness [nm]	0.6/1.,9	—
	Density [g/cc]	4.3/3.8	4.50/4.25
SiO ₂	Thickness [nm]	45.9	120
	Roughness [nm]	0.3	—
	Density [g/cc]	2.5	2.65

Table 1. Summary of parameters obtained from XRR fitting compared with expected values.

Note that for the underlying SiO₂ layer the obtained density is quite precise. However, we did not expect the proper thickness for that layer because the angular resolution limits the maximum accessible value (usually below 150 nm).

To define whether a pure Ti or a TiO₂ layer is present, secondary ion mass spectroscopy (SIMS) was performed at room temperature (**Figure 6b**). This is a destructive technique in which an Ar beam impacts the sample detaching its constituent atoms, which are collected by a detector. In this way, as the Ar beam etches the surface progressively, a profile composition is obtained (depending on the etching rate, the time variable can be regarded as the depth function). Starting with an exposed HfO₂ layer, as the sputter time increases, traces attributed to deeper layers can be observed. When the HfO⁺ signal decreases, Ti and TiO⁺ traces

increase pointing out the interface location. **Figure 6b** allows one to recognize oxygen presence through the full titanium layer. Complete oxidation of the titanium layer implies an absence of the Ti bottom electrode and, in that case, the bottom electrode would be formed by the highly doped silicon substrate. According to such an observation, and as it was suggested by electrical measurements, a thicker dielectric material has to be considered.

2.3. Additional deposition process

Thus, both electrical and chemical evidence indicate a clear layer modification by which the stack is significantly modified compared to the designed stack. Nonetheless, RS was positively affected in the way that some desirable properties were improved. From the technological point of view, extremely low leakage currents, free-forming behavior, complementary bipolar junctions, and low power consumption are at the core of qualities that the next memory generation has to achieve. All these properties were attained by samples presented herein (for more details see Ref. [19]). Thus, it is of paramount importance to disentangle the oxygen source and metal precursor effects of the ALD HfO₂ process on the titanium oxidation.

So far, ALD HfO₂ deposition has not been reported for such underlying layers' modification. To validate our hypothesis about O₃ influence, an additional fabrication proposal was dealt with. The aim of such exploration is to use H₂O instead of O₃ as an oxygen source, maintaining the hafnium precursor as before. As shown in **Table 2**, different combinations of layer thicknesses were explored. Thicker and thinner Ti layers (than the one used in the initial batch) will allow us to understand the impact of oxygen diffusion on the Ti metal-layer oxidation. Also, different HfO₂ thicknesses will help to clarify whether the ALD cycles, the temperature persistence, or the longer diffusion times give rise to the discovered oxidation of the full Ti layer.

2.4. Microscopic picture beyond the macroscopic behavior

Structural and electrical characterizations do not show any significant variation with respect to usual HfO₂-based RS devices reported elsewhere [20, 21]. All of them show a forming requirement and are needed to be externally limited to avoid current runaway. After the forming operation, states of high power consumption (mW) were observed. Besides, no

SiO ₂ thickness	Ti thickness	HfO ₂ thickness	Access to BE
120 nm	20 nm	10 nm	Scratch
120 nm	20 nm	20 nm	SiO ₂ removal from back contact
120 nm	10 nm	20 nm	Scratch
120 nm	20 nm	20 nm	SiO ₂ removal from back contact
120 nm	—	20 nm	Scratch
120 nm	—	—	Scratch

Table 2. Details of complementary batch designed to disentangle oxidant and/or precursor effects.

double rectification was appreciated within the new batch. All those remarkably features, highlighted as desired in the former case (with ozone as oxidant), seem to be related with the TiO_x layer formed in the experiments. **Figure 7** constitutes one example of the referred characteristics: forming operation, no-self limitation, and crossing behavior. Moreover, Yoon et al. [22] who follow a similar deposition process (O_3 -based ALD-deposited HfO_2 over a Ti layer) demonstrate current-voltage dependence strikingly similar to that reported here. Although they attribute such behavior to the interface quality, structural analysis is missing, leading to thinking about an effect of Ti oxidation (in the following referred to as TiO_x), analogous to what was demonstrated in this study. **Figure 8** summarizes the subsequent steps that would explain the proposed stack composition of the ozone-based samples.

In this framework a picture of the involved mechanism in such unusual switching is required. Since the resultant stack was shown to be composed by a multilayer insulator (20 nm of HfO_2 , 30 nm of TiO_x and 120 nm of SiO_2), it is hard to justify any reversible switching operation.

We will now focus on the role of the SiO_2 dielectric layer, which was thermally grown from the very initial Si wafer.

Thermal oxidation is closely related with semiconductor doping. Si doping, related with wafer resistivity (4–40 m Ω cm, provided by the manufacturer), is about $4 \cdot 10^{18}$ – $4 \cdot 10^{19}$ cm $^{-3}$ and allows one to understand that although a semiconductor behavior is expected, such high doping screens its nature. Within this scenario Si behaves like a metal and explains capacitance independence with respect to bias stimulus. Nonetheless, this issue hinders capacitance-temperature dependence explanation. Besides, a highly doped semiconductor affects the growth rate [23] and the impurity content of the resultant oxide [20]. This explains the current flow across a 200 nm dielectric as trap assisted [16] and justifies such a low current level, even at LRS.

Within a multilayered dielectric, the voltage drop on each layer (Eq. (3)) is subjected to each layer's permittivity, ϵ_i [24]. Although such an estimation seems very complex in this situation,

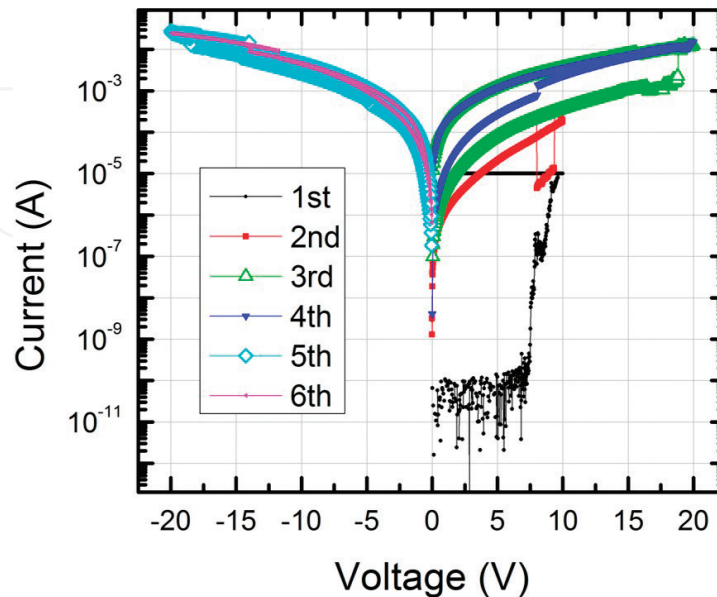


Figure 7. Prototypical behavior of one sample SiO_2 (120 nm)/Ti (10 nm)/ HfO_2 (20 nm)/Pt of the new fabrication process. After the first voltage excursion, the device is found in an irreversible low resistance state.

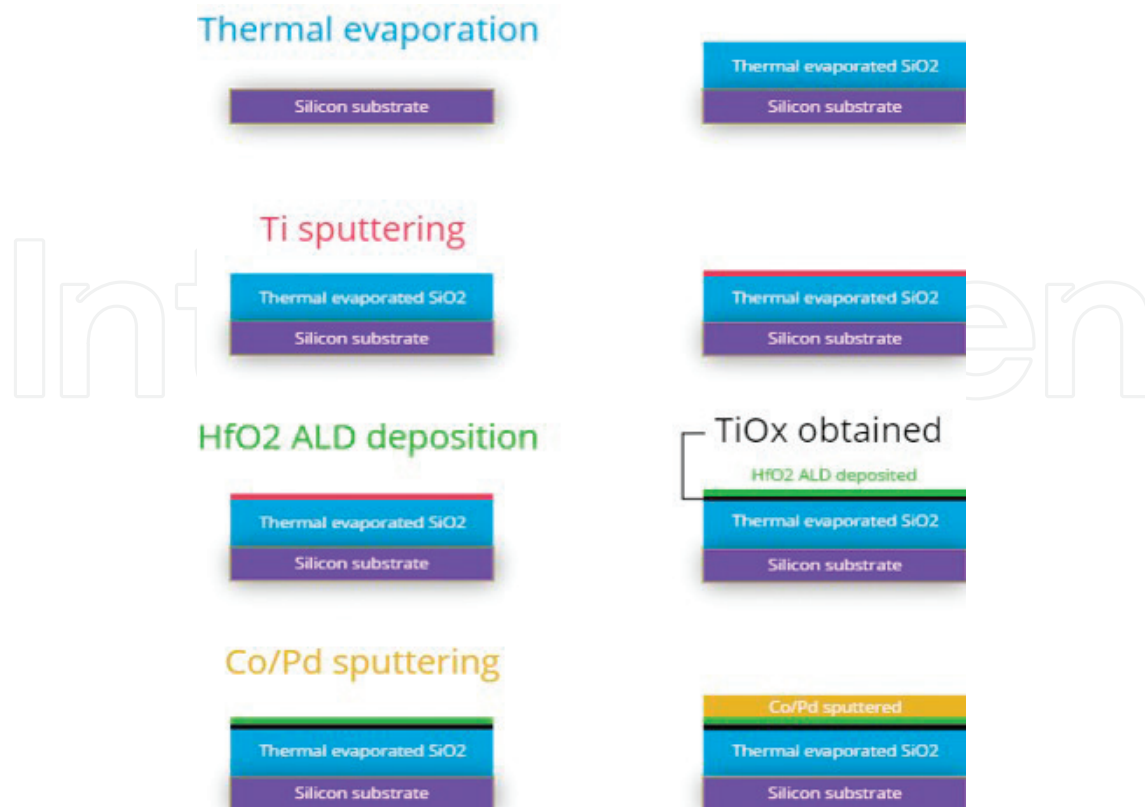


Figure 8. Sketch of process flow and the changes produced during ALD process using ozone as oxidant.

at least it is possible to argue that HfO_2 has a higher permittivity than it was ever reported to SiO_2 [20] and lower than what could be attributed to TiO_2 and its related sub-oxides (generally denoted as TiO_x [25, 26]). **Table 3** presents an estimation of voltage drops on each dielectric sub-layer. This means that most of the voltage drop is restricted to the SiO_2 layer avoiding HfO_2 and/or TiO_x to be formed and/or switched.

$$V_i = \eta_i V_{tr} \quad \text{where} \quad \eta_i = \frac{t_i}{\epsilon_i} \cdot \frac{1}{\sum_j \frac{t_j}{\epsilon_j}} \quad (3)$$

The situation could be summarized as follows: a multilayered dielectric sandwiched between two metal-like electrodes (Pd/Co and highly doped Si) shows RS. Such behavior cannot be explained by usual HfO_2 or TiO_2 switching because of the voltage drop competition, associated with their individual dielectric constants. On the other hand, Eq. (3) relies on the fact that no charges are present at the interfaces and, consequently, no voltage drop is expected in those regions. It is not clear whether this assumption is correct or not but even if so, the voltage drop on the HfO_2 and/or TiO_x should be indeed lower than considered (making harder the switch of each layer).

We can also use the impedance spectroscopy (IS) technique to deepen the understanding of the mechanisms involved in the resistive switching. In this particular case, to measure the impedance, in the range 100 Hz–10 MHz, we set the oscillator amplitude of the impedance analyzer to 5 mV and applied a DC bias of 3 V. In this context, the obtained results for the complex impedance are presented in a complex plane plot usually called the Nyquist diagram [27],

Material	ϵ_i	Thickness (nm)	V_i (V)
HfO ₂	20	10	0.24
TiO _x	80 (40)	30	0.18 (0.36)
SiO ₂	3.9	120	14.58 (14.40)
Total		160	15

Table 3. Voltage drop on each dielectric sublayer. Quantities between parentheses indicates voltage drop variation depending on the permittivity attributed to TiO_x.

where minus the imaginary part of the impedance is plotted as function of the real one. In **Figure 9a** and **b** the Nyquist diagrams corresponding to pHRS and pLRS are shown. In these plots, each point corresponds to the imaginary and real components of the impedance at different frequencies. It is interesting to remark that the capacitive behavior of the measured devices is evidenced by the negative values of the measured imaginary part of the impedance. If a model is proposed for the equivalent circuit of the device, the value of each equivalent component can be found.

In **Figure 9a** and **b**, the inset show the equivalent circuit used to model the impedance of each state. In the pHRS (**Figure 9a**), two blocks connected in series were necessary to properly fit the measurements while only one was required in the pLRS case (**Figure 9b**). Both the low- and high-resistance states have a common block composed of a resistor in parallel to a constant-phase element (CPE) [27]. In addition, the high-resistance state has also another block constituted by a resistor in parallel with a capacitor. The obtained values for all these elements are summarized in **Table 4**. A CPE is an artificial way of representing a wide dispersion of characteristic times. It can be thought as a capacitor but instead a unique resonant condition, a dispersion of them (usually related with different species underneath), is taken into account. Its mathematical expression is given by $Z_{CPE} = A(j\omega)^{-\alpha}$ where A and α are related specifically with the system, while ω is the angular frequency.

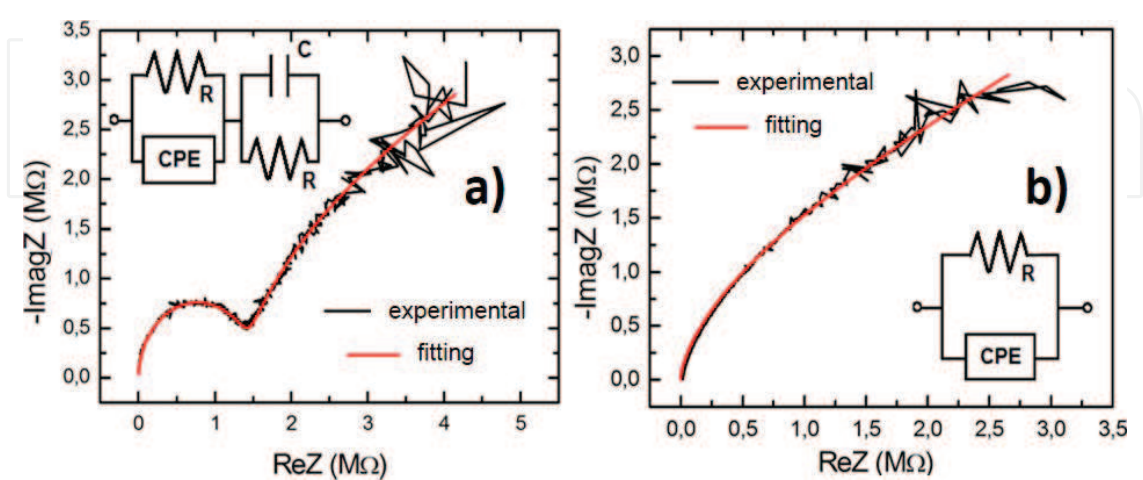


Figure 9. Nyquist plot constructed from impedance measurements under +3 V bias and 5 mV AC signal in (a) pHRS, and (b) pLRS.

		pHRS	pLRS
R-CPE	R	$1.1 \cdot 10^7 \Omega$	$9.6 \cdot 10^6 \Omega$
	m (CPE)	0.71	0.74
	p (CPE)	$3.7 \cdot 10^{-10}$	$2.8 \cdot 10^{-10}$
R-C	R	$1.3 \cdot 10^6 \Omega$	—
	C	$4.7 \cdot 10^{13} \text{ F}$	—

Table 4. Parameters of the models used to fit the Cole-Cole diagrams of **Figure 9a** and **b**.

In this case, we will not focus on the model for each state (pHRS and pLRS) but in the comparison of them. It is worth to point out that an equivalent behavior was obtained also in the comparison of the nHRS and nLRS. For that reason, in the following, we will refer generically to HRS and LRS even though only the positive case is being presented. Our aim is to get a more detailed comprehension of the switching behind the macroscopic behavior. Compared with **Figure 9a**, experimental data of **Figure 9b** could be mimicked with only one of the two arrays mentioned before. It seems that the LRS maintains the wide dispersion of species that gives rise to the CPE element while the parallel capacitor-resistor block disappeared. This finding, together with the fact that the parallel resistor-CPE remains constant, reveals that a diode has been overcome. A block consisting of a parallel capacitor-resistor is the usual model to represent a diode below the forward-biased threshold. Thus, the removal of that block to model the LRS implies a diode-like behavior during the HRS and consequently a barrier to overcome in order to get the conductive condition.

Finally, we suggest a plausible mechanism for switching operation: TiO_2 interfaces with HfO_2 and SiO_2 could play the role of a barrier, originating two junctions. Band bending would assist the current to flow through one of them, while the other has to be overcome after charge trapping had taken place. That would offer possible states in the forbidden gap to the electrons. A condition for which this happens could be related with each sharp switching operation (observed in I-V dependence). This could be the reason why half of a loop in the DC I-V curve was also identified in Ref. [22]. In that case, TiO_x had only one interface with an oxide suitable to be switched. Thus, a trapping-based mechanism would be attributed to such behavior which cannot be reflected by capacitance measurements. In such a way, no capacitance change could be expected. Moreover, the TiO_x semiconductor nature would explain the capacitance-temperature dependence that we observed. It is worth to point out that resistive switching mechanisms without ion movement requirement have attracted attention since it would be less downgrading to the memory cell neighborhood, in terms of chip integration [28].

3. Conclusions

We described the ALD technique in detail, pointing out many interesting, efficient and unique capabilities. Besides, we highlighted the problem found when there is an interaction of a

material to be deposited or the precursors used in its growing process, with the pre-deposited layers on the substrate. We exemplified the case describing a particular case, where the non-volatile memory device of the ReRAM type was grown.

The ALD technique was used to obtain HfO_2 -based devices with some remarkable features. The use of different precursors, and the fact that a non-negligible interaction between these precursors and pre-existent stacks could produce unconsidered phases, has been discussed in detail. A careful analysis of the device's structure (initially suggested by difficulties in the understanding of measured electrical features) triggered the comprehension of the actual structure of the device. An additional oxide layer was formed because the precursor reacted with the buffer material, giving rise to a completely different stack. Remarkably, this fact rendered advantageous properties which could be useful in the field of multifunctional memory applications.

While an MIM stack was expected (consisting of $\text{Pd/Co/HfO}_2/\text{Ti}$), a post-deposition structural characterization proved oxidation of the metallic layer underlying the ALD-deposited oxide. Using water instead of ozone as an oxidant allowed to attribute titanium oxidation to the very high reactivity of the oxidant primary employed. Once the complete stack composition was determined, a feasible scenario about the switching mechanism was proposed. This gathers the evidence obtained, through electrical and structural measurements, in a unique picture that captures all features highlighted within memory behavior.

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Conflict of interest

The authors do not declare any conflict of interest.

Notes/thanks/other declarations

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