Chapter 1

Modeling of Nano-Transistor Using 14-Nm Technology Node

Soheli Farhana

Additional information is available at the end of the chapter

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Abstract

Latest process technologies in transistor development demonstrate massive changes in the size of transistor chip. In this chapter, a 14-nm technology node is used to model nanosize transistor. The 14-nm technology node consists of multiple numbers of carbon nanotube. Carbon nanotube is a very good energy efficient and low-cost material. Carbon nanotube demonstrates excellent characteristics in metallic and semiconducting characteristics by analyzing electrical properties. At first, the nanotube device physics and material properties are briefly explained in this chapter. Further, a nanotube device is designed for semiconducting properties. The gate length of nanotube is 14 nm which is placed on the gate channel. Finally, the model of 14-nm nano-transistor will be demonstrated for low-energy consumption which can be considered as a better replacement of CMOS.

Keywords: nano-transistor, 14 nm, electrical properties, I-V characteristics, low energy

1. Introduction

Nanoelectronics research is upgrading due to the increases of consumer demand of electronics device in small scale. Nanotechnology research area encourages the researchers to work on nanomaterials as an immerging technology for future. Carbon nanotube (CNT) is a potential material in the field on nanotechnology that has the ability to overcome almost all the limitations of other nanomaterials for its excellent electrical and mechanical properties. Therefore, one of the potential uses of CNT is to place as gate channel of a FET is called carbon nanotube field effect transistor (CNTFET). Silicon-based circuit is moving towards its physical limitation point according to the proven experiment [1]. Due to similar ballistic transport and high career portability of silicon material, CNTFET can be a good replacement of silicon [2] while CNT can

be acted as a semiconducting material [3, 4]. Nanotube is able to show its excellent electrical properties in designing digital devices [5, 6] in small scales. Another special characteristic also to be highlighted for nanotube is I-V features which enable to use the CNT in MOS transistors [7–10]. According to device physics, the performance of the chip can be improved by reducing the size but there is a limitation about the reduction of silicon device size. Nano-hardware, which was created from the 1990s, has turned out to be a standout amongst the most dynamic research subjects in this day and age. The nanoelectronics innovation, which can fundamentally diminish the transistor measure, is particularly alluring to individuals. Single-walled carbon nanotube is mostly used in transistor [11]. Ballistic transport properties of MOS transistor are unchanged while the gate channel Si is substituted by nanotube [12]. In perspective of the outstanding size-lessening issues of traditional Si-based hardware, there have as of late been serious examinations on new advances in light of nano-organized materials which are shaped by sorted-out development and self get-together strategies. CVD process was used in the laboratory to grow nanotube from dielectrophoresis in early ages of its generation [13]. The first CNTFET was fabricated for prototype testing [14] which allows the researchers to work on this promising field of nanotechnology. CNTFET shows good performance in designing logic gates for integrated circuit modeling [15, 16]. Therefore, CNTFET can be a promising research in the near future.

2. Carbon nanotubes properties

2.1. Geometry of carbon nanotubes

A carbon nanotube can be characterized by chiral vector and its length and a vector called the chiral vector. Chiral vector is the sum of the multipliers of the two base vectors, like Eq. (1) [17–20]

$$C_h = m\mathrm{a}_1 + n\mathrm{a}_2 \tag{1}$$

The coordinates of the graphene sheet (m,n) allows finding the chiral vector (C_h) of the nanotube.

The two-dimensional graphene lattice in real space can be created by translating one unit cell by the vectors $\overline{T} = n\overline{a}_1 + m\overline{a}_2$ with integer combinations (n, m), where $\overline{a}_1$ and $\overline{a}_2$ are basis vectors and is shown in **Figure 1**,

$$\begin{aligned} \overline{a}_1 &= a_0\left(\frac{\sqrt{3}}{2}\widehat{x} + \frac{1}{2}\widehat{y}\right) \\ \overline{a}_2 &= a_0\left(\frac{\sqrt{3}}{2}\widehat{x} - \frac{1}{2}\widehat{y}\right) \end{aligned} \tag{2}$$

$a_0 = 3a_{cc}$ is the length of the basis vector, and $a_{cc} \approx 1.42$ Å is the nearest neighbor C-C bonding distance.

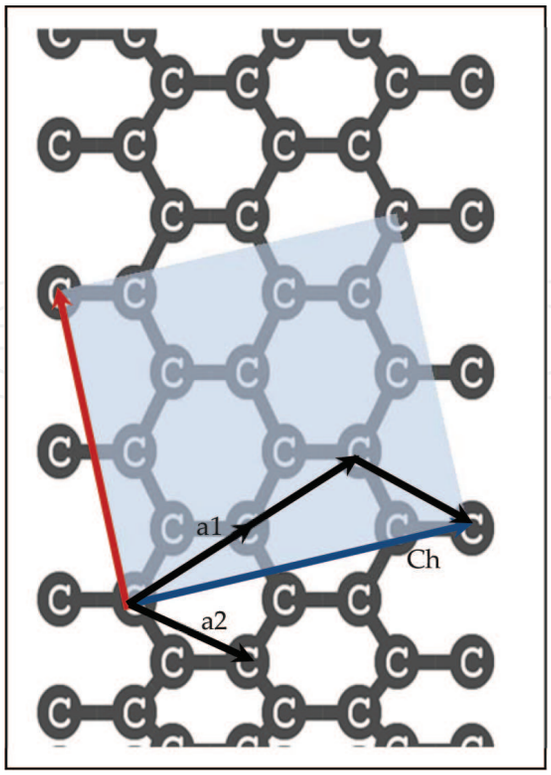

Figure 1. The nanotube unit cell.

To all the more decisively acquire the moment vector T, we can get it from the m, n segments of the C_h vector. On the off-chance that we demonstrate the parts of T with t_1 and t_2, as T is opposite to the C_h, the inward result of these vectors is equivalent to zero and we can conclude Eq. (3)

$$t_1 * a_1 + t_2 * a_2 = 0 \tag{3}$$

The briefest vector t_1 and t_2 that are legitimate as per Eq. (3) can be isolated t_1 and t_2 by their most prominent normal devisor or in short shape most noteworthy basic divisor (gcd), to acquire the briefest nuclear site vector towards the path, opposite to the C_h vector. d_R as in Eq. (4), t_1, t_2 can be accomplished in Eqs. (5) and (6)

$$d_R = \gcd\,(m + n, 2n + m) \tag{4}$$

$$t_1 = \frac{2m + n}{d_R} \tag{5}$$

$$t_2 = \frac{2n + m}{d_R} \tag{6}$$

The angle between the chiral vector and the a_1 base vector is called the chiral angle, the twist angle or the helix angle and is denoted by θ_c and can be obtained in Eq. (7)

$$\theta_c = Arctg\left(\frac{\sqrt{3}m}{2n+m}\right) \tag{7}$$

Here, we should take note of that to consider a one of a kind chiral plot for each nanotube; the point is expressed by an incentive in the locale (0, 30°). Utilizing these definitions, the breadth of the tube can be processed utilizing the balance of the length of the C_h and the nanotube's periphery; lastly, we can acquire the measurement characterized by

$$d_t = \frac{L}{\pi} = \frac{a}{\pi}\sqrt{n^2 + nm + m^2} \tag{8}$$

The length of the chiral vector is the peripheral length of the nanotube:

$$L = |C_h| = a\sqrt{n^2 + nm + m^2} \tag{9}$$

The bandgap of a single wall nanotube (SWNT) is defined by

$$E_g = 2\gamma_0 a_{cc}/d_t \tag{10}$$

From Eq. (4), if (n-m) is divisible by 3, then nanotube is metallic, otherwise the nanotube is semiconducting.

Now, the number of atom of the nanotube is defined by

$$N_{at} = 4*\frac{n^2 + m^2 + nm}{d_R} \tag{11}$$

2.2. Classification of carbon nanotubes

Carbon nanotube (CNT) is classified into three groups as shown in **Figure 2**: (1) armchair, (2) zigzag and (3) chiral, based on the geometrical arrangements of the graphene during the form tube formation.

If the C_h is defined as $(n, 0)$, it is given the name zigzag nanotube and if the C_h is defined as (n, n), then the tube is called armchair, and these refer to the form shaped on the circumference of the tube.

2.3. Carbon nanotube formation

2.3.1. Armchair tubes

If the chiral indices (m, n) of a nanotube in a zone-folding region can be divisible by 3, then it becomes metallic. These nanotubes are called 'zone folding metallic', or shortly, $Z_{F\text{-}M}$ tubes.

2.3.2. Zigzag tubes (semiconducting tubes with bandgap)

The primary band gap of a nanotube is considered as semiconducting material if the Chirality (m, n) in the zone folding area is not divisible by 3. We should allude to these nanotubes as 'zone collapsing semiconducting', or in a matter of seconds, ZF-S tubes.

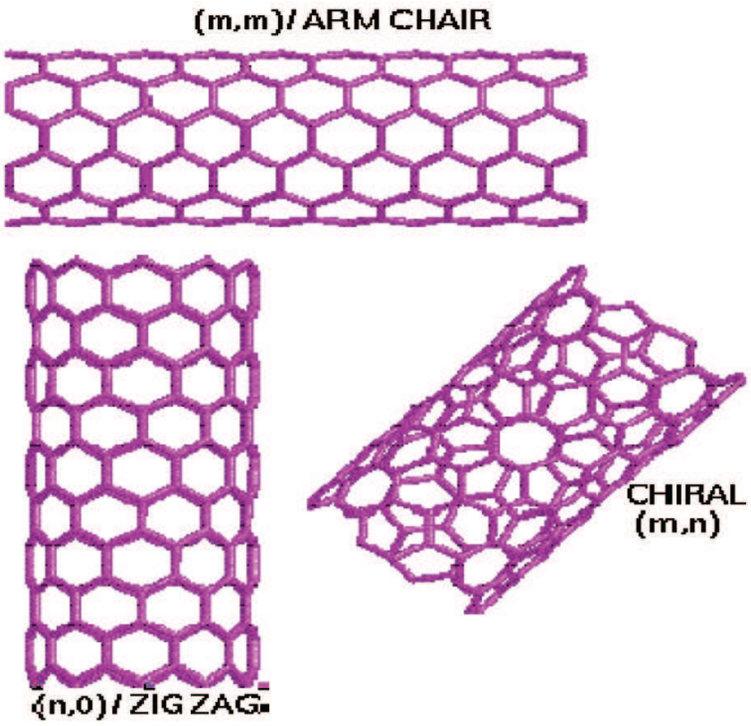

Figure 2. Classifications of different CNTs: (a) armchair, (b) zigzag and (c) chiral (François, 2009).

2.4. Electrical properties

Carbon nanotubes (CNTs) have outstanding electrical properties based on the chirality. There are two types of carbon nanotube, such as single-walled carbon nanotube (SWCNT) and multiple-walled carbon nanotube (MWCNT) based on the requirements of the CNT in the integrated circuit (IC) design [21–23]. **Figure 3** shows the different types of carbon nanotube. A single-walled carbon nanotube has only one shell with a small diameter usually less than 2 nm.

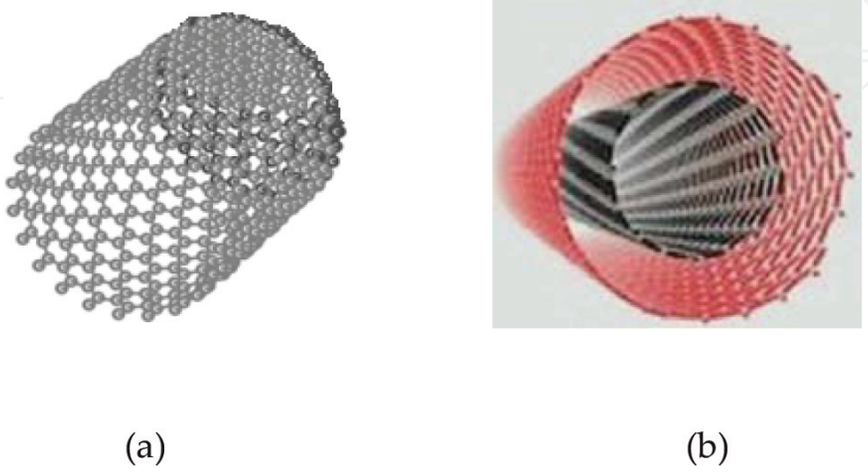

Figure 3. Diagram of carbon nanotube: (a) single-walled and (b) multi-walled (François, 2009).

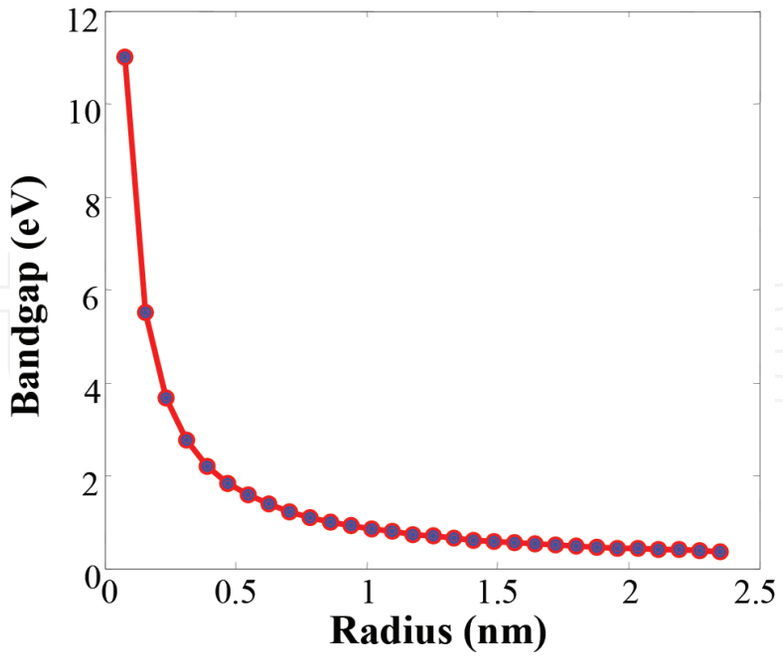

Figure 4. Bandgap versus radius for zigzag nanotube.

As well as multi-walled carbon nanotube consists of two or more concentric cylindrical shells with the diameter of 2–30 nm.

The electrical properties of a nanotube can be realized from its bandgap. Semiconducting nanotube is a novel choice for the transistor development. Thus, **Figure 4** shows bandgap versus radius for semiconducting (zigzag) nanotubes. The bandgap decreases inversely with an increase in diameter. The points with a zero bandgap correspond to metallic nanotubes which satisfy n = 3i, where i is an integer.

3. Modeling process of 14-nm CNTFET

This research consists of the design and verification of the CNTFET device's small signal model. **Figure 5** shows a solid model of CNTFET with a built-in circuit model in this work.

3.1. CNTFET biasing

Three different types of biasing structure are seen in the CNTFET device. They are common-drain, common-gate and common-source structure. Common-source transistor circuit is considered in this modeling. The common-source circuit is shown in **Figure 6**; the DC shows bias on drain and gate with an AC signal present as the input at the gate.

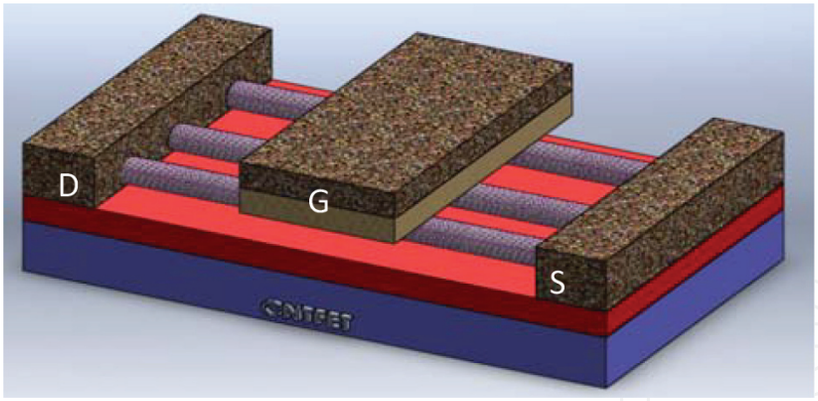

Figure 5. Perspective view of the CNTFET 3D solid model.

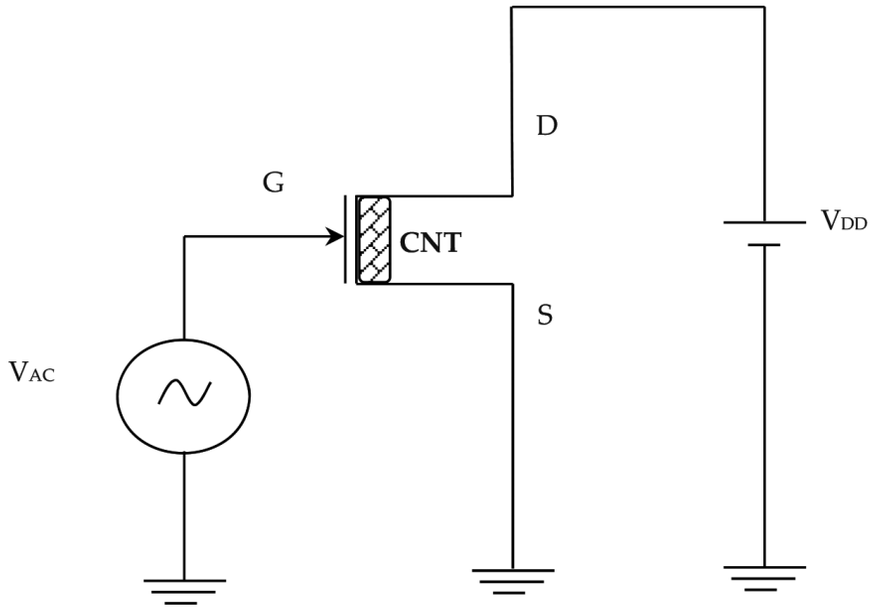

Figure 6. Common-source biasing circuit.

3.2. CNTFET small signal model

This section describes about the design and analysis of the small signal model circuit for CNTFET. The proposed small signal model of a CNTFET is shown in **Figure 7**. In **Figure 7**, $C_{g\text{-}CNTS}$ refers to the capacitance between gate electrodes to source, $C_{g\text{-}CNTD}$ refers to the capacitance between gate electrodes to drain, $C_{g\text{-}CNTS}$ refers to the capacitance between gate electrodes to source, and Ri represents the internal resistance. Furthermore, g_m refers to the intrinsic transconductance and g_d refers to the drain conductance of the circuit as shown in **Figure 7**. In this circuit, the parasitic elements are excluded for the analysis purpose.

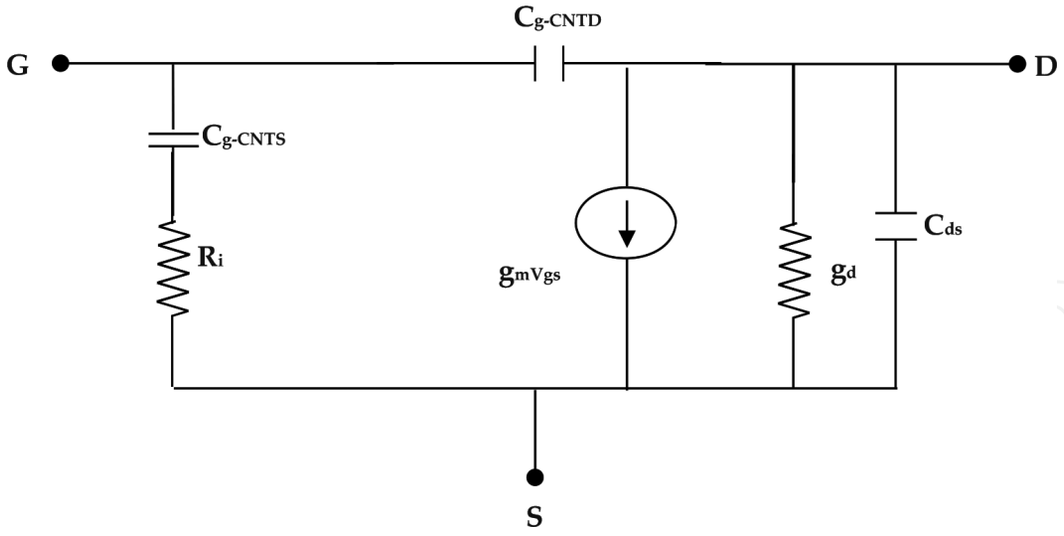

Figure 7. Intrinsic circuit model for CNTFET.

4. Analysis of CNTFET model

4.1. Transconductance of CNTFET SPICE model

Figure 8(a) and **(b)** shows the simulation results of frequency versus transconductance while the transconductance is increased linearly. This is as a result with μS through the stage of the lower frequency as well as mS through the stage of increasing frequency. Therefore, high-frequency small signal model of CNTFET is obtained in 10 THz with 1.8 mS. On analyzing the data, we first calculate and simulate the transconductance value in μS and in mS.

Figure 8(a) shows the plot for the value of transconductance in μS and **Figure 8(b)** shows the plot for the value of transconductance in mS.

Tables 1 and **2** show the selected values of transconductance necessary for the small signal model obtained from the analysis of the model as shown in **Figure 8(a)** and **(b)**. By comparing the two tables, transconductance in mS performs the higher frequency rather than to use in μS. Therefore, we consider transconductance in mS in this research.

4.2. I-V characteristics of CNTFET

The proposed CNTFET circuit model is implemented in PSpice. A CNTFET DC characteristic is analyzed and simulated to check the output characteristics. Modeling of CNTFET with the I-V characteristics analysis is obtained from the channel length of 14 nm and width of two times the length of the proposed CNTFET. The I-V characteristic curves validate the proposed circuit model by getting drain current of 6.9×10^5 A at the applied gate voltage of 0.4 V as shown in **Figure 9**.

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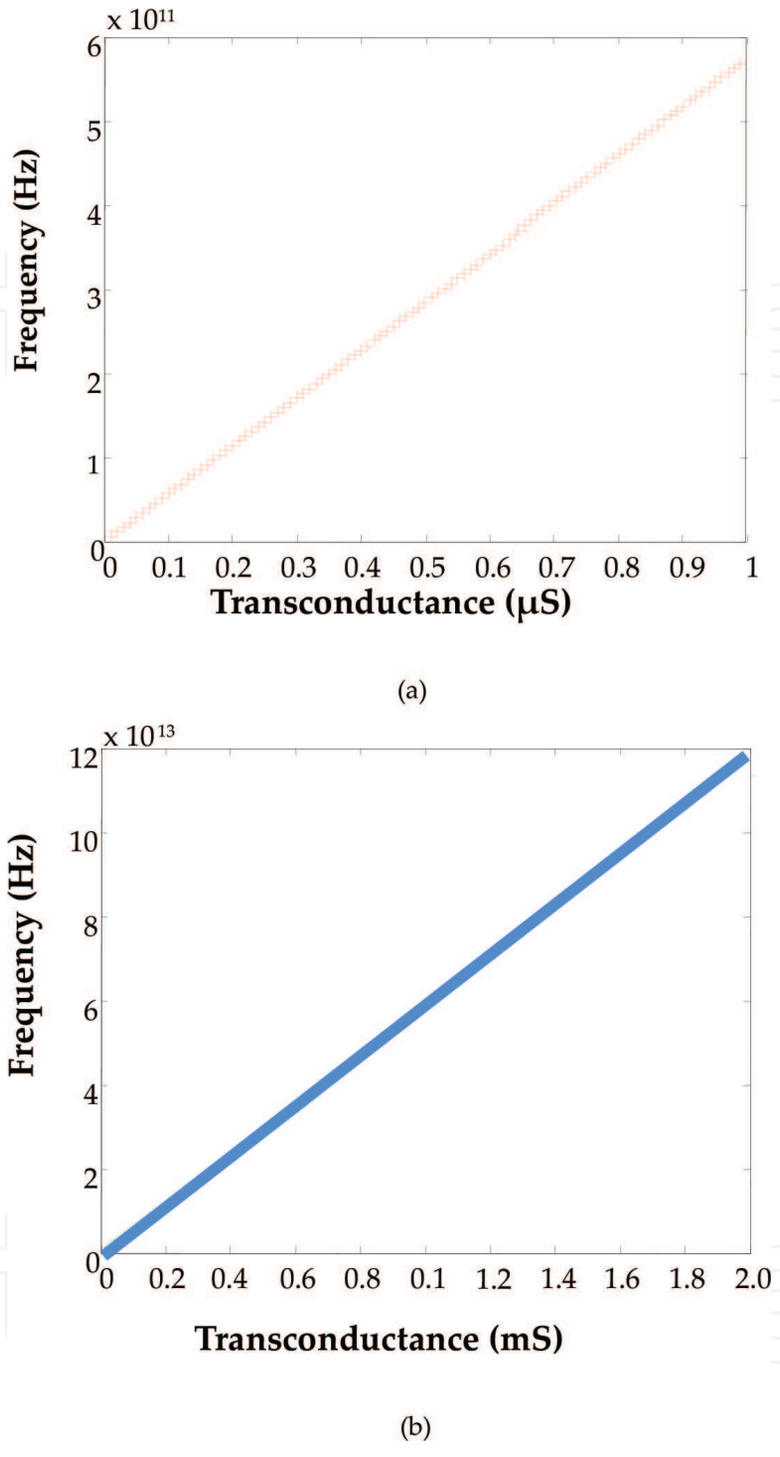

Figure 8. Simulation of frequency, fT, versus transconductance, gm: (a) transconductance in μS and (b) transconductance in mS.

4.3. Frequency response of CNTFET

The current gain of the proposed CNTFET is shown in **Figure 10**. Current gain magnitude is found in 45 dB while the frequency is operated in 10 THz. The value of the CNTFET's

Gm (μS)	F_T (Hz)
19	1.0800×10^{11}
22	1.2505×10^{11}
28	1.5915×10^{11}
32	1.8189×10^{11}
36	2.0463×10^{11}
45	2.5578×10^{11}
50	2.8421×10^{11}
55	3.1263×10^{11}
60	3.4105×10^{11}

Table 1. Frequencies for different current gain of small signal model while transconductance in μS.

Gm (mS)	F_T (Hz)
1.0	5.68×10^{12}
1.1	6.25×10^{12}
1.2	6.82×10^{12}
1.3	7.39×10^{12}
1.5	8.52×10^{12}
1.6	9.00×10^{12}
1.7	9.66×10^{12}
1.8	10.00×10^{12}

Table 2. Frequencies for different current gain of small signal model while transconductance in mS.

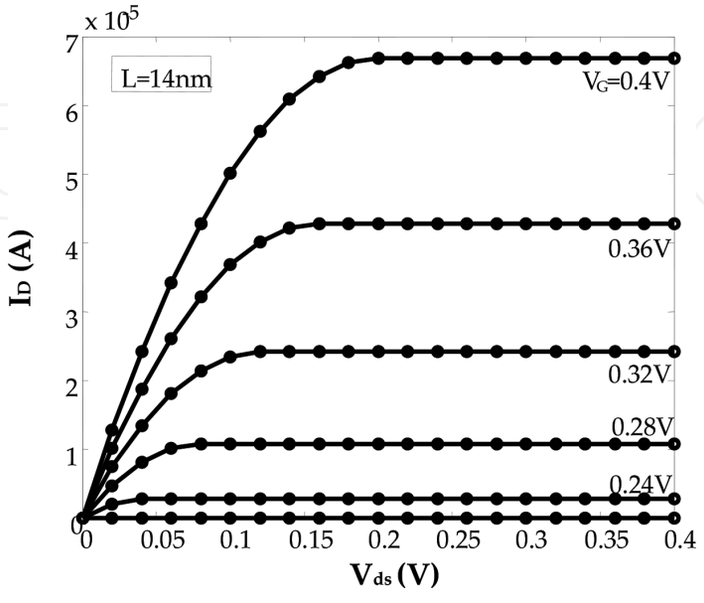

Figure 9. I-V transfer characteristics of CNTFET.

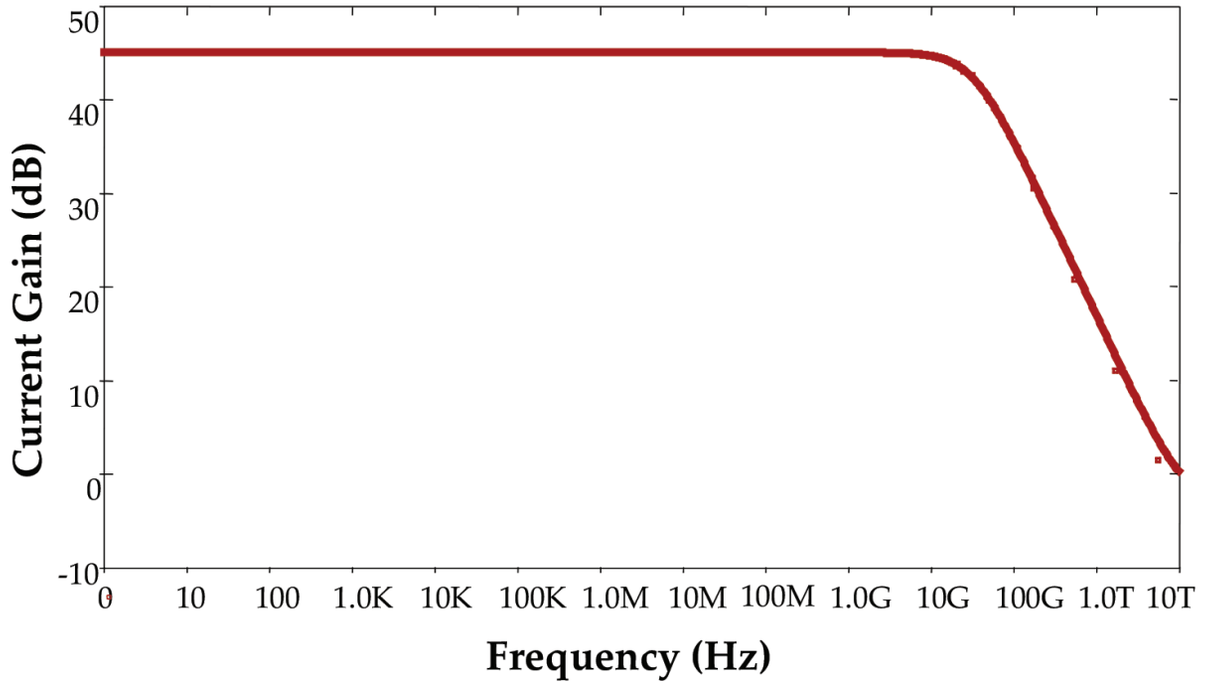

Figure 10. Output current gain of the CNTFET at 10-THz frequency.

Device Parameters	CNTFET [25]	This Research
Current gain (db)	20	45
g_m (mS)	3.8	1.8
C_{gs} (F)	65f	14a
C_{gd} (F)	52f	14a
Cut-off-Freq (Hz)	30G	10T

Table 3. Comparison of current research.

transconductance gm is set as 1.8 mS from the analysis as shown in **Figure 10** at the gate voltage of 0.4 V [24].

To validate the output characteristics of the current development of proposed CNTFET, we compare the work with other researches. **Table 3** shows the comparison of the performance of the proposed model. From this performance comparison, we would like to conclude that the proposed CNTFET model is capable of operating in high frequency.

5. Conclusion

This chapter discussed the development of the CNTFET model using 14-nm technology. We delineated a short examination of the proposed plan of CNTFET little banner show. The arrangement contains a suitable blueprint of the little banner procedure and demonstrated the displays by re-enacting little banner parameters for CNTFET with respect to that of 45 dB.

The inherent capacitance of 14 aF and transconductance of 1.8 mS are used as a piece of this examination. A benchmark is showed up for the immense execution of the exhibit made by differentiating and late research data. Particular characteristics are showed up by a course of action of multiplication. Besides, this system has familiar capacitance with survey, the charge defending capacitance at the repeat of 10 THz.

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Conflict of interest

There is no conflict of interest with this publication.

Author details

Soheli Farhana

Address all correspondence to: soheli.farhana@live.iium.edu.my

International Islamic University Malaysia, Kuala Lumpur, Malaysia

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