Chapter 6

High-Speed Electronic Memories and Memory Subsystems

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Additional information is available at the end of the chapter

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Abstract

Memories have played a vital role in embedded system architectures over the years. A need for high-speed memory to be embedded with state-of-the-art embedded system to improve its performance is essential. This chapter focuses on the development of high-speed memories. The traditional static random access memory (SRAM) is first analyzed with its different variant in terms of static noise margin (SNM); these cells occupy a larger area as compared to dynamic random access memory (DRAM) cell, and hence, a comprehensive analysis of DRAM cell is then carried out in terms of power consumption, read and write access time, and retention time. A faster new design of P-3T1D DRAM cell is proposed which has about 50% faster reading time as compared to the traditional three-transistor DRAM cell. A complete layout of the structure is drawn along with its implementation in a practical 16-bit memory subsystem.

Keywords: SRAM, DRAM, memory subsystem, P-3TD, static noise margin

1. Introduction

In today's modern evolving electronics, manufacturing semiconductor memory technology is an essential element. Normally, based on semiconductor technology, memories, which are being used in any equipment, use processor in one form or the other. Processors have recently become much popular with an increasing number of multiprocessor system being fabricated on a single chip to increase the performance of a system. In order to support this system, memory technology needs to be escalated to compete with processor technology. An additional driver has been endowed with the fact that the software associated with the processors and computers has become more sophisticated and much larger, and this too has greatly

increased the necessity for semiconductor memory. In view of the pressure on memory, new and upgraded semiconductor memory technologies were being researched, and development could have been very expeditious. The mature semiconductor memory technologies are still extensively used and would form the paradigms of manufacturing for years to come.

The requirement for semiconductor memories with rapid advancement in technologies has been an overabundance of technologies and types of memories that have emanated viz. ROM, RAM, EPROM, EEPROM, Flash memory, static random access memory (SRAM) [1, 2], dynamic random access memory (DRAM) [3, 4], synchronous dynamic random access memory (SDRAM), and the very new magnetoresistive random access memory (MRAM) that could now be seen in the electronics literature. Each one has its own merits and areas in which it may be used. In addition to these new applications such as digital cameras, PDAs and many more applications have given rise to the exigency of memories. This chapter discusses the advancement made in the field of SRAM and DRAM memory cells while proposing a new architecture of a faster DRAM cell.

2. Static random access memory (SRAM)

In high-performance integrated circuits, static random access memories (SRAMs) have been used as on-chip memories, due to its intense access speed and compatibility with process and supply voltage. Due to aggressive complementary metal oxide semiconductor (CMOS) technology scaling, the demand for a high-performance technology has increased the amount of on-chip memory integrated into modern semiconductor devices. Recently, there has been a rapid increase in the total area occupied by these memories. The continued scaling of CMOS technology has also resulted in problems which were less severe in earlier generations. These include process-induced variations, soft errors, transistor degradation mechanism, and so on. SRAM dominates the memory hierarchy in performance, but due to area limitations and high cost per bit, they are often integrated in lesser capacity. Furthermore, as the technology scales deepen into nanometer levels, there is a reduction of the stability of SRAM to noise and radiation is reduced. It is becoming increasingly challenging to maintain an acceptable static noise margin (SNM) of SRAMs while scaling the minimum feature sizes and supply voltages. Static noise margin (SNM) degradation, which characterizes the data integrity of SRAM during a read operation, has driven the development of SRAM cell design into a new direction as the supply voltage reaches near the threshold voltage. However, the shrinking of the transistor dimensions has also increased the probability of radiation-induced errors. This chapter has the following outline. We discuss the background information on different SRAM cells and describe the SRAM stability concept along with equations. In this section, we present our simulations and discuss the results [5].

2.1. Different types of SRAM cells

2.1.1. SRAM 6T cell

The conventional SRAM cell consists of two cross-coupled CMOS inverters with two access transistors connected to supportive bit lines. **Figure 1** shows the circuit diagram of a SRAM 6T cell. During read operation, pre-charge the bit lines (BL), BLB (bit line bar) to VDD. Turn on

WL (word line). BL or BLB will pull down to low depending on storage node QD and QB. For write operation, drive bit line (BL) and bit line bar (BLB) with necessary values (0.1 or 1.0) [6]. Turn on word line, bit lines (BL or BLB overpower cell with a new value).

2.1.2. SRAM 11T cell

An SRAM 11T cell is shown in **Figure 2**. The circuit enumerates a circuit which exists as two cross-coupled inverters along with an access transistor which is controlled by the read word line (RWL) for read operation and two more access transistors which are controlled by the write word line (WWL) for write operation [3]. **Figure 2** depicts the circuit diagram of an SRAM 11T cell.

2.1.3. SRAM 8T cell

In SRAM 8T cell, two voltage sources S1 and S2 are used, one connected to the output of the bit line and the other with the bit bar line. Two NMOS transistors are connected with inputs of bit line and bit bar line, respectively, straight to switch ON and OFF the power source supply during write 0 write 1 operations. The SRAM 8T cell is shown in **Figure 3**. These power supply sources diminish the voltage swing at the output node when write operation is being performed [7]. **Figure 3** shows the circuit diagram of SRAM 8T cell.

2.2. Static noise margin

The stability of an SRAM cell is critically functional in nanometer technologies as it determines the ability to retain stored information. The static noise margin (SNM) is a measure

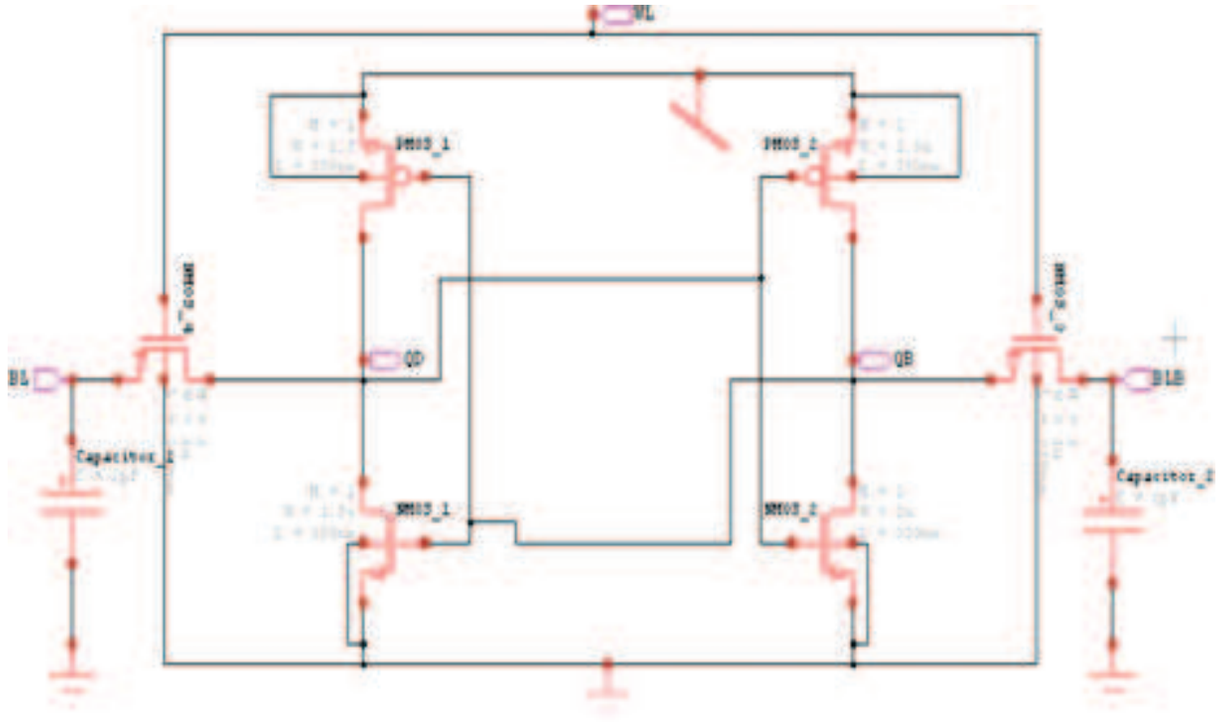

Figure 1. SRAM 6T cell.

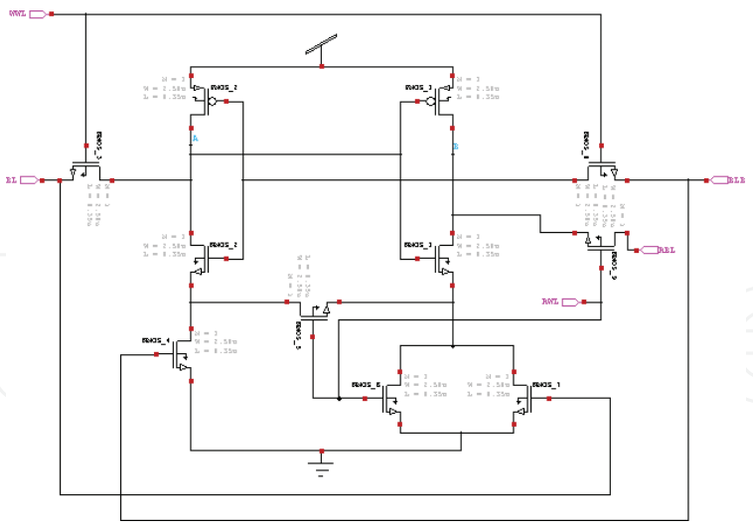

Figure 2. SRAM 11T cell.

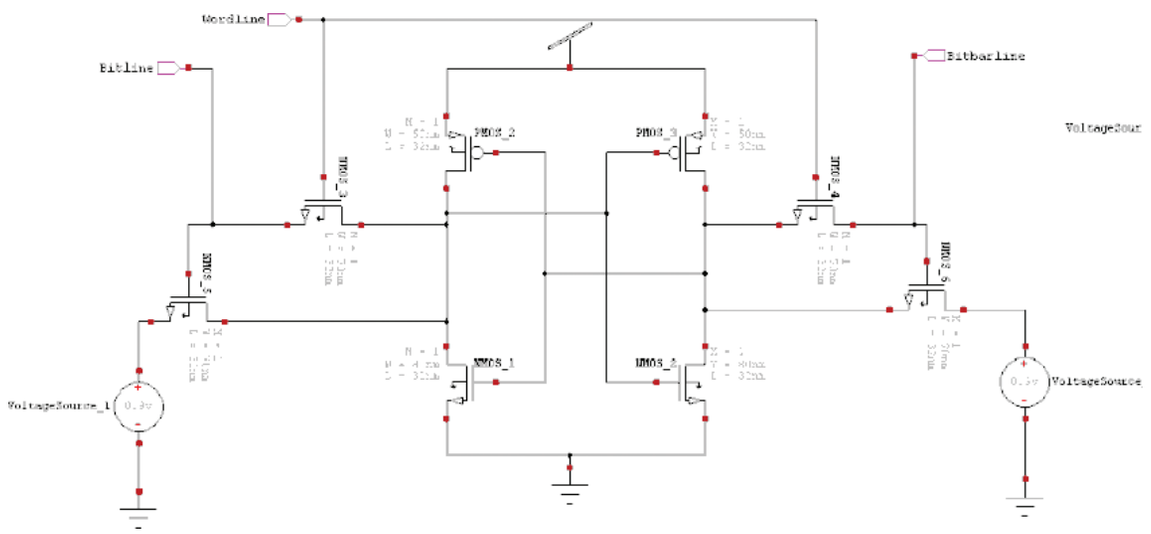

Figure 3. SRAM 8T cell.

of the SRAM stability; it is defined as the maximum static noise voltage that could be tolerated by the SRAM stability and without the loss of stored information. In other words, SNM quantifies the amount of noise voltage V_n required to flip the cell data during a read access or a standby mode. **Figure 4** shows an SRAM cell presented as two equivalent inverters with the noise voltage inserted between the corresponding inputs and outputs. Both series voltage noise sources have the same value and act in a synchronized way to upset the state of the cell.

The SNM of an SRAM cell can be represented graphically using the superimposed voltage transfer characteristics (VTC) of the inverters as shown in **Figure 5**. The resulting two-lobed curves are generally referred to as the "butterfly curve." The SNM is now defined as the length of the side of the largest embedded square inside the butterfly plot. In an ideal SRAM cell, the VTC of both inverts would be symmetrical. However, due to process variations, change in

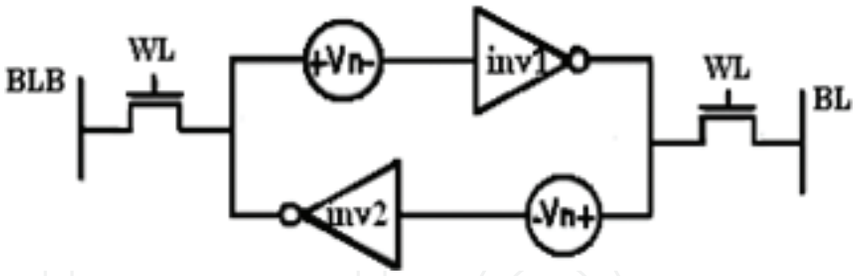

Figure 4. SRAM cell with a noise source.

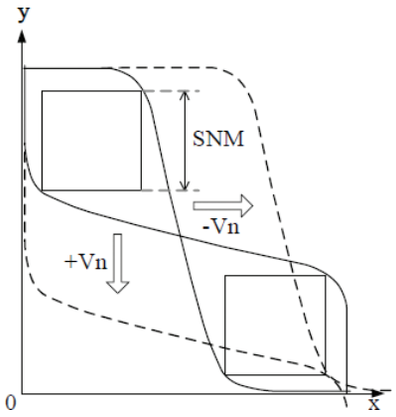

Figure 5. Static noise margin.

Cell ratio (CR)	SNM 6T SRAM (mV)	SNM 11T SRAM (mV)	SNM 8T SRAM (mV)
1	136.84	328.7	336.4
1.4	141.4	343.2	391.2
1.8	150.53	348.5	411.5
2.0	159.65	354.6	429.6

Table 1. SRAM variation with CR.

transistor attributes could result in cell imbalance. If the inverters of cell are not identical, one lobe is smaller than the other. Then, the SNM of the cell is the length of the side of the largest square that fits inside the smaller of the two lobes [8].

2.3. Measurement results

Table 1 presents the SNM variation of different SRAM cells with the cell ratio (CR) during the read operation. It can be seen that as the CR of the SRAM cell increases, the SNM also increases. Cell ratio: the ratio of driver transistor to access transistor is an important cell parameter called the cell ratio.

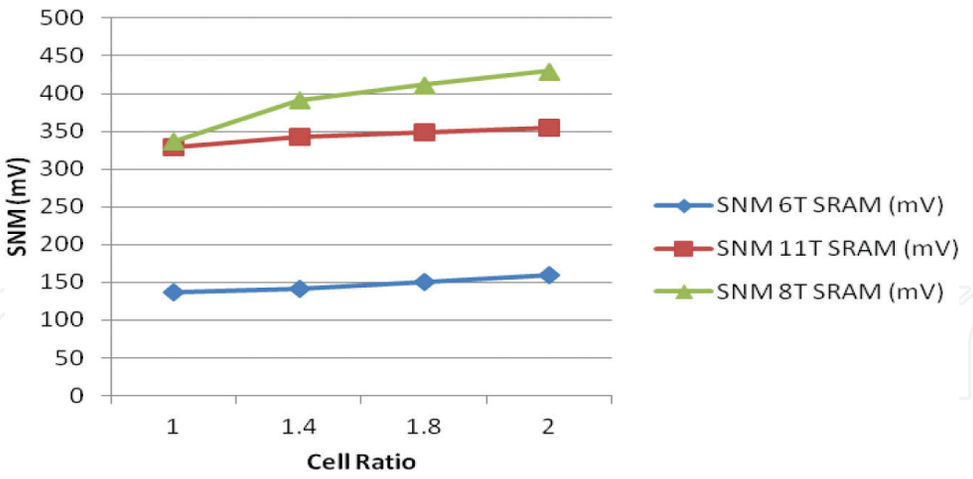

Figure 6. Cell ratio versus static noise margin.

In **Figure 6**, the SNM variation of different SRAM cells with cell ratio is shown. It can be concluded from the graph that the noise tolerance of 8T SRAM cell is more than the other two cells [9].

3. Dynamic random access memory (DRAM)

Economical and faster dynamic random access memories (DRAMs) have been widely used in all kinds of electronic devices. DRAMs have found extensive application; their mass production embarks the maturity of a semiconductor technology, which is continuously driven to give smaller dimension devices. A new semiconductor technology era having a relatively higher yield has led to the mass production of novel DRAM-generation structures. DRAM refers to a volatile memory, that is, data stored have to be dynamically refreshed to generate a correct memory data value. DRAM bits are randomly accessible compared to a conventional tape recorder. Read and write operations are necessary for DRAM cells. For reading a DRAM cell, row addresses are sent to row decoders in order to select the cell to be read by activating the necessary word line driver. When one of the word line drivers is high, the turned-on DRAM cell capacitance will charge the bit line capacitance, forming a voltage in the range of 100–200 mV [10].

In order to amplify the bit line voltage value and recover the stored data, sense amplifier is used. One sense amplifier is connected to multiple cells; hence a large amount of data is available at the same time, and large data are divided into pages, which can be accessed simultaneously. To indicate the completion of reading process, word line is turned on to isolate the DRAM cell from the bit lines. A write operation follows the similar process, with a global bit line giving the row address to the decoder and local bit lines of the cell are activated. With the help of sense amplifiers, VDD or "0" are written into the cell. A refresh operation is required to compensate for the leakage current and to refurbish the storage cell value of the cell as it elapses gradually with time. For refresh process, column access is not required as compared to the read process. First-stage sense amplifiers easily refresh the memory cells [12].

The number of data bits per unit area is the area efficiency of a memory array. It is one of the essential parameters of a memory cell along with access times. These parameters determine the overall storage capacity and memory cost per bit. Access time is essential in determining

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the time required to store and/or retrieve data from the memory array. Access time helps in the determination of the speed of the memory array cell structure. Power consumption both static and dynamic is also a significant factor of the design. In this section, we would instigate various types of DRAM cells with speed and power consumption comparison being carried out between the designs. A new DRAM cell design has been described which considerably improves the speed of DRAM. The improvement in data rate consists of improvement in read access time, write access time, and retention time. These improvements will help in gaining a DRAM cell design that will be capable of giving a high performance in terms of delay and power consumptions [11, 12].

3.1. Different DRAM cells

Different DRAM cell designs based on their power and retention time are analyzed. Different DRAM cell designs are as follows:

1. 1T1C DRAM CELL
2. 3T DRAM CELL
3. 4T DRAM CELL
4. 3T1D DRAM CELL

These DRAM structures differ in the form of a number of transistors, area occupied. All these different designs have different structures and properties. The first three DRAM architectures use parasitic capacitance to store data values while the last one utilizes gated diodes to store the values. These gated diodes are generally formed from N-type metal oxide semiconductor field-effect transistor (MOSFET), but in order to reduce the power dissipation, P-type MOSFET can be utilized in their place. The advantage of this modification has been shown in comparing the various DRAM structures based on power consumption (during full cycle operation of write "0," read "0," write "1" and read "1"), write access time, read access time, and retention time (refresh time) (**Figure 7**).

3.2. Performance comparison

A new cell structure with a P-type MOSFET as a gated diode working as a capacitor has been compared on the basis of data rate and power consumption with the already existing DRAM cell structures. This gated diode cell structure is much faster than the already existing cell structures. All the cell structures are compared in an identical environment with their simulation profile as described in **Table 2**. Write and read operations are carried out on these cell structures, and their performances have been compared in **Table 3**. **Figure 8** shows the operation read-write waveform [14, 15].

3.2.1. Analysis of DRAM designs

Power consumption and access times decrease the P-3T1D DRAM cell, hence making it a faster and a low power cell as compared to the other variations. While the retention time also tends to decrease slightly, this means the memory has to be refreshed after a slightly smaller duration [11].

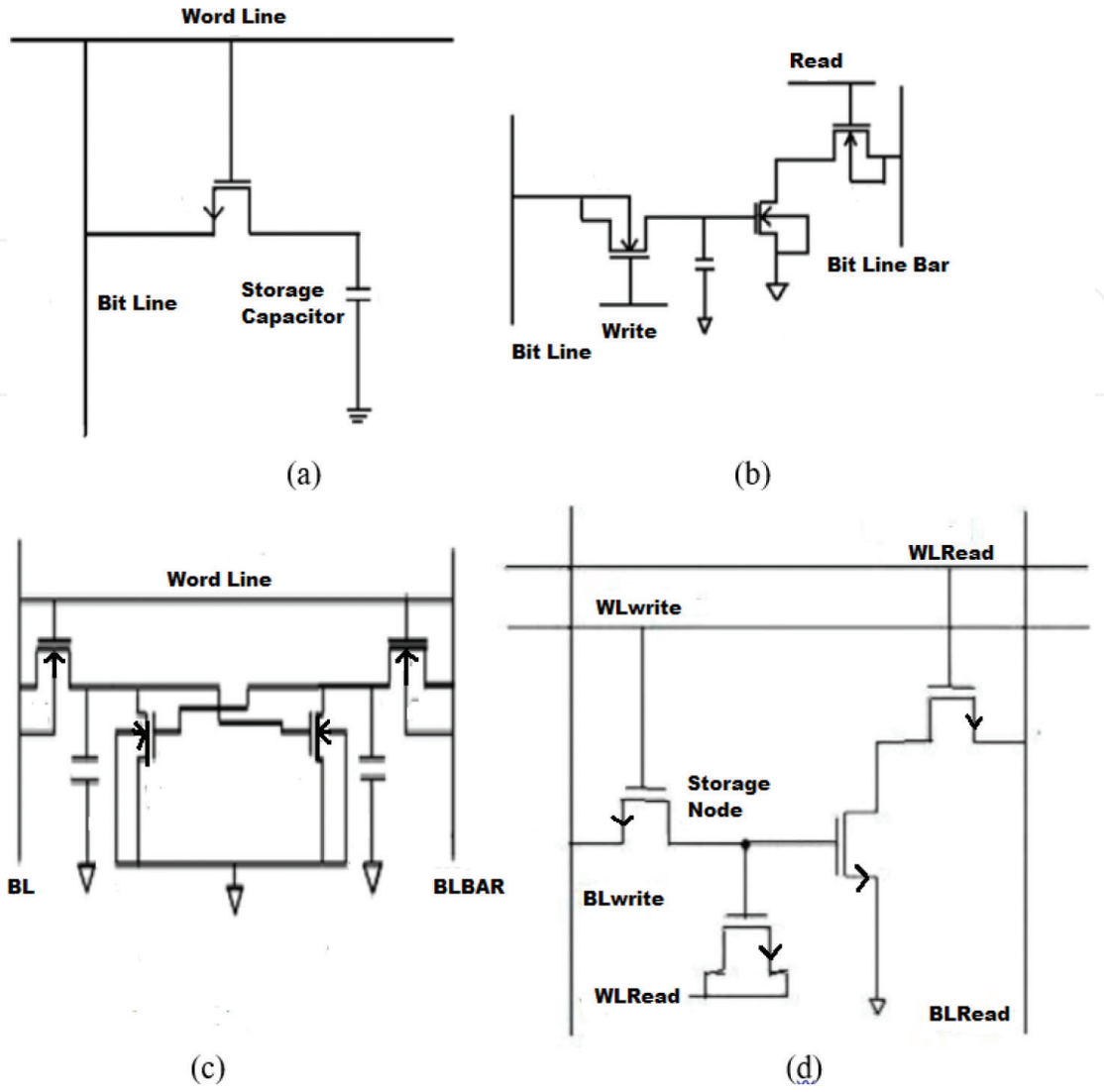

Figure 7. (a) 1T1C DRAM cell, (b) 3T DRAM cell, (c) 4T DRAM cell, and (d) 3T1D DRAM cell [13].

Operation	Time period (ns)
WRITE "1"	2–3
READ "1"	4–5
WRITE "0"	6–7
READ "0"	8–9

Table 2. Working operation of cells.

Power consumption for the proposed cell is less than the existing cells. However, the write access time is quite comparable to gated diode type DRAM cell. Read access time is almost 50% less than traditional 3T and 4T DRAM cells and approximately 34% less than N-3T1D DRAM cell. One of the most important parameters for DRAM cell is the retention time

Parameter	4T DRAM	3T DRAM	N-3T1D DRAM	P-3T1D DRAM
Average power consumption (μW)	2.384711	2.262632	2.170092	2.149554
Write access time (ps)	37.45	20.89	385.45	312.69
Read access time (ps)	71.19	70.7	68.65	44.89
Retention time (μs)	2.45621	3.49827	40.07223	33.716

Table 3. Parameter comparison for DRAM cell simulation results.

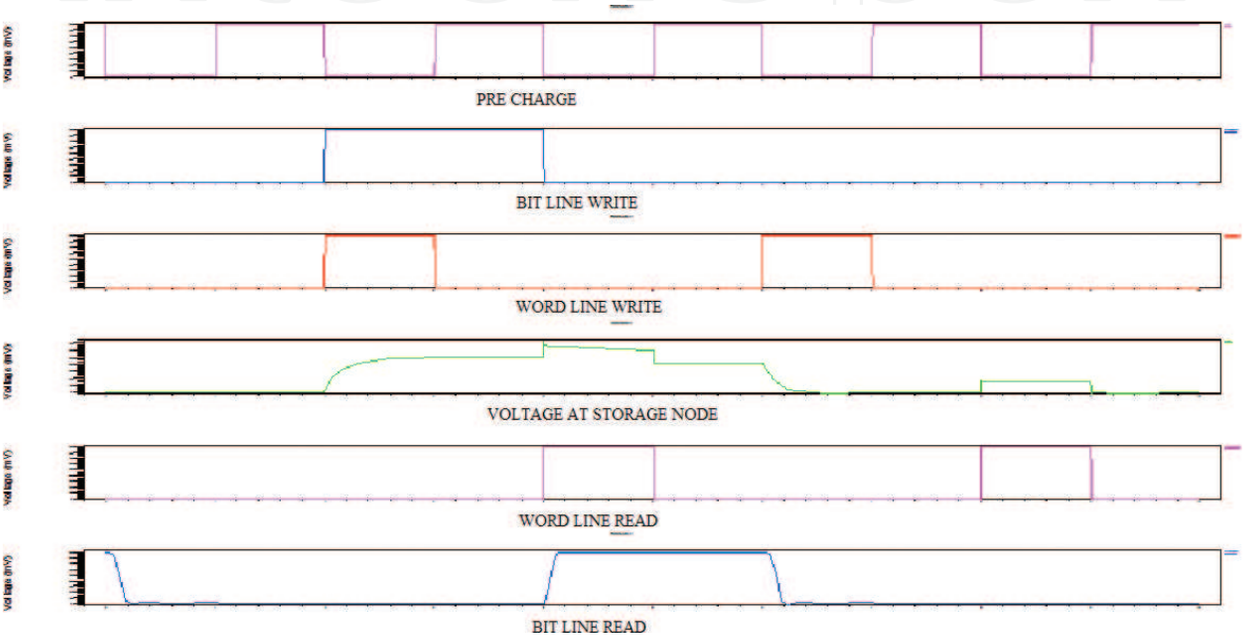

Figure 8. Read-write waveform.

or the time after which the cell needs to be refreshed while the traditional cell has a very small retention time; it is quite comparable with the already existing gated diode-based DRAM cell.

3.3. Layout for P-3T1D DRAM cell

The layout of P-3T1D cell is drawn on a 250-nm technology occupying an area of 1139.29 μm^2. The layout is drawn on LEDIT and it perfectly resembles the circuit implementation as being verified by layout versus schematic verification (**Figure 9**).

3.4. Full 16-bit memory subsystem using P-3T1D DRAM cell

A full memory is being implemented using the P-3T1D DRAM cell. The memory consists of a writing decoder, a reading decoder, 16 instances of P-3T1D DRAM cell, and four instances of output cell-reading circuitry. This output cell-reading circuitry consists of a precharge circuitry and a gated diode sense amplifier (**Figure 10**).

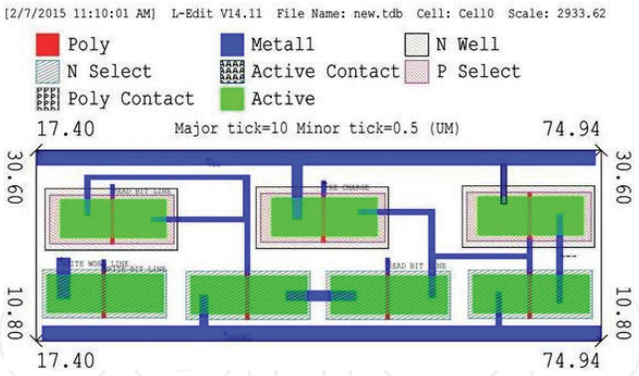

Figure 9. P-3T1D layout on 250 nm.

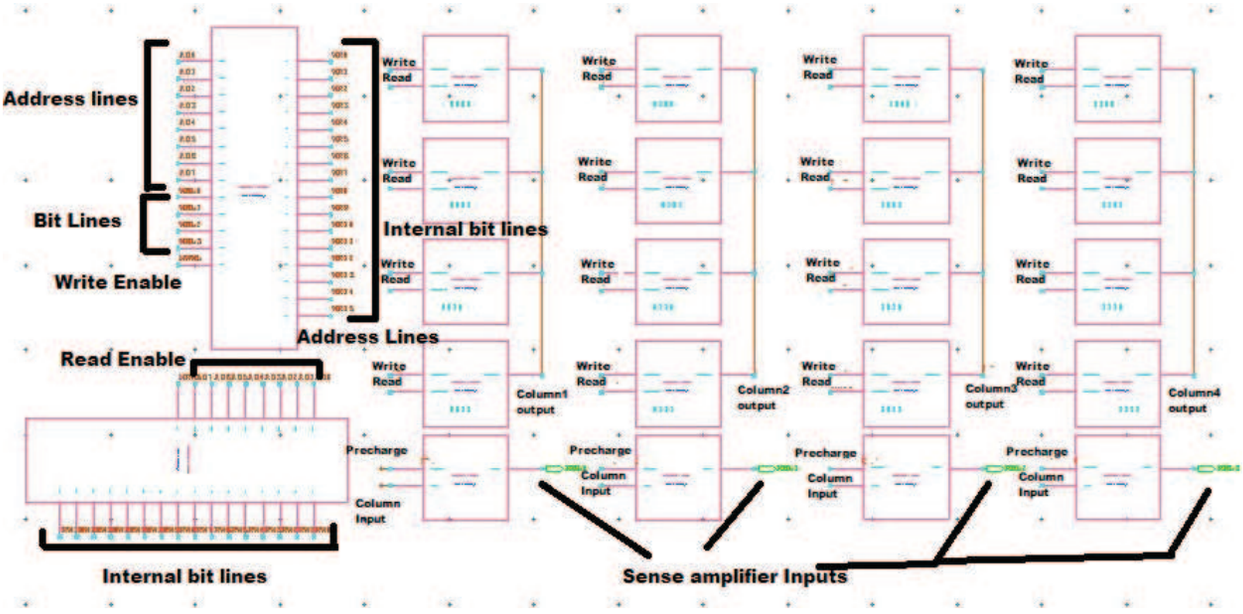

Figure 10. 16-bit memory using P-3T1D.

There are eight address lines AD0–AD7. AD0 and AD1 are used to select a bit cell from Column 1. AD2 and AD3 are used to select a bit cell from Column 2. AD4 and AD5 are used to select a bit cell from Column 3. AD6 and AD7 are used to select a bit cell from Column 4. WBL0, WBL1, WBL2, and WBL3 are 4-bit write data lines that are used in this memory cell subsystem design (**Figure 11**). RBL0, RBL1, RBL2, and RBL3 are 4-bit read data lines that are used in this memory cell subsystem design (**Figure 12**). RWL is used to control read operation turned 1 to read. WWL is used to control write operation turned 1 to write. The time for execution of the circuit is 0–50 ns. In these data 1, 0, 1, and 0 is written into CELL0, CELL 5, CELL 10, and CELL 15, respectively.

For the time period 0–10 ns, reading and writing are both turned off and PRECHARGE is at one.

For the time period 10–20 ns, PRECHARGE is low, writing is turned on, reading is off, and address line selected the cells. Using the writing decoder and address lines, data from write bit line are written onto the CELLS 0, 5, 10, and 15.

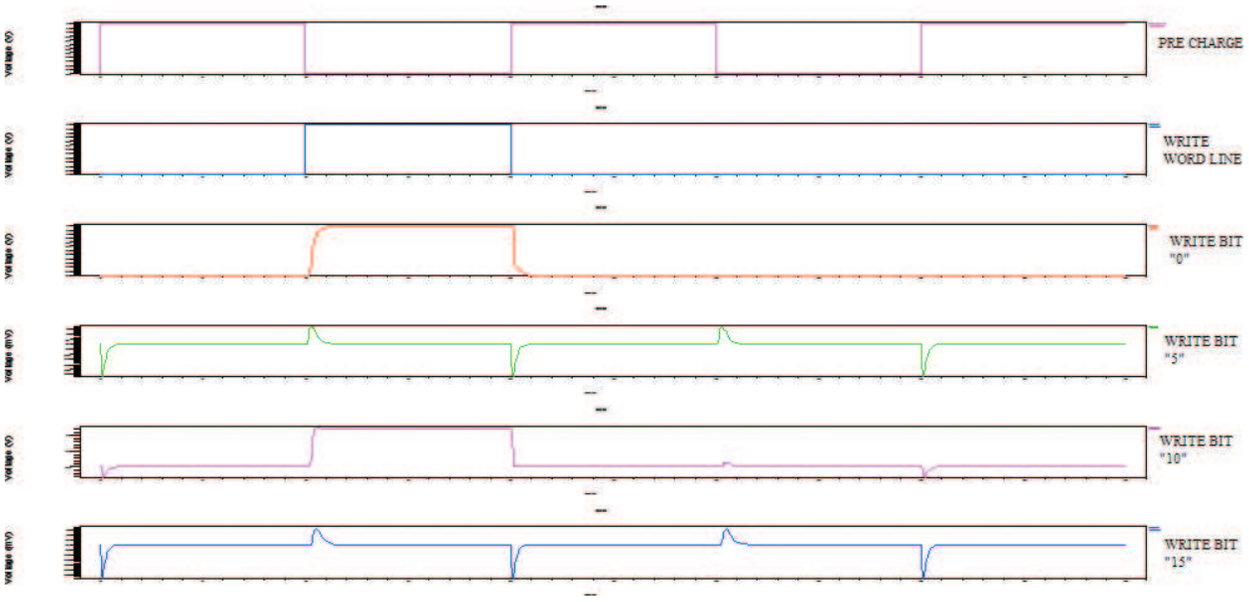

Figure 11. Writing waveform.

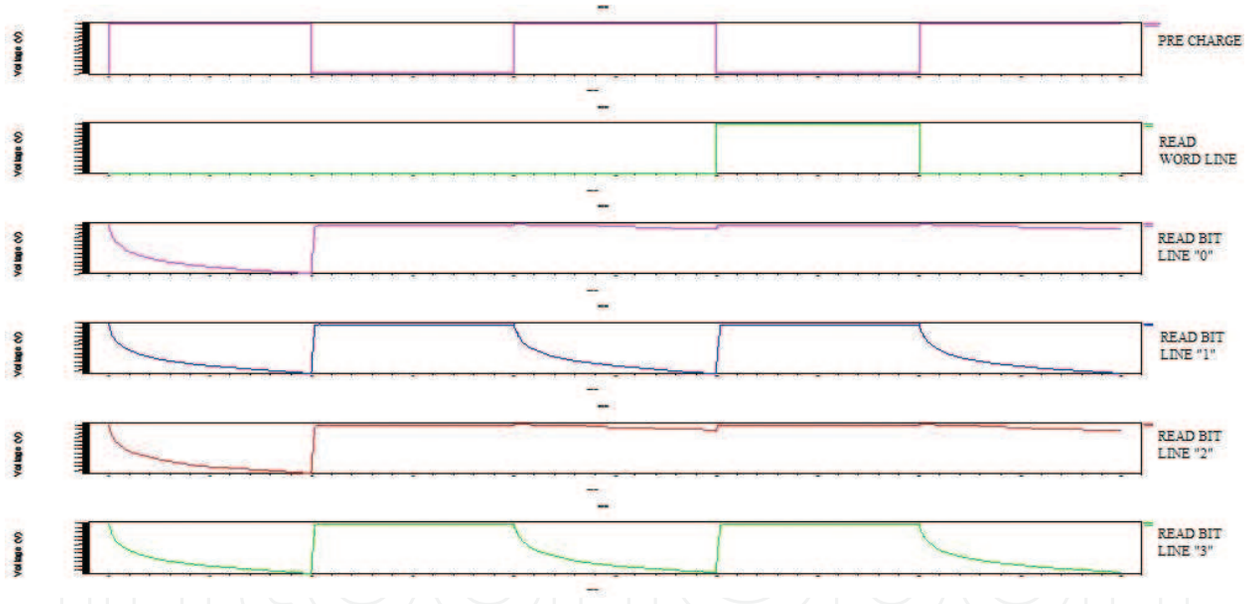

Figure 12. Reading waveform.

For the time period 20–30 ns, PRECHARGE is high, reading and writing both turned off, and data are stored in the cell.

For the time period 30–40 ns, PRECHARGE is low, writing is turned off. Reading is on as READ WORD LINE is turned on. Address line selects the cells. Using the reading decoder and address lines, data are read from the CELLS 0, 5, 10, and 15 and transferred to the output circuitry of the required column.

For the time period 40–50 ns, PRECHARGE is high after performing sensing and amplification of the required data. Data are read from READ BIT LINES 0, 1, 2, and 3 together (**Figure 13**).

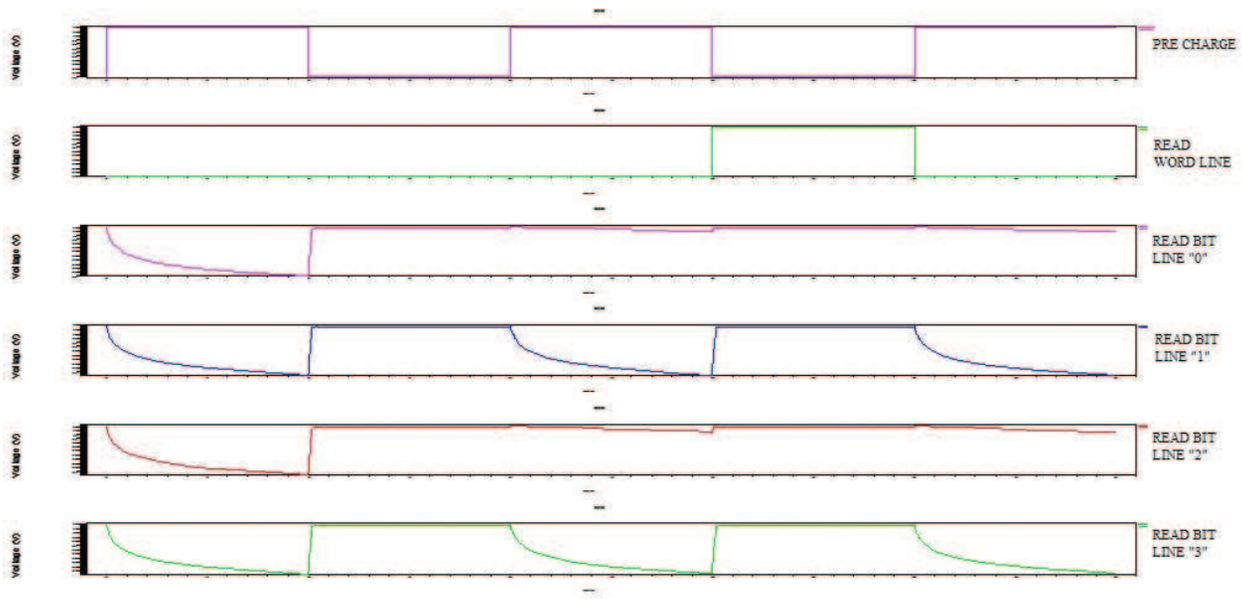

Figure 13. Final read output.

4. Conclusions

A memory architecture has been proposed in this chapter. From the analysis of static noise margin (SNM) for SRAM cell, it could be concluded that the SRAM 8T cell has a higher SNM than the SRAM 6T and SRAM 11T, that is, SRAM 8T cell has a greater noise tolerance. The only drawback of the SRAM 8T and SRAM 11T is the area overhead over the SRAM 6T cell. In order to reduce this area overhead, DRAM-based memory systems are being used. Different types of DRAM cell structures have been used in the study. A novel structure using P-type-gated diode-based capacitor has been utilized in this work. The average power consumption for the structure is lower than those being implemented in the study. A significant reduction in both write and read access time has been achieved when the structure is compared with a similar structure. Area layout for the structure shows the reduction in the area overhead compared to the other implemented designs. A full memory subsystem implementation depicts the working of the architecture in practical working environment, achieving greater results. The memory subsystem implemented could successfully store 16 bits of data and the saved data could also be read effectively.

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