Chapter 7

Optimization of the Phase Change Random Access Memory Employing Phase Change Materials

Daolin Cai, Zhitang Song and Yifeng Chen

Additional information is available at the end of the chapter

http://dx.doi.org/10.5772/intechopen.74786

Abstract

Phase-change random access memory (PCRAM) is a semiconductor device based on phase change material (PCM). The SET speed is the bottleneck of limiting the speed of PCRAM. Extract the electrical parameters of the SET operation of the PCRAM test chip and analyze the process of the SET operations. It is found that adding a high and narrow pulse before a single pulse (SP) benefits the SET resistance reduction and the SET speed improvement. A dual pulses SET (D-SET) method is proposed and optimized. The mechanism of D-SET is that the first pulse forms a large optimum temperature field cover over all regions of the PCM material. When the first pulse is converted to the second pulse, the optimum temperature field shrinks and causes the amorphous regions to rapidly crystallize from the edge to the center. On the 40 nm PCRAM test chip, the SET time of D-SET method is under 300 ns. Compared with the conventional SET method such as SP and staircase down pulses (SCD), the D-SET method is optimal for SET performance such as SET resistance distribution, SET speed, and the anti-drift ability.

Keywords: PCRAM, phase change material (PCM), SET operation, resistance distribution, anti-drift

1. Introduction

Phase-change random access memory (PCRAM) is widely investigated as one of the most promising candidates for nonvolatile memory [1]. The storage cell in PCRAM is based on a phase change material (PCM). Interest in PCRAM technology was renewed by the discovery of fast recrystallizing materials, GeTe [2], $Ge_{11}Te_{60}Sn_4Au_{25}$ [3], $Ti_{0.4}Sb_2Te_3$ [4], and $Cr_{0.2}Sb_2Te_3$ [5]. A pseudo-binary alloys along the GeTe-Sb_2Te_3 tie line, such as $Ge_1Sb_2Te_4$, $Ge_1Sb_4Te_{7,}$ and the most commonly applied material for both optical and electrical applications, $Ge_2Sb_2Te_5$ (GST) [6].

Employing PCM, in 2006, 512 MB PCRAM chip was reported. Intel and Micron recently announced a new 128 GB "3D XPoint memory" technology [7]. High speed, high density, low voltage, and compatibility with standard CMOS technology performance ensure PCRAM superiority [8–10]. The storage cell is constituted by a thin-film PCM layer in contact with a metallic heater. When a programming voltage or current is applied to the storage cell, a high current density will flow into the resistive heater, raising the temperature by Joule effect. PCM in the active region close to the heater heats up, thus causing the phase transition between the RESET and SET states. The PCM can be changed from low resistive (crystalline) to high resistive (amorphous) state, named as RESET operation; vice versa, from high resistive (amorphous) to low resistive (crystalline) state named as SET operation.

Conventionally, SET program operation is achieved by means of a single pulse (SP) of a couple of hundreds of nanoseconds. The resulting SET-state cell resistance distribution (hereafter referred to as SET distribution) typically turns out to be affected by spreads in cell physical parameters, which can degrade the SET distribution width. This leads to a reduced spacing between the SET and the RESET distribution and, hence, to a decreased safe margin for read operations. Compared with the RESET speed of PCRAM, the SET speed of PCRAM is much slower; so the SET speed is the bottleneck of limiting the speed of PCRAM. This chapter focuses on the SET operation optimization of PCRAM, mainly research on the influence of the relevant factors of SET operation pulse on SET operation and how to optimize the SET operation pulse. The SET operation speed is improved by optimizing the SET operation pulse. The mechanism of the SET process is analyzed, and the improved SET operation pulse is proposed and implemented. It is mainly divided into three aspects as follows: (1) the influence of the magnitude and width of the SET pulse on PCRAM; (2) study on the dual pulse SET (D-SET) operation; (3) comparison of D-SET with the common SET methods.

Many improved SET operation methods are proposed and applied in the PCRAM chip. In 2005, the multiple step-down pulse generator (MSPG) SET technique (**Figure 1(a)**) was applied to the 64 MB PCRAM chip released by Samsung [11]. Because of the influence of the path resistance, different address storage cells require a different SET pulse to full crystallization. In the MSPG technology, the SET current pulse is swept to cover all the cell-to-cell variations of the SET current windows, so the probability of the SET failure can be reduced. Not only can the SET success rate but also the consistency of SET resistance can be improved. **Figure 1(b)** illustrates that the utilization of MSPG to the SET operation reduces the broadness of the right side of SET distribution and widens the margin for reading window.

In 2007, Samsung reported an arbitrary slow-quench (ASQ) pulse scheme to improve the write time of the SET data in a 512 MB PCRAM chip based on 90 nm process [12]. It is composed of a maximum current decision part, a slow-quench slop decision part, a minimum current decision part, and a voltage driver with wide operation range as shown in **Figure 2(a)**. The scheme is used effectively to enhance distributions and reliability of cell data through write-verify process. **Figure 2(b)** shows a measured data of voltage level of SET signal and output of the ASQ, which has a slow quench waveform with 500 ns pulse width.

In addition, STMicroelectronics proposed a technology similar to ASQ technology knows as Set-Sweep Programming (SWP) [13, 14], as shown in **Figure 3**. It consists in applying a conventional RESET pulse to melt the GST but with a very slow-stepped or linear quenching so that, thanks to the slow falling edge, the material has time enough to crystallize and to move into the low resistance state.

http://dx.doi.org/10.5772/intechopen.74786

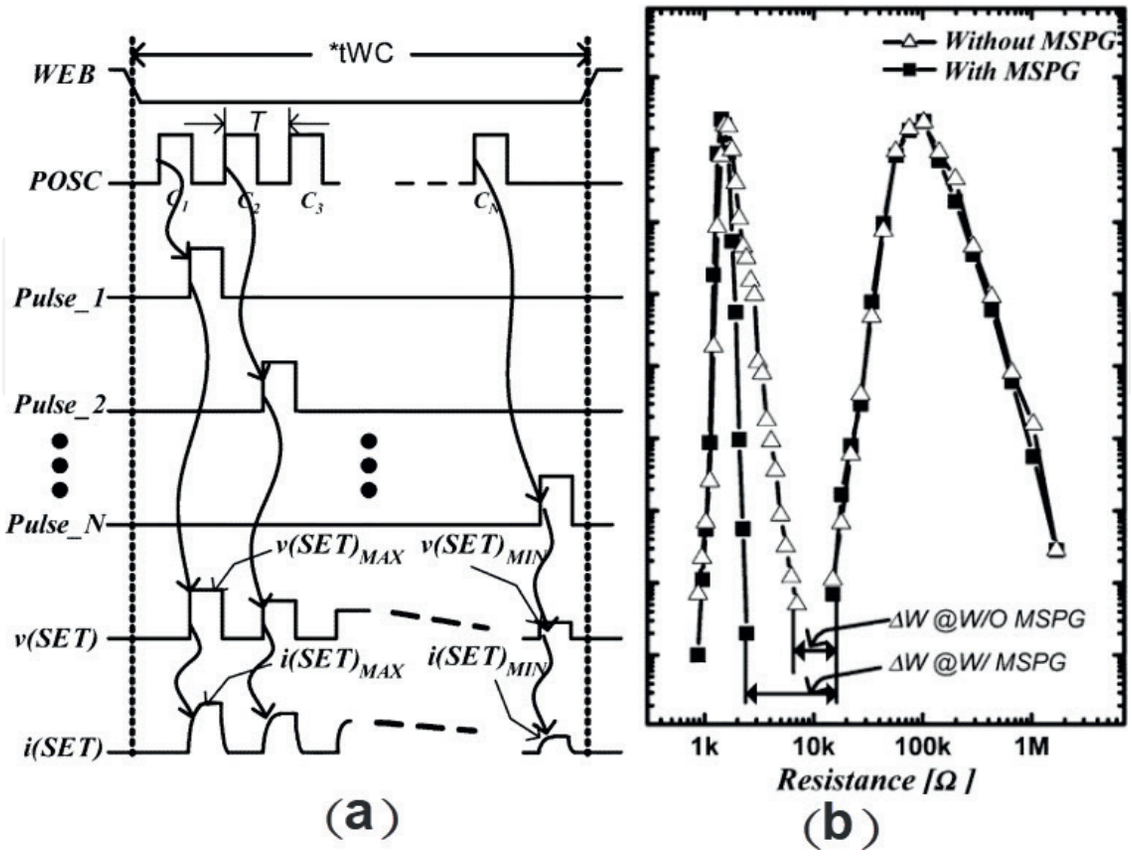

Figure 1. (a) Multiple and step-down pulse generator (MSPG); (b) GST resistance distribution without/with MSPG [11].

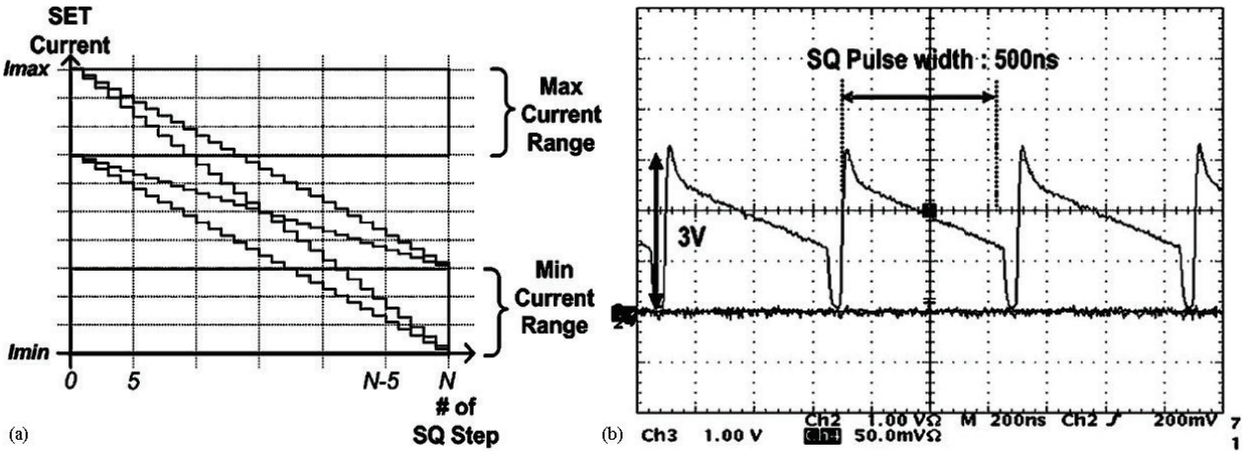

Figure 2. Arbitrary slow-quench shaper. (a) Versatile SQ pulse waveforms. (b) Measured waveform of SET node [12].

A staircase-down (SCD) SET pulse is reported [15], which can be seen as the sequence of N elementary pulses having the same length T_S and decreasing magnitudes S_{N-1}, S_{N-2},…, S_0 (**Figure 4**). This SCD technique allows different optimum SET voltages to be applied to different cells being programmed simultaneously. It can compensate for spreads in cell physical parameters, thus obtaining narrow SET distributions and improved read margin.

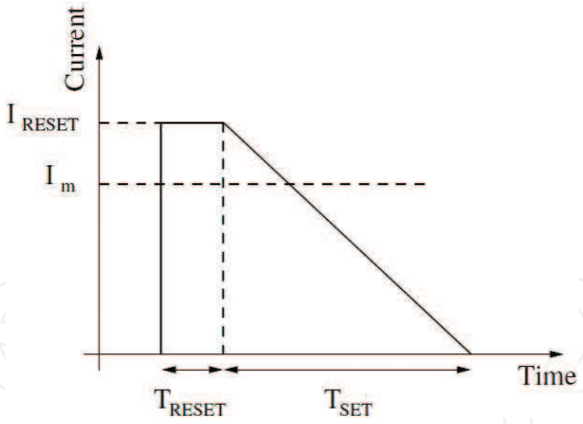

Figure 3. Set program pulse. The constant current level IRESET is higher than the melting current Im in order to melt the chalcogenide before the slow cooling [13].

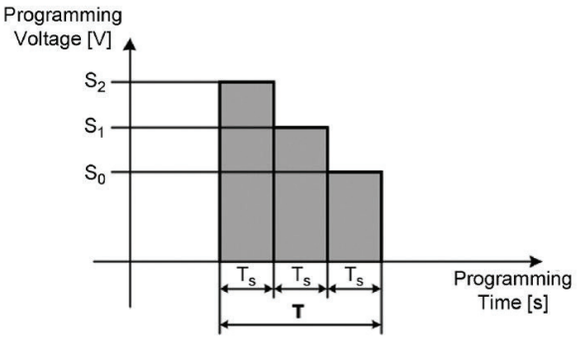

Figure 4. Staircase-down programming pulse (N = 3) [15].

2. SET pulse magnitude and width

2.1. Thermal properties

In order to RESET the PCRAM cell into its amorphous state, a short electrical pulse is applied to the bottom electrode contact (BEC). The thermal pulse is quenched rapidly to cause the molten region to cool to its amorphous state. For the case of SET programming, an electrical pulse is applied to the PCRAM cell that is sufficient to increase the temperature of the programming region above the crystallization temperature (Tcryst) over a time period sufficiently long to crystallize the phase change material. Typically, a material offering high Tcryst generally leads to a better thermal stability and thus longer data retention of stored data. Note that at Tx, crystallization occurs in microseconds. In contrast, at the higher temperature of Tcryst shown in **Figure 5**, sufficient recrystallization of the amorphized portion to create a high conductance path through a memory cell can occur in less than 1 μs. This crystallization temperature Tx can be readily measured on blanket films of PCRAM using electrical techniques. Thus, Tx is widely used to characterize new candidate PCRAM [16].

http://dx.doi.org/10.5772/intechopen.74786

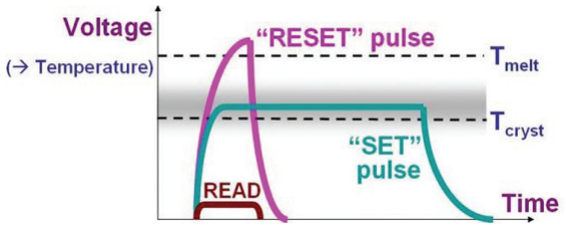

Figure 5. Programming of a PCM device involves application of electrical power through applied voltage, leading to internal temperature changes that either melt and then rapidly quench a volume of amorphous material (RESET), or hold this volume at a slightly lower temperature for sufficient time for recrystallization (SET). The temperature at which recrystallization is very rapid (<1 μs), Tcryst ~ 400°C, is lower than the melting temperature, Tmelt ~ 600–650°C. A low voltage is used to sense the device resistance (READ), so that the device state is not perturbed [16].

2.2. SET pulse magnitude

In order to study the effects of the SET pulse magnitude on the resistance of the PCRAM cell, a fixed width SET pulse is used to SET operation for the RESET state of PCRAM test chip samples. The SET distributions with the different SET pulse magnitudes are shown in **Figure 6(a)**. The cell percent of the SET resistance value less than 100 kΩ (log(resistance) < 5) is listed in **Table 1**.

From the perspective of the SET distribution of array with SET resistance less than 100 kΩ as the standard, it can be seen that 0.3 mA SET current is the optimal SET pulse magnitude. For each cell, its optimal SET current is inconsistent, and its optimal SET current (obtaining the minimum SET resistance) is shown in **Figure 6(b)**. The cell proportion with 0.3 mA SET current operation as the optimal SET current is majority, and the optimal SET current of most cells (98.94%) in the array is between 0.2 and 0.6 mA. It is obvious that the optimal SET conditions are in favor of the array resistance distribution.

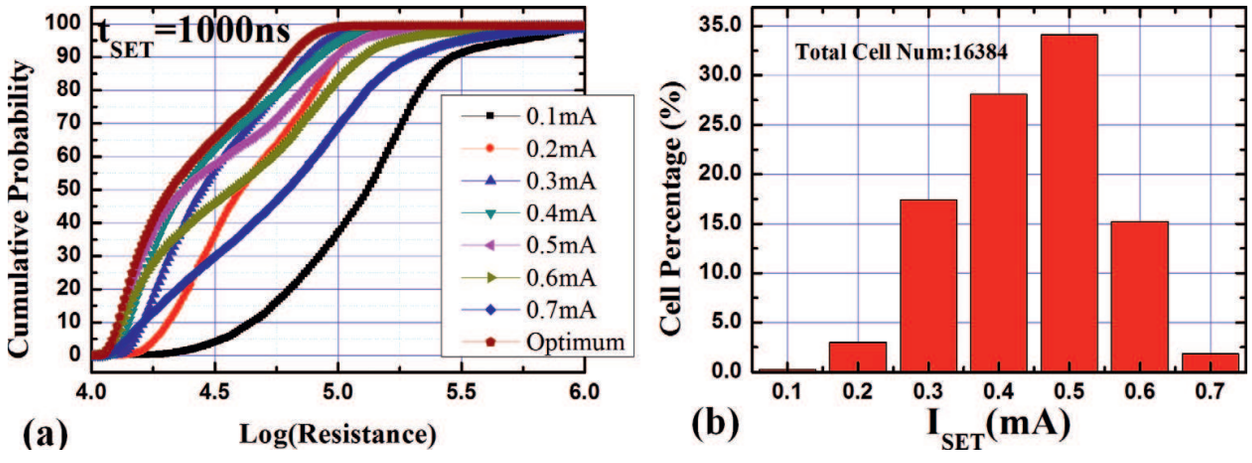

Figure 6. (a) SET distribution with the different SET pulse magnitude; (b) histogram statistics of the cell percent with the different SET current [21].

SET current (mA)	0.1	0.2	0.3	0.4	0.5	0.6	0.7
Cell percent (%)	37.183	90.55	96.58	94.75	91.06	83.41	69.54

Table 1. Cell percent of the SET resistance value (<100 kΩ) with the different SET pulse magnitude.

2.3. SET pulse width

In order to study the effect of the SET pulse width on the resistance of the PCRAM cell, a fixed magnitude SET pulse is used for SET operation from the RESET state of PCRAM test chip samples. 1.5 mA 200 ns RESET current was used to RESET to the amorphous state of the PCRAM array, and then the array was operated with the SET pulse with the different pulse width. According to the experimental results of the SET pulse magnitude, the optimal SET pulse magnitude is 0.3 mA and the pulse width is 200, 300, 500, 1000, and 2000 ns, respectively. The SET distribution with the different pulse width is shown in **Figure 7**, with a cell percent of the SET Resistance value less than 100 kΩ (log(resistance) < 5) is listed in **Table 2**.

The results show that the longer SET pulse width is, the better SET distribution of the array is. When the time is more sufficient, the ratio of crystallization is higher. And with the SET time increasing, the effect of the optimization of the SET distribution is smaller and smaller because the crystallization ratio in the cell is higher and higher until it is saturated. In the sample, the SET pulse width needs to reach 1000 ns to obtain a better resistance distribution. It can be seen that when SP is used in a SET operation, the pulse width demand is longer and the SET speed is slow.

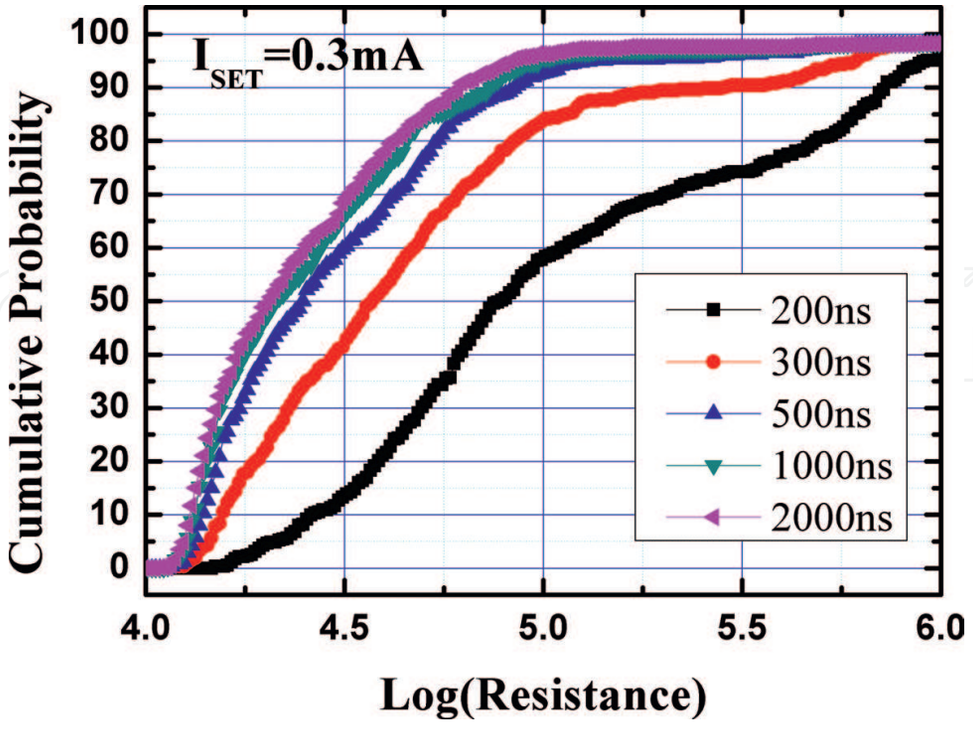

Figure 7. SET distribution with the different pulse width.

SET width (ns)	200	300	500	1000	2000
Cell percent (%)	58.49	84.12	92.77	95.51	96.29

Table 2. Cell percent of the SET resistance value (<100 kΩ) with the different SET pulse width.

2.4. SET process research

To ensure a high enough SET success rate, it is necessary to ensure a sufficient width pulse, which poses a challenge to the speed of the SET operation. In order to have a deeper understanding of the SET operation process, we also need to understand the change of the SET resistance of the array at all times when the SET operation starts. Therefore, we tested the variation of the average resistance of the array with the SET pulse operation time, as shown in **Figure 8**. The array size is 16 kbits, and the test time is 60–630 ns, and the resistance value is tested every 30 ns. Before the SET operation, 1.5 mA 200 ns RESET pulse is used to operate the array. In order to study the influence of SET current, repeated experiments are performed under the different sets of SET current.

The test results show that the resistance variation with the time in the SET process can be divided into three stages. In the first stage, the resistance maintains high resistance. It is particularly

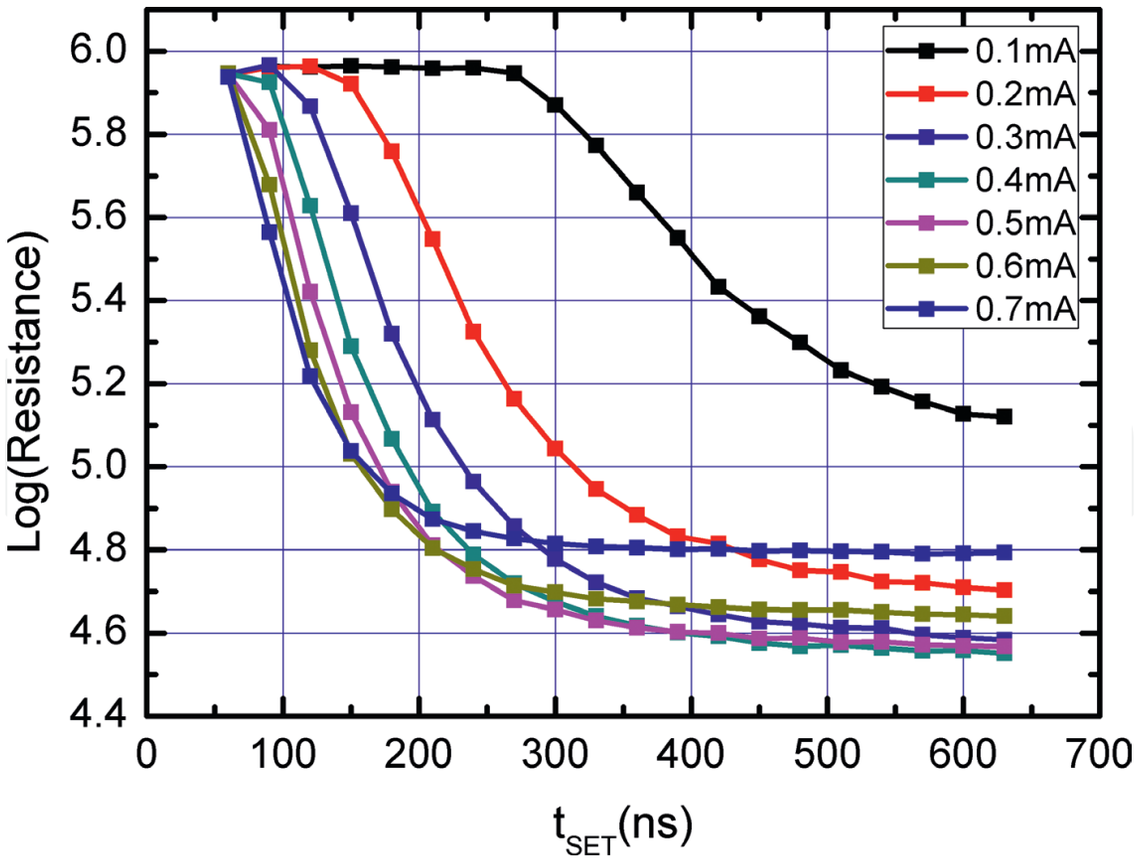

Figure 8. SET resistance variation with the time in the set process.

noticeable when the SET current operation is 0.1 mA. This stage time is affected by the SET current. The larger SET current is, the less time it will take. In the second stage, the resistance variation is the most intense, which decreases rapidly with the increase in SET time. In the third stage, the resistance variation will enter a stationary phase, and the resistance will decrease slowly with the increase in SET time. The larger SET current is, the faster third stage occurring is, and the resistance at this stage is determined by the SET current magnitude.

The variation of SET resistance in different time periods in the SET process is calculated to analyze the SET speed as shown in **Figure 9**. In the SET process, the SET speed is not constant, but at some time, the speed will reach the extreme value. Furthermore, the larger the SET current is, the earlier extreme value appearing is.

The crystallization of the phase change materials is divided into nucleation and crystal growth, and the GST alloy is reflected in the nucleation dominated recrystallization [17]. The crystallization process of the GST alloy is the incubation of crystal nucleus and then the crystal grows. For the SET operation of the PCRAM chip, when the SET pulse is injected, on the one hand, due to the parasitic parameters of the circuit and the cell itself, the cell threshold switching needs some time [18]. On the other hand, the inside of the cell goes through an incubation process [19]. These two causes lead to the first stage of the SET process. However, when the SET current is larger, the influence of the parasitic parameters can be more favorably overcome. When the temperature field formed by the current is higher, it is more favorable for the nucleation incubation [19]. Therefore, the larger is the SET current, the shorter is the first stage.

When the nucleus of the cell begins to grow, the resistance begins to drop rapidly and enters the second stage of the SET process. The SET current heats the electrode and forms a temperature field

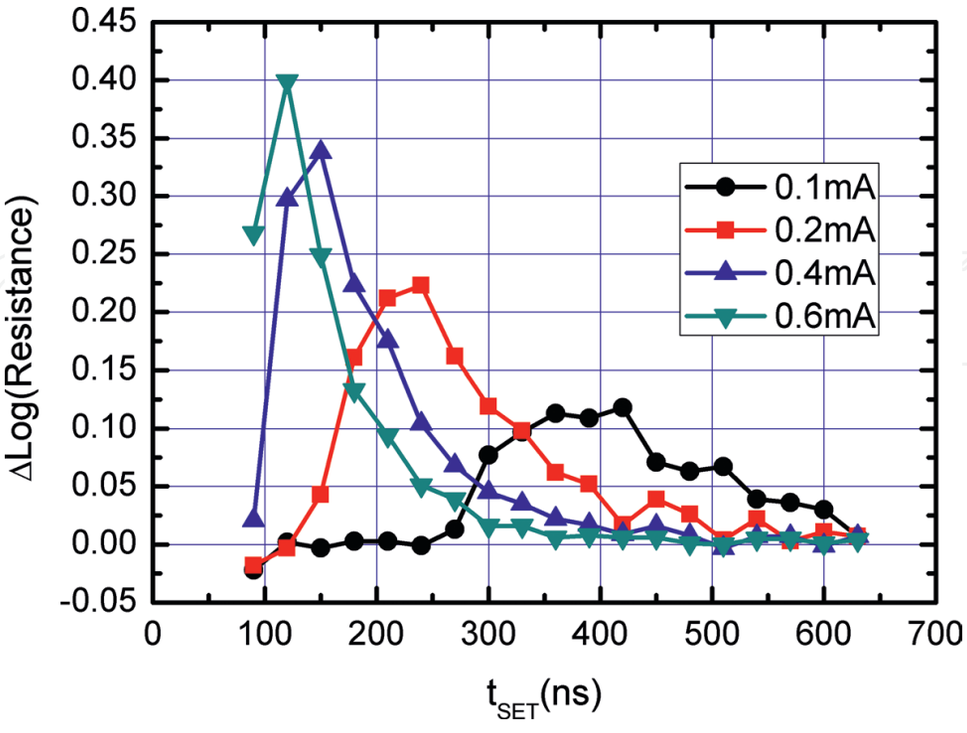

Figure 9. Relationship between the SET resistance variation velocity with the SET time.

inside the cell. There is a temperature gradient in this temperature field as shown in **Figure 10**. This makes the internal temperature of the cell not consistent; the center temperature is higher, and the edge temperature is lower. This makes the incubation time for each region inconsistent. A phenomenon appears in **Figure 9**, whereby the speed of the cell resistance decreasing in the early stages will gradually increase; this is because the cells within different areas do not match the moment into the growth stage. When the area of the cell into growth stage is more and more, the resistance decreases faster. When all amorphous areas of the cell begin to grow, it will reach a rate of extreme value. Except the temperature effect of nucleation speed, the study of Sebastian et al. [20] shows that the velocity of crystal growth also has a great relationship with temperature. The relationship between the velocity and temperature of crystal growth is shown in **Figure 11**.

As shown in **Figure 11**, there is a temperature that allows the crystal to grow the fastest, at about 750 K. In the second stage of the SET process, the growth velocity in the different regions of the cell is different due to the different temperatures, so the time required for completing crystallization of each part is different. The SET process will enter the third stage when the crystal of each region gradually grows to form a crystal channel within the cell. At this stage, as the SET time continues to lengthen, the crystal channels in the cell become more and more, and the resistance still slowly decreases. The three stages of the SET process are shown in **Figure 12**. When the SET current is small, the growth rate of the amorphous region edge can be slow, which can make the crystal channel difficult to form, and the resistance cannot be reduced rapidly in the SET pulse time. This is the reason why the SET distribution is poor using the SET current operation of 0.1 mA in **Figure 5**. When the SET electric current is larger, the growth velocity is faster in the edge. But it may cause the temperature to be too high to be RESET in the center and also can lead to residual amorphous. Therefore, the SET distribution is very poor using the 0.7 mA SET current.

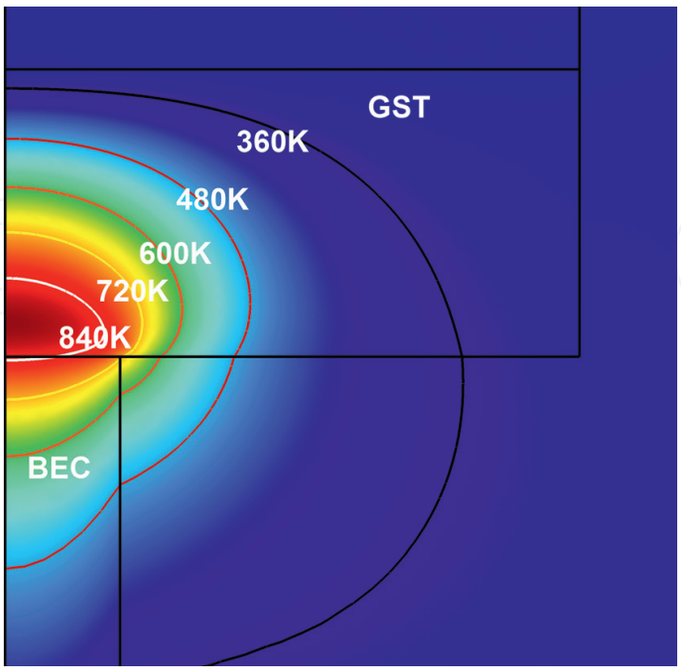

Figure 10. Internal temperature field of the unit within the SET process.

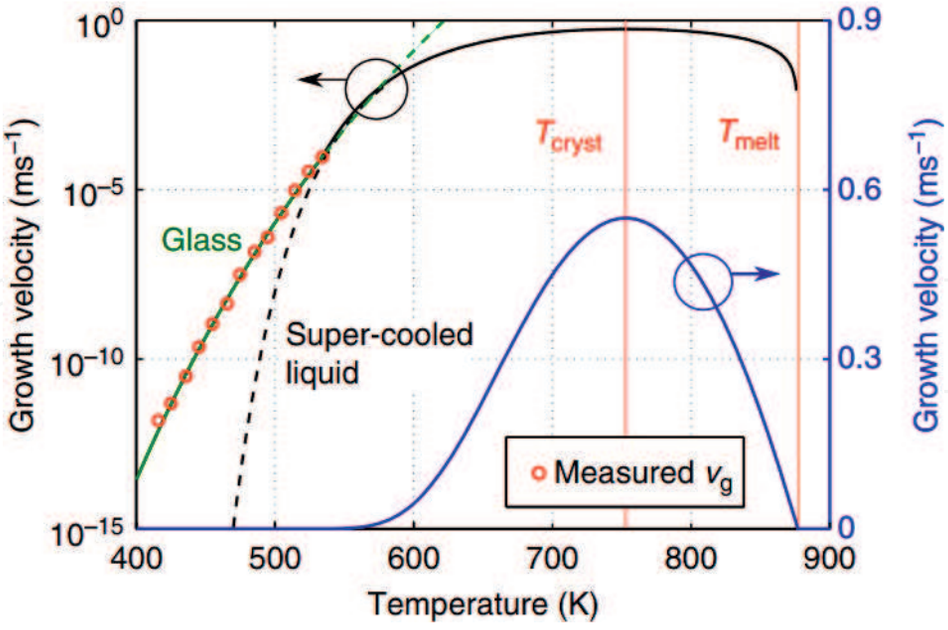

Figure 11. Relationship between the velocity of crystal growth and temperature [20].

Figure 12. Nucleation, growth and saturation stage diagram of PCM cell in the SET process.

3. D-SET operation method

Given the study of the SET process in the last section, it can be seen that the large SET operation current is beneficial to improve the SET speed. On the one hand, because the larger operation current can overcome the influence of the parasitic parameters, which promotes the rapid nucleation; On the other hand, the higher temperature can increase the growth rate of PCRAM crystal, which reduces the time of the second stage. However, a single high SET current can cause too high temperature in the phase change cell and cannot be crystallized, resulting in too many amorphous residues, which in turn result in the failure of the SET operation. Therefore, it is not feasible to use a single lifting SET current to speed up the SET operation, and the shape of SET pulse needs to be optimized.

http://dx.doi.org/10.5772/intechopen.74786

3.1. D-SET

Considering the large SET current required for the promotion of the SET speed, a high power pulse (HPP) is added before the single box SET pulse to improve the SP SET effect on the SET distribution and speed. To verify the feasibility of this improved pulse, we verified the SET effect of SP and improved SET pulse in 16 kbits PCRAM array. The illustration shows that the shape of SP (without HPP) and improved pulse (with HPP) in **Figure 13**.

Figure 13(a) shows the relationship between the SET current I_{SET} and the average SET resistance obtained by the experiment. According to the test results, the relationship between the single pulse and the HPP pulse is consistent with that of the SET resistance. The SET resistance is the minimum when the I_{SET} is moderate. The difference is that in any I_{SET} comparison, the average SET resistance obtained by using the HPP pulse is much lower than that of SP. When the I_{SET} is smaller, the gap is larger. In addition, using the HPP pulse, when 0.3 mA I_{SET} made the smallest average SET resistance, its minimum average SET resistance below 20 kΩ, but the corresponding minimum average SET resistance using SP is over 40 kΩ. The HPP pulse can effectively improve the SET effect.

Figure 13(b) shows the relationship between SET pulse width t_{SET} and average SET resistance. In this case, the array used the same RESET pulse operation prior to the SET operation to make the array initial high resistance state. The magnitude and width of the RESET pulse is 1.5 mA, 200 ns respectively. The I_{SET} SET current of SP and the HPP pulse is 0.3 mA, while for the HPP pulse, the magnitude of HPP before its SET pulse is 1.5 mA and the pulse width is 100 ns. As you can see, for SP, the first stage is about 100 ns, and the SET resistance is still high in this stage. In the second stage, the SET resistance begins to decline slowly with the length of the SET pulse width. The average SET resistance dropping below 100 kΩ takes 250 ns, and it is not capable of reducing the resistance under 50 kΩ within 500 ns. For the HPP pulse, the

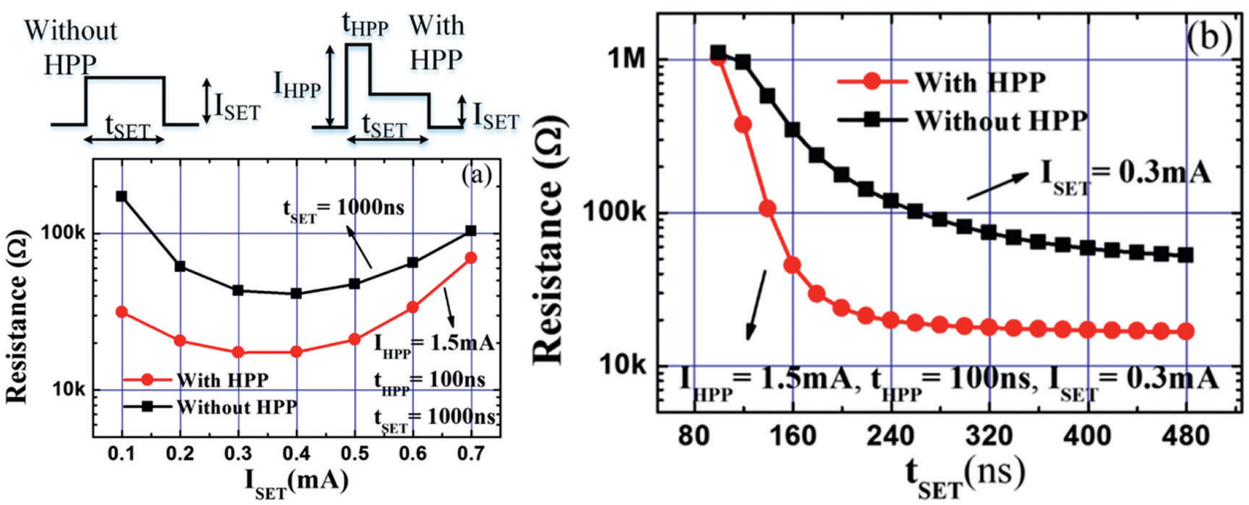

Figure 13. Comparison of SP and improved pulse SET effect [21].

average SET resistance drops rapidly to below 20 kΩ within 240 ns. It can be seen that the HPP pulse can effectively accelerate the SET speed so that the cell is fully crystallized.

Based on the abovementioned comparison experiment, the SET velocity of the HPP pulse was increased and the SET resistance was reduced. So, we designed a new SET operation method called Dual Pules SET (D-SET) [21]. A pulse sequence containing two pulses used in SET operation of the PCRAM cell, in which the first pulse is the HPP pulse, and the subpulse is a regular SET pulse.

3.2. Optimization of the D-SET method

The specific choice of the first pulse and the subpulse is related to the effect of the SET operation for the D-SET. In order to further study the mechanism of the first HPP pulse and further optimize the HPP pulse, the magnitude and pulse width of the HPP pulse were experimentally studied. Firstly, the SET distribution of the HPP pulse width is studied.

From **Figure 14**, it can be seen that when the HPP pulse width increased from 50 to 100 ns, the SET resistance obtained is gradually moving to a lower value. When the HPP pulse width is over 100 ns, the improvement of the SET distribution is increased with increasing HPP pulse width. Considering that the HPP pulse magnitude is the same as that of the RESET pulse, this is similar to the effect of the RESET pulse width.

To optimize the HPP, the effect of I_{HPP} on SET distribution is characterized. As shown in **Figure 15**, the I_{HPP} ranges from 1.1 to 1.5 mA while the I_{RESET} is fixed at 1.5 mA. In the D-SET pulse operation, the HPP pulse width is 100 ns, the subpulse magnitude is 0.3 mA and the width is 900 ns.

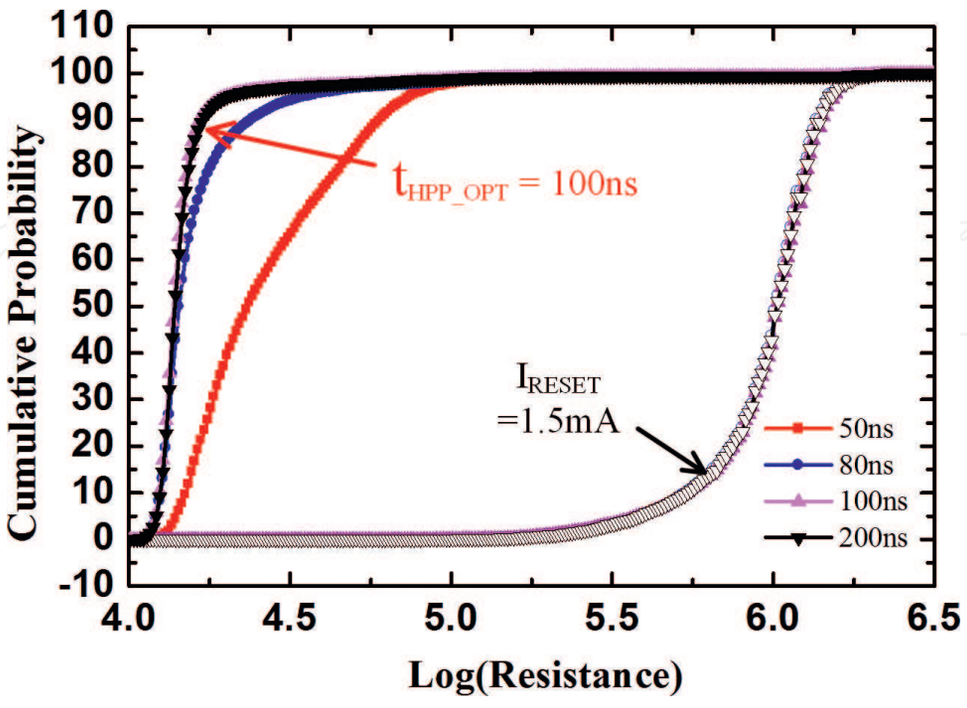

Figure 14. Effect of the HPP pulse width on the SET resistance distribution [21].

http://dx.doi.org/10.5772/intechopen.74786

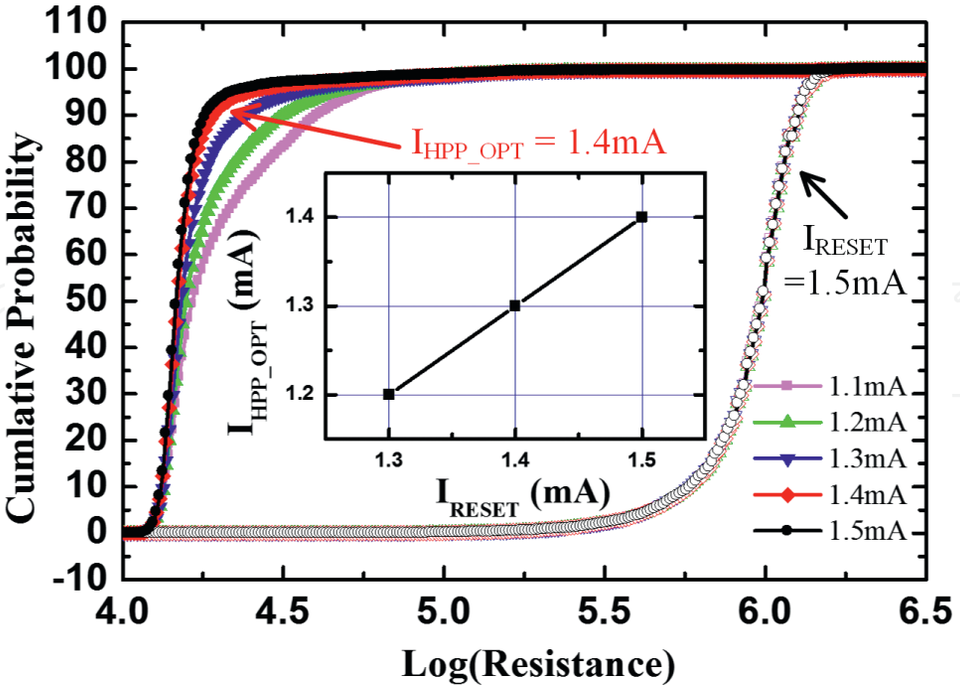

Figure 15. Influence of the HPP magnitude on SET distribution [21].

As the I_{HPP} increases, the SET distribution improves. And when I_{HPP} is over 1.4 mA, this improvement on the SET distribution saturates. This is because that increasing I_{HPP} will extend the favorable temperature annulus. The larger the annulus is, the more amorphous regions meet the favorable temperature when the annulus shrinks. When the annulus is beyond the active region, all the amorphous regions are covered and the improvement on SET resistance is optimal. The specific I_{HPP} that achieves optimal SET performance is called I_{HPP_OPT}. Since the favorable temperature is lower than the melt temperature, I_{HPP_OPT} is lower than I_{RESET}. The correlations of I_{RESET} vs. I_{HPP_OPT} is shown in the inset of **Figure 15**. The corresponding I_{HPP_OPT} to I_{RESET} of 1.5, 1.4, and 1.3 mA are 1.4, 1.3 and 1.2 mA, respectively. It suggests that the smaller the amorphous area that RESET pulse creates, the smaller the favorable temperature annulus needed.

3.3. Analysis of the mechanism of D-SET

For SET process, the crystal growth plays an important role in crystallization and the crystal growth velocity has a huge dependence on temperature. It is reported that the crystal growth velocity is over 8 orders of magnitude spanning a temperature range from 415 to 580 K [22], and the maximal crystal growth velocity appears at near 750 K [9]. A fast crystallization needs to ensure the amorphous region crystallized under favorable temperature range for crystal growth.

When applying the SP without HPP, the favorable temperature annulus is small and near the BEC as shown in **Figure 16**. The temperature near the interface is too low to ensure fast growth. As a result, there is amorphous residual at the outside of the active region when SET pulse terminates. As for the single pulse with HPP, the HPP creates a favorable temperature annulus of large radius, which may be beyond the amorphous region depending on I_{HPP}. When the HPP switches to the single pulse, the device cools off to a steady state temperature

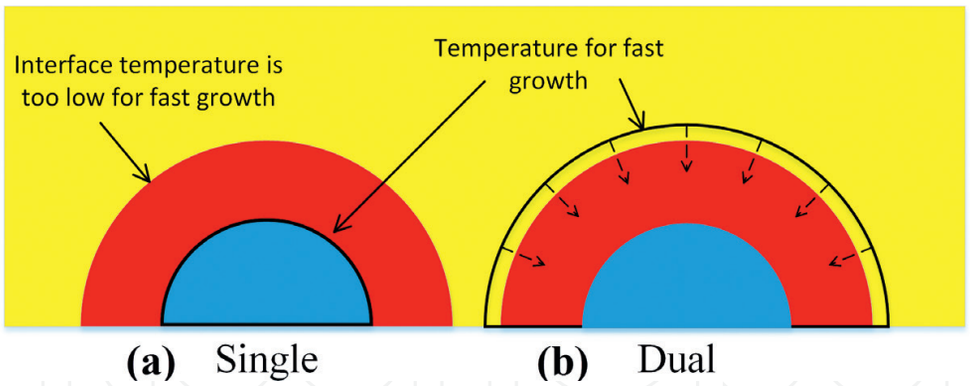

Figure 16. Schematic illustration of the different crystallization process when applying (a) single pulse, and (b) dual pulse [21].

and the favorable temperature annulus shrinks toward the center. As this annulus sweeps in, the outside of the active region also has an opportunity to crystallize at favorable temperature. This is probably the reason why for crystallization that applying HPP pulse is much faster and more sufficient.

3.4. Performance test of D-SET

The D-SET method has excellent advantages to the SET speed and the resistance distribution.

The specific currents as well as the timing for each pulse procedure are described in the inset of **Figure 17**. The SET distributions obtained with those three kinds of SET methods are showed in **Figure 17**. The same RESET pulses are applied before each SET operation, which results in the same RESET resistance distribution. As shown in **Figure 17**, it is found that D-SET results in the lowest and narrowest SET resistance distribution. In the same limited SET time of 300 ns, the proportion of cells with SET resistance under 30 kΩ (log(resistance)<4.5) for D-SET, SP and SCD is 98, 8, and 35%, respectively.

In addition to achieving a good SET distribution, the SET resistance of D-SET is more prominent than the other two SET methods. The resistance drift of the SET resistance obtained by applying those three SET methods are also evaluated. The resistance drift has been described in the literature according to the power-law empirical equation (1) [23]:

$$\mathrm{R}(t) = R_0 \left(\frac{t}{t_0}\right)^{v} \tag{1}$$

where t_0 is a normalizing time value, R_0 is the resistance at time t_0, and v is the drift exponent. To extract the drift exponent, both the resistance of PCRAM cells right after SET operation and after an annealing of 3 h at 110°C (resistance read performed at room temperature) are collected firstly. The statistical results are presented in **Figure 18(a)**. Then the corresponding drift coefficients of each cell are calculated by Eq. (1) and the statistics are reported in **Figure 18(b)**. As shown in **Figure 18(a)** and **(b)**, the D-SET method results in the smallest resistance drift as well as in the smallest drift coefficient dispersion. The mean drift coefficients of SET resistance obtained by SP, D-SET, and SCD are 0.056, 0.018, and 0.041, respectively. The correlations of

http://dx.doi.org/10.5772/intechopen.74786

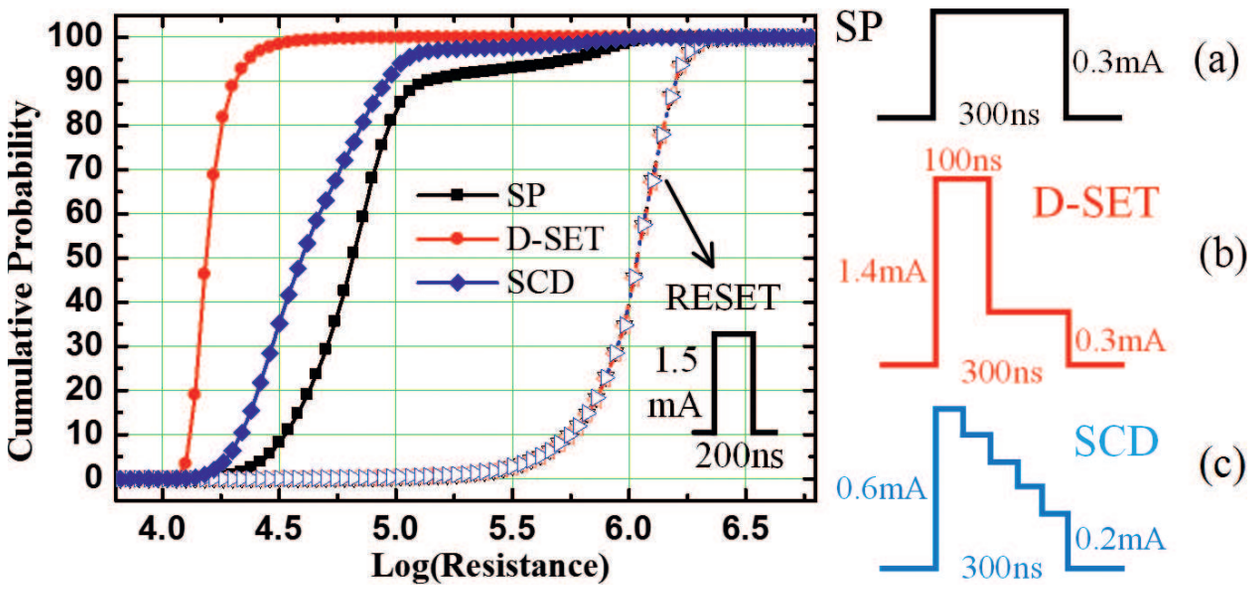

Figure 17. Resistance distributions obtained with three kinds of SET pulses: (a) SP, (b) D-SET, and (c) SCD. The schematic of the SET pulses are showed in the inset figure [21].

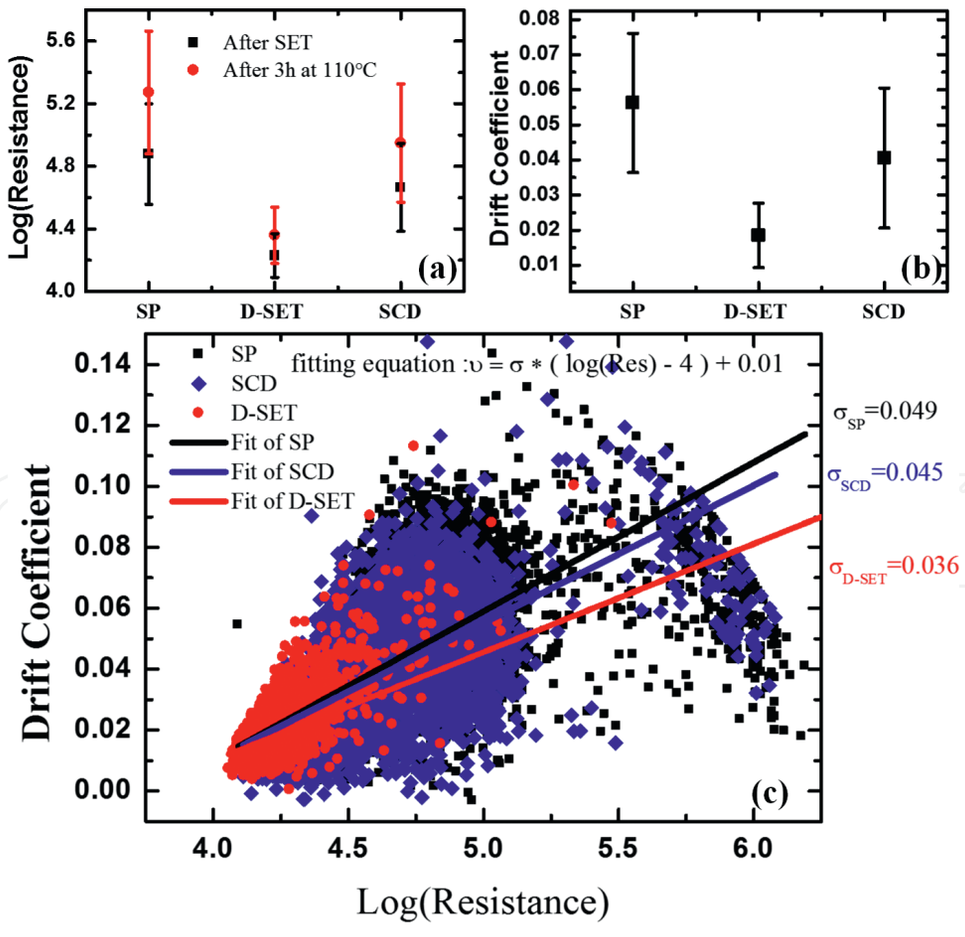

Figure 18. Comparison of (a) the programmed SET resistance, (b) the corresponding drift coefficient, and (c) correlations of drift coefficient vs. SET resistance obtained with SP, D-SET and SCD [21].

drift coefficient vs. SET resistance are shown in **Figure 18(c)**. A strong correlation between the drift coefficient and the programmed resistance has been observed. It shows that the higher the resistance, the higher the value of ν, as described in the literature [24, 25] According to Ref. 22, the drift coefficient values of SET state resistance (less than 10 kΩ) are lower than 0.01. The correlations are fitted with the fitting equation (2):

$$\nu = \delta * (\log(R) - 4) + 0.01 \tag{2}$$

where ν is the drift coefficient value, R is the SET resistance and δ is the fitting parameter which stands for the gradient of drift coefficient. The smaller the gradient is, the slower the drift coefficient increases with resistance. The fitting parameters of SP, SCD, and D-SET are 0.049, 0.045, and 0.036, respectively. It suggests that the drift benefits arise not only from the lower SET resistance but also the smaller gradient. It can be seen that the anti-drift property of the dual pulse is not only because of the smaller SET resistance but also because its drift factor is smaller with the change of resistance.

4. Conclusions

The field of PCRAM based on PCM research has gained momentum in the last decade because of its interesting device and material properties that make them an excellent candidate for future nonvolatile memory applications. This chapter gives an overview of the SET operation method. D-SET has been presented applying HPP before a single SET pulse which benefits the SET speed and SET resistance. The mechanism and performance of the D-SET has been characterized and analyzed. This D-SET is capable of achieving lower SET distribution and smaller resistance drift than the conventional SET method within 300 ns on a 64 MB PCRAM test chip in 40 nm CMOS process.

Acknowledgements

This work was supported in part by the “Strategic Priority Research Program” of the Chinese Academy of Sciences (XDA09020402), National Natural Science Foundation of China (61176122, 61106001).

Author details

Daolin Cai*, Zhitang Song and Yifeng Chen

*Address all correspondence to: caidl@mail.sim.ac.cn

State Key Laboratory of Functional Materials for Informatics and Nanotechnology Laboratory, Shanghai Institute of Micro-system and Information Technology, Chinese Academy of Sciences, Shanghai, China

References

[1] Bez R. Chalcogenide PCM: A memory technology for next decade. In: Proceedings the IEEE International Technical Digest on the Electron Devices Meeting (IEDM' 09); 7-9 December 2009; Baltimore, Maryland, USA. New York: IEEE; 2009. pp. 89-92

[2] Chen M, Rubin KA, Barton RW. Compound materials for reversible, phase–change optical–data storage. Applied Physics Letters. 1986;**49**(9):502-504

[3] Yamada N, Takenaga M, Takao N. Te–Ge–Sn–Au phase change recording film for optical disk. In: Proceedings the International Society for Optics and Photonics (SPIE' 86); 1986. p. 7

[4] Song Z, Zhan Y, Cai D, Liu B, Chen Y, Ren J. A phase change memory chip based on TiSbTe alloy in 40-nm standard CMOS technology. Nano-Micro Letters. 2015;**7**(2):172-176. DOI: 10.1007/s40820-015-0030-z

[5] Rao F, Ding K, Zhou Y, Zheng Y, Xia M, Lv S, Song Z, Feng S, Ider R, Mazzarello R, Zhang W, Ma E. Reducing the stochasticity of crystal nucleation to enable subnanosecond memory writing. Science. 2017;**358**:1423-1427. DOI: 10.1126/science.aao3212

[6] Yamada N, Ohno E, Nishiuchi K, Akahira N, Takao M. Rapid–phase transitions of GeTe–Sb_2Te_3 pseudobinary amorphous thin–films for an optical disk memory. Journal of Applied Physics. 1991;**69**(5):2849-2856. DOI: 10.1063/1.348620

[7] 3D XPoint: A Guide To The Future Of Storage-Class Memory 2015 [Internet]. 2016. Available from: http://www.tomshardware.com/reviews/3d-xpoint-guide,4747.html [Accessed: 2016-11-25]

[8] Cai D, Chen H, Wang Q, Chen Y, Song Z, Wu G, Feng S. An 8-Mb phase-change random access memory chip based on a resistor-on-via-stacked-plug storage cell. IEEE Electron Device Letters. 2012;**33**(9):1270-1272. DOI: 10.1109/LED.2012.2204952

[9] Kolobov AV, Fons P, Frenkel AI, Ankudinov AL, Tominaga J, Uruga T. Understanding the phase-change mechanism of rewritable optical media. Nature Materials. 2004;**3**(10):703-708. DOI: 10.1038/nmat1215

[10] Sun ZM, Zhou J, Ahuja R. Structure of phase change materials for data storage. Physical Review Letters. 2006;**96**(5):055507-1-055507-4. DOI: 10.1103/PhysRevLett.96.055507

[11] Oh HR, Cho BH, Cho WY, Kang S, Choi BG, Kim HJ, Kim KS, Kim DE, Kwak CK, Byun HG. Enhanced write performance of a 64-Mb phase-change random access memory. IEEE Journal of Solid-State Circuit. 2006;**41**(1):122-126. DOI: 10.1109/JSSC.2005.859016

[12] Lee KJ, Cho BH, Cho WY, Kang S, Choi BG, Oh HR, Lee CS, Kim HJ, Park JM, Wang Q, Park MH, Ro YH, Choi JY, Kim KS, Kim YR, Shin IC, Lim KW, Cho HK, Choi CH, Chung WR, Kim DE, Yoon YJ, Yu KS, Jeong GT, Jeong HS, Kwak CK, Kim CH, Kim K. A 90 nm 1.8 V 512 Mb diode-switch PRAM with 266 MB/s read throughput. IEEE Journal of Solid-State Circuit. 2008;**43**(1):150-159. DOI: 10.1109/JSSC.2007.908001

[13] Bedeschi F, Boffmo C, Bonizzoni E, Resta C, Torelli G, Zella D. Set-sweep programming pulse for phase-change memories. In: Proceedings the IEEE International Symposium on the Circuits and Systems (ISCAS '06); 21-24 May 2006; Greece. New York: IEEE; 2006. pp. 967-970

[14] Sandre GD, Bettine L, Calvetti E, Giacomi G, Posotti M, Borghi M, Zuliani P, Tortorelli I, Pellizzer F. Program circuit for a phase change memory array with 2 MB/s write throughput for embedded applications. In: Proceedings of the 34th European Solid-State Circuits Conference (ESSCIRC '08); 15-19 September 2008; Scotland, 2008. pp. 198-201

[15] Bedeschi F, Boffino C, Bonizzoni E, Resta C, Torelli G. Staircase-down SET programming approach for phase-change memories. Microelectronics Journal. 2007;**38**(10):1064-1069. DOI: 10.1016/j.mejo.2007.07.121

[16] Geoffrey W, Burr S, Matthew JB, Sebastian A, Cheng HY, Wu JY, Kim S, Norma E, Papandreou N, Lung HL, Pozidis H, Eleftheriou E, Lam CH. Recent progress in phase-change memory technology. IEEE Journal on Emerging and Selected Topics in Circuits and Systems. 2016;**6**(2):146-162. DOI: 10.1109/JETCAS.2016.2547718

[17] Kalb J, Spaepen F, Wuttig M. Atomic force microscopy measurements of crystal nucleation and growth rates in thin films of amorphous Te alloys. Applied Physics Letters. 2004;**84**(25):5240-5242. DOI: 10.1063/1.1764591

[18] Kang DH, Cheong BH, Jeong JH, Lee TS, Kim IH, Kim WM, Huh JY. Time-resolved analysis of the set process in an electrical phase-change memory device. Applied Physics Letters. 2005;**87**(25):253504. DOI: 10.1063/1.2149172

[19] Redaelli A, Ielmini D, Lacaita A, Pellizzer F, Pirovano A, Bez R. Impact of crystallization statistics on data retention for phase change memories. In: Proceedings the IEEE International Technical Digest on the Electron Devices Meeting (IEDM' 05); 5-7 December 2005; Washington, DC. New York: IEEE; 2005. pp. 742-745

[20] Sebastian A, Gallo ML, Krebs D. Crystal growth within a phase change memory cell. Nature Communications. 2014;**5**:4314. DOI: 10.1038/ncomms5314

[21] Wang YQ, Cai DL, Chen YF, Wang YC, Wei HY, Huo RR, Chen XG, Song ZT. Optimizing set performance for phase change memory with dual pulses set method. ECS Solid State Letters. 2015;**4**(7):Q32-Q35. DOI: 10.1149/2.0041507ssl

[22] Jeyasingh R, Fong SW, Lee J, Li ZJ, Chang KW, Mantegazza D, Asheghi M, Goodson KE, Wong HSP. Ultrafast characterization of phase-change material crystallization properties in the melt-quenched amorphous phase. Nano Letters. 2014;**14**(6):3419-3426. DOI: 10.1021/nl500940z

[23] Ielmini D, Lavizzari S, Sharma D, Lacaita AL. Physical interpretation, modeling and impact on phase change memory (PCM) reliability of resistance drift due to chalcogenide structural relaxation. In: Proceedings the IEEE International Technical Digest on the Electron Devices Meeting (IEDM' 07); 9-11 December 2007; Washington, DC. New York: IEEE; 2007. pp. 939-942

[24] Braga S, Cabrini A, Torelli G. Experimental analysis of partial-SET state stability in phase-change memories. IEEE Transactions on Electron Devices. 2011;**58**(2):517-522. DOI: 10.1109/TED.2010.2090157

[25] Kostylev S, Lowrey T. Drift of programmed resistance in electrical phase change memory devices. In: Proceedings of the European Phase Change and Ovonics Symposium (EPCOS, 08), 8-9 September 2008; Germany. pp. 117-124

IntechOpen

IntechOpen