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Ge_{0.83}Sn_{0.17} P-Channel Metal-Oxide-Semiconductor Field-Effect Transistors: Impact of Sulfur Passivation on Gate Stack Quality

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Additional information is available at the end of the chapter

http://dx.doi.org/10.5772/intechopen.74532

Abstract

The effect of sulfur passivation of the surface of Ge_{0.83}Sn_{0.17} is investigated. X-ray photoelectron spectroscopy (XPS) was used to examine the interfacial property between HfO₂ and Ge_{0.83}Sn_{0.17}. Sulfur passivation is effective in reducing both the Ge oxides and Sn oxides formation and the Sn atoms segregation. In addition, sulfur passivation reduces the interface trap density D_{it} at the HfO₂/Ge_{0.83}Sn_{0.17} interface from the valence band edge to the midgap. After the implementation of sulfur passivation, Ge_{0.83}Sn_{0.17} p-MOSFETs show improved subthreshold swing S and effective hole mobility μ_{eff} . 25% μ_{eff} enhancement can be observed in Ge_{0.83}Sn_{0.17} p-MOSFETs with sulfur passivation at a high inversion carrier density N_{inv} of 1 × 10¹³ cm⁻².

Keywords: GeSn, p-MOSFETs, sulfur passivation, XPS, dangling bond

1. Introduction

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Materials with high carrier mobilities such as germanium (Ge) could replace Silicon (Si) as the channel material in metal-oxide-semiconductor field-effect transistors (MOSFETs) for future high performance logic applications [1–10]. Recently, germanium-tin (GeSn) was reported to have a higher hole mobility than Ge and is a promising channel material for p-channel MOSFETs (p-MOSFETs) [11–18].

Theoretical calculation [11] shows that the light hole effective mass of GeSn decreases with increasing Sn composition. It is also demonstrated experimentally [19] that increasing Sn

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composition in GeSn p-MOSFETs increases the effective hole mobility. However, due to the low surface energy and large covalent radius of Sn, Sn atoms may segregate to the surface during growth of GeSn [20–22]. Hence, the thermal stability may be worse at a higher Sn composition. Li et al. reported that a Sn-rich surface layer would form when $Ge_{0.922}Sn_{0.078}$ is annealed at 620°C [23]. A similar phenomenon occurs on $Ge_{0.915}Sn_{0.085}$ surface after annealing at 500°C [24]. For Sn composition as high as 17%, self-assembled Sn wires can form at an annealing temperature as low as 280°C [25]. Severe Sn segregation may reduce carrier mobility and degrade the drive current in MOSFETs. Therefore, in order to achieve high performance GeSn p-MOSFETs with high Sn composition, a fabrication process with low thermal budget may be required to maintain a good quality of the GeSn channel material and the GeSn/high-*k* dielectric interface.

Various passivation techniques have been demonstrated to be effective in improving the gate stack quality of both Ge and GeSn channel p-MOSFETs, such as Si_2H_6 passivation [12, 17], Ge capping [26], GeSnO_x passivation [27, 28], and sulfur passivation [15, 29, 30]. Among these passivation techniques adopted for GeSn p-MOSFETs fabrication, Si_2H_6 passivation and GeSnO_x passivation require a process temperature higher than 370°C and 400°C, respectively. It has already been reported that Sn can segregate out to the GeSn surface during Si passivation process at a temperature of 370°C and degrades the device performance [17]. Therefore, low temperature passivation technique was investigated in this work for the fabrication of GeSn p-MOSFETs with Sn composition of 17%.

The adsorption of sulfur atoms is a promising route to chemically and electrically passivate the highly reactive Ge and GeSn surface [15, 29–31]. Compared with other passivation techniques, room temperature sulfur passivation using $(NH_4)_2S$ solution has several advantages: (1) GeSn surface could be effectively passivated through the formation of covalent S-Ge and S-Sn bond. This will reduce oxide formation which degrades device performance; (2) The formed sulfur passivation layer is very thin with very little increase on the effective oxide thickness (EOT); (3) Sn segregation can be suppressed during the passivation process owning to a lower thermal budget. Sulfur passivation has already been implemented into $Ge_{0.947}Sn_{0.053}$ p-MOSFETs fabrication and demonstrated enhanced peak hole mobility as compared with Si₂H₆ passivation [15]. However, the mechanism of the effect of sulfur passivation on the GeSn/HfO₂ interface quality has not been investigated. In addition, the impact of sulfur passivation on the reduction of D_{it} was not quantified.

In this chapter, sulfur passivation of GeSn surface at room temperature was investigated and implemented in the fabrication of Ge_{0.83}Sn_{0.17} p-channel MOSFETs. To study the impact of sulfur passivation on the quality of high-*k* dielectric/GeSn interface, extensive X-ray photoelectron spectroscopy (XPS) analysis was carried out. Sulfur passivation is found to be effective in suppressing the formation of Sn oxides and Ge oxides, and Sn surface segregation. In addition, sulfur passivation helps to reduce the high-*k* dielectric/GeSn interface trap density D_{it} as extracted using the conductance method. Material study of nickel stanogermanide [Ni(GeSn)] contact formation at low temperatures was also performed for low resistivity [Ni(GeSn)] S/D contact. The sulfur-passivated Ge_{0.83}Sn_{0.17} p-MOSFETs exhibit smaller subthreshold swing *S*, higher intrinsic transconductance $G_{m,int'}$ and higher effective hole mobility μ_{eff} as compared to the non-passivated control. At a high inversion carrier density of 1 × 10¹³ cm⁻², sulfur passivation enhances μ_{eff} by 25% as compared with the non-passivated control.

2. Experiment

2.1. Material growth and characterization of Ge_{0.83}Sn_{0.17} substrate

The high quality Ge₀₈₃Sn₀₁₇ sample was grown using molecular beam epitaxy (MBE). 4-inch (001)-oriented Ge wafers with n-type doping concentration of 5×10^{16} cm⁻³ were used as the starting substrates. After the cyclic cleaning of Ge substrates using dilute hydrofluoric acid (DHF) (HF:H₂O = 1:50) and deionized (DI) water, the unintentionally p-type doped $Ge_{0.83}Sn_{0.17}$ film was grown on the Ge substrate using the solid source low temperature MBE system [32, 33]. The growth temperature was set at 100°C. 99.9999% pure Ge and 99.9999% pure Sn were used as Ge and Sn sources, respectively. The growth chamber has a base pressure of 3×10^{-10} Torr. Ge_{0.83}Sn_{0.17} film with the thickness of 10 nm was grown on the Ge substrates. **Figure 1** shows the 5 × 5 μ m AFM scan of the as-grown Ge_{0.83}Sn_{0.17} surface. The surface is very smooth with a root-mean-square (RMS) roughness as small as 0.198 nm. High-resolution transmission electron microscopy (HRTEM) was employed to analyze the crystalline quality of the as-grown Ge_{0.83}Sn_{0.17} sample. Figure 2(a) shows a low magnification cross-sectional TEM (XTEM) image of an as-grown Ge_{0.83}Sn_{0.17} sample, indicating that the GeSn surface is smooth. The GeSn layer thickness is ~10 nm. The high resolution TEM (HRTEM) image in Figure 2(b) shows the smooth $Ge_{0.83}Sn_{0.17}$ surface. In addition, very clear lattice fringes and defect-free GeSn/Ge interface can be observed, as shown in the HRTEM image of Figure 2(c).

High resolution X-ray diffraction (HRXRD) was also used to analyze the Sn composition and strain property of the as-grown $\text{Ge}_{0.83}\text{Sn}_{0.17}$ substrate. **Figure 3(a)** shows the (004) ω -2 θ rocking scan of the as-grown sample. Both Ge and GeSn peaks are well-defined. The peak at smaller 2 θ value is the GeSn peak. The relative broad full-width-half-maximum (FWHM) is due to the thin GeSn layer thickness (~10 nm). (115) reciprocal space mapping (RSM) of an as-grown Ge_{0.83}Sn_{0.17}/ Ge (001) sample is shown in **Figure 3(b)**. The GeSn film is fully strained to the Ge substrate and the substitutional Sn composition is calculated to be 17% from XRD measurement.

Figure 4(a) summarizes the key process steps for fabricating $Ge_{0.83}Sn_{0.17}$ p-MOSFETs. After the MBE growth of ~10 nm $Ge_{0.83}Sn_{0.17}$ film on the lightly n-type doped Ge (100) substrate, pre-gate cleaning using DHF (HF:H₂O = 1:50) and DI water was performed. Two splits were

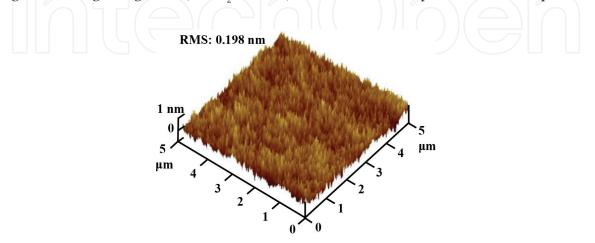


Figure 1. $5 \times 5 \mu m$ AFM scan of the as-grown $Ge_{0.83}Sn_{0.17}$ substrate. The GeSn surface is very smooth with a RMS roughness as small as 0.198 nm.

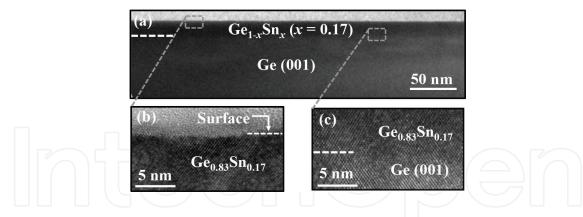


Figure 2. (a) Low magnification XTEM image of an as-grown $Ge_{0.83}Sn_{0.17}$ sample showing the smooth GeSn surface. High magnification XTEM images of the $Ge_{0.83}Sn_{0.17}$ sample shows (c) the zoom-in view of smooth GeSn surface and (d) defect-free $Ge_{0.83}Sn_{0.17}$ /Ge interface.

introduced: one with 10 minutes sulfur passivation using $(NH_4)_2S$ solution (24% by weight) at room temperature (25°C) and the other one without sulfur passivation. After that, the samples were loaded into the atomic layer deposition (ALD) chamber immediately to avoid surface oxidation due to air exposure. Surface treatment was done using Trimethylaluminum (TMA) as precursor with pulse duration of 30 ms. This was followed by deposition of 3 nm-thick hafnium dioxide (HfO₂) at 250°C using Tetrakis (dimethylamido) hafnium and H₂O as precursors. The total ALD process duration including the pumping and venting steps is ~ 15 min. After that, 110 nm-thick tantalum nitride (TaN) was deposited using a reactive sputtering system. The metal gate was then patterned by photolithography and etched using chlorine (Cl₂)-based plasma. A 10 nm-thick nickel (Ni) was then deposited using e-beam evaporator and the self-aligned Ni(GeSn) metallic contact was formed by rapid thermal annealing (RTA) at 250°C for 30 s in the N₂ ambient. Finally, excess Ni was removed by selective wet etch using concentrated sulfuric acid (H₂SO₄) (96% by weight). The maximum processing temperature of

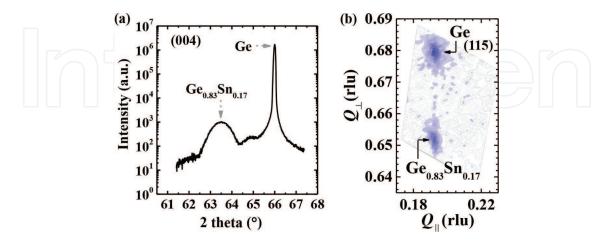


Figure 3. (a) (004) rocking scan of the as-grown sample shows both the $Ge_{0.83}Sn_{0.17}$ and Ge peaks. The well-defined GeSn peak indicates the good crystalline quality of the GeSn layer. The peak is relatively broader than the Ge peak because of the thin layer thickness of the GeSn layer. (b) (115) RSM showing that the $Ge_{0.83}Sn_{0.17}$ film is fully strained to the Ge (001) substrate. The substitutional Sn composition is calculated to be 17%. Device fabrication of $Ge_{0.83}Sn_{0.17}$ p-MOSFETs.

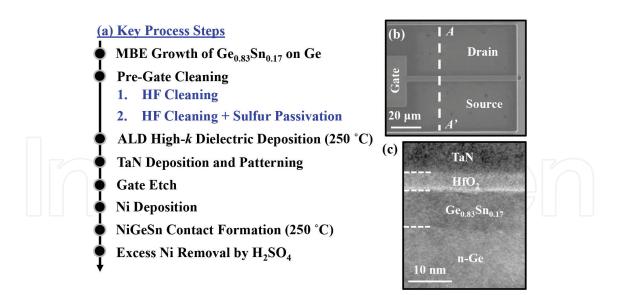


Figure 4. (a) Process flow for fabricating $Ge_{0.83}Sn_{0.17}$ channel p-MOSFETs where a sulfur passivation step was introduced prior to the deposition of high-k gate dielectric (HfO₂). The maximum processing temperature is 250°C. (b) Top-view SEM image showing a completed $Ge_{0.83}Sn_{0.17}$ p-MOSFET with self-aligned NiGeSn S/D contacts. (c) HRTEM image of a $Ge_{0.83}Sn_{0.17}$ channel p-MOSFET as seen in a cross-section along the dash line *AA'* in (b).

the whole fabrication process was 250°C to limit out-diffusion of Sn to the channel surface or into the gate dielectric. A top-view scanning electron microscopy (SEM) image of a completed $Ge_{0.83}Sn_{0.17}$ p-MOSFET with a gate length L_G of 4 µm is shown in **Figure 4(b)**. **Figure 4(c)** shows a HRTEM image of the transistor along the dash line *A*-*A*′ indicated in **Figure 4(b)**.

3. Results and discussion

3.1. Sulfur-passivated gate stack study

The (001) surface of a diamond-structure semiconductor has two dangling bonds per surface atom. GeSn grown on Ge (001) surface has a (001) surface as shown in the atomic structure in **Figure 5(a)** viewed into the [110] direction. One monolayer (ML) of a Group VI element can passivate all the dangling bonds by occupying the bridge site in a (1 × 1) geometry [34, 35]. Sulfur atoms could obtain an ideal (1 × 1) termination of the bivalent (001) surfaces of silicon and Ge. Although sulfur could desorb from the Si surface at room temperature or diffuse into the Si bulk during heating [36], Weser et al. found that an ordered (1 × 1) structure with one sulfur atom bonded on a bulk-like bridge site could be achieved by introducing elemental sulfur atoms on the Ge (001) surface under ultrahigh vacuum (UHV) condition [34, 35]. The formation of Ge-S-Ge bridge bonds after a treatment in (NH₄)₂S solution has also been reported based on various characterization techniques, such as photoelectron spectroscopy [37], ion scattering spectroscopy [38], as well as X-ray standing wave measurements [39]. Similarly, sulfur passivation should also be able to passivate the GeSn (001) surface through the formation of S-Ge and S-Sn covalent bonds which suppress the formation of Ge and Sn oxides at the surface, as illustrated in the atomic schematic shown in **Figure 5(b)**. In this Section, the

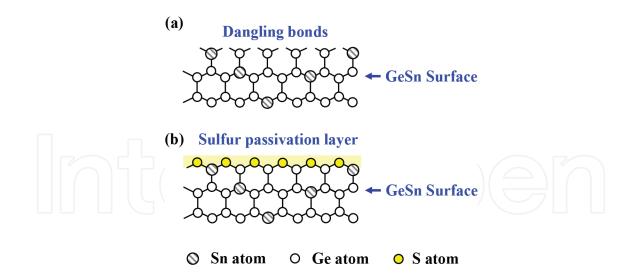


Figure 5. Side view into the [110] direction of (a) non-passivated (1 × 1) and (b) the sulfur-passivated GeSn (001) surfaces.

effectiveness of sulfur passivation on the gate stack of GeSn p-MOSFETs is investigated using XPS. The interface trap density value is also extracted using conductance method and compared with the non-passivated control.

3.2. XPS study on the effect of sulfur passivation

To investigate the interfacial property between the high-*k* dielectric and $Ge_{0.83}Sn_{0.17}$ after sulfur passivation, XPS measurement was carried out to study the change of the interfacial chemical bonds. Two blanket $Ge_{0.83}Sn_{0.17}$ samples were prepared for the measurement. After the cyclic DHF (1:50) cleaning, one of the sample went through 10 minutes aqueous $(NH_4)_2S$ solution (24% by weight) and the other one did not. After that, an ultra-thin (~1 nm) HfO₂ layer was deposited by ALD on these two samples. The HfO₂ layer thickness should be smaller than the XPS information depth [40]. XPS characterization was then performed using a VG ESCALAB 220i–XL imaging XPS system. Monochromatic aluminum (Al) K α X-ray (1486.7 eV) was used to obtain the core level spectra of these samples. Binding energy was calibrated with standard samples for some pure metals. The binding energy of Carbon (C) 1 s from adventitious hydrocarbon surface contamination was set at 285.0 eV for further charge correction.

In order to confirm the incorporation of S after the $(NH_4)_2S$ passivation, core level XPS spectra of the S 2*p* peak were captured for HfO₂-capped Ge_{0.83}Sn_{0.17} blanket samples with and without sulfur passivation, as shown in **Figure 6(a)**. The black curve represents the S 2*p* signal obtained from the non-passivated Ge_{0.83}Sn_{0.17} sample. The circles are the raw data points obtained from the sulfur-passivated sample. Gaussian and Lorentzian line shapes with a Shirley background subtraction were used to fit the raw data. The blue line is the overall fitting of the core level spectra and the gray lines are the fitted peak components. For the S 2*p* core level spectra, the well-resolved two peaks correspond to S $2p_{1/2}$ (163.4 ± 0.02 eV) and S $2p_{3/2}$ (162.0 ± 0.02 eV) [41]. The S 2*p* signal obtained from the sulfur-passivated Ge_{0.83}Sn_{0.17} sample indicates that S is introduced onto the GeSn surface by the (NH₄)₂S treatment and is still present after the deposition of HfO₂. **Figure 6(b)** shows N 1 *s* core level spectra for both samples. The N 1 *s*

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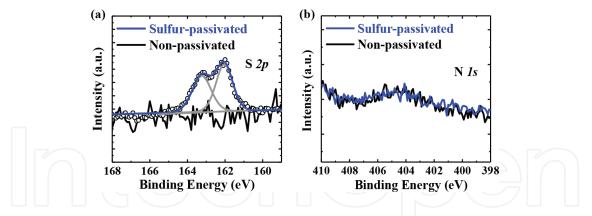


Figure 6. (a) S 2*p* core level XPS spectra for ~1 nm HfO₂-capped Ge_{0.83}Sn_{0.17} samples with and without sulfur passivation. The circles, blue lines and gray lines are the raw data points, the overall fitting curves, and the S $2p_{1/2}$ or S $2p_{3/2}$ peak components, respectively. The black curve represents the S 2*p* signal obtained from the non-passivated sample. (b) N 1*s* core level spectra for both samples.

peak (399.0 ± 0.02 eV) [41] on the sulfur-passivated sample is not observed, indicating that nitrogen is not incorporated. The sulfur passivation layer thickness is calculated using two different photoelectron peaks of the same element at kinetic energies E_1 and E_2 (E_1 and E_2 have sufficiently large differences in λ) [42, 43]. Ge 3*d* and Ge 2 p_3 data (not shown) are used and the equation is shown below:

$$d = \cos\theta \cdot \frac{\lambda_A(E_1) \cdot \lambda_A(E_2)}{\lambda_A(E_1) - \lambda_A(E_2)} \cdot \ln \frac{I_B(E_1)}{I_B(E_2)'}$$
(1)

where $\lambda_A(E_1)$ and $\lambda_A(E_2)$ are the attenuation length of Ge 3*d* and Ge $2p_{3'}$, $I'_B(E_1)$ and $I'_B(E_2)$ are corrected photoelectron intensities, and θ is take-off angle. The sulfur passivation layer thickness is calculated to be 0.44 nm using the Ge 3*d* and Ge $2p_3$ XPS signals.

Figure 7(a) and **(b)** show the Sn *3d* core level spectra of HfO₂-capped Ge_{0.83}Sn_{0.17} blanket samples with and without sulfur passivation, respectively. The circles, blue lines, and gray lines shown in **Figure 7** are the raw data points, the overall fitting curves, and fitted peak components, respectively. Due to spin orbit splitting, two separated Sn *3d* peaks (Sn *3d*_{3/2} and Sn *3d*_{5/2}) can be observed on both samples. The left shoulders, binding energy at 486.7 ± 0.2 eV and 494.9 ± 0.2 eV, can be attributed to the formation of Sn oxides (SnO_x) [41]. Similarly, **Figure 7(c)** and **(d)** show the Ge *3d* core level spectra of HfO₂-capped Ge_{0.83}Sn_{0.17} blanket samples with and without sulfur passivation, respectively. Ge oxides (GeO₂ and GeO_x) can also be observed in both samples. The Ge and Sn oxide signals can be detected on both samples and could come from two sources: (1) ALD HfO₂ deposition as H₂O pulses were introduced in the chamber with a temperature of 250°C, (2) sample transfer before loading into the XPS chamber as the samples were exposed to the air ambient. However, the intensities of both Ge oxides and SnO_x are reduced significantly after the sulfur passivation, indicating the effectiveness of sulfur passivation in suppressing both Ge oxides and SnO_x formation.

The native Ge and Sn oxides formation at the high-k/GeSn interface could result in high D_{it} value and gate leakage current. Lee et al. reported that the native Ge oxide could react with Ge at the interface and form GeO which is easily desorbed during thermal processing [44].

$$\text{GeO}_2 + \text{Ge} \rightarrow 2\text{GeO}(\uparrow).$$
 (2)

This could generate a huge amount of interface states which degrade the gate stack quality [45]. The Sn oxide could also be detrimental to the GeSn gate stack as SnO_2 is known to exhibit metallic behaviour, which leads to high gate leakage current [46, 47]. Therefore, suppressing the Ge and Sn oxides formation is important for achieving good gate quality for $Ge_{0.83}Sn_{0.17}$ p-MOSFETs.

To quantify the impact of sulfur passivation on Ge oxides and SnO_x formation at the high-k/GeSn interface, angle-resolved XPS (ARXPS) was performed. Both SnO_x and Ge oxide signals can be detected. The ratio of oxidized Sn (or Ge) atoms to the total Sn (or Ge) atoms can be calculated using

$$\gamma_{Sn-O} = \frac{A_{Sn-O}}{A_{Sn-Sn} + A_{Sn-O}'}$$
(3)

$$\gamma_{Ge-O} = \frac{A_{Ge-O}}{A_{Ge-Ge} + A_{Ge-O}}'$$
(4)

where $A_{Sn-O'}$, $A_{Sn-Sn'}$, $A_{Ge-O'}$ and A_{Ge-Ge} are the normalized Sn-O peak area, normalized Sn-Sn peak area (also including Sn-Ge bonding), normalized Ge-O peak area, and normalized Ge-Ge peak area (also including Ge-Sn bonding), respectively [48]. With consideration of Scofield photoionization cross-sections and the transmission function of the spectrometer, γ_{Sn-O} and γ_{Ge-O} can be plotted as a function of the photoelectron take-off angle θ and are shown in **Figure 8**. The inset in **Figure 8** illustrates the definition of θ . θ of 0° , 30° , 45° , and 60° were used. It is observed that γ_{Sn-O} and γ_{Ge-O} increase with increasing θ . This is due to the fact that more Ge and Sn atoms at the surface get oxidized than those at the sub-surface. For larger θ , the information depth is smaller and ARXPS becomes more surface sensitive. For Ge oxides, the oxide percentages of the sulfur-passivated Ge_{0.83}Sn_{0.17} sample increase from 20 to 42% when θ increases from 0 to 60°. However, all the values are 10–20% smaller than those of the non-passivated one. A similar trend is also observed for SnO, and the sulfurpassivated Ge_{0.83}Sn_{0.17} sample shows more than 50% reduction in SnO_x percentage than the non-passivated one at all take-off angles. The reduction of oxide formation is more obvious in Sn atoms than Ge atoms. This reveals that sulfur passivation is more effective in suppressing Sn oxide formation than Ge oxide formation. The reduction of both Ge and Sn oxides can be ascribed to the formation of S-Ge and S-Sn bonds on the sample surface. Since both samples went through the DHF treatment, most native oxides were removed and the sample surface becomes H-terminated. As a result, the Ge_{0.83}Sn_{0.17} sample surface has Ge-H, Sn-H bonds, and possibly Ge-O and Sn-O bonds due to the incomplete surface oxide removal in DHF [49]. After sulfur passivation, Ge-H bond (bond energy: 263 kJ/mol [50]) and Sn-H bond (bond energy: 264 kJ/mol) are replaced by more stable Ge-S bond (bond energy: 534 kJ/ mol) and Sn-S bond (bond energy: 467 kJ/mol), respectively. The S passivation layer formed at the GeSn surface can suppress the further oxidation of sub-surface Ge and Sn atoms.

To further investigate the effect of sulfur passivation on the interface quality between the high-k dielectric and Ge_{0.83}Sn_{0.17}, the extent of surface segregation of Sn atom was analyzed

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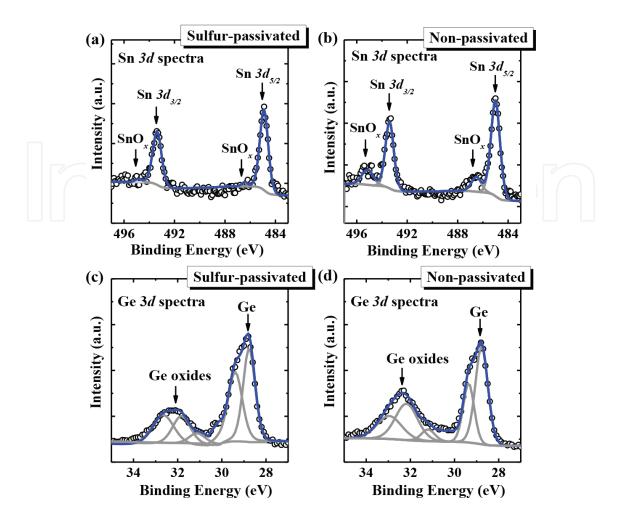


Figure 7. Sn 3*d* and Ge 3*d* core-level spectra of (a) and (c) sulfur passivated and (b) and (d) non-passivated $Ge_{0.83}Sn_{0.17}$ samples obtained by XPS. A 1 nm-thick HfO₂ was deposited on both samples.

using the obtained ARXPS data. The Ge and Sn atomic concentrations can be calculated using the stabilized Ge 3*d* and Sn 3*d* spectra. The atomic concentrations of Sn ($\gamma_{Sn/(Ge + Sn)}$) and Ge ($\gamma_{Ge/(Ge + Sn)}$) can be expressed as

$$\gamma_{Sn/(Ge+Sn)} = \frac{A_{Sn-Sn} + A_{Sn-O}}{A_{Sn-Sn} + A_{Sn-O} + A_{Ge-Ge} + A_{Ge-O}}$$
(5)

$$\gamma_{Ge/(Ge+Sn)} = \frac{\Lambda_{Ge-Ge} + \Lambda_{Ge-O}}{A_{Sn-Sn} + A_{Sn-O} + A_{Ge-Ge} + A_{Ge-O}}$$
(6)

and plotted as a function of θ . **Figure 9** shows $\gamma_{Ge/(Ge + Sn)}$ and $\gamma_{Sn/(Ge + Sn)}$ near the surface of $Ge_{0.83}Sn_{0.17}$ as a function of θ for both the sulfur-passivated and non-passivated samples. The calculated $\gamma_{Sn/(Ge + Sn)}$ increases with the increase of θ , indicating that surface segregation of Sn occurred in both samples. The Sn composition of the non-passivated $Ge_{0.83}Sn_{0.17}$ sample even exceeds 20% at θ of 60°. This is because Sn tends to segregate toward the surface, with the severity increasing at higher Sn compositions. Wang et al. reported that Sn segregation can occur at a temperature as low as 200°C for strained $Ge_{0.915}Sn_{0.085}$ grown on Ge [24]. Since our

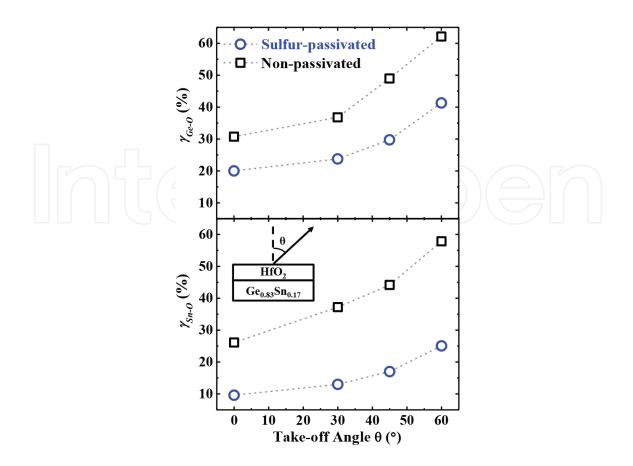


Figure 8. $\gamma_{\text{Sn-O}}$ and $\gamma_{\text{Ge-O}}$ calculated from angle-resolved XPS measurement for both the sulfur-passivated and non-passivated GeSn samples as a function of photoelectron take-off angle θ . The inset shows the definition of θ , which is set to be 0°, 30°, 45°, or 60° in the measurements.

 $Ge_{0.83}Sn_{0.17}$ sample went through the ALD deposition process with a temperature of 250°C, Sn segregation could also occur. Although the segregation of Sn occurs on both GeSn samples, the calculated $\gamma_{Sn/(Ge+Sn)}$ of the sulfur-passivated GeSn sample is smaller than that of the non-passivated one at all take-off angles. The S passivation layer appears to suppress the underlying Sn atoms from segregating to the surface and from further oxidation during ALD. The good integrity of high-*k* dielectric/GeSn interface maintained by sulfur passivation through the prevention of Sn out-diffusion and interfacial oxidation may help to improve the carrier transport characteristics in transistors.

3.3. Extraction of interface trap density

In order to extract the D_{it} of HfO₂/Ge_{0.83}Sn_{0.17} interfaces with and without sulfur passivation, Ge_{0.83}Sn_{0.17} MOS capacitors (MOSCAPs) with 4 nm-thick HfO₂ were fabricated. TaN and Al were deposited as the front gate and backside metals by reactive sputtering, respectively. Low temperature *C*-*V* measurement with frequencies ranging from 10 kHz to 1 MHz was performed on the Ge_{0.83}Sn_{0.17} capacitors. D_{it} was extracted using the conductance method [51]. At a particular gate bias, the peak of the G_p/ω versus frequency curve can be obtained at one sweeping frequency and is referring to the maximum of per-cycle energy loss. The per-cycle energy loss is due to charge trapping and detrapping at certain oxide-semiconductor

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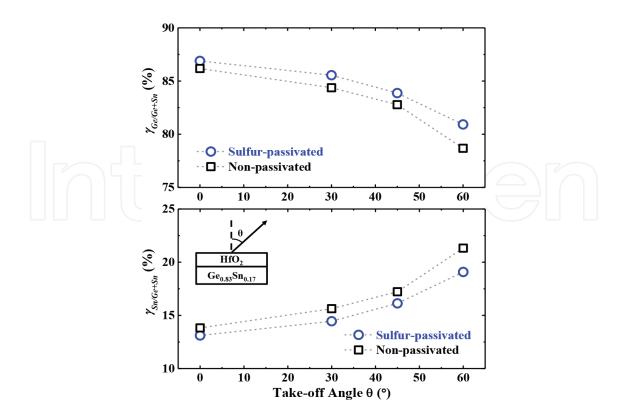


Figure 9. The Ge and Sn atomic concentrations at surface region of $Ge_{0.83}Sn_{0.17}$ as a function of photoelectron take-off angle θ , as determined by angle-resolved XPS.

interface and its maximum occurs when the energy level of the trap states is aligned with the semiconductor surface Fermi-level. The value of D_{it} can be extracted using the following equation:

$$D_{it} = 2.5 \cdot \frac{\left(G_{p}/\omega\right)_{max}}{qA},\tag{7}$$

where $(G_p/\omega)_{max}$ is the peak energy loss value, q is the electronic charge, and A is the area of capacitor. The band-gap of fully compressively strained $\text{Ge}_{0.83}\text{Sn}_{0.17}$ on Ge (100) substrate is ~0.45 eV [52]. D_{it} values from the valence band edge to the midgap of GeSn for both sulfur-passivated and non-passivated GeSn capacitors are extracted and plotted as a function of energy in the GeSn band-gap as shown in **Figure 10**. For the sample with sulfur passivation, D_{it} of $10^{13} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ was obtained at $E \cdot E_v$ of 0.13 eV. This is much smaller as compared with the non-passivated sample which has D_{it} of $6 \times 10^{13} \text{ cm}^{-2} \cdot \text{eV}^{-1}$. In addition, sulfur passivation also leads to significant reduction in D_{it} near the valence band edge. Sulfur passivation suppresses Ge and Sn oxide formation and Sn out-diffusion, leading to the reduction of D_{it} . As a result, S of the sulfur-passivated GeSn p-MOSFETs is improved as compared with the non-passivated sample. In terms of the Ge_{0.83}Sn_{0.17} p-MOSFETs, high density interface traps near the valence band edge can be charged when the device is biased to strong inversion, and degrade the effective hole mobility. In order to further improve the effective hole mobility of the Ge_{0.83}Sn_{0.17} p-MOSFETs, further optimization and significant improvement are needed to reduce the D_{it} near the valence band for the high-k/GeSn gate stack.

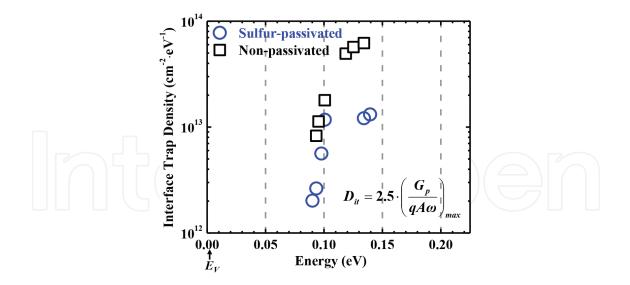


Figure 10. D_{it} distribution from valence band edge to the midgap of GeSn as a function of energy. The sulfur-passivated GeSn sample demonstrates reduced midgap D_{it} as compared to the non-passivated control.

3.4. Electrical characterization of Ge_{0.83}Sn_{0.17} p-MOSFETs

 $I_{DS} - V_{GS}$ curves of Ge_{0.83}Sn_{0.17} p-MOSFETs with and without sulfur passivation are shown in Figure 11(a). The blue circles represent the sulfur-passivated sample and the black circles are the data points of the non-passivated one. Both devices have L_G of 4 µm and gate width W_G of 100 µm. The sulfur-passivated GeSn p-MOSFET exhibits *S* of 100 mV/decade. This is also the smallest reported *S* for any GeSn p-MOSFETs (non-passivated control shows *S* of 118 mV/decade). Figure 11(b) shows the output characteristics of the same devices in Figure 11(a). 10% on-state current enhancement was demonstrated by sulfur-passivated Ge_{0.83}Sn_{0.17} p-MOSFET as compared to non-passivated control. Drive current of 32 µA/µm was achieved at a gate over drive of −1.0 V and V_{DS} of −1.0 V by the sulfur-passivated device. Table 1 benchmarks *S* of the sulfur-passivated Ge_{0.83}Sn_{0.17} p-MOSFETs reported using various

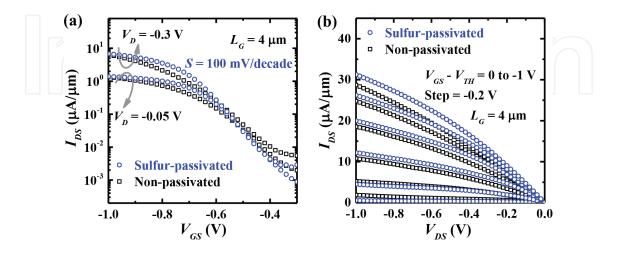


Figure 11. (a) $I_{DS} - V_{GS}$ curves of the sulfur-passivated $Ge_{0.83}Sn_{0.17}$ p-MOSFET show *S* of 100 mV/decade and I_{ON}/I_{OFF} ratio of more than 3 orders of magnitude. *S* of the sulfur-passivated sample is smaller than that of the non-passivated one. (b) $I_{DS} - V_{DS}$ curves of the same devices in (a).

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Work	Passivation Technique	Sn composition (%)	S value
[12]	Si passivation	5.3	250
[15]	Sulfur passivation	4.2	220
[53]	Si passivation	3	113
[13]	No passivation	3	250
[16]	Si passivation	-4.2	135
[17]	Si passivation	3	158
[14]	Si passivation	8	198
[18]	Ge capping	9	160
This work	Sulfur passivation	17	100

Table 1. S values of GeSn p-MOSFETs with different Sn compositions and passivation techniques.

passivation techniques [12–18, 53]. Despite the highest Sn composition, the Ge_{0.83}Sn_{0.17} p-MOSFET realized in this work shows the smallest *S* as compared with the other GeSn p-MOSFETs. This could be attributed to the relative low D_{it} at the mid-gap ($3.4 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$) as compared with the other passivation techniques (7–9 × 10¹² cm⁻² eV⁻¹) [17]. This indicates the high quality of the Ge_{0.83}Sn_{0.17} film grown by MBE which was maintained throughout the fabrication process using low processing temperatures, as well as the Ge and Sn oxides formation between Ge_{0.83}Sn_{0.17} and high-*k* dielectric enabled by sulfur passivation. However, the D_{it} value near the valence band is still high (~1 × 10¹³ cm⁻² eV⁻¹) as shown in the D_{it} plot in **Figure 10**. This may degrade the effective hole mobility which will be discussed in the following sections.

Figure 12 shows the capacitance *C* as a function of gate voltage V_{GS} for the sulfur-passivated $Ge_{0.83}Sn_{0.17}$ p-MOSFET ($L_G = 8 \mu m$, $W_G = 100 \mu m$) measured at frequency of 50 kHz, 100 kHz, and 1 MHz. The schematic in the inset illustrates the configuration for *C-V* measurement. A quantum-mechanical *C-V* simulator [54] was used to fit the measured inversion *C-V* curve at 100 kHz and the simulated data were plotted using solid line in **Figure 12**. In the *C-V* simulator, the *C-V* characteristics are obtained through the calculation of hole and electron distributions by solving Schrödinger's and Poisson's equations self-consistently with the Fermi-Dirac distribution. In the simulation, the heavy hole effective mass of 0.27 m₀ and light hole effective mass of 0.025 m₀ (m₀ is the free electron mass) were used for $Ge_{0.83}Sn_{0.17}$ channel [11]. From the simulated *C-V* curve, the equivalent oxide thickness (EOT) is extracted to be 7.5 Å. **Figure 13** shows the forward and backward inversion *C-V* sweeps of one $Ge_{0.83}Sn_{0.17}$ p-MOSFET ($L_G = 8 \mu m$, $W_G = 100 \mu m$) measured at a frequency of 100 kHz. The hysteresis is small, which indicates good dielectric quality with low density of oxide traps.

The $G_{m,int}$ curves versus V_{GS} at V_{DS} of -0.05 V for both sulfur-passivated and non-passivated devices are shown in **Figure 14**. L_G is 4 µm. $G_{m,int}$ is extracted using:

$$G_{m,int} = \frac{G_{m,ext}}{1 - 0.5 \cdot R_{SD} \cdot G_{m,ext}},$$
(8)

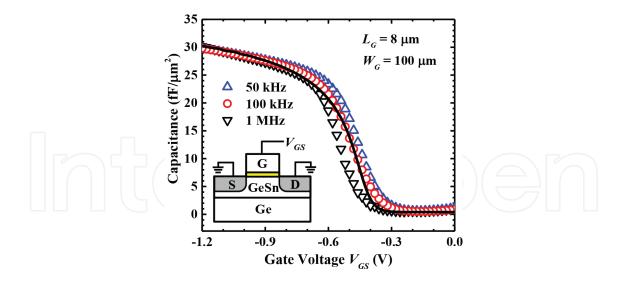


Figure 12. *C* vs. V_{GS} plot of a sulfur-passivated $Ge_{0.83}Sn_{0.17}$ p-MOSFET measured at frequency of 50 kHz, 100 kHz, and 1 MHz. The measured data points are plotted as symbols. The solid curve is obtained using a quantum-mechanical *C-V* simulator to fit 100 kHz *C-V* curve. The inset shows the *C-V* measurement configuration.

where $G_{m,ext}$ is the measured extrinsic transconductance and R_{SD} is the source/drain resistance. Higher peak $G_{m,int}$ was achieved in sulfur-passivated $\text{Ge}_{0.83}\text{Sn}_{0.17}$ p-MOSFET as compared with that of the non-passivated control. Improvement in $G_{m,int}$ is attributed to better HfO₂/GeSn interface achieved using sulfur passivation.

The μ_{eff} of Ge_{0.83}Sn_{0.17} p-MOSFETs with and without sulfur passivation is extracted using the split *C*-*V* method:

$$\mu_{eff} = \frac{1}{W_{c} Q_{inv} \frac{\Delta R_{Total}}{\Delta L_{c}}}$$
(9)

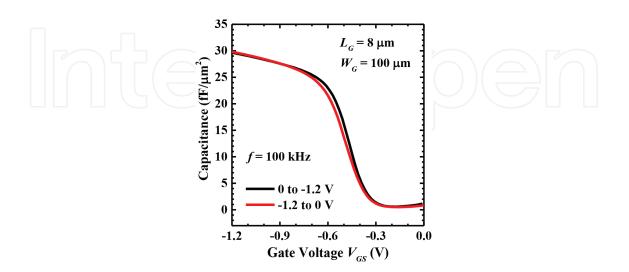


Figure 13. Forward and backward inversion *C-V* sweeps at 100 kHz for one $Ge_{0.83}Sn_{0.17}$ p-MOSFET with a L_G of 8 µm. The hysteresis is small.

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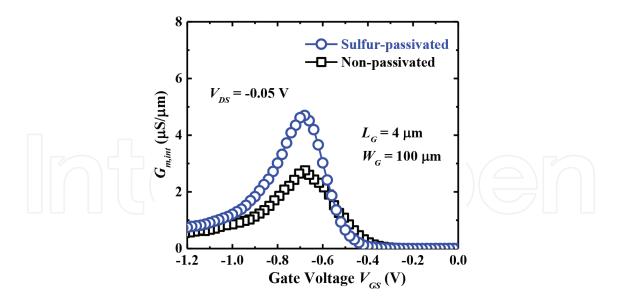


Figure 14. Intrinsic transconductance $G_{m,int}$ vs. V_{GS} characteristics for $\text{Ge}_{0.83}\text{Sn}_{0.17}$ p-MOSFETs with and without sulfur passivation at V_{DS} = -0.05 V. The L_G of the device is 4 µm and W_G is 100 µm.

where Q_{inv} is the inversion charge density in the GeSn channel, and $\Delta R_{Total}/\Delta L_G$ is the slope of total resistance (R_{Total}) versus L_G . Q_{inv} can be obtained by integrating the measured inversion *C*-*V* curve as shown in **Figure 12**. Using this approach, the impact of R_{SD} on extraction of hole mobility is taken out. **Figure 15** shows the extracted μ_{eff} versus the inversion carrier density (N_{inv}) for both the sulfur-passivated and non-passivated Ge_{0.83}Sn_{0.17} p-MOSFETs. The sulfur-passivated Ge_{0.83}Sn_{0.17} p-MOSFET shows a peak hole mobility of 478 cm²/V·s at N_{inv} of ~2 × 10¹² cm⁻². At N_{inv} of 1 × 10¹³ cm⁻², 25% higher hole mobility is achieved by the sulfur-passivated Ge_{0.83}Sn_{0.17} p-MOSFET as compared with the non-passivated one. This is consistent with the peak intrinsic transconductance results shown in **Figure 14**.

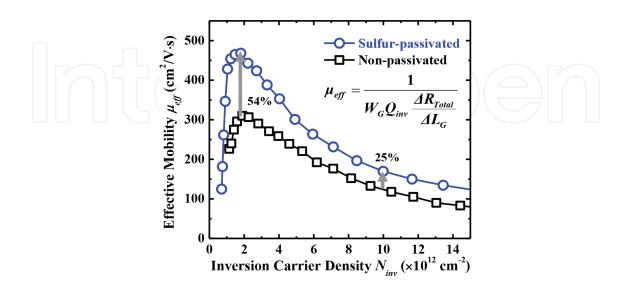


Figure 15. μ_{eff} vs. N_{inv} for Ge_{0.83}Sn_{0.17} p-MOSFETs with and without sulfur passivation. The impact of R_{SD} on μ_{eff} extraction was taken out using the inset equation through the total resistance slope method.

4. Conclusion

Sulfur passivation and low temperature process modules are developed and used in the fabrication of Ge_{0.83}Sn_{0.17} p-MOSFET. Reduction in *S* and improvement in peak $G_{m,int}$ and μ_{eff} are observed for the sulfur-passivated Ge_{0.83}Sn_{0.17} p-MOSFETs as compared with the non-passivated control. This is attributed to the effective suppression of Ge and Sn oxides formation, and suppression of Sn surface segregation by sulfur passivation. In addition, the effect of sulfur passivation on D_{it} reduction is also investigated. It is observed that sulfur passivation reduces the D_{it} from the valence band edge to midgap of GeSn. As a result, the lowest *S* of 100 mV/ decade is achieved by the sulfur-passivated Ge_{0.83}Sn_{0.17} p-MOSFETs. D_{it} level of 10^{13} cm⁻² eV⁻¹ in the sulfur-passivated sample is still very high. Further improvement to significantly reduce D_{it} is needed to increase the hole mobility.

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