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# Low Power Design Methodology

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Additional information is available at the end of the chapter

<http://dx.doi.org/10.5772/intechopen.73729>

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## Abstract

Due to widespread application of portable electronic devices and the evaluation of micro-electronic technology, power dissipation has become a critical parameter in low power VLSI circuit designs. In emerging VLSI technology, the circuit complexity and high speed imply significant increase in the power consumption. In low power CMOS VLSI circuits, the energy dissipation is caused by charging and discharging of internal node capacitances due to transition activity, which is one of the major factors that also affect the dynamic power dissipation. The reduction in power, area and the improvement of speed require optimization at all levels of design procedures. Here various design methodologies are discussed to achieve our required low power design concepts.

**Keywords:** power modeling, switching activity, self-transition, coupling transition, low power dissipation, VLSI

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## 1. Introduction

As VLSI technology advances, the complexity and speed circuit increase, resulting in high power consumption. In VLSI design, small area and high performance are two conflicting constraints. The integrated circuit (IC) designer's activities have been involved in trading of these constraints. There are many possible design considerations, due to which the power efficiency has become important. The most portable systems used in recent era, which are powered by batteries, are performing tasks requiring lots of computations. The most important aspect of Moore's Law is that it has become a universal predictor for the growth of the entire semiconductor industry. From Moore's law, it is understood that the number of devices in a chip doubles every 18 months. This will increase the number of transistors used and hence increase the area and power consumption of the circuit (**Figure 1**).

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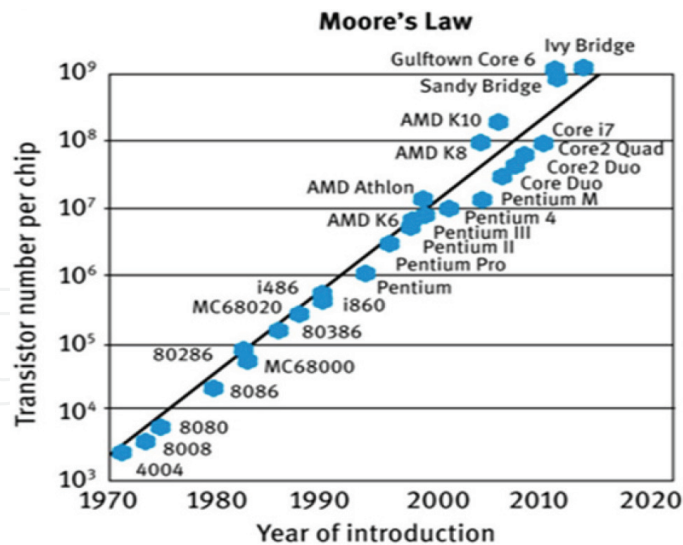


Figure 1. Graphical representation of Moore’s law.

1.1. Need for low power design

Power dissipation is the main constraint when it comes to portability. Hence, it is necessary to take care of the system’s total power consumption. Minimizing the overall power consumption in such devices is essential because it is advantageous to exploit the run time with least possible requirements on weight, battery life and size owed to batteries. Therefore, in portable devices, ‘the low power design is the most decisive factor to think while designing system on chip. Normally, mobile users demand additional features and prolonged battery life at a lower cost. Almost 70% of users look for longer talk time and standby time as key feature for mobile phones. One of the top operator requirements in 4G is Power efficiency. Customers always look for smaller, trim and graceful mobile devices. This is the need of high levels of silicon integration in modern processes, but sophisticated processes have intrinsically higher power indulgence. So, design is very important in low power consumption devices.

1.2. Impact of power dissipation

Whenever there is power dissipation, it unvaryingly leads to an increase in chip temperature. This temperature rise affects devices when it is switched on and off. With device in OFF condition, power dissipation increases the number of intrinsic carriers  $n_i$  provided by the below relation:

$$n_i \propto e^{-E_G / V_T} \tag{1}$$

From the above equation, it is very clear that when temperature increases, intrinsic carriers also increase. With temperature increase, the less affected ones are the majority carriers which are contributed by impurity atoms. As the temperature increases further, the leakage current that depends on the concentration of the minority carrier, increases which leads to further increase in temperature. Ultimately, the device might break down, if the dissipated heat is not removed properly. An ON device will not be affected much by the increase of

minority carrier, but will be affected by the threshold voltage ( $V_T$ ) and mobility ( $\mu$ ). These parameters decrease with increase in temperature and this leads to change in drain current ( $I_D$ ). Hence the device performance might not meet the required specifications. Also, power dissipation is more critical in battery-powered applications as the greater power dissipated, the battery life will be less.

### 1.3. Reduction of temperature

Heat sinks are used to dissipate heat generated by power dissipation. The thermal resistance of heat sink is lower than that of the package. So heat sink draws the heat. To eliminate heat efficiently, the rate of heat transferred to the environment should be greater than heat generated. This heat transfer rate depends on thermal resistance  $\theta$ , as provided by the below relation:

$$\Theta = l / \sigma_c A \quad (2)$$

where:

$l$  is the length,  $A$  is the area and  $\sigma_c$  is the thermal conductivity of the heat sink.

From the above relation, it can be seen that large  $\sigma_c$  implies smaller  $\theta$ .  $\theta$  is also given by the relation

$$\Theta = \delta T / \delta P \quad (3)$$

Using this relation, we can see that for a given power dissipation,  $P_D$

$$\Theta \leq (T_j - T_a) / P_D \quad (4)$$

where  $T_j$  is the junction temperature and  $T_a$  is the ambient temperature.

Heat sink materials are generally coated black to radiate more energy.

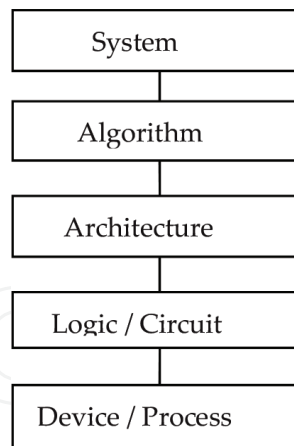
### 1.4. Low power design methodology

Historically, VLSI designers have used circuit speed as the performance metric. In fact, power considerations have been the ultimate design criteria in special portable applications. The main aim of these applications was maximum battery life time, with minimum power. Low power design is also required to reduce the power in high-end systems with huge integration density and thus improve the speed of operation.

To optimize power dissipation specifically with low power methodology in digital systems, the method should be applied all over the design from system to process level. It is very important to have knowledge about the power distribution. So the blocks or parts consuming fraction of power could be clearly optimized for saving power. Different design levels specifically of power reduction are shown in **Figure 2**.

#### 1.4.1. Power reduction through process technology

Minimizing the supply voltage of a device is one of the best solutions to reduce power dissipation. The trade-off of this approach is that delay may increase significantly, when  $V_{DD}$



**Figure 2.** Power reduction design aspects.

approaches the threshold voltage. So devices must be properly scaled to overcome this problem. The advantages of scaling are:

- Improve the device characteristics
- Reduce the geometric and junction capacitances
- Enhanced interconnect technology
- High density of integration

#### *1.4.2. Power reduction through circuit/logic design*

- Use of more static than dynamic circuits
- Reduce switching activity by optimized algorithm
- Optimize clock and bus loading
- Smart circuit techniques which minimizes no of devices used in the circuit
- Custom design may improve the power
- Reduces VDD in non-critical paths and proper transistor sizing
- Use of multi-VT circuits
- Re-encoding of sequential circuits

#### *1.4.3. Power reduction through architectural model*

- Techniques for power management like shut down of unused blocks
- Architectures based on pipelining, parallelism etc.,
- Memory partitioning by enabling selective blocks
- Reduction in the numbers of global busses
- Instruction set minimization for easier decoding and execution

#### 1.4.4. Power reduction by algorithm level

- Minimizing the number of operation and hence reduce the number of hardware resources
- Data coding for reduce the switching activity.

#### 1.4.5. Power reduction through system integration

- Utilize low system clocks
- Use high level of integration

### 1.5. Power modelling

Numerous power components and their outcome must be identified to reduce power consumption of certain circuit. Out of two power dissipation types, the maximum power dissipation relates to peak instantaneous current and the second type is average power dissipation. Due to power line resistance, peak current affects the noise in supply voltage. This causes heating of device and hence results in performance degradation. With a view on battery life time, this average power dissipation becomes more important. The three important power dissipation components are [1]

- Static power due to leakage current  $I_{Leak}$  and other static component  $I_{St}$  due to the value of the input voltage
- Dynamic power caused by the total output capacitance  $C_L$  and short circuit current  $I_{SC}$  during the switching transient
- Short circuit power dissipation

Thus the total power dissipation  $P_T$  is

$$P_T = P_S + P_D + P_{SC}$$

#### 1.5.1. Static power dissipation

Static power dissipation is the power consumed during the standby mode of a design. CMOS gates typically have some amount of sub-threshold leakage current even when gates are not turned on. The drain to source leakage current is the main component of static power consumption. The leakage power is a very small part of the overall power consumption. In a typical chip 10% of the power consumed is leakage and 90% is dynamic power. So, clearly the major concern is dynamic power dissipation. **Figure 3** shows static power calculation model.

$$\text{Instantaneous power } P(t) = i_{DD}(t)V_{DD} \quad (5)$$

$$\text{Energy } E = \int_0^T p(t)dt \quad (6)$$

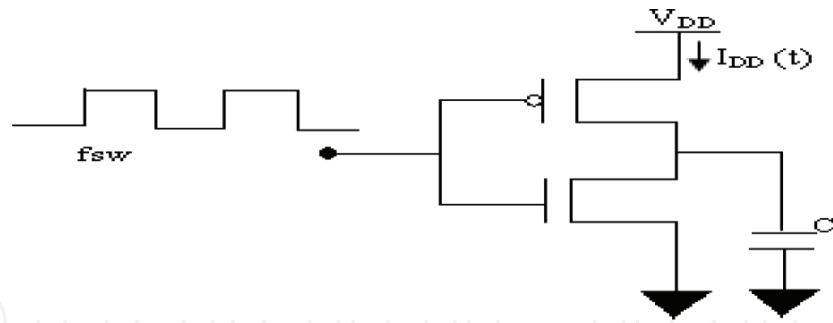


Figure 3. Static power calculation model.

$$E = \int_0^T i_{DD}(t) V_{DD} dt \quad (7)$$

$$\text{Static power } P_S = E/T \quad (8)$$

$$P_S = 1/T \int_0^T i_{DD}(t) V_{DD} dt \quad (9)$$

### 1.5.2. Dynamic power dissipation

A dynamic power vector describes an event in which power is dissipated due to a signal switching at the cell input during charging and discharging of load capacitance. Dynamic power is further divided into switching power and internal power.

- Switching power

Switching power is dissipated when the load capacitance at the output of the cell is being charged or discharged. The load capacitance is composed of interconnect capacitance and gate capacitances. Switching activity of cells depend on the quantity of switching power. On the cell output, if there are huge logic transitions, then switching power surges.

- Internal power

Within a cell, internal power is specifically consumed for charging and discharging cell capacitances. When logical transitions occur, Pmos and Nmos transistors are ON at the same time for a short period. This causes a connection between Vdd and ground rails.

The power dissipation can be estimated by the load capacitance  $C_L$ . This power loss is due to the charging and discharging of load capacitance  $C_L$  [1]. The average dynamic power  $P_D$  is required to charge and discharge a capacitance  $C_L$  at a switching frequency  $f_{sw}$  and equivalent dynamic power calculation model is shown in **Figure 4**.

$$P_D = f_{sw} \int_0^T i_o(t) V_o(t) dt \quad (10)$$

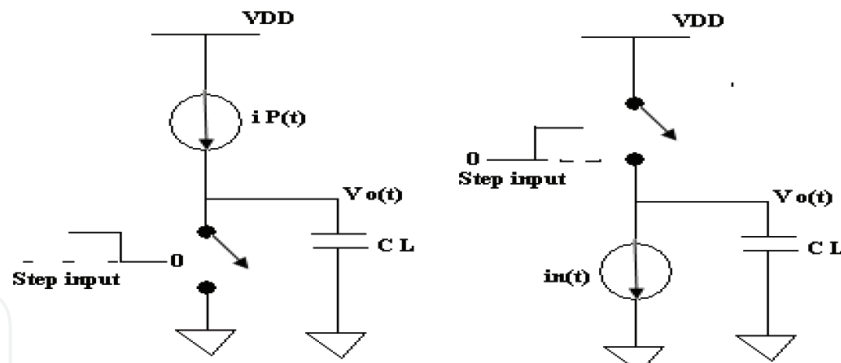


Figure 4. Equivalent circuits for dynamic power calculation.

During charging cycle

$$i_p = C_L \cdot \frac{dV_o}{dt} \quad (11)$$

During the discharge cycle

$$i_n = -C_L \cdot \frac{dV_o(t)}{dt} \quad (12)$$

$$P_D = f_{sw} \left[ \int_0^{V_{DD}} C_L V_o dV_o - \int_{V_{DD}}^0 C_L V_o dV_o \right] \quad (13)$$

$$P_D = f_{sw} \left[ C_L \left[ \left[ \frac{V_o^2}{2} \right]_0^{V_{DD}} - \left[ \frac{V_o^2}{2} \right]_{V_{DD}}^0 \right] \right] \quad (14)$$

$$P_D = f_{sw} \left[ C_L \left[ \frac{V_{DD}^2}{2} + \frac{V_{DD}^2}{2} \right] \right] \quad (15)$$

$$P_D = f_{sw} C_L V_{DD}^2 \quad (16)$$

Assuming a logic gate goes through one complete charge/discharge cycle for every clock cycle, suppose the system clock frequency is  $f$ .

Let  $f_{sw} = E f$ , where  $E$  is the energy transition activity factor.

Most gates do not switch every clock cycle,

$$P_D = E C_L V_{DD}^2 f \quad (17)$$

A clock has  $E = 1$  because it rises and fall every cycle, but most data have a maximum energy transition activity factor  $E = 0.5$  because they transit only once every cycle.

The dynamic component of power consumption arises when the capacitive load  $C_L$  of a CMOS circuit is charged through PMOS transitions to make a voltage transition from 0 to 1, half of which is stored in the output capacitor and half is dissipated in the PMOS device [2]. No



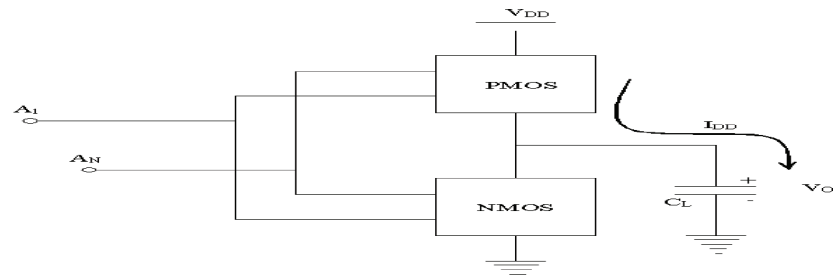


Figure 5. Energy per transition.

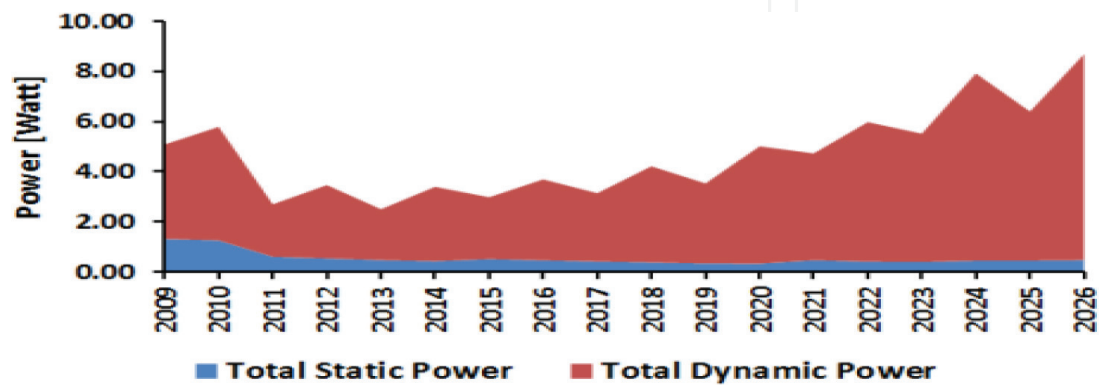


Figure 6. Power analysis chart, IRTS-2011.

charge is drawn from the  $V_{DD}$  during the 1 to 0 transition at the output. But the energy stored in the capacitor is dissipated in the pull-down NMOS device shown in **Figure 5**. The main cause of energy dissipation in CMOS circuits is due to charging and discharging of the node capacitances. The power analysis chart is also shown in **Figure 6**.

### 1.6. Short circuit power dissipation

Short circuit current occurs during signal transitions when both the NMOS and PMOS are ON and there is a direct path between  $V_{dd}$  and GND. Also called crowbar current, the total power dissipation is more than 20% of total power. As clock frequency increases, transitions increases and consequently short circuit power dissipation increases. It can be reduced by

- faster input and slower output
- $V_{dd} \leq V_{tn} + |V_{tp}|$

So both NMOS and PMOS are not ON at the same time.

The short-circuit power dissipation is given by

$$P_D = I_{\text{mean}} * V_{DD} \tag{18}$$

For the input waveform shown in **Figure 8**, which depicts the short circuit in an unloaded inverter,

$$I_{sc} = 2x \frac{2}{T} \int_{t_1}^{t_2} \frac{\beta}{2} (V_{in}(t) - V_t)^2 dt \quad (19)$$

assuming that  $V_{tn} = -V_{tp}$  and  $\beta_n = \beta_p$  and that the behaviour is symmetrical around  $t_2$ .

$$I_{sc} = 2x \frac{2}{T} \int_{t_1}^{t_2} \frac{\beta}{2} (V_{in}(t) - V_t)^2 dt \quad (20)$$

With

$$V_{in}(t) = \frac{V_{DD}}{t_r} t \quad (21)$$

$$t_1 = \frac{V_t}{V_{DD}} t_r \quad (22)$$

$$t_2 = \frac{t_r}{2} \quad (23)$$

$$t_r = t_f = (t_{tr}) \quad (24)$$

Assuming an inverter without load,

$$P_{sc} = \frac{\beta}{2} (V_{DD} - 2V_t)^2 \frac{t_r}{t_p} \quad (25)$$

where  $t_p$  is the period of the waveform.

The equation suggests that, depending on the input rise and fall times and  $\beta$ , the short circuit current varies. For load inverters, on nodes, slow rise times significantly reduces (20%) SC power dissipation. If power dissipation is a concern, then it is good if all the edges are kept fast. Further increase in load capacitance significantly reduces the short circuit dissipation by reduced capacitive dissipation  $P_D$ .

### 1.7. Transition activity

The internal power and the capacitive load power are the two key components for dynamic power dissipation in a complex design, like the internal node. The power in an internal node is determined by the amount of the power dissipated by the internal capacitive nodes [3]. Sometimes, internal node short circuit power is also included in the node to calculate the dynamic power at the internal node. So the dynamic power cannot be calculated by the simple equation  $C_L V_{DD}^2 f$  because MOS devices might not switch when the clock is switching. The transition activity determines how often this transition occurs on a power. Considering capacitive node for  $N$  periods of time  $0 \rightarrow 1$  and  $1 \rightarrow 0$  transitions will occur. The transition activity  $E$  determines how many low to high and high to low transitions occur at the output [4]. In other words, the activity  $E$  represents the probability that a transition  $0 \rightarrow 1$  will occur during the period  $T = 1/f$ . The average dynamic power of a complex design due to the output load capacitance is given by

$$P_D = E C_L V_{DD}^2 f \quad (26)$$

The internal power dissipation, due to internal nodes, the internal dynamic power of a cell is given by

$$P_{\text{int-dyn}} = \sum_{i=1}^{\infty} E_i C_i V_i V_{DD} f \quad (27)$$

Due to charging and discharging the data changed from 1 to 0 or from 0 to 1 vice versa between adjacent bus wires or on the same bus wire. This is classified into two types:

- Self-transition
- Coupling transition

#### 1.7.1. Self-transition

A Self-transition (ST) is defined as a transition from  $0 \rightarrow 1$  or  $1 \rightarrow 0$  on bus with reference to the previous data on it [5]. Energy transition analysis is shown in **Table 1**.



#### 1.7.2. Coupling transition

A coupling transition (CT) is defined as a transition from  $0 \rightarrow 1$  or  $1 \rightarrow 0$ , between two adjacent bus wires [5]. The corresponding energy transition analysis is shown in **Table 2**.



### 1.8. Design parameter

The low power design work mainly focuses on estimating the dynamic power dissipation. In the past, the major concern of the designer was about area, speed and cost. The secondary importance was provided for power considerations. In recent years, power has become as the primary

Transition of bits	State	Energy stored initially	Energy stored finally	Energy dissipated	Energy consumed
$0 \rightarrow 1$	charge	0	$E_S/2$	$E_S/2$	$E_S$
$1 \rightarrow 0$	discharge	$E_S/2$	0	$E_S/2$	0

**Table 1.** Energy transition analysis for self-capacitance, Yan Zhang et al. 2002.

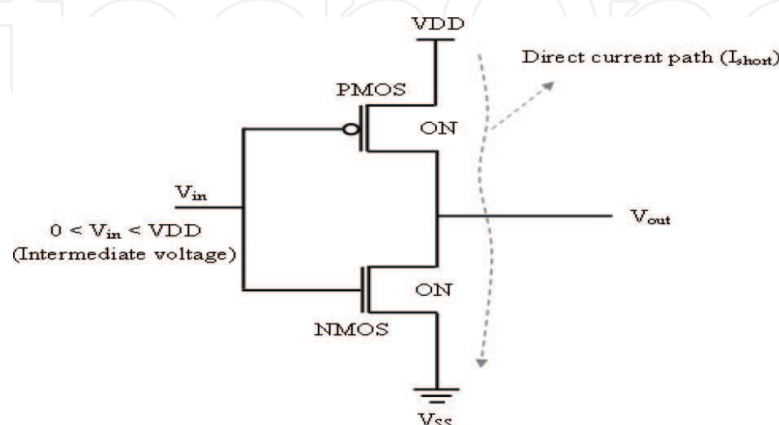
Transition of bits	State	Energy stored initially	Energy stored finally	Energy dissipated	Energy consumed
00 → 00	-	0	0	0	0
00 → 01	charge	0	$E_C/2$	$E_C/2$	$E_C$
00 → 10	charge	0	$E_C/2$	$E_C/2$	$E_C$
00 → 11	-	0	0	0	0
01 → 00	discharge	$E_C/2$	0	$E_C/2$	0
01 → 01	-	0	0	0	0
01 → 10	Toggle	$E_C/2$	$E_C/2$	$2E_C$	$2E_C$
01 → 11	discharge	$E_C/2$	0	$E_C/2$	0
10 → 00	discharge	$E_C/2$	0	$E_C/2$	0
10 → 01	Toggle	$E_C/2$	$E_C/2$	$2E_C$	$2E_C$
10 → 10	-	0	0	0	0
10 → 11	discharge	$E_C/2$	0	$E_C/2$	0
11 → 00	-	0	0	0	0
11 → 01	Charge	0	$E_C/2$	$E_C/2$	$E_C$
11 → 10	Charge	0	$E_C/2$	$E_C/2$	$E_C$
11 → 11	-	0	0	0	0

**Table 2.** Energy transition analysis for coupling capacitance, Yan Zhang et al. 2002.

design consideration. Several factors contribute to this trend like the growth of personal computing devices such as portable desktops, audio and video-based multimedia products and wireless communication systems which demand high-speed computation and complex functionality with low power consumption [6]. So there is a strong requirement for power consumption reduction so as to reduce packaging and cooling cost and improve product reliability. When the target is a low power application, a power analyser/estimator ranks the various design aspects, thus helps in selecting the one that is potentially more effective from the power standpoint.

### 1.8.1. Two-dimensional design flow

A top-down two-dimensional ordinary VLSI design approach is illustrated in **Figure 7**. The figure summarizes the flow of steps that are required to follow from a system-level specification to the physical design. The approach is aimed to estimate the design parameters such as the performance optimization and area minimization, as shown in **Figures 8–10**.



**Figure 7.** Short circuit power calculation model.

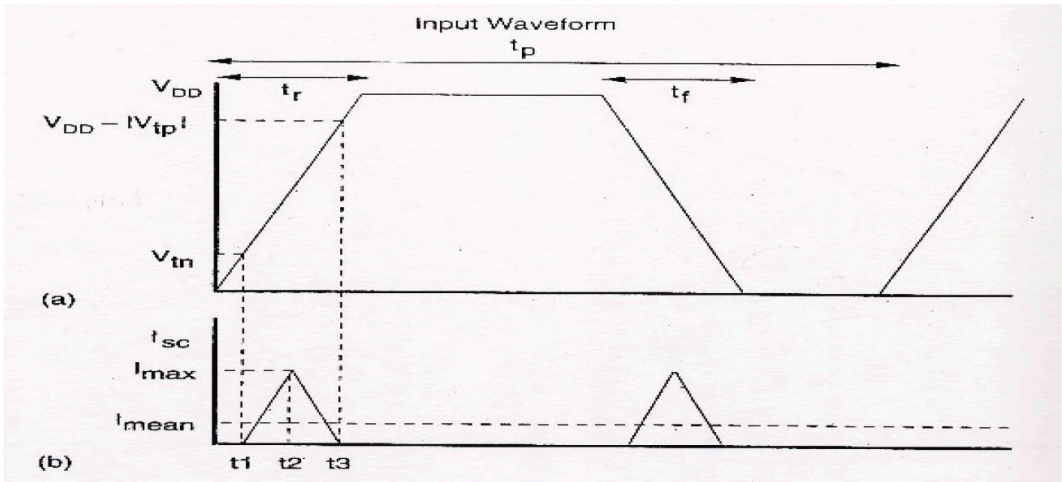


Figure 8. Short circuit behaviour of CMOS inverter without load.

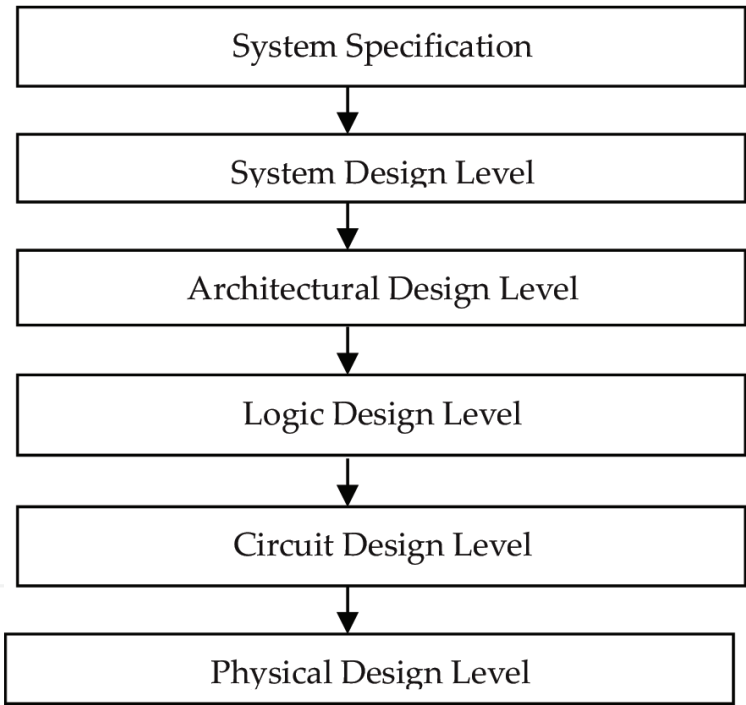


Figure 9. Two-dimensional (2D) VLSI design flow.

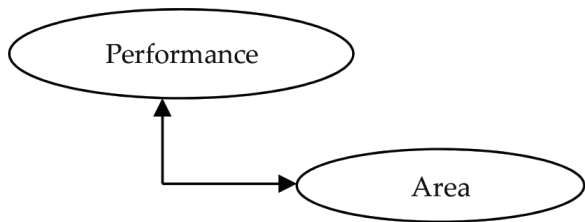
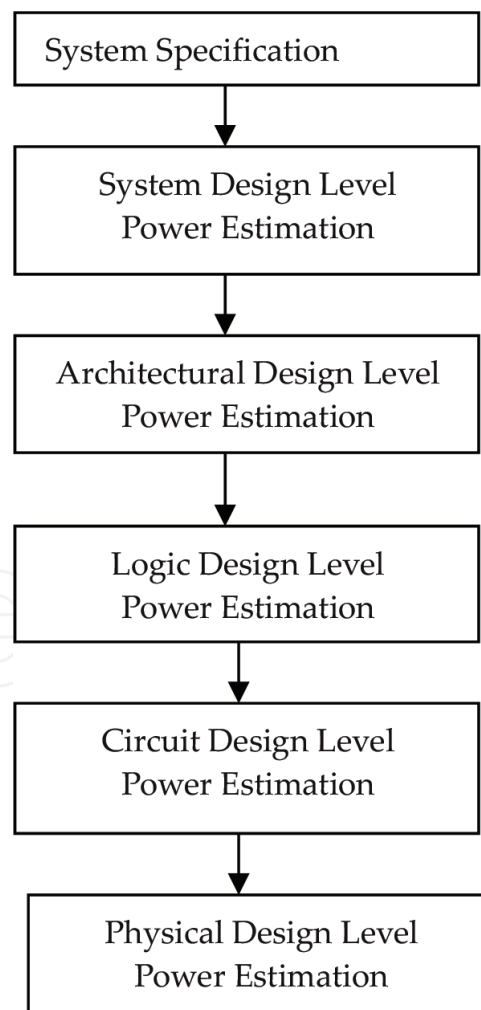


Figure 10. Two-dimensional (2D) design parameter.

### 1.8.2. Three-dimensional design flow

A three-dimensional top-down VLSI design approach is illustrated in **Figure 11**. The figure summarizes the flow of steps that are required to follow from a system-level specification to the physical design. The approach is aimed to estimate the design parameters at performance optimization, area minimization and power optimization shown in **Figure 12**. In each of the design levels, there are two important power factors, namely, power optimization and power estimation. Power optimization is the process of obtaining the best design knowing the design constraints and without violating design specifications. Power estimation is determined as the process of computing power and energy dissipated with a definite percentage of precision and at different stages of design process. This technique also estimates the outcome of several optimization and design alterations on power at different levels of abstraction, as shown in **Figure 12**. Design attains power optimization first and then does power estimation. But for certain design, there is no specific design procedure. Each design might include a lot of low power techniques and thus significantly reduce power dissipation. But certain combination of low power designs can provide better result than certain other combination techniques. Usually



**Figure 11.** Three-dimensional (3D) VLSI design flow.

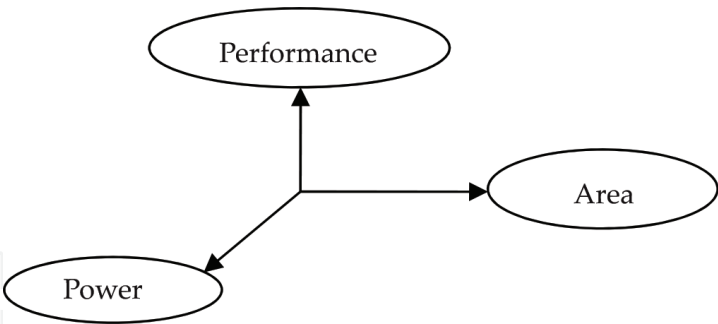


Figure 12. Three-dimensional (3D) design parameter.

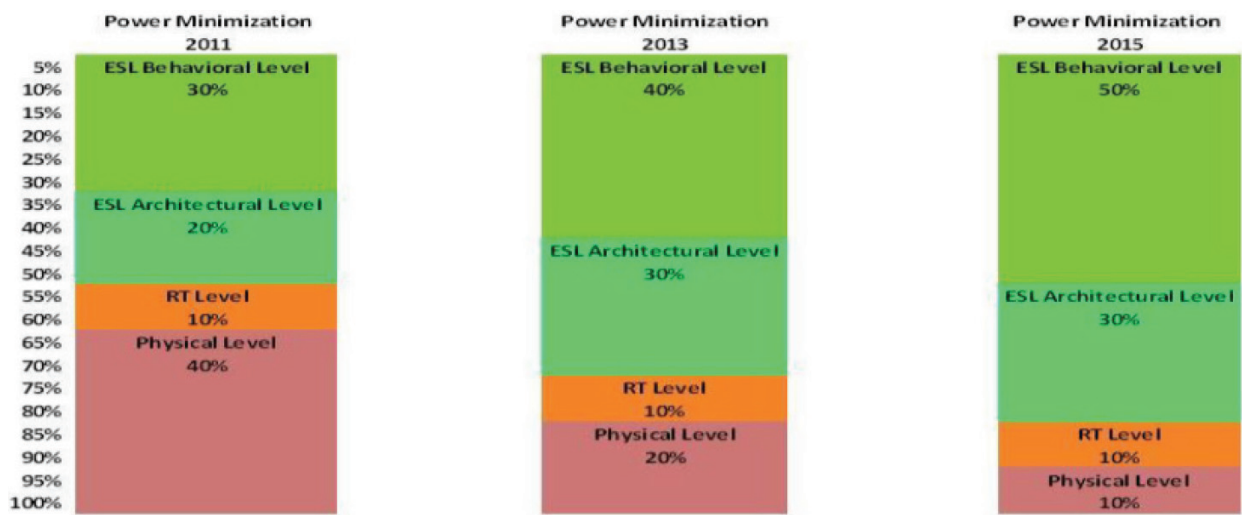


Figure 13. Relationship between different abstraction level and power estimation techniques.

power will be consumed due to transition activities as the capacitors gets charged and discharged. So for higher level systems, power dissipation is preserved by shutdown of system portions when not required and thus the transition activities are reduced (Figure 13).

### 1.9. Power estimation tool

Recently, complexity levels of device size and programmable devices have grown to amazing complexity levels. Years ago, an average design had nearly twelve thousand gates. Presently, there are hundreds of thousands and sometimes multimillion gates. So when size of design increases, power consumption also increases. In the meantime, there is huge demand for battery-powered systems, specifically, handheld devices which are constantly sensitive and smaller to power usage. So it is clearly understood that in programmable logic devices design power consumption cannot be ignored. This chapter deals more on power calculations using Macros and is experimented using power tools. Prior to the power tools, other tools have been used to provide the necessary input to the power tools. More importance is provided to the tools specifically involved in low power estimation, which has been classified as power tools and non-power tools.



### 1.9.1. Non-power tool

Non-power tools include simulation tools, synthesis tools, layout tools, extraction tools and waveform viewers.

### 1.9.2. Power tool

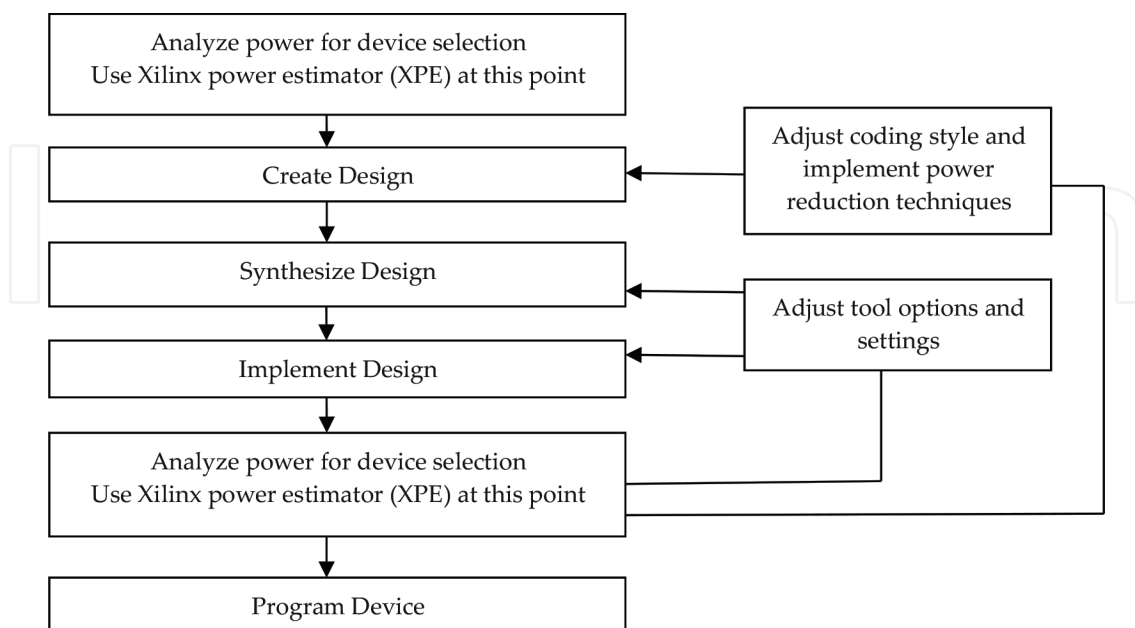
Varieties of power analysis tools are available to estimate the power of a design. Among them are Xilinx, Tanner, Microwind, etc. These EDA power tools are very familiar and user-friendly. The power products are tools that comprise a complete methodology for low power design. Xilinx power tool XPower offers power analysis and optimization throughout the design cycle (from RTL to the gate level). Tanner and Microwind are used for transistor-level analysis. Analysing power early in the design cycle can significantly affect design quality. Design modifications done at RTL level can get good results. Power tools used to calculate power quickly as well as do measurements accurately. The following tools are used to calculate the power at these levels.

- a. Tanner EDA, Microwind: Transistor level
- b. RTL Power Estimator: RTL level
- c. Power Compiler: Gate level.

Power analysis and estimation is available throughout the design process, as shown in **Figure 14**.

- XPower analysis tool

Activity rates are the basis of Xilinx Power tool. They are defined by the rate at which a logic element or net capacitance switches. Activity rates for dynamic calculations are expressed in



**Figure 14.** Power analysis flow chart.



frequency. The activity rate might be relative to clock and hence net or logic element might switch at any fraction of the clock frequency. Thus the main use of activity rate is in the recalculation of power and could be easily achieved by varying system clock frequency. So simulation data could be used, and this saves time. Also Xilinx Power supports several numbers of input clocks. Expressed in percentage scale, 100% activity rate means that standard signal state changes once every clock cycle. Switching rate will be the activity rate if net and logic are not clock sync (Figures 15–22).

- Microwind

This software tool is dedicated to microelectronics and nanotechnology. The microwind software allows the designer to simulate and design an integrated circuit at physical description level. It provides innovative EDA solutions to the analog, digital and mixed-signal IC market. With MOS characteristic viewer, mix signal simulator, in-built layout editing tools, it is easier to complete design process. Microwind unifies netlist extraction, pattern-based simulator, layout compilation, SPICE extraction of schematic, Verilog extractor, schematic entry on layout

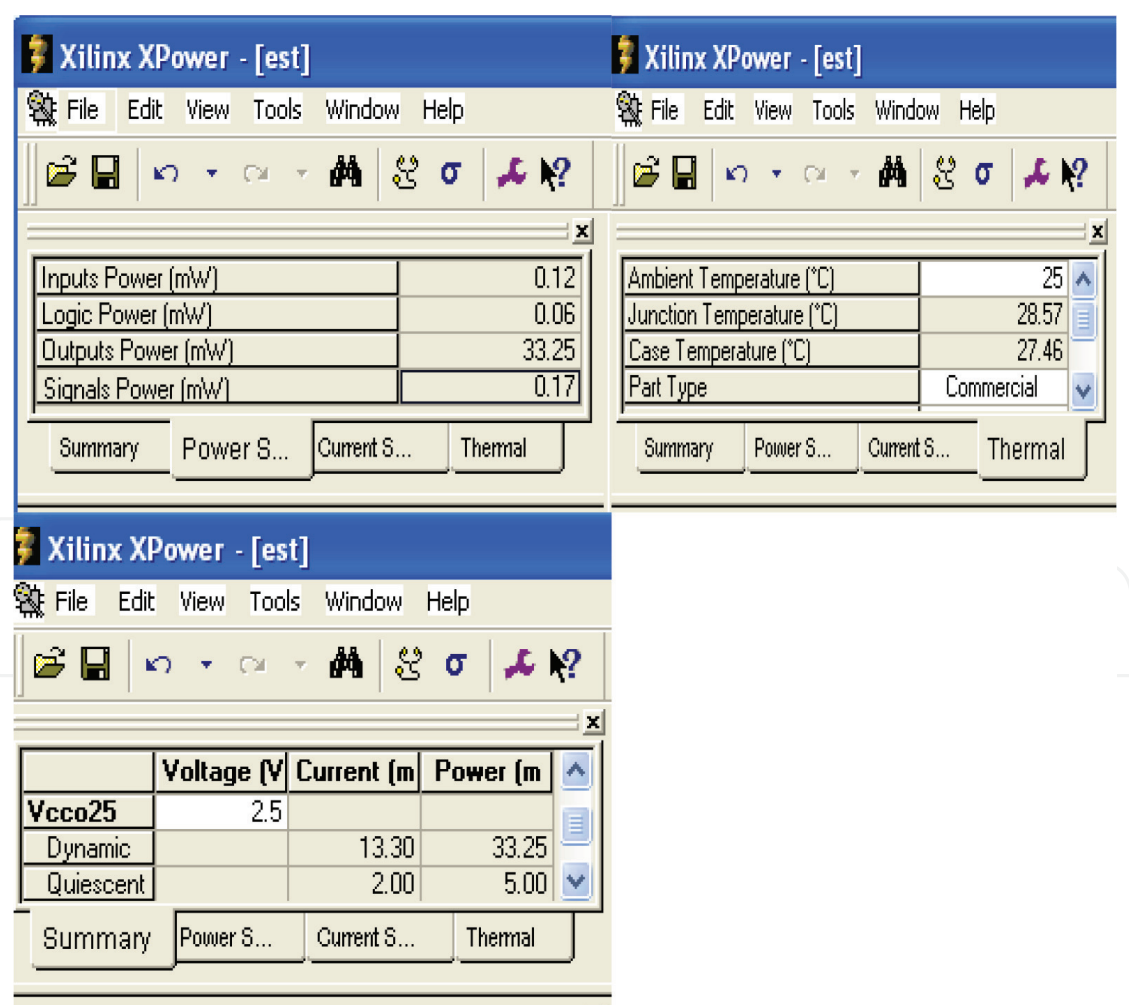


Figure 15. Power output calculation using XPower.

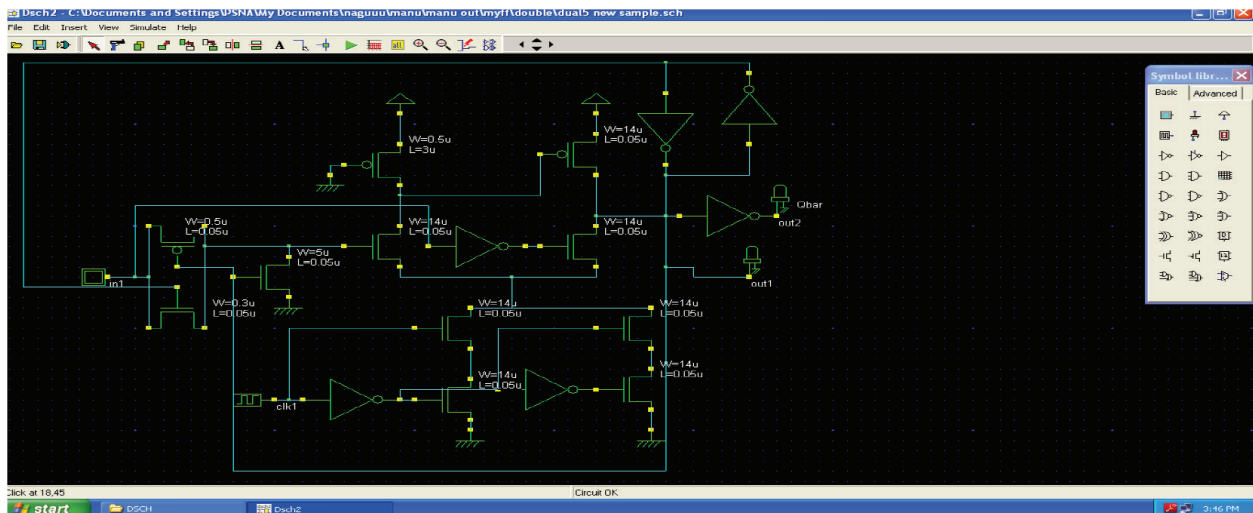


Figure 16. Simulation of digital CMOS circuits.

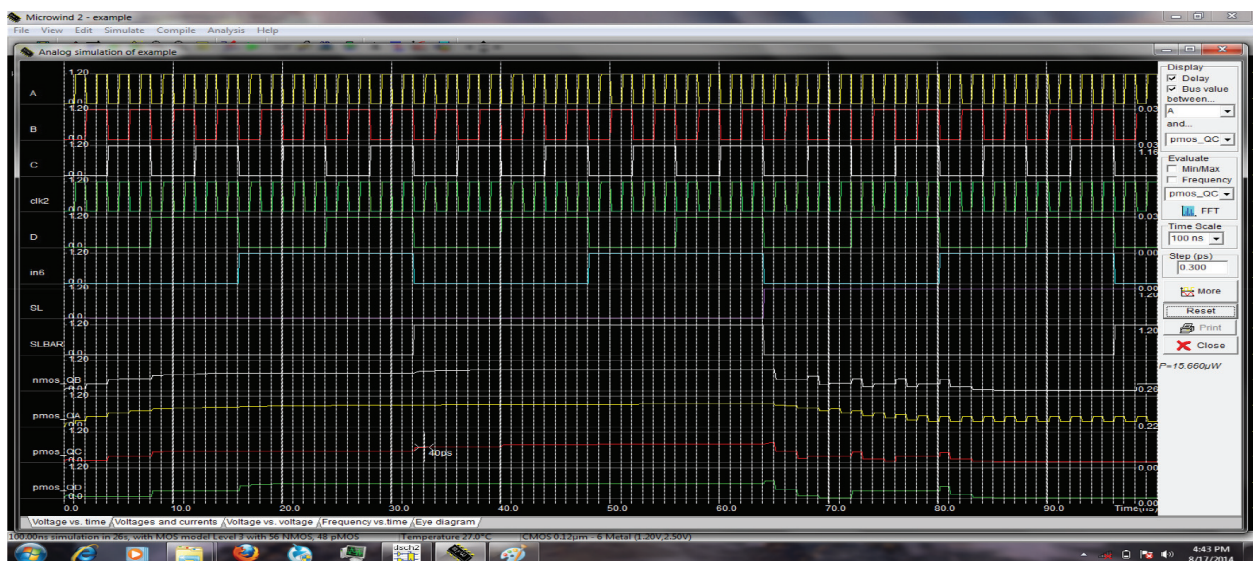


Figure 17. Power calculation of digital CMOS circuits.

mix-signal circuit simulation, sign-off correlation, BSIM4 tutorial on MOS devices, cross-sectional and 3D viewer to deliver matchless architecture productivity and performance.

- Tanner EDA Tool

Tanner tool is a suite of tools to perform spice analysis for analog integrated circuits. Following are the Tanner tool engine machines:

1. Schematic Edit (S-EDIT)
2. Simulation Edit (T-EDIT)
3. Waveforms Edit (W-EDIT)
4. Layout Edit (L-EDIT)

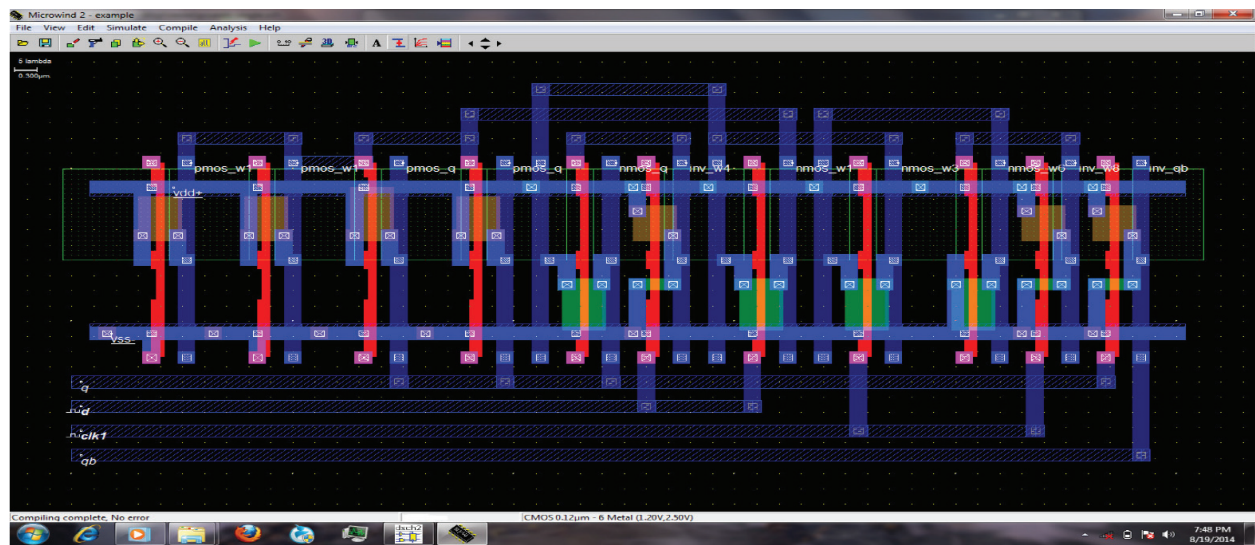


Figure 18. Layout of digital CMOS circuits.

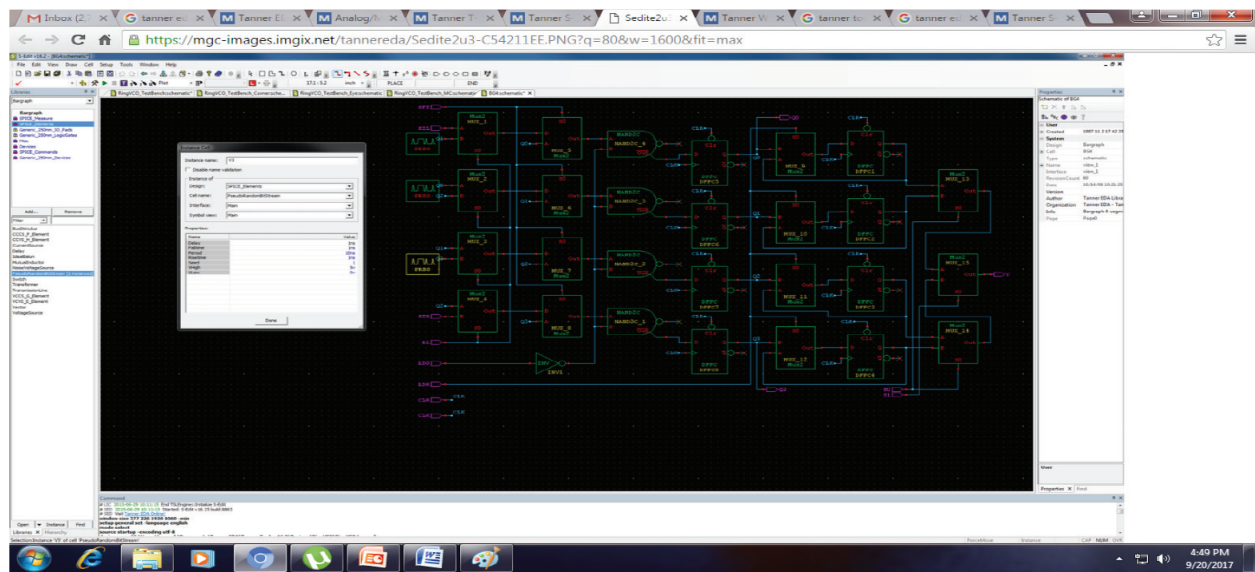


Figure 19. Tanner S-Edit schematic capture.

The Tanner engine tools are used to design and simulate new ideas in analog-integrated circuits; this saves time and cost of chip fabrication.

1.10. Conclusion

In CMOS circuits, most of the power dissipates through dynamic power dissipation than static power dissipation. In CMOS circuits, static power dissipation is in the range of nano watts. The most significant source of dynamic power dissipation is caused by transition activities of the circuits. A higher operating frequency leads to more transition activities in the circuits and results in increased power dissipation. Using proper encoding techniques may reduce switching activity in the circuit. This will reduce the overall transition activity. Hence, the dynamic power dissipation can be reduced in VLSI circuits effectively.



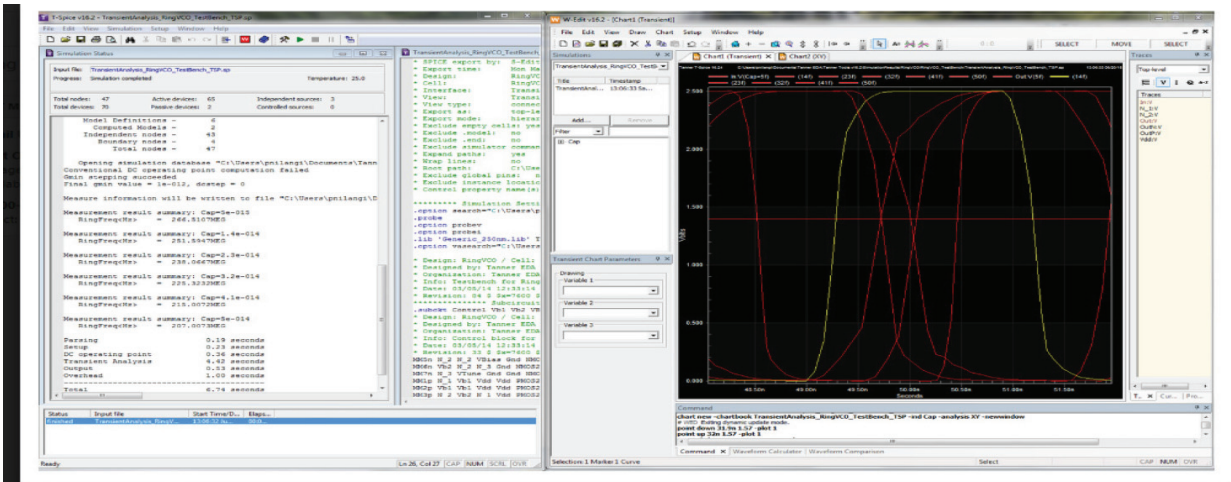
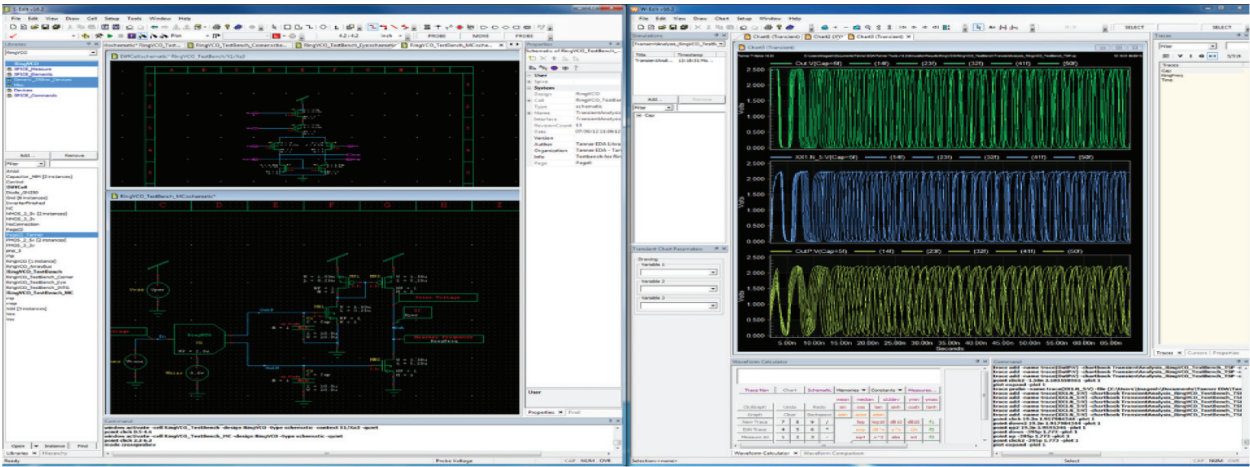


Figure 20. T-spice simulation.



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