Chapter 7

6T CMOS SRAM Stability in Nanoelectronic Era: From Metrics to Built-in Monitoring

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Additional information is available at the end of the chapter

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Abstract

The digital technology in the nanoelectronic era is based on intensive data processing and battery-based devices. As a consequence, the need for larger and energy-efficient circuits with large embedded memories is growing rapidly in current system-on-chip (SoC). In this context, where embedded SRAM yield dominate the overall SoC yield, the memory sensitivity to process variation and aging effects has aggressively increased. In addition, long-term aging effects introduce extra variability reducing the failure-free period. Therefore, although stability metrics are used intensively in the circuit design phases, more accurate and non-invasive methodologies must be proposed to observe the stability metric for high reliability systems. This chapter reviews the most extended memory cell stability metrics and evaluates the feasibility of tracking SRAM cell reliability evolution implementing a detailed bit-cell stability characterization measurement. The memory performance degradation observation is focused on estimating the threshold voltage (V_{th}) drift caused by process variation and reliability mechanisms. A novel SRAM stability degradation measurement architecture is proposed to be included in modern memory designs with minimal hardware intrusion. The new architecture may extend the failure-free period by introducing adaptable circuits depending on the measured memory stability parameter.

Keywords: SRAM reliability, process variability, memory cell stability margins, lifetime monitoring

1. Introduction

CMOS technology has been adopted by the digital IC market for a wide range of applications from high-performance computing and graphics to mobile applications, wearable

electronics and IoT applications. Technology scaling has been constantly evolving offering new opportunities to adapt each technology node to new challenging applications. Modern multi-core system trends result in a significant percentage of the total die area being dedicated to memory blocks. As larger densities of static memories are embedded inside complex SoC designs, analyzing memory reliability becomes more critical, as it may be an important source of the overall system error rate. For instance, the contribution of the SRAM parameter variability dominates the overall circuit parameter characteristics, including leakage and yield [1]. In addition, a deep knowledge and analysis about the SRAM cell noise margin and the impact of physical parameters variation is therefore becoming a must in modern CMOS designs.

The IC technologies have been constantly and aggressively scaled down due to efficient computation requirements. The critical dimension reduction in poly and diffusion features entails an increase in statistical physical parameters variation in the transistor parameters: threshold voltage (V_{th}), channel length, and mobility [2]. In this sense, embedded SRAM circuits are becoming more vulnerable because memory cells are scaled near the minimum available size in each technology node and the power supply is reduced. In this scenario, memory failures are drastically increasing due to higher device parameter variability, more defect density and new reliability mechanisms [3]. This has a direct impact on many parameters like SRAM performance, bit density, V_{DDmin}, leakage, dynamic power reduction, yield and failure probability. In addition, new reliability mechanisms may produce changes in the initial statistical parameter variability depending on user workload application, boosting the emergence of failures in field like bias temperature instability [4, 5].

The initial memory cell parameter variability profile due to fabrication process is defined using a combination of metrics. The most used ones are: the cell stability metrics (noise margins), the functional access time, the power consumption profile and the minimum V_{DD}. Due to the reliability degradation mechanisms, mainly due to V_{th} drift, the initial profile may change dramatically while the circuit is on field, increasing the functional failure probability and/or lowering the circuit performance profile.

Traditionally, on field circuit reliability effects have been minimized using several techniques at the design step. The first common methodology to reduce vulnerability of memory cells is based on introducing some reliability safety margins by design, in addition to the variability guard bands needed to overcome process variation issues. These margins lead to some cost in terms of performance, consumption or area. A second mitigation alternative has been proposed in the literature based on including operational assistance circuits, like read and write assist circuits introduced in memories to assure fault-free operations [5–7]. In more recent approaches, adaptive solutions are also proposed to mitigate BTI effects recovering the V_{th} drift [8]. These approaches involve memory modification to include additional adaptive circuits that in some scenarios have demonstrated to contribute to increase the functional failure probability [6, 7]. Therefore, in some applications, it may be important to periodically monitor the profile changes to detect which memory cells are likely to fail in the near future, and try to take some decision to avoid the failure [9]. The objective is to reduce the failure

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in time rate, and to improve the overall system reliability while remaining compatible with assist techniques or improved memory cell designs.

The next sections will review the conventional and novel SRAM noise metrics proposed in the literature and their suitability as observable parameters to estimate the threshold voltage (V_{th}) drift of 6T-based SRAM cells. The stability metrics will be analyzed and compared keeping in mind their suitability to be used in an implementable built-in monitor architecture. It is well known that the V_{th} variability is caused by process variation and reliability mechanisms but the implementation of a direct V_{th} measurement built-in monitor without affecting the memory array performance is difficult due to the need of internal memory-array node accessibility. Therefore, this approach analyses the stability metrics defined in the literature and proposes a built-in monitor architecture taking profit of their feasibility to measure and track the evolution of the memory cell effects due to reliability mechanism by observing the effect of the stability margin drift caused by the V_{th} drift.

2. Static random allocate memory

A typical SRAM is designed as a memory-cell matrix organized in N rows and M columns, see **Figure 1**. The SRAM performs three operations: Hold, Read and Write. The hold operation consists in storing the cell values and remains unaltered while the memory is powered on. The read operation accesses to a specific memory cell to read-out the value stored without destroy it. Finally, the write operation updates the stored value in a concrete memory cell changing the previous value.

During an operation, the row and column decoders translate the memory address into an internal cell matrix position. The row address identifies only one row (shadowed row in **Figure 1**) during a read/write access. The column address selects which specific cell from the selected row is actually read-out or write-in (dark cell in **Figure 1**). Finally, the read/write circuits perform the read/write operation to the selected memory cell.

While the memory cell addressed by the row and column decoder is the "selected" cell because both decoders point out the cell, the rest of the row cells are the "Half-Selected" cells, because only the row decoder is pointing out them but the read/write circuits have not access to those memory cells. In each read/write operation, there are M-1 half-selected cells for each selected cell. The presence of half-selected cells is important to understand why read operation is considered during the cell design as the weakest operation in terms of memory stability [10].

2.1. Memory cell with six transistors

The conventional 6T SRAM memory cell is formed by two cross-coupled CMOS inverters connected to the complementary bit-lines through two pass transistors. **Figure 2** shows this well-known memory cell and the main signals to perform read/write operations. Following

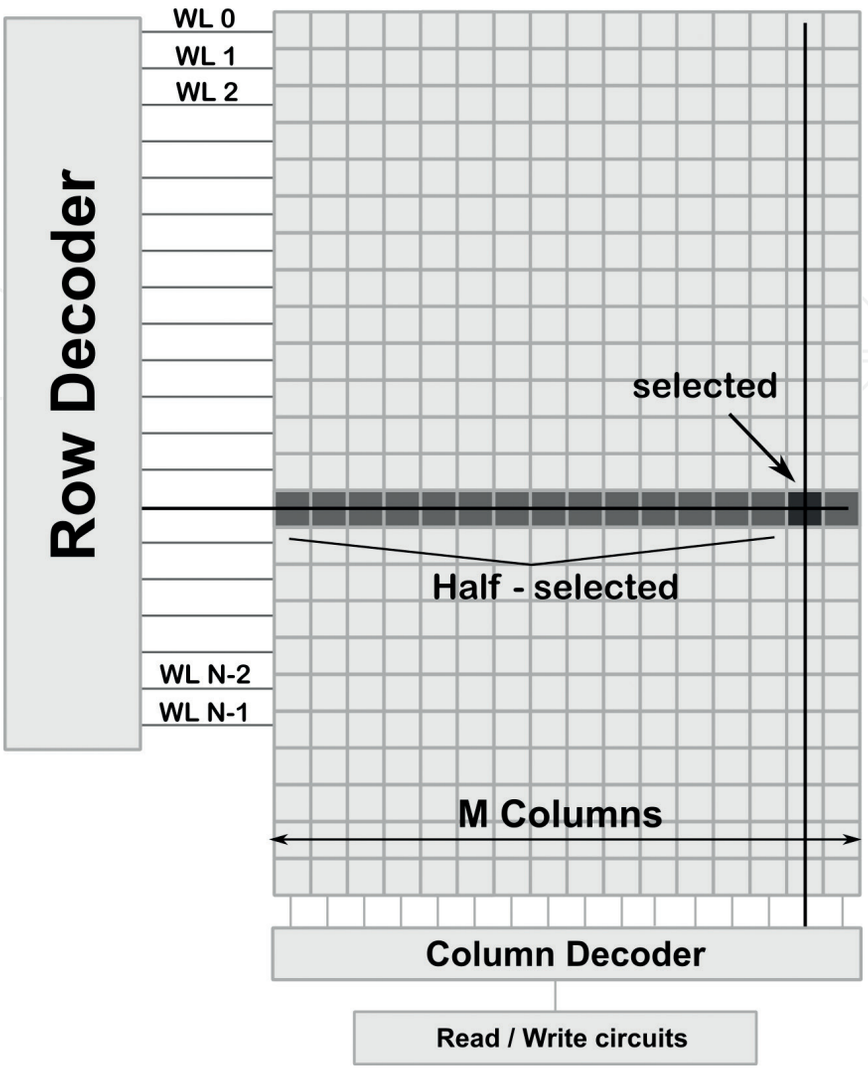

Figure 1. Typical SRAM internal organization with the main parts.

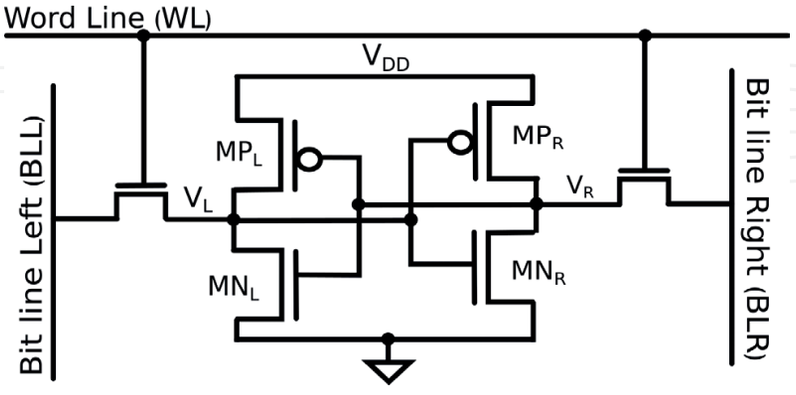

Figure 2. The six CMOS transistors SRAM cell schematic (6T).

the matrix distribution showed in **Figure 1**, all cells in the same row share the word line (WL in **Figure 2**) signal that is connected to the corresponding output of the row decoder. In the same way, all cells in the same column share the bit-lines (BLL and BLR in **Figure 2**) forming the column signals to the read/write circuits, see **Figure 1**.

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The access transistors have their gate node connected to the WL to open or close the connection of internal cell nodes (V_L and V_R in **Figure 2**) to the bit-lines (BLL and BLR respectively in **Figure 2**). So, bit-lines act as input/output nodes carrying the data from the selected cell to the read circuits in a read operation, or from write circuits to the selected cell in a write operation.

During the hold period the memory cell maintains a stable value due to the feedback reinforcement of cross-coupled inverters. The WL signal remain low, the BLL and BLR signals are high (are pre-charged waiting for the next operation) and the memory cell has their internals nodes disconnected from the bit-lines.

A read operation is performed connecting the internal memory nodes to both bit-lines precharged to high value. The internal node (V_L or V_R) at low value discharges the connected bit-line (BLL or BLR) though the voltage divider formed by the access transistor and the pull-down transistor (MN_L or MN_R in **Figure 2**). The read circuit senses and amplifies the difference between both bit-lines and the read-out value is latched.

A write operation starts when the write circuits set up the bit-lines with the adequate complementary value to write (BLL with the data value, and BLR with the complementary data value or vice versa). Then, the WL connects the selected memory cell to the bit-lines and the external values force the update of the stored value. In this case, the new value is written though the voltage divider formed by the access transistor and the pull-up transistors (MP_L or MP_R in **Figure 2**). Finally, the memory cell is disconnected from the bit-lines and the new value is stored.

When the memory is performing a write operation on a selected memory cell, there are half-selected memory cells that operate like in a read operation. These cells share the same word-line than the cell which is actually being written, for this reason, their internal nodes are connected to the bit-lines, which sense the cell stored value as in a read operation. In this situation, the cell is in its worst-case cell stability mode as it is reported in [11, 12]. In general, the read operation is more critical that write operation, and the presence of half-selected cells has motivated that the read vulnerability is guaranteed with bigger guard bands in exchange for writability degradation.

3. Memory stability metrics

Stability has been used for years as a useful metric to optimize the design of SRAM cells and predict the effect of parameter variation. Cell stability has been traditionally obtained by computing the noise margins for each memory operation. The noise margins represent the quantification of the cell ability to tolerate a certain presence of noise (in terms of current or voltage). This section will introduce the proposed noise margins considering the kind of nodes involved in the measurement: Internal cell nodes or External cell nodes. In both cases, noise margins will be organized in terms of the measured electrical variable (voltage, current or digital value) and the operation performed (read or write).

3.1. Stability metrics defined on internal cell nodes

The stability defined from the noise metrics on internal cell nodes tries to analyze the impact of voltage or current noise presence on the internal nodes and the maximum range tolerated

by the cell. These metrics are widely used for their ability to be implemented in computer simulations at the design phases. It is, therefore, a metric based on the internal nodes ability to tolerate noise in the form of voltage or current.

3.1.1. Based on voltage transfer characteristics

The popular definition for the cell noise margin is obtained using the voltage transfer curves (VTC) considering both read and write operations.

3.1.1.1. Read static noise margin

The read operation is the weakest situation because the cell transistors must be stronger enough to discharge the pre-charged bit-line without flipping its value stored. In a read operation, the memory cell is connected to the bit-lines and the internal nodes are disturbed. The node (V_L or V_R) at low voltage value must remain at this value to maintain the stored value in the cell, while the bit-line is discharged through the pull-down transistor. The static noise margin (SNM) quantifies the maximum amount of voltage noise that can be tolerated at the cross-inverters output nodes without flipping the cell. In the case of a read operation, **Figure 3** shows the node values setup and the noise voltage sources (V_n) to introduce the disturbance simulating a DC sweep between 0 and V_{DD}. The transistor MN_L is trying to maintain the V_L node as low as possible discharging the BLL. The effect of V_n introduces an extra voltage step that produces, if high enough, the loss of the stored value. The maximum extra voltage tolerated by the cell previous to lose the data is defined as the read static noise margin (RSNM).

The graphical method to determine the RSNM uses the static voltage transfer characteristics of the SRAM cell inverters. **Figure 4** superposes the voltage transfer characteristic (VTC) of one cell inverter to the inverse VTC of the other cell inverter. The resulting two-lobed graph is called a "butterfly" curve and is used to determine the RSNM. Its value is defined as the side length of the largest square that can be fitted inside the lobes of the "butterfly" curve [13]. **Figure 4** shows the hold/read operation dependence of the "butterfly" curves. **Figure 4(b)** shows how read operation reduces the noise margin due to the internal nodes connection to the bit-lines.

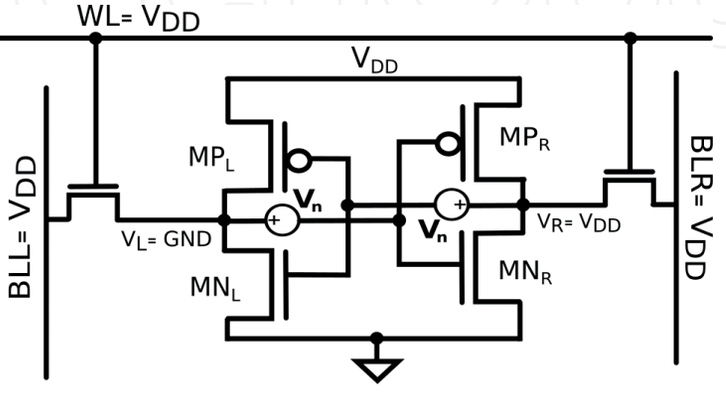

Figure 3. The setup for the read static noise margin definition.

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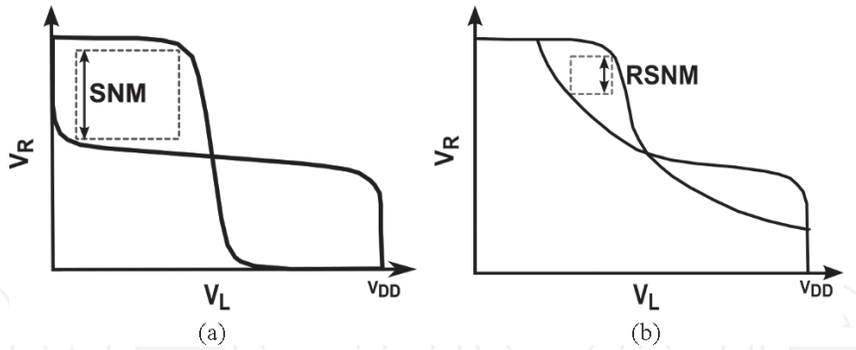

Figure 4. The VTCs of 6T CMOS based memory cell during (a) hold and (b) read access and graphical noise margin representation.

The memory cell designers try to maximize the RSNM value in order to obtain an optimum stability profile during read operation. To maximize the RSNM, the pull-down transistors width (MN_L and MN_R) must be set higher than the access transistors width. The size relationship between the pull-down and access transistors is called cell ratio (CR) and its value is usually designed to be higher than 1.

3.1.1.2. Write noise margin

During a write operation the stability is defined considering that the objective of the write operation is to force a new value into the cell, so break the cell stability. In that case, **Figure 5(a)** shows the cell setup considered to measure the write noise margin (WNM). The case where the new value is equal to the stored value is not considered because the cell does not change the internal values. When the cell is written and the value must be updated to the opposite value, both sides of the cross-coupled inverters (V_L and V_R) are confronted to two different situations. The first one, the cell side where internal node is at low value and the bit-line is at high value (V_L and BLL in **Figure 5(a)**), the transistor involved is the pull-down transistor (MN_L). In the second case, the cell side where internal node is at high and the bit-line is at low value (V_R and BLR in **Figure 5(a)**), the transistor involved is the pull-up transistor (MP_R).

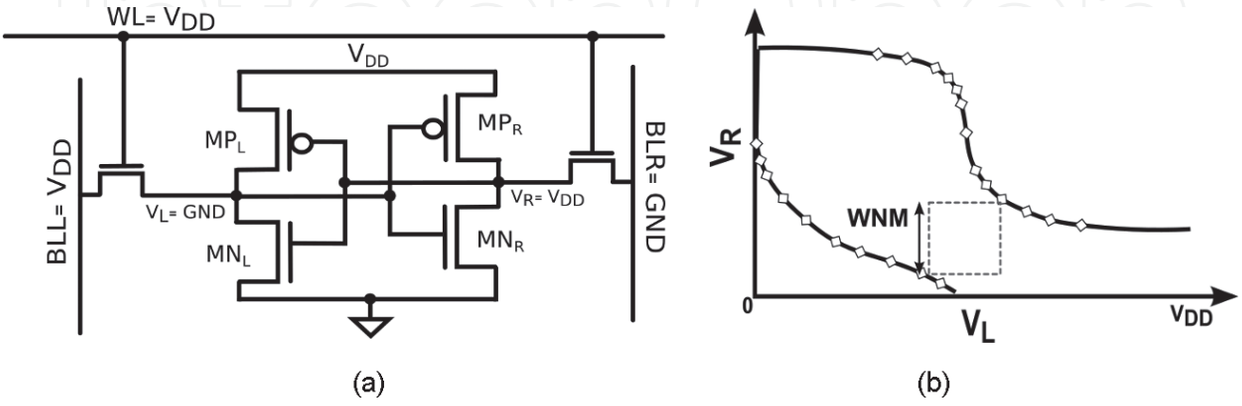

Figure 5. (a) The 6T CMOS based memory cell setup for the write static noise margin and (b) the VTCs during write access and graphical WNM representation.

Therefore, the write margin will be measured by the side of the smallest square embedded between the read and the write VTC measured from the same memory cell at the lower half of the read curves, past the trip point. **Figure 5(b)** shows the graphical representation of WNM.

In this case, the higher WNM is, the lower the writability of the memory cell results. Therefore, memory-cell designers try to slightly reduce the WNM value to obtain an optimum stability profile during write operation without affect the read operation. In order to reduce the WNM, the pull-up transistors width (MP_L and MP_R) must be established lower than the access transistors width. The size relationship between the pull-up and access transistors is called pull-up ratio (PR) and its value is usually designed to be slightly lower than 1.

3.1.2. Based on N-curve

Alternative SRAM noise metrics can be characterized using the N-curve [14]. In this case, the read and write noise margins are defined using the N-curve trip points showed in **Figure 6(b)** as A, B and C. The trip points are obtained using the setup showed in **Figure 6(a)**. The N-curve represents the current (I_{LX}) injected to the internal grounded node when the voltage source (V_{LX}) is swept from 0 to V_{DD}. A pair of current and voltage components defines the read/write noise margins. The N-curve values between trip points A and B, see **Figure 6(b)**, define the read metrics: the static voltage noise margin (SVNM), as the maximum DC voltage tolerable at the internal node previous to flip the memory cell content, and the static current noise margin (SINM), as the maximum DC current value that can be injected in the memory cell before its content changes.

The N-curve values between trip points B and C, see **Figure 6(b)**, define the write metrics: the write trip voltage (WTV), as the DC voltage drop needed to flip the memory cell content, and the write trip current (WTI), as the amount of DC current injected in the memory cell to change its content.

3.2. Stability metrics defined on external cell nodes

The main drawback of stability margin metrics defined on internal cell nodes is that they overestimate read failures and underestimate write failures since it assumes an infinitely long operating duration. However, those parameters are easy to simulate and have a graphical interpretation.

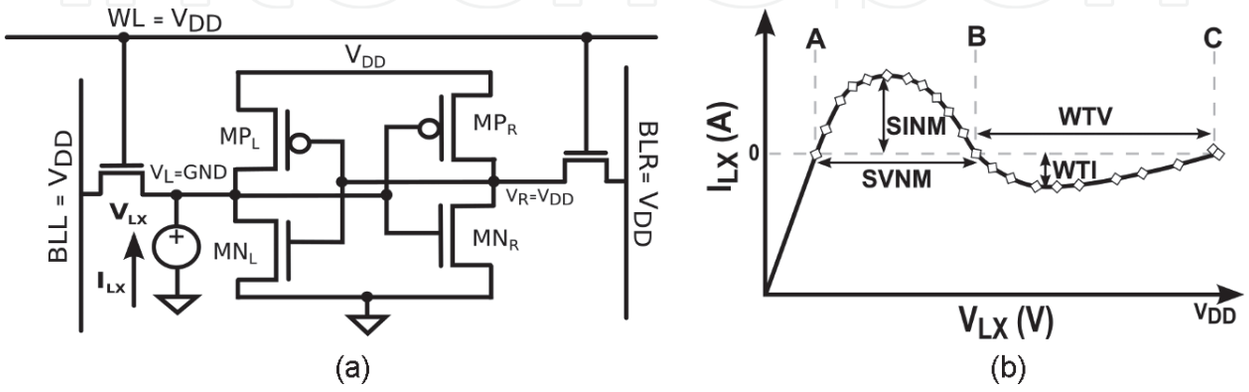

Figure 6. (a) The N-curve measurement setup and (b) the stability parameters defined.

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Other metric alternatives are based on direct access to external memory cell nodes: power supply, word-line, and bit-line nodes [15]. In addition, bit-line current or digital stored value measurements are proposed to characterize the stability with less memory array intrusions [16].

3.2.1. Based on a bit-line current observation

These methodologies measure the bit-line current variation while adjusting voltages of bit-lines, word-lines or cell power supply node to obtain read and write stability data.

3.2.1.1. Supply read retention voltage (SRRV)

The SRRV metric based on the observation of I_{BL} estimates the read margin based on the power supply swept. The I_{BL} is monitored to determine when the memory cell losses their ability to remain unaltered and changes the stored value.

Figure 7(a) shows the cell setup values when the bit-lines are set to pre-charged value. The word-line is ramped up until the sudden transition of I_{BL} appears to remain at a low current value. **Figure 7(b)** represents graphically the evolution of I_{BL} versus power supply voltage. When the current drops from its maximum value, the SRRV is defined as the maximum power supply voltage drop to produce a successful read operation. Therefore, SRRV is obtained from the difference between the nominal power supply voltage and the minimum power supply voltage to disturb the stored value.

3.2.1.2. Word-line read retention voltage (WRRV)

The WRRV metric is based on the observation of I_{BL} and estimates the read ability of the cell when the word-line is swept above V_{DD}. The I_{BL} is monitored to determine when the memory cell changes the stored value losing their ability to perform a non-destructive read operation.

Figure 8(a) shows the cell setup values when the bit-lines are pre-charged to V_{DD}. The WL is ramped up until a sudden transition of I_{BL} appears. **Figure 8(b)** represents graphically the evolution of I_{BL} for values of word-line voltage above V_{DD}. When the current drops from its maximum value, the WRRV is defined as the difference between the maximum word-line voltage and the nominal power supply voltage.

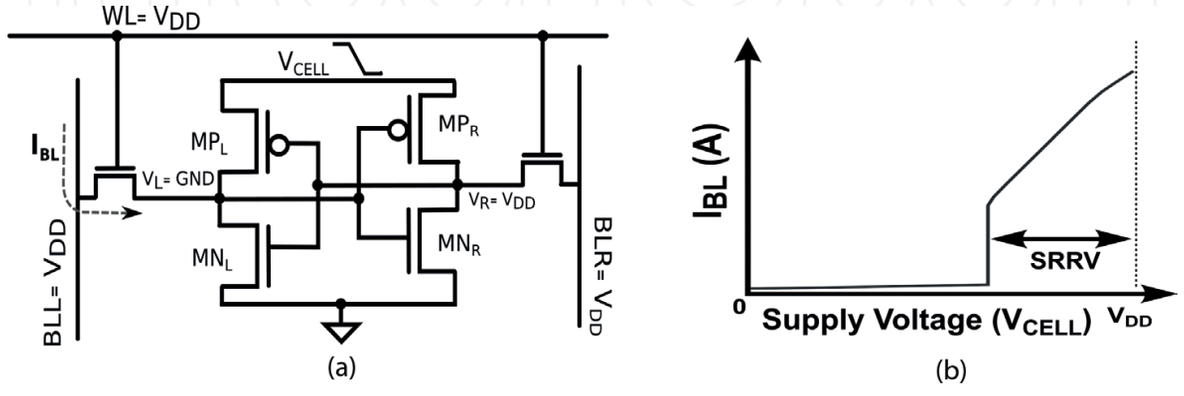

Figure 7. (a) The setup for the supply read retention voltage observation and (b) the graphical SRRV definition from current-voltage transfer curves.

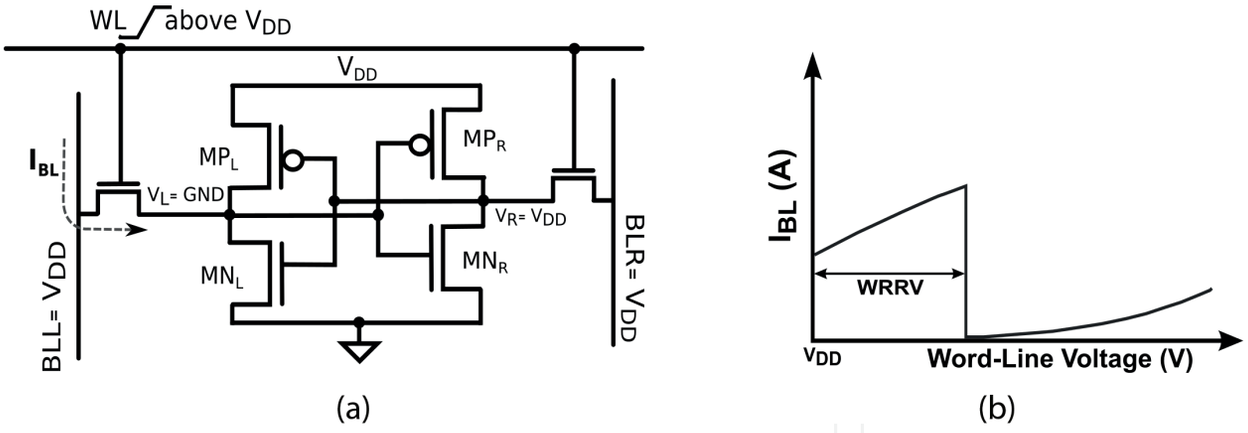

Figure 8. (a) The setup for the word-line read retention voltage observation and (b) the graphical WRRV definition from current-voltage transfer curves.

3.2.1.3. Bit-line write trip voltage (BWTV)

The BWTV estimates the cell writability as the maximum bit-line voltage tolerated by the BLR node (see **Figure 9(a)**) able to flip the cell value during a write cycle.

Figure 9(a) shows the cell setup to perform the margin measurement when it is initialized to store a '0' (V_L retains the '0' and V_R the '1'). The word-line (WL) and the left bit-line (BLL) are biased to V_{DD}, while the right bit-line (BLR) is ramped low from V_{DD}. The current measured on BLL node (I_{BL}) is monitored expecting a sudden drop (see **Figure 9(b)**). When this condition occurs, it indicates a successful write operation and defines the lower bit-line voltage tolerable by the cell. **Figure 9(b)** shows the bit-line current waveform and graphically shows the noise margin.

3.2.1.4. Word-line write trip voltage (WWTV)

The WWTV metric based on the observation of I_{BL} estimates the write margin based on word-line sweep. The I_{BL} is monitored to determine when the memory cell changes the stored value.

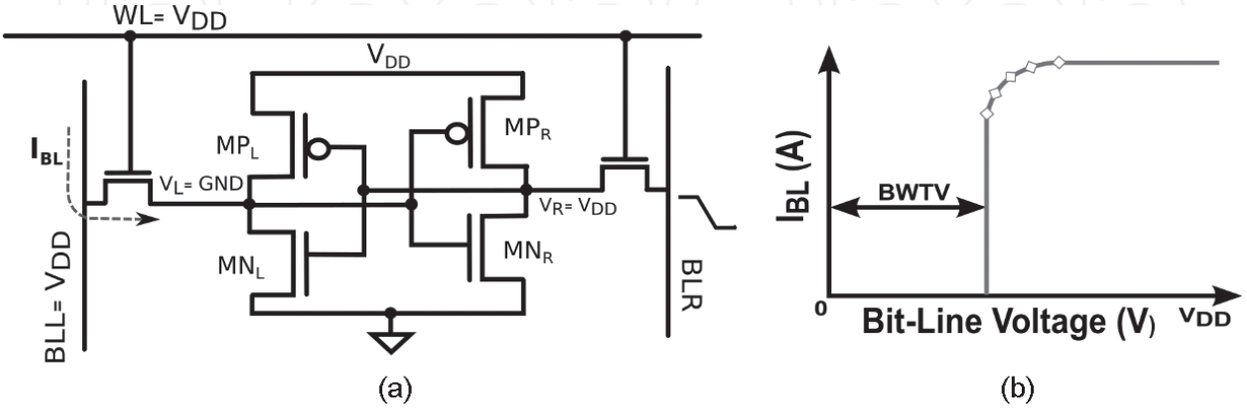

Figure 9. (a) The setup for the bit-line write trip voltage observation and (b) the graphical BWTV definition from current-voltage transfer curves.

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Figure 10(a) shows the cell setup values when the bit-lines are set with inverted values. The WL is ramped up until the sudden transition of I_{BL} appears. **Figure 10(b)** represents graphically the evolution of I_{BL} for different values of word-line voltage. When the current drops from its maximum value, the WWTV is defined as the maximum word-line voltage drop to produce a successful write operation. Therefore, WWTV is obtained from the difference between the nominal power supply voltage and the minimum word-line voltage to change the stored value.

3.2.2. Based on stored value observation

The current based noise metrics requires analogue measurements from bit-lines requiring memory cell array modifications. To overcome these requirements, another metric is proposed in [17] with minimal redesign requirements. It is based on word-line voltage sweep and requires read/write memory operations because the stored value is the observation parameter.

3.2.2.1. Maximum word-line voltage margin (MWLV)

The MWLV estimates the writability margin finding the minimum word-line voltage level to produce an effective write on a specific cell [17].

For each value in the word-line voltage level the stored value is read to determine when the memory cell changes the value. **Figure 11(a)** shows the cell setup values when the bit-lines are set with inverted values. The V_{WL} is ramped up until the new value is written. **Figure 10(b)** represents graphically the evolution of stored value for different values of word-line voltage. When the write operation is successful, the MWLV is defined as the maximum word-line voltage drop to produce a successful write operation. Therefore, MWLV is obtained from the difference between the nominal power supply voltage and the minimum word-line voltage to change the stored value.

This technique was proposed in previous works [11] to improve the read/write stability with minimal SRAM circuit modifications. The reduction of word-line voltage during read/write

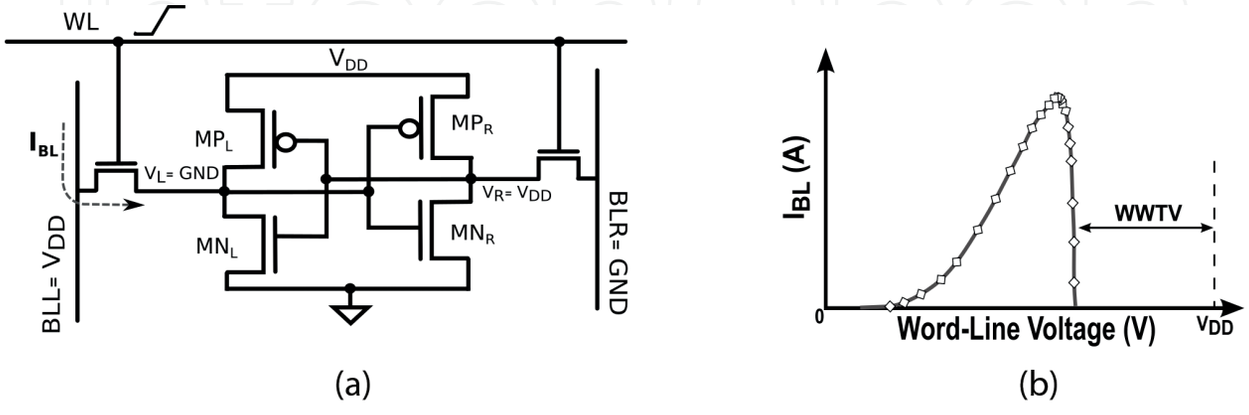

Figure 10. (a) The setup for the word-line write trip voltage observation and (b) the graphical WWTV definition from current-voltage transfer curves.

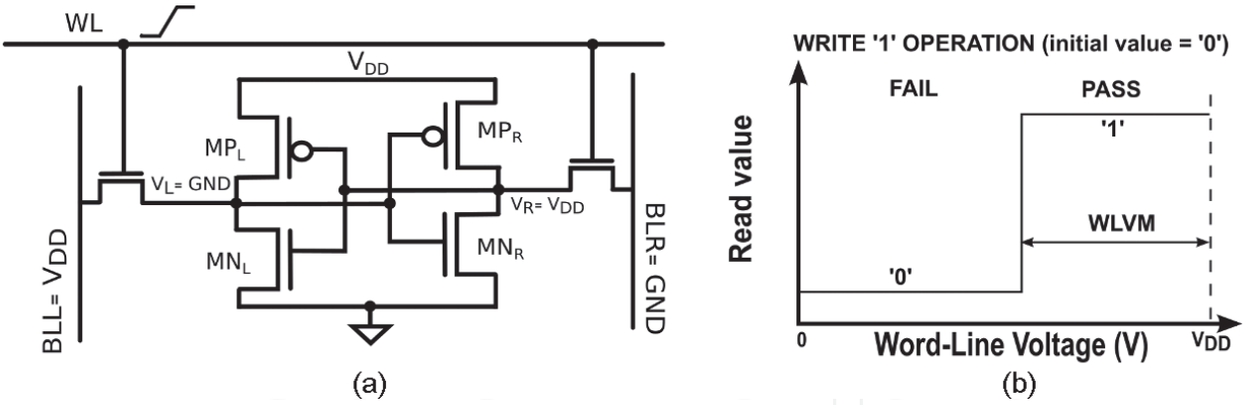

Figure 11. (a) The setup for the maximum word-line voltage margin observation and (b) the graphical MWLV definition from digital-voltage transfer curves.

operation increases cell stability during operations because the internal nodes of half-selected cells are connected to the bit-lines through a weaker connection, and thus the memory cell becomes more stable.

Finally, it is important to note that the MWLV metric is similar to WWTV metric because in both cases the word-line voltage is used to disturb the write operation. In this sense, the voltage conditions showed in **Figures 9(a)** and **10(a)** are equivalent. The main difference consists in how the behavior of the cell is monitored. In WWTV the I_{BL} current is used to detect a successful write on cell, while the word-line voltage is ramped up. Therefore, the WWTV

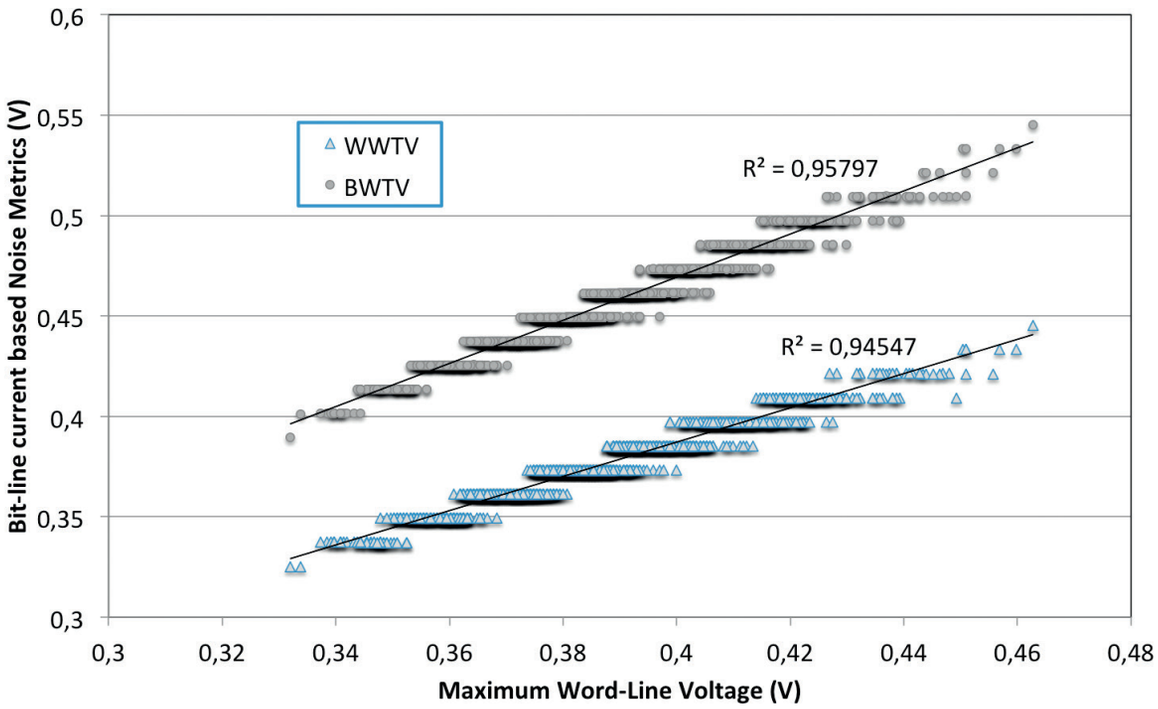

Figure 12. High grade of correlation between MWLV and WWTV/BWTV using Monte Carlo simulations with 65 nm CMOS technology.

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considers the DC behavior response. By contrast, in MWLV a successful write operation is observed reading the stored value after a regular write operation at lower word-line voltage. That is, the cell memory is operated using memory read/write operation at regular designed timings. Therefore, the MWLV metric analyses the transient behavior because timing and dynamic features of write operation are included.

The existence of several metrics combining different methodologies to monitor the cell stability requires a deep analysis. In this sense, intensive Monte-Carlo simulations considering process variation on a commercial 65 nm CMOS technology have been performed to determine the correlations between current based writability margins and the digital based MWLV metric. **Figure 12** shows the linear correlation obtained between BWTV, WWTV and MWLV metrics. A linear correlation between metrics with a coefficient near to 0.95 is archived in both cases. This result suggests a remarkable equivalence between the different metrics and highlights the opportunity for freely selecting the most adequate methodology.

4. Defining a built-in stability monitor

Detecting SRAM performance shifts due to parameter variation and BTI involves sensing SRAM cell and peripheral circuit degradation. In this work, we center our attention on the sensing process and on the long-term variability effects on the memory cell margins, which depend on the threshold voltage shift of all NMOS and PMOS devices. It is well known that the fabrication processes in nanometer era introduce parameter variability, which translates in functionality effects at the device level.

The process variability has an impact on the noise margins, showed in **Figure 13**, where corner and Monte-Carlo analysis results show a high variability in the read static noise margin.

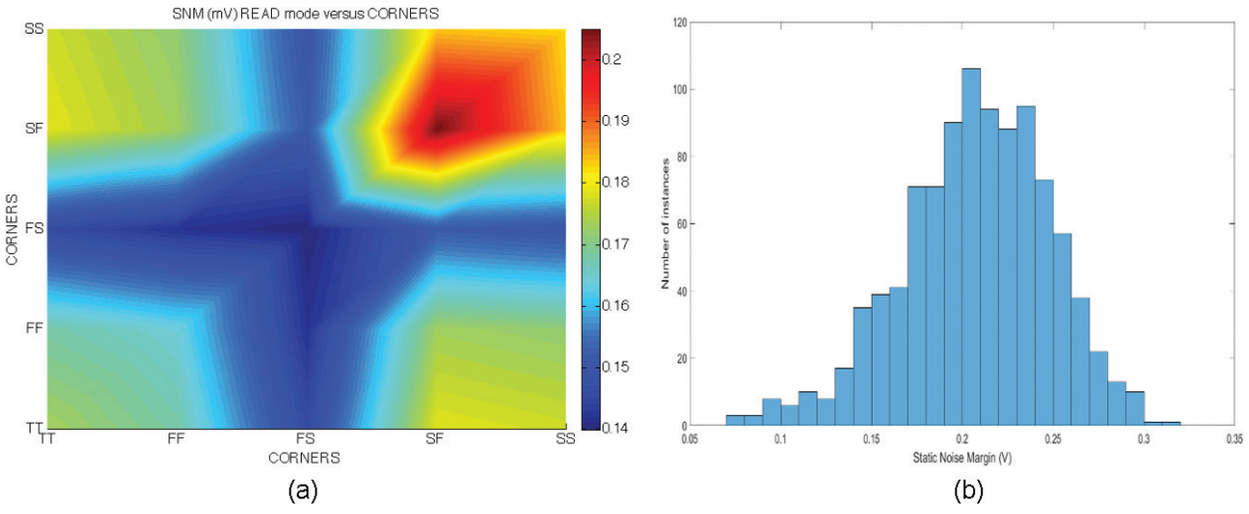

Figure 13. Process variability on read static noise metric obtained from (a) corners and (b) Monte-Carlo analysis with a commercial 65 nm CMOS technology.

The corner analysis assigns the slow-fast corner (SF in **Figure 13(a)**) as the most stable one that increases the stability in 17.1% from typical-typical corner (TT in **Figure 13(a)**), while the weakest is the fast-slow corner (FS in **Figure 13(a)**) and decrease the stability in 25% from TT corner. The maximum variability of RSNM is in the range of 60 mV.

The RSNM histogram, showed in **Figure 13(b)**, has been obtained from a 1000 iterations Monte-Carlo analysis considering process variation with a 65 nm CMOS technology. The variability spread is 240 mV with the mean value of 207.4 mV, and the standard deviation of 40.8 mV. Similar process variability impact may be observed using other noise margins.

In addition to the process variability, the use of the device may introduce extra parameter variability due to wearout/aging mechanisms. The influence of V_{th} variability on SRAM write margin metrics has been reported in **Figure 14(b)** [15, 17], where different write metrics (write noise margin, bitline write trip voltage, wordline write trip voltage and maximum wordline voltage) are explored considering V_{th} deviations due to wearout/aging effects.

Figure 14(a) shows the V_{th} variability impact on SRAM read noise margins (read static noise margin, supply read retention voltage, wordline read retention voltage). In the case of read noise margins, the variability behavior shows that the V_{th} drift decrease the read stability.

In the case of write noise margins, the write stability increases, this is, the memory cells are more easily written. Consequently, BWTV, WWTV and MWLV ramp up with V_{th}. According to their metric definitions, it means that the bit-line or word-line voltage can be lower previous to produce a fail in a write operation. However, WNM decreases with V_{th}, pointing out that the memory cell reduces its ability to tolerate noise during a write operation, because it is weaker against write processes. Therefore, although the four write metric curves showed in **Figure 14(b)** evolve in different directions, the meaning is equivalent in all of them: the memory cell is more stable during write operations allowing easy write operations with the increment of V_{th} value.

Finally, external variables may influence on metric values. To illustrate this impact, **Figure 15** reports the impact of power supply reduction on RSNM considering corners analysis (**Figure 15(a)**). The temperature decreases the noise margin during read operations. This temperature effect

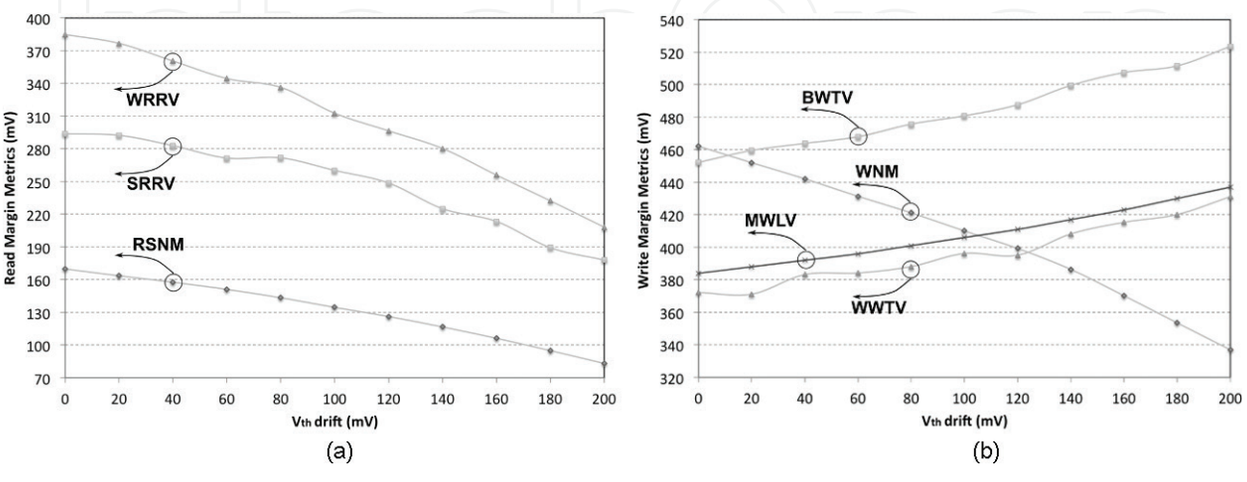

Figure 14. V_{th} drift impact on (a) read and (b) write noise margin definitions using a commercial 65 nm CMOS technology.

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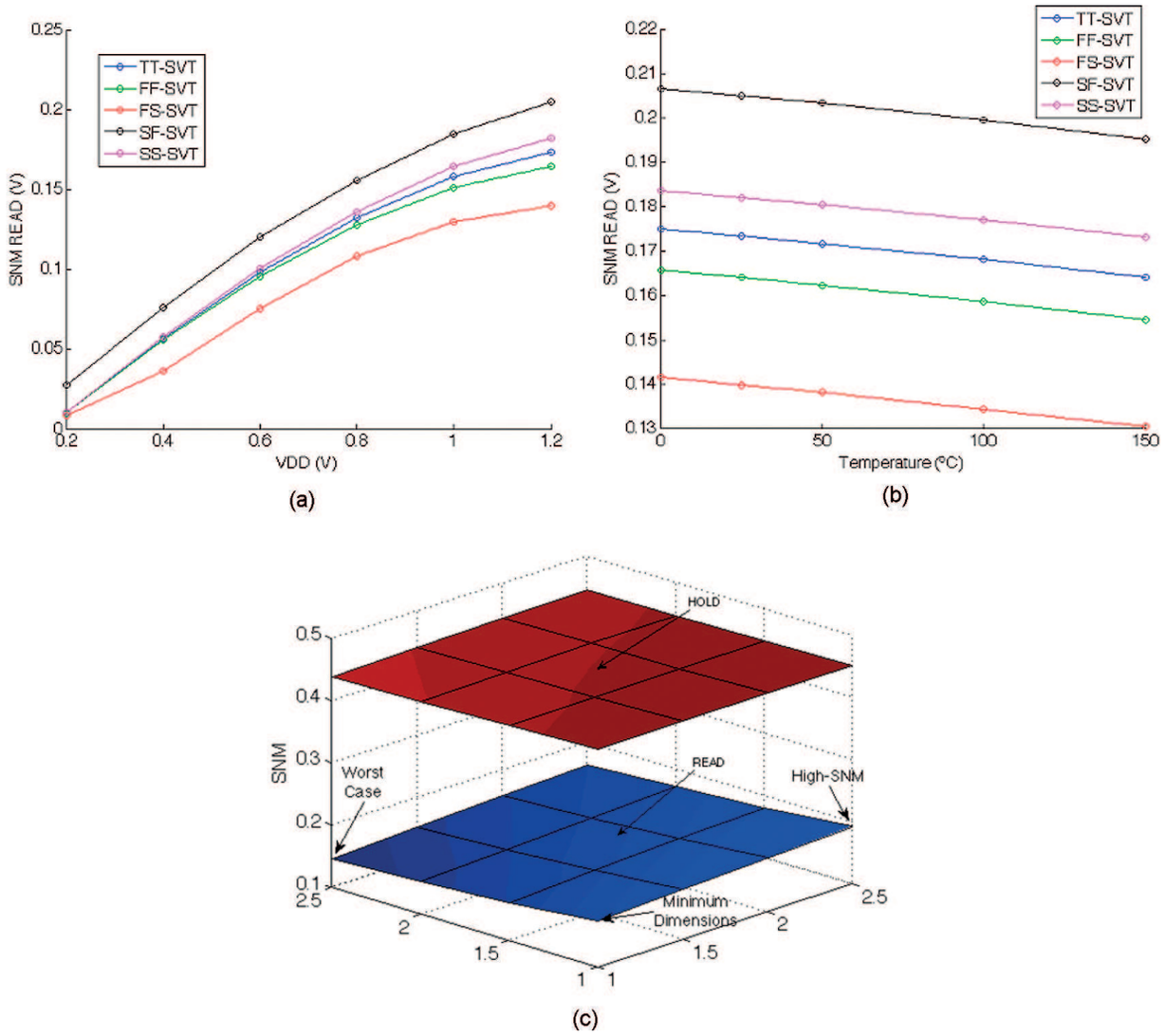

Figure 15. Impact of (a) power supply, (b) temperature and (c) operation and transistor width on read static noise metric using a commercial 65 nm CMOS technology.

considering corners analysis is showed in **Figure 15(b)**. And finally, the functional state (hold or read) of the circuit also is reported to influence the noise margin. **Figure 15(c)** warms about this effect representing the static noise margin of a memory cell in hold and read operation.

4.1. Stability metrics: from simulation to implementation

Although, the described static stability margin definitions are proposed to help designers during the pre-silicon step, the large number of devices in a memory array, and the increasing variability of technology processes, difficult the development of accurate models to simulate random effects in critical design parameters. Therefore, post-production or livelong memory measurements strategies are becoming important issues in modern system designs with high number of memory instances per chip.

Those popular metrics are suitable for simulation estimation but are too difficult to measure on real circuits. In this sense, DC read/write margins measurements were proposed using similar simulation methodologies. Direct access to internal storage nodes was implemented in [18] using large analogue switch networks circuits to connect internal cell nodes to external voltage sources and current monitoring circuits. Although, this methodology may achieve higher accuracy in SRAM failure analysis than simulation, its main drawback is the memory array redesigning efforts and hardware complexity required to perform voltage/current DC sweeps. In addition, the stability results and memory performance may also be affected negatively.

To decrease the intrusion on the memory array layout, the metrics based on bit-line current measurements have been proposed for large memory arrays [15]. Direct bit-line current measurement has been proposed in the literature to characterize noise metrics [15] or aging effect [19] in large memory instances with less memory cell array modifications. These approaches measure bit-line current variation, while adjusting bit-lines, word-lines and cell supply voltages to obtain writability data. Therefore, it is necessary to analyze the voltages and currents to obtain stability margins. Even though bit-line based metrics report good dependence with V_{th} drift, their implementation is resource demanding mainly in terms of SRAM redesign and area overhead. In this sense, several previous works have proposed an SRAM array schema designed for large-scale memories to perform bit-line current measurements [15]. The hardware requirements of [15] are: independent cell supply, cell ground, N-well bias, and P-well bias used for voltage adjusting conditions. Furthermore, column read/write circuitry must be shut off while a complex switch network for direct bit-line access enables to measure bit-lines current. The total area overhead is estimated to be around 20% [15]. Hence, the costs in terms of hardware redesign are elevated. In addition, these direct bit-line measurement methodologies may accelerate transistor aging because, during its measurement, the memory cell is forced to work at non-nominal DC voltage or above the nominal values as in the WRRV metric. In addition, DC currents values flowing through the devices may increase the faulty probability due to electro-migration effects.

Finally, the digital based metric is proposed in [16, 17] reducing the hardware requirements, and the needs of memory redesign, while maintaining the capabilities to estimate the write margin. Apart from not requiring the redesign of memory array, the memory cell operates at nominal values, i.e. Accesses time schedule and voltage/current levels. **Table 1** compares the features of the different noise margin metrics included in this work.

MWLV is measured reducing the word-line voltage peak value during a write operation, without alterations on memory cell performance, and requiring minimal memory overhead. In fact, it is obtained performing only a sequence of read/write operations on the target cell with different word-line voltages. Despite of that, the authors do not focus the attention only on MWLV noise margin, but also on some of the preciously introduced metrics, discussing their feasibility for lifetime aging effects monitoring. Next section will propose a built-in monitor approach feasible for noise metrics based on bit-line current or digital value observation.

4.2. Built-in monitor proposal

The built-in aging monitor approach based on noise margin measurements is feasible for different noise metric search. **Figure 16** shows the monitor schema adding the yellow blocks

		RSNM	*WNM*	*SVNM*	*SINM*	*WTV*	*WTI*	*SRRV*	*WRRV*	*BWTV*	*WWTV*	*MWLV*
ΔWM / ΔVth	*SYM*	-0.431	-0.613	-0.009	0.051	0.141	-0.075	-0.598	-0.884	0.350	0.291	0.263
	ASYM	-0.446	-0.311	1.111	0.175	-1.012	-0.018	0.853	0.379	0.234	0.291	0.329
Lineal coefficient (R^2)	*SYM*	0.987	0.988	0.999	0.983	0.996	0.997	0.947	0.985	0.986	0.966	0.989
	ASYM	0.999	0.999	0.998	0.999	0.999	0.921	0.92	0.986	0.993	0.966	0.993
Variable observed		V	V	V	I	V	I	I	I	I	I	D
Implementation		DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	TRAN
Cell Array redesign		high	high	high	high	high	high	medium	high	medium	high	low
Area Overhead Needs		high	high	high	high	high	high	medium	medium	medium	medium	low
Access to cell nodes		Y	Y	Y	Y	Y	Y	N (V_{DD}, BL)	N (WL, BL)	N (BL)	N (WL, BL)	N

Table 1. Stability metrics comparison for lifetime monitoring.

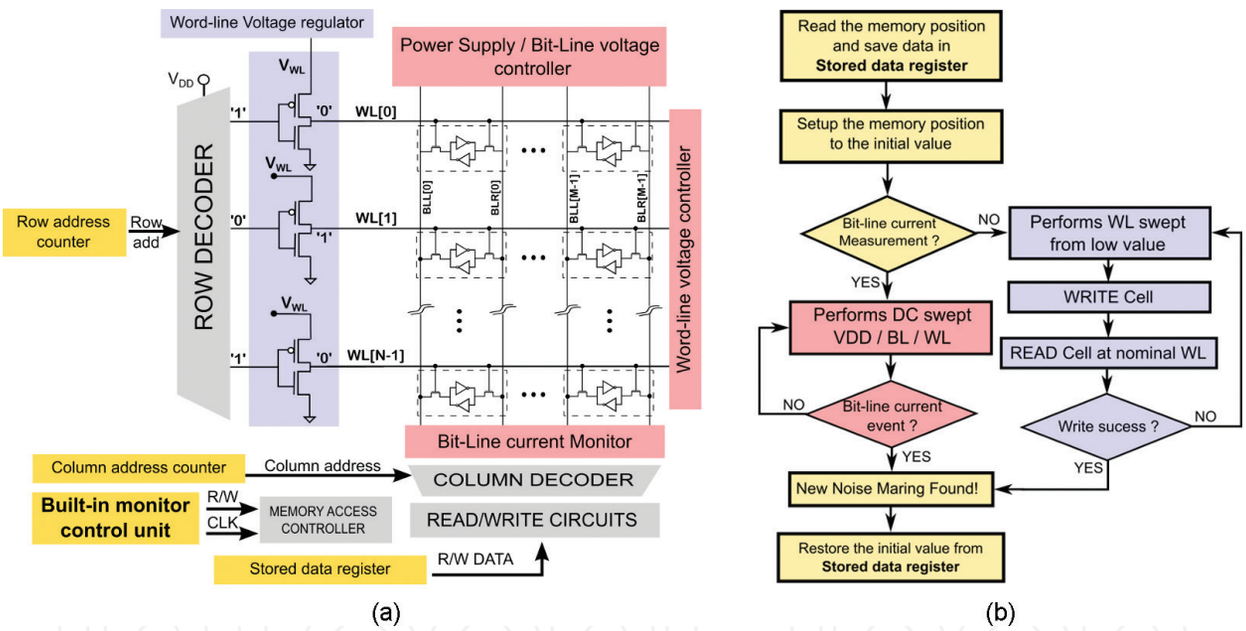

Figure 16. (a) The lifetime NM monitor schematic basics and (b) the NM search algorithm proposal for the built-in monitor schema approach.

needed in all noise margins implementations, the red blocks needed in direct bit-line current measurements and the blue blocks needed only for MWLV metric.

The Built-in monitor schema is supposed to perform the noise metric search in field, such as between activity periods. Therefore, the memory array will be disconnected from external signals to run the monitor algorithms. The common elements needed are the row and column counters (proposed to store the current memory address and run sequential accesses), and the stored data register (that saves temporarily the previous data read from current memory address), because the noise margin search algorithms are destructive (DC voltage swept or write operations).

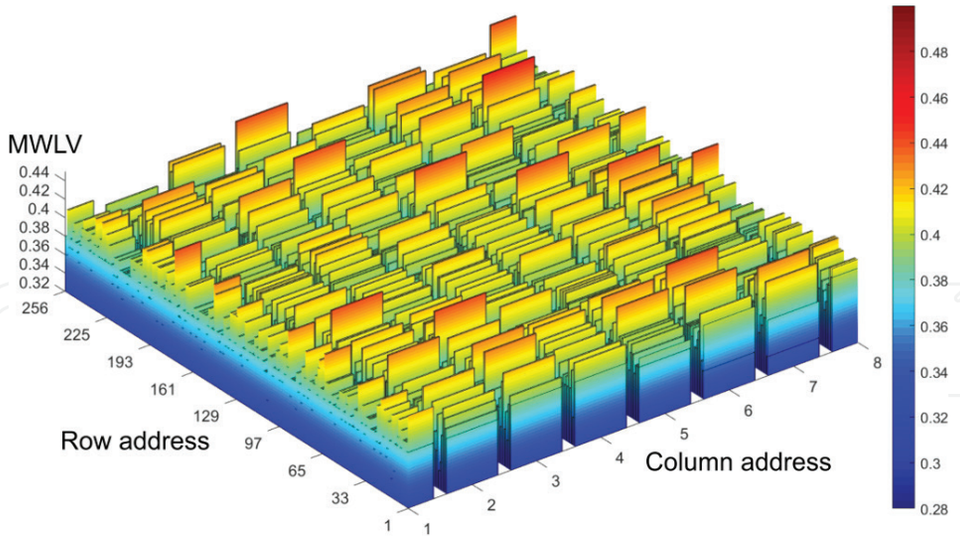

Figure 17. Spatial MWLV margin distribution due to process variability considering an 8 × 256 memory cell array using a commercial 65 nm CMOS technology.

The direct bit-line current-based noise metrics have the following requirements: the bit-line current monitor, the power supply/bit-line voltage controller and the word-line voltage controller. The voltage controllers are introduced to generate the desired DC voltage swept on the internal memory array nodes. The bit-line current monitor is able to detect the value sudden drop signaling the new noise margin.

The MWLV noise margin has less hardware requirements because the circuit changes are mainly centered on controlling the word-line voltage peak. The built-in approach proposes a word-line voltage controllability implementation based on using as isolated power supply node of all last row decoder gates. A feasible digitally controlled word-line regulator was reported in [17].

The build-in control unit implements the search algorithm depending on the noise metric implemented. A feasible algorithm proposal is showed in **Figure 17** highlighting the functions related with each metric methodology. The direct bit-line current measurement is based on the implantation reported in [15], while the MWLV metric is based on the design reported in [17]. **Figure 17** shows a 3D representation of the MWLV values measured from a 256 × 8 bytes memory implemented using a 65 nm CMOS technology [17] showing the suitability of this built-in approach.

Finally, it is important to note that the proposed search algorithm may be applied at any time during the normal lifetime of the memory. To determine the degradation evolution is not necessary to perform a whole exploration and the NM value may be estimated using a random address evaluation.

In addition, a novel online bit-line current measurement strategy has been recently proposed by [19] to measure aging effects on memory cell PMOS devices that the interest to perform online aging estimations is increasing in importance and is a challenging topic.

5. Conclusions

The runtime Reliability monitoring challenge in 6T CMOS SRAM has been addressed. The post-silicon stability profile has been highlighted as an observable signature to extract performance degradation due to reliability mechanisms. The different noise margins are identified as a suitable metric considering SRAM design with extra reliability guard bands. In addition, the write margins are suitable for designs oriented to guarantee read operation in exchange for writability degradation.

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References

[1] Vishvakarma SK, Reniwal BS, Sharma V, Kushwah CB, Dwivedi D. Nanoscale memory design for efficient computation: Trends, challenges and opportunity. In: Proceedings of the IEEE International Symposium on Nanoelectronic and Information Systems; 2015. pp. 29-34. DOI: 10.1109/iNIS.2015.58

[2] Mann RW, Hook TB, Nguyen DPT, Calhoun BH. Nonrandom device mismatch consideration in nanoscale SRAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. Jul. 2012;**20**(7):1211-1220. DOI: 10.1109/TVLSI.2011.2158863

[3] Khan S, Hamdioui S. Trends and challenges of SRAM reliability in the nano-scale era. In: Proceedings of the Inter. Conf. on Design & Technology of Integrated Systems in Nanoscale Era; 2010. DOI: 10.1109/DTIS.2010.5487565

[4] Lin JC, Oates AS, Yu CH. Time dependent Vccmin degradation of SRAM fabricated with high-k gate dielectrics. In: Proceedings of the IEEE International Reliability Physics Symposium; 2007. pp. 439-444. DOI: 10.1109/RELPHY.2007.369930

[5] Pilo H, Barwin C, Braceras G, Browning C, Lamphier S, Towler F. An SRAM design in 65 nm technology node featuring read and write-assist circuits to expand operating voltage. IEEE Journal of Solid-State Circuits. 2007;**42**(4):813-819. DOI: 10.1109/VLSIC.2006.1705289

[6] Karl E, Guo Z, Ng Y-G, Keane J, Bhattacharya U, Zhang K. The impact of assist-circuit design for 22 nm SRAM and beyond. In: Proceedings of the IEEE International Electron Devices Meeting; 2012. pp. 561-564. DOI: 10.1109/IEDM.2012.6479099

[7] Chiu YT, Wang YF, Lee Y-H, Liang YC, Wang TC, Wu SY, Hsieh CC, Wu K. Analysis of the reliability impact on high-k metal gate SRAM with assist-circuit. In: Proceedings of the IEEE International Reliability Physics Symposium; 2014. pp. 4.1-4.4. DOI: 10.1109/IRPS.2014.6861171

[8] Faraji R, Naji HR. Adaptive technique for overcoming performance degradation due to aging on 6T SRAM cells. IEEE Transactions on Device and Materials Reliability. 2014;**14**(4):1031-1040. DOI: 10.1109/TDMR.2014.2360779

[9] Kim W, Chen C-C, Liu T, Cha S, Milor L. Estimation of remaining life using embedded SRAM for wearout parameter extraction. In: Proceedings of the IEEE International Workshop on Advances in Sensors and Interfaces; 2011. DOI: 10.1109/IWASI.2015.7184952

[10] Alorda B, Torrens G, Bota S, Segura J. Adaptive static and dynamic noise margin improvement in minimum-sized 6T-SRAM cells. Microelectronics Reliability. 2014;**54**:2613-2620. DOI: 10.1016/j.microrel.2014.05.009

[11] Alorda B, Torrens G, Bota S, Segura J. Static and dynamic stability improvement strategies for 6T CMOS low-power SRAMs. In: Proceedings of the Design Automation & Test in Europe Conference; 2010. pp. 429-434

[12] Bota S, Torrens G, Alorda B. Critical charge characterization of 6T SRAMs during read mode. In: Proceedings of the IEEE International On-Line Testing Symposium; 2009. pp. 120-125. DOI: 10.1109/IOLTS.2009.5195993

[13] Seevinck E, List FJ, Lohstroh J. Static-noise margin analysis of MOS SRAM cells. IEEE Journal of Solid-State Circuits. 1987;**SC-22**(5):748-754

[14] Wann C, Wong R, Frank DJ, Mann R, Ko S-B, Croce P, Lea D, Hoyniak D, Lee Y-M, Toomey J, Weybright M, Sudijono J. SRAM cell design for stability methodology. In: Proceedings of the IEEE Symposium on VLSI-TSA; 2005. DOI: 10.1109/VTSA.2005.1497065

[15] Guo Z, Carlson A, Pang L-T, Duong KT, King T-J, Nikolic B. Large-scale SRAM variability characterization in 45nm CMOS. IEEE Journal of Solid-State Circuits. 2009;**44**(11):3174-3192. DOI: 10.1109/JSSC.2009.2032698

[16] Alorda B, Carmona C, Torrens G, Bota S. On-line write margin estimator to monitor performance degradation in SRAM cores. In: Proceedings of the International On-Line Testing Symposium; 2016. DOI: 10.1109/IOLTS.2016.7604678

[17] Alorda B, Carmona C, Torrens G, Bota S. An affordable experimental technique for SRAM write margin characterization for nanometer CMOS technologies. Microelectronics Reliability. 2016;**65**:280-288. DOI: 10.1016/j.microrel.2016.07.154

[18] Bhavnagarwala A, Kosonocky S, Chan Y, Stawiasz K, Srinivasan U, Kowalczyk S, Ziegler M. A sub-600 mV fluctuation tolerant 65 nm CMOS SRAM array with dynamic cell biasing. IEEE Journal of Solid-State Circuits. 2008;**43**(4):946-955. DOI: 10.1109/VLSIC.2007.4342773

[19] Ahmed F, Milor L. Online measurement of degradation due to bias temperature instability in SRAMs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 2016;**24**(6):2184-2194. DOI: 10.1109/TVLSI.2015.2500900