Chapter 9

MEMS Technologies Enabling the Future Wafer Test Systems

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Additional information is available at the end of the chapter

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Abstract

As the form factor of microelectronic systems and chips are continuing to shrink, the demand for increased connectivity and functionality shows an unabated rising trend. This is driving the evolution of technologies that requires 3D approaches for the integration of devices and system design. The 3D technology allows higher packing densities as well as shorter chip-to-chip interconnects. Micro-bump technology with through-silicon vias (TSVs) and advances in flip chip technology enable the development and manufacturing of devices at bump pitch of 14 μm or less. Silicon carrier or interposer enabling 3D chip stacking between the chip and the carrier used in packaging may also offer probing solutions by providing a bonding platform or intermediate board for a substrate or a component probe card assembly. Standard vertical probing technologies use microfabrication technologies for probes, templates and substrate-ceramic packages. Fine pitches, below 50 μm bump pitch, pose enormous challenges and microelectromechanical system (MEMS) processes are finding applications in producing springs, probes, carrier or substrate structures. In this chapter, we explore the application of MEMS-based technologies on manufacturing of advanced probe cards for probing dies with various new pad or bump structures.

Keywords: wafer and package test systems, MEMS technology, interconnects, interposer, wafer probes

1. Introduction

Increased connectivity and functionality is driving the evolution of 2D technology toward 3D technology for integration of silicon devices and system design. This technology is becoming a scaling engine for silicon technology [1] allowing higher packing densities and shorter chip-to-chip interconnects. Shrinking die dimensions and pitch pose challenges on

the probing and test side of the equation forces development of newer probes, interposers, interconnects and robust assembly systems [2, 3]. As 3D IC packaging is becoming mature, there is a strong push toward 3D IC Si integration. In a 3D IC integration, some of the chips, a microdisplay, microelectromechanical systems (MEMSs), memory, microprocessor, application-specific IC (ASIC), micro-controller unit, digital signal processor, microbattery and analog-to digital mixed signal are combined and stacked in three dimensions [4, 5]. These system and component level challenges are being addressed by silicon carriers or 3D-stacking, interposers, substrates and newer probe materials by MEMS processes. Developing a common intermediate board for a substrate or space transformer and probe card assembly will help solve technical challenges and reduce cost of test in both wafer and package level testing. An optimal design, which includes the IC design, the automated test equipment (ATE) test cell and the probe card solution, of the test flow between wafer sort and final test can yield benefits. Standard vertical probing technologies use microfabrication technologies for probes, templates and substrate-ceramic packages [6]. Pitches below 50 μm pose enormous challenges on fabrication of probe card components and nanotechnology and MEMS processes are required for producing probes, carrier or substrate structures for precision requirements. Probe structures must be designed with precision and their power delivery properties must be optimized. Advanced probe cards must be able to support high-speed testing and cold and hot temperature cycle testing with precision contact capability. They also need to address contact challenges for multi-row pads/bumps, full array Cu-pillar micro-bumps with various solder-bump metallurgies at temperature. Application of various technology approaches in test systems against the test requirements of silicon logic or memory or mixed signal devices is discussed.

2. Trends in silicon and systems for test

The cost of scaling is rapidly increasing and the expected development cost for system-on-chip (SoC) for 10 nm is 400M USD and for 7 nm it is projected to be approaching 600M USD [2]. This means that it requires multibillion dollar lifetime revenue to be economically feasible per design. System solutions need to balance performance, power and cost. The industry of moving to 3D architectures adds challenges in variability in manufacturing next generation devices, requires more stringent variability control by data analytics and Industry 4.0 applications [7]. Advanced packaging also adds multiple levels and variability can happen across multiple die, as memory chip stack with through-silicon vias (TSVs) placed on a logic device which is integrated to a substrate with copper pillar bumps, SnAg bumps or micro-bumps. At 10 nm process node, 3D TSVs are projected to be at 6 μm diameter with depth of 55 μm [2]. Logic-memory integration improves the bandwidth and provides higher performance per watt while SoC partitioning increases yield and helps cost optimization. In a total package stack-up, thin silicon layers become an issue due to low-k modulus reliability while the substrate can become subjected to a thermal mismatch stress and induced warpage problems, as well as routability issues.

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The cost is increasing with decreasing pitch, increasing probe count and increasing parallelism. The area-array type of logic test is challenging below 100 μm bump pitch and push for MEMS type of probe solutions are required to scale with the technology. Design for tests (DFTs) with wrappers are targeted to reduce number of I/O's that need to be contacted during test. Also, the ability to reuse testers is also studied to lower the total cost of test. A test system architecture with vertical style probe card is shown is **Figure 1**. In the system, ST stands for space transformer, multilayer ceramic substrate (MLC) and device under test (DUT).

When the roadmaps for probe card requirements are reviewed, there are many critical test system parameters that must be considered especially for large-sized highly parallel cards. They are mainly:

- Controlled overdrive
- Reduced temperature drifts
- Planarity self-adjustable function
- Low voltage test operation
- Reduced pad damage and increased uniformity
- Less particle generation
- Smart repair concepts
- Expanded temperature range
- Diagnostic functions on probe cards
- Smart alignment features
- Cost efficiency
- Lower lead times

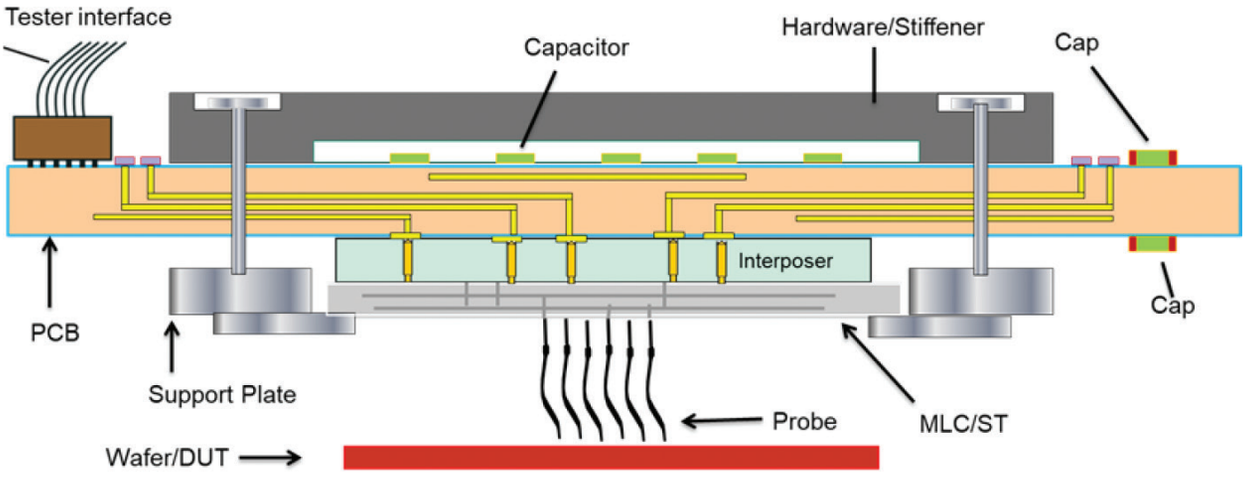


Figure 1. Probe card system architecture is shown.

3. Probe technology and designs for fine-pitch probing

Cantilever probing technologies, both traditional and MEMS-style cantilever, have limitations for multi-DUT probing at 50 μm or below. Wafer test becomes challenging because of design complexity of devices. For instance, one limit is the number of rows of bond pads that can be tested at one time, dependent heavily on pad density. Another parameter of a design test limitation with cantilever-style technologies is the corner keep-out in device layouts. Yet another requirement of this mode of technology is the need for skip DUT configurations, compromising test stepping efficiency.

Vertical style technology approaches allow more rows of peripheral pads and array patterns for contacts. Images of probe cards of a traditional cantilever, vertical and MEMS-memory types are illustrated in **Figure 2**. The market for devices with multiple peripheral pads is moving to finer pitches and the demand for higher levels of parallel testing is increasing for such logic configurations. These requirements are driven by higher I/O requirements, smaller device dies, longer test times and more challenging cost of test economics. It is required to probe devices at higher levels of parallelism and finer pad pitches. Pads can be arranged inline, dual or multi inline rows or staggered pads. This design space is typically not addressable by standard vertical, advanced memory cards or standard cantilever cards but a new segment for advanced fine-pitch MEMS type probe technologies. Major product families in this space at increasingly higher parallelism requirements are high-end ASICS, SoCs/high level digital signal processor (DSPs) and low-end DSPs/low-end microcontrollers.

Cantilever probe cards are used in addressing 1-row peripheral multi-DUT or 1–2 row peripheral layouts of pads on devices, as shown in **Figure 3**. Probe card with 2-row cantilever probes

Figure 2. Cantilever, standard vertical and MEMS type probe cards.

is illustrated on the right. There are significant limitations to standard cantilever probes technologies as the number of rows or DUTs rises. For three rows of pads, a vertical style technology is needed for efficient probing, as shown in **Figure 4**. Traditional vertical buckling beam style probes of three different diameters (4-mil, 3-mil and 2-mil) which address different device pitch requirements in wafer test are also shown. MEMS-vertical technologies enable probing of full arrays, as shown in **Figure 5**, that are typically not feasible with conventional vertical probe technologies.

Probe action, scrub mark size and depth must be precisely controlled to prevent damage to bond pads, typically Al or Cu, and low-k dielectrics during wafer probe. Fine-pitch probing requires precise control of alignment at pad sizes smaller than 40 μm.

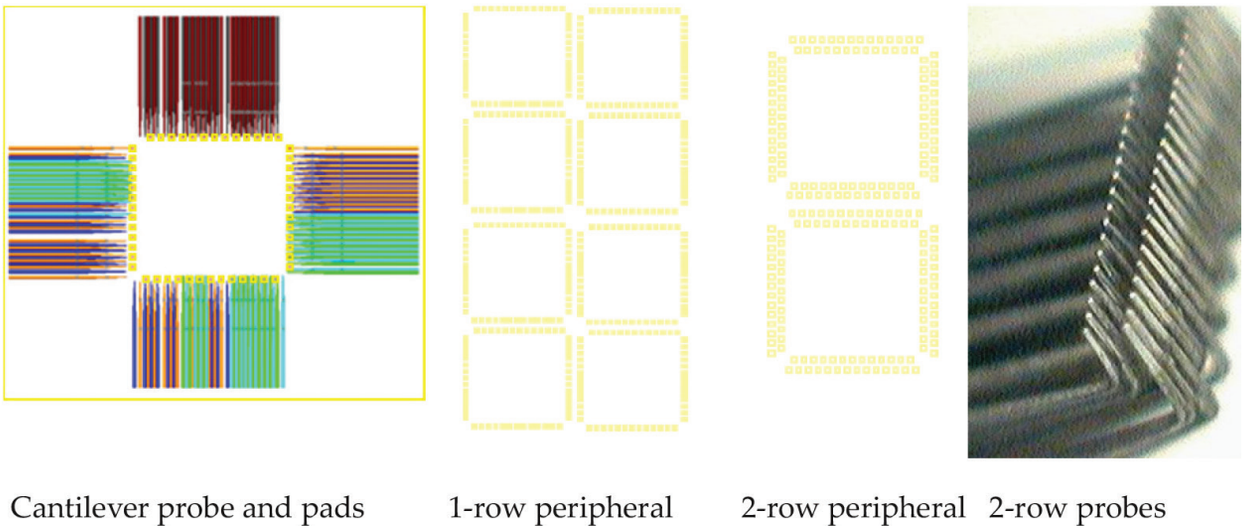


Figure 3. Cantilever design and contact pad layouts.

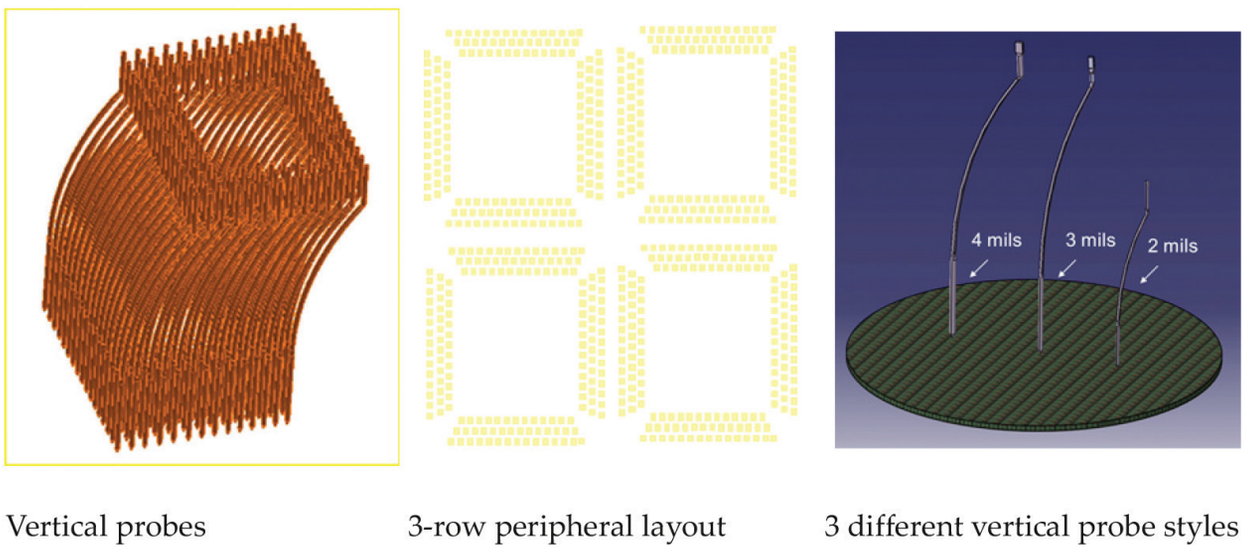
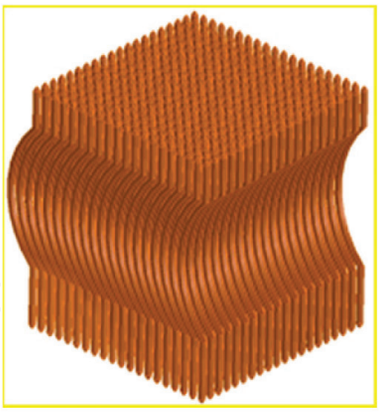
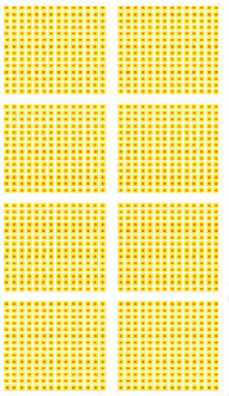


Figure 4. Vertical probes, 3-row peripheral layouts on a device and illustrations of three different vertical probe designs on a wafer.



MEMS probes



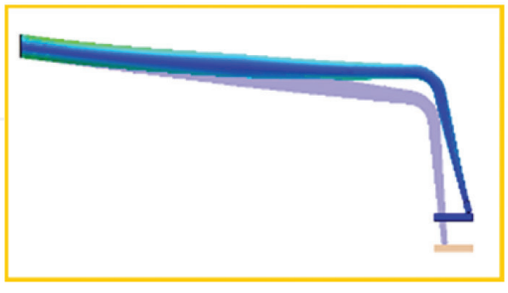
Array layout

Figure 5. MEMS-vertical probes for contacting an array of bumps.

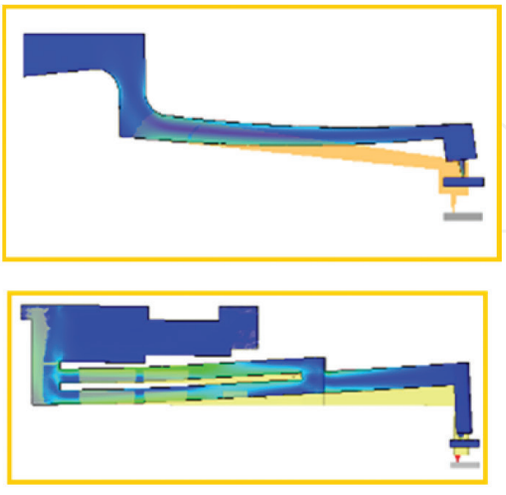
The contact model for vertical probe contacts is different than cantilever-style beams. Scrub marks generated by cantilever beams by design are typically longer than marks by vertical probes. Accurate guiding of probes permits finer controls and precise scrub marks for vertical. The tolerances on guiding holes as well as probes are critical for positions.

Figure 6 illustrates results of deflection and stress simulations for the models of cantilever probe designs and MEMS-cantilever probe designs exhibiting deflection upon pad contact and generating scrub motion on probe tips. MEMS-cantilever type designs are well suited for memory device testing up to 1–4 touchdowns for 300 mm wafers with probe counts up to 60,000 probes.

Vertical buckling beam model and MEMS-fine pitch vertical probe design contacts and simulations of deflection under load are shown in **Figure 7**. Vertical probes are typically manufactured



Cantilever probe



MEMS-cantilever probes

Figure 6. Cantilever probe design (conventional) and MEMS-cantilever probe designs showing deflection and scrub on pad during contact.

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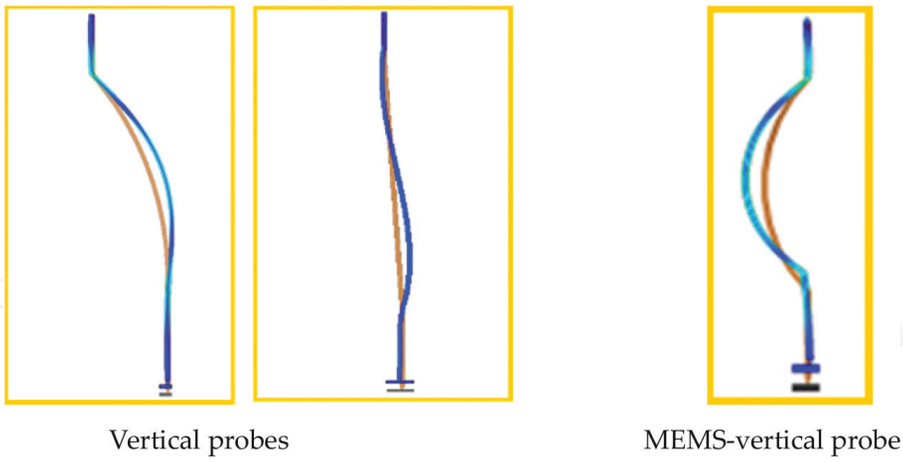

Figure 7. Vertical buckling beam probe design and MEMS-vertical probe designs showing deflection and contacting a pad/bump.

from Paliney 7™ or BeCu materials by stamping a wire version followed by a final finishing process. MEMS-vertical or cantilever probes are lithographically produced and involves many process steps typical in MEMS technologies. Different types of nickel alloys (Ni-Co and Ni-Mn) are commonly used for MEMS spring or probe manufacturing. Probe tips may be coated with harder alloys for better lifecycle, which may involve Pd and Pt alloys such as PdCo, PtIr, PtNi, Rh or hard gold and other alloys. It should be noted that MEMS-based vertical technology has an edge over buckling beam technologies for design flexibility for highly parallel peripheral devices as well as the accuracy of scrub signatures required for smaller pad sizes.Flip chip type area-array applications such as microprocessors, graphics chips and microcontrollers, are addressed by traditional vertical or MEMS-style vertical probe technologies. **Figure 8** shows MEMS probe products, advanced vertical probe technologies for testing full area-array (A) or testing multi-row peripheral or partial arrays (B) and advanced cantilever types for testing memory devices (DRAM or flash).

The electrical contact resistance measurements for MEMS-vertical probe technology as illustrated in **Figure 5** were performed on various emerging bump types. **Figure 9** provides the eutectic bump resistance measurements done by MEMS-vertical probes on a test system.

The contact resistance (Cres) was indicated to be stable at 25 μm overdrive (3 gf) for all tip sizes (9, 12, 16, 36 μm) studied. The Cres is the path resistance including connections from tester to the probe tip. The effective contact resistance of just the bump and the probe tip is estimated to be less than 0.2 Ohms.

The contact resistance on copper pillar bumps is illustrated for MEMS-vertical technology in **Figure 10**. It that shows the Cres with 12 μm probe tips is much higher than those from 9 μm tips. For probes with 9 μm-tips, Cres was stable at 50 μm overdrive (5–6 gf). The copper pillars are much harder than eutectic or Sn-Ag type bumps, therefore it requires higher forces to establish good contact. However, the probe tips remain much cleaner in life testing on copper pillars compared to solder-based bumps.

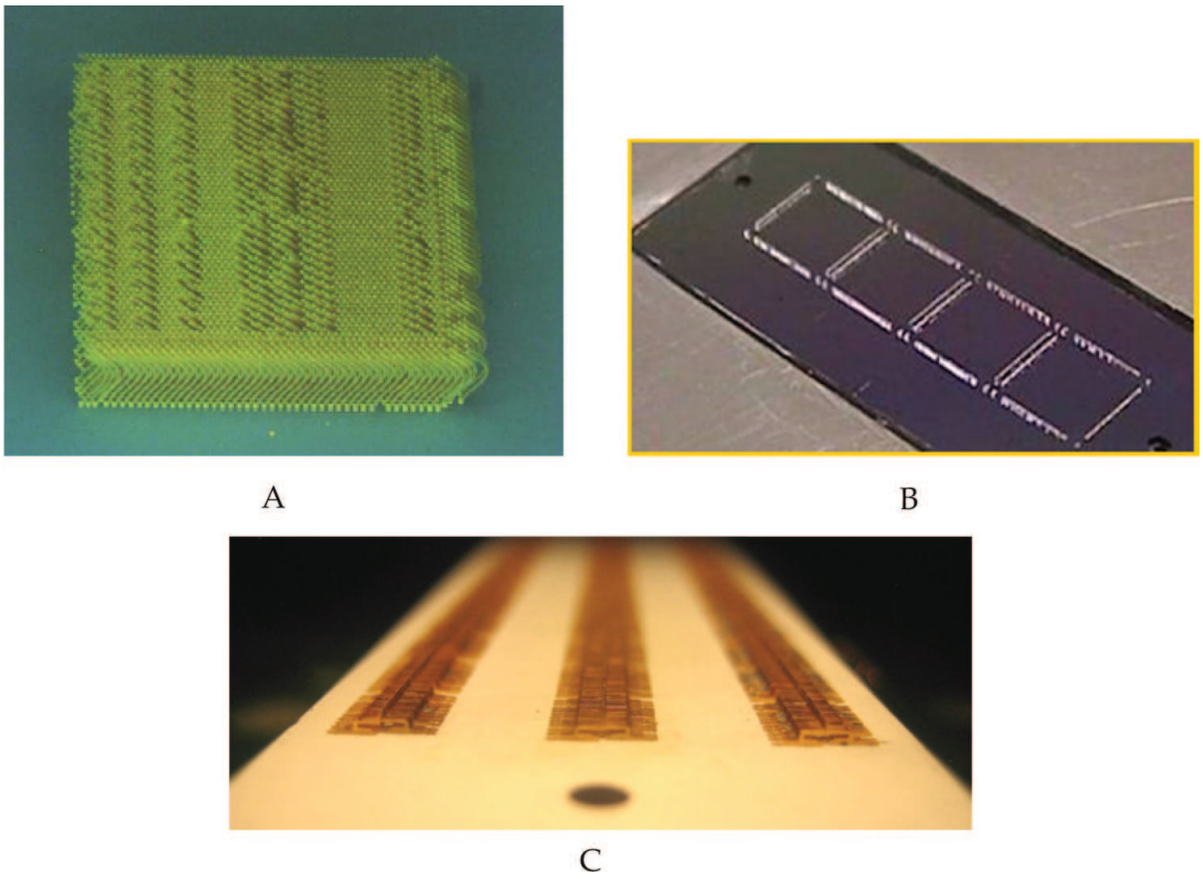

Figure 8. MEMS type advanced vertical probe technologies are used for (a) full area-array, (B) peripheral-rows or partial-array and (C) advanced cantilever probes for inline memory testing.

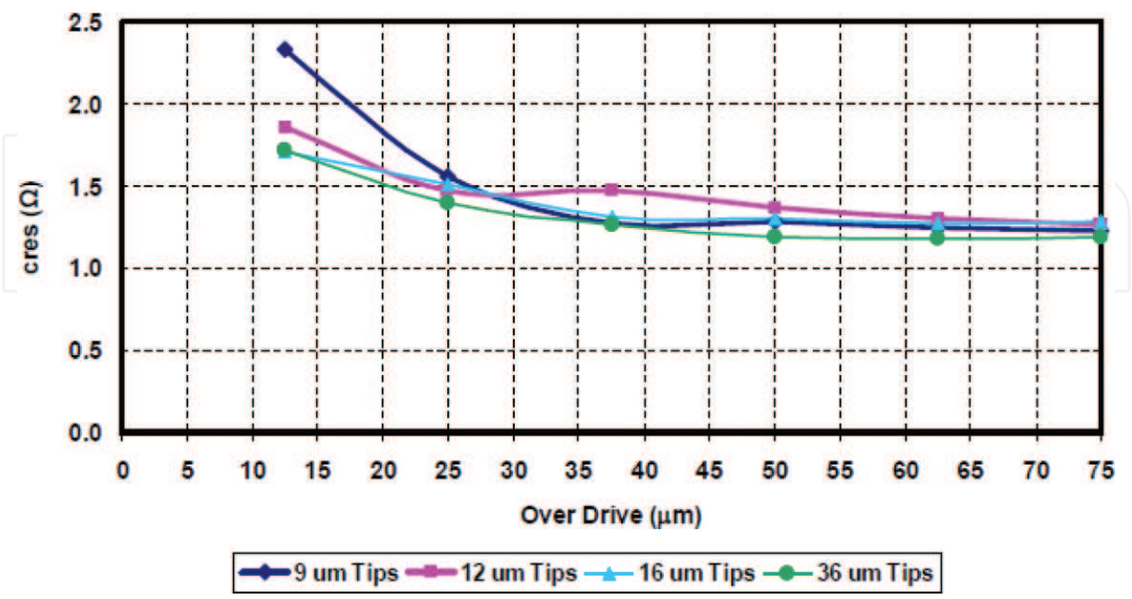

Figure 9. The results from the eutectic bump resistance measurements.

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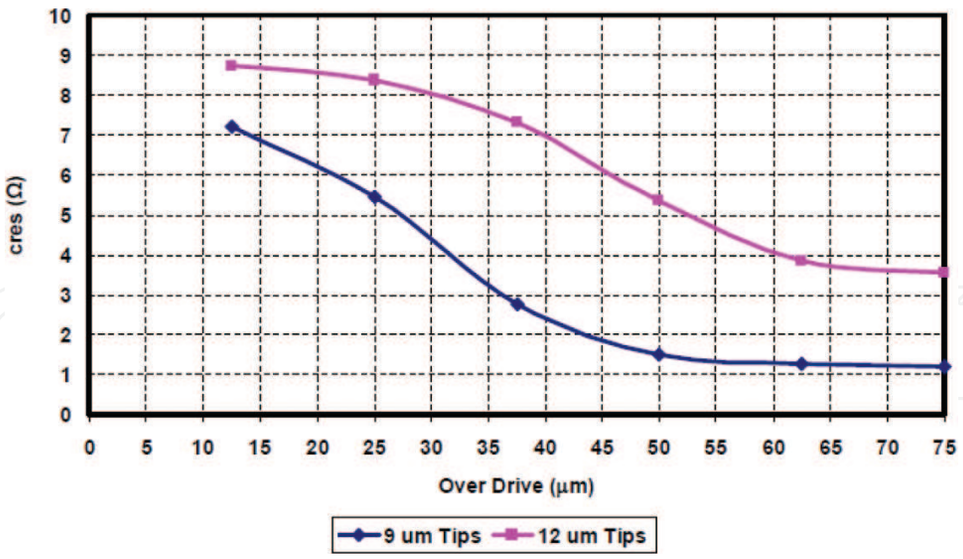

Figure 10. The eutectic bump resistance measurements done by MEMS-vertical probes on a test system are shown.

4. Next generation interconnects and substrates for probing systems

Higher levels of system integration and new IC technologies allow placement of significant test resources on the probe card, such as caps or resistors to very close proximity to the DUT, device supplies, digital channels and analog test circuitry, to improve signal integrity and performance. This capability helps overcome some test limitations, and make it possible to add RF test structures, and circuits enabling high-speed loop-back solutions. These solutions help in the cost-effectiveness of the test strategy. Advanced probe cards have to be designed to support high-speed testing and cold and hot temperature testing (from −55 to 150°C). Providing robust precision contact capability enables reliable contacts on smaller die sizes with better signal fidelity. Probe structures can be manufactured in a cost-effective way by MEMS methods to enable scaling to a finer bump pitch well below 50 µm area-arrays. Probe repair concepts are available on a restricted basis and this capability usually strongly requested by wafer test houses when high number of touchdowns on wafers is required.

4.1. Space transformers

Substrates are typically perform the function of space transformers in advanced probe cards, routing fine pitch of a device to a larger pitch of a PCB and tester boards in wafer test systems. Although the probe count is very large, memory type probe cards can handle 200mm or 300mm wafers due to device geometries with 1 or 2 row peripheral layouts. Space transformer in this case is typically a single-layer thin film on MLC.

Space transformers need to be able feature following requirements to support next generation advanced probe cards: (1) very low pitch fanout (30 µm), (2) high frequency operation with a high bandwidth of 3 GHz, signal length matching, low crosstalk for analog and digital

signal, shielding, (3) high pin counts for dense device designs (> 5000), (4) large arrays, (5) path resistance <2 Ohms, (6) no skip DUT and (7) peripheral device test with ore than 3 rows of pad per side and array configuration. Some of these requirements may not possible with MLC ceramic manufacturing with extra polyimide (PI) layers. Multilayer organic substrate (MLOs) is lower cost versions, but also have similar geometric and process limitations along with some thermal test restrictions.

MLS (multilayer substrate) is proposed as a type of silicon interposer manufacturable using MEMS technology to reach these target requirements. Space transformer technology comparison is provided for fine-pitch probing applications in **Figure 11**. WST stands for wired space transformer used in standard vertical probe cards. These are quickly changing with various capability enhancing feature every year. WST, MLC and MLO are well established while MLS and other high density ST scenarios are emerging. BGA and LGA stands for ball-grid array or land grid array versions of MLC. CTE is the coefficient of thermal expansion of a material.

Substrate interconnect process flow is shown in **Figure 12**(**A**, **B**) for creation of a silicon interposer with fine pitch and its bonding onto a MLC carrier. This type of a silicon interposer allows for fine pitch top surface routing capability for fanout on a MLC. Silicon interposer will have TSVs for connecting the top to bottom side. It features a probing contact pad on the surface and a bump connection to 200 μm-pitch MLC on the other side.

	WST	MLC +Multi layer thin film	MLO / MiniPCB	MLS-Novel
				
Material	•Copper alloy wire	•Ceramic (Alumina or HiTCE) •Tungsten or Cu conductor •Cu/PI Multilayer thin film	•Epoxy/PI/FR4 •Copper	•Si core •Cu/PI/SiOx Multi layer
Pitch mini & Configuration (density)	•In line : 60μm •Peripheral (1row) : 60μm •Peripheral (2row) : 60μm •Peripheral (3row) : 60μm*	•In line : 60μm •Peripheral (1row) : 60μm •Peripheral (2row) : 80μm (60μm w Skip) •Peripheral (3row) : 120μm (80μm w Skip) •Array : 120μm (PAD size is 35x35μm)	•In line : 100μm •Peripheral (1row) : 100μm •Peripheral (2row) : 200μm (100μm w Skip) •Peripheral (3row) : 200μm (200μm w Skip) •Array : 200μm (PAD size is about 50x50μm)	•target is 50μm or below at any configuration !
Pin count	1000	>5000 (for pitch >120μm)	>5000	>5000
Pros	•Cycle time •Cost •Probe depth adjustable •Generic PCB	•High pin count •BGA/LGA •Good mechanical resistance •Low CTE •Good electrical performance	•High pin count •Hard Gold possible •NRE lower than MLC •Shorter lead time than MLC •Good electrical performance	•Very low pitch potential •Hard gold •Low CTE •Good electrical performance
Cons	•Risky above 1000 wires •Electrical performance limitation	•Cost at low qty •Cycle time •Probe Depth limitation •Hard Gold none std	•Density & pitch limitation vs MLC/MLO •Probe Depth limitation •No PGA •Low mechanical stiffness (deflection) •Planarity after reflow	•New technology •Cost at low qty •Probe Depth limitation

Figure 11. The space transformer technology capabilities for advanced probe cards.

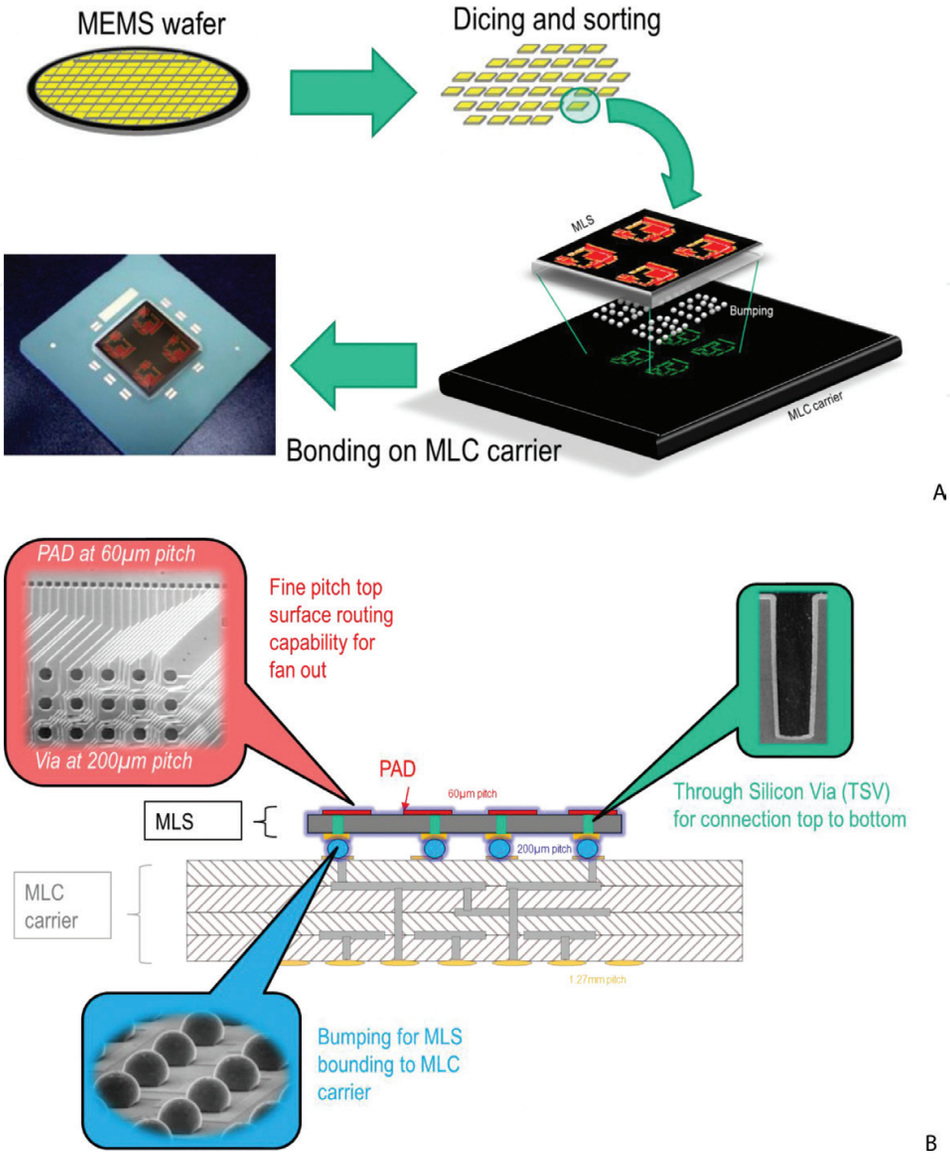

Figure 12. Substrate interconnect process flow is shown in (A) process steps for MLS and (B) substrate interconnect features.

MLC process may involve ceramic manufacturing process and additional polyimide (PI) process layers. Fine pitch on the surface is reached by stacking up three layers of PI. Vias on ceramic layer are routed to pad locations. As the pin count is raised, thin film layer count increases to match the required probing pads. In some cases as row count increases, then a test scheme requires skipping a DUT due to such substrate density restrictions. 3-row pad structure is shown in **Figure 13** and the pin count versus the pad density is also shown.

4.2. Copper pillar bumps

The increasing requirement for more functionality in smaller packages forces trends toward 3D packaging approaches for portability [8]. Higher routing density enabled by finer pitch flip chip technology using copper pillars is highly desirable for lower costs and

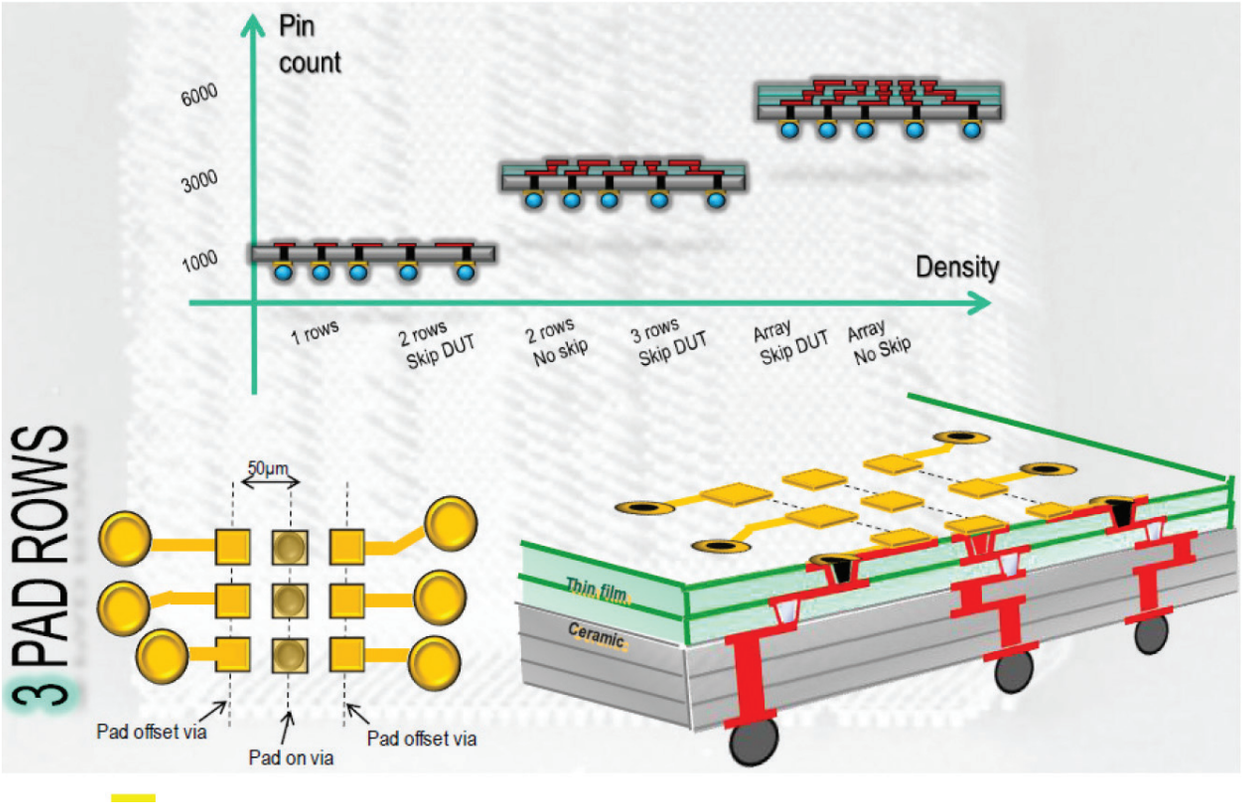

Figure 13. Density on substrates is illustrated for various configurations.

scalability. Copper pillar bumps typically consist of a copper base and a solder capped top [6]. These copper pillars, sometimes called high pillars or micro-bumps, act as an interconnect structure which lowers stress on low-k layers in finer silicon nodes and increase reliability. Use of such micro-bumps simplifies substrates for packages, thereby decreasing cost, and allows natural migration toward TSV technologies of the future. On the other hand, as the metallurgy of the bump structure changes from eutectic to lead-free solders and more importantly to solder-cap on copper pillars with varying contact geometries, probing very fine-pitch bumps presents new test, process and precision challenges [8]. There is also an increasing trend toward performing the final test in wafer level to reduce both cycle time and cost of test while moving to environment friendly manufacturing processes. It is important for IC design and packaging development and test engineers to understand the material impacts of new wafer bumping system and technology. They need to address both reliability and manufacturability of the entire process, which includes test process development early in the cycle so that the overall system level cost is optimized [8].

Probing of traditional solder bumps at 120 μm pitch or above, whether eutectic, high-lead or lead-free solder balls are performed typically by buckling beam/vertical technologies. The contact area formed on the top of a round bump after a probe contact is related to the metallurgy

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and the mechanical properties of bump materials as well as the probe tip geometry and probe force [6]. Fine-pitch technologies for ICs below 40-nm node are accelerating the move toward copper pillar lead-free bumps and interconnections. Probing lead-free solder micro-bumps or copper pillars at 40 μm-array pitch requires MEMS-style probe technologies. There are many known benefits of using copper pillars reported in the literature. **Figure 14** shows images of copper pillars and lead-free micro-bumps at 50 μm pitch. The bump profile on the right illustrates a minor scrub mark, 9 μm wide, on top of the Cu-pillar. In this case, the probe makes good and reliable electrical contact, however, the scrub signature is not easily seen on optical images because of the hardness of copper. **Figure 15** illustrates Sn-Ag based solder micro-bumps on top a copper pillar before and after probing at 50 μm pitch. The solder deformation is observed on the probed bump on the image on the left side. The solder bumps on the left are of eutectic type.

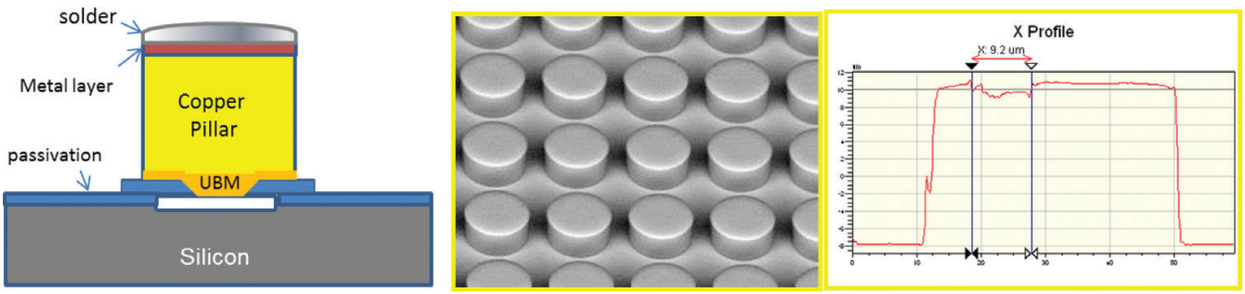

Figure 14. Images of copper pillars and lead-free micro-bumps at 50 μm pitch. The profile shows the pillar bump after probing with vertical MEMS probe technology.

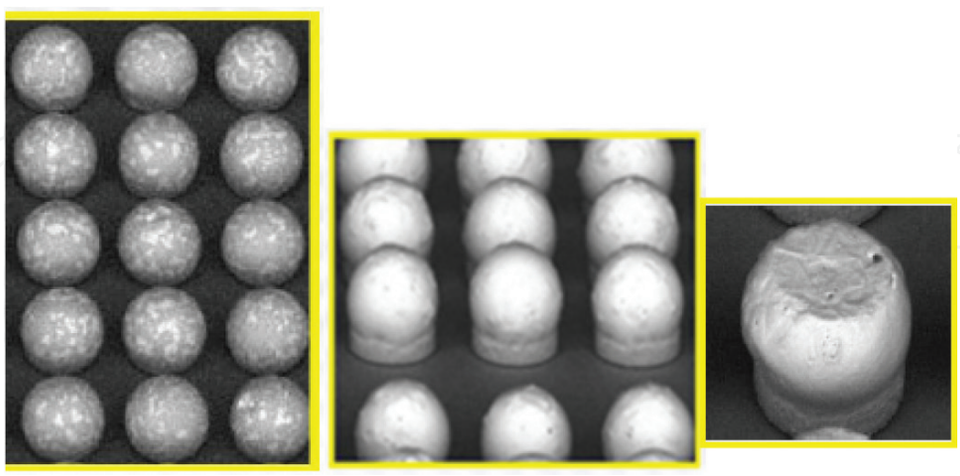

Figure 15. Solder micro-bumps illustrated on the left have no copper pillar-base. Solder micro-bumps on top a copper pillar before and after probing (on the right) at 50 μm pitch.

5. Final test and spring pins

The decision on how to partition test between wafer and package tests and where to focus efforts to increase parallel testing is always on the agenda of test practitioners in the industry. A wafer test probing is a short-cut in addressing both wafer test and package test, if it can be a bundled solution for productivity of the test floors. This potentially reduces total cost of test substantially. The trend nowadays is to focus on wafer sort in high parallelism mode.

The wafer level chip scale package (WLCSP) format has been rising and in the final test, there is strong push for cost-effective RF testing solutions [9, 10]. The spring-pin technology for the final test still inexpensive workhorse of the package test industry. The system board level functionality is moving into package-level (SiP) or chip-level (SoC) implementations. The spring pins, are not scalable at fine pitches and will not support test speeds necessary.

A socket-contactor design is proposed for reliable electrical contact and allows testing for best wafer yields. This type of approach must replace known vertical probe technology or membrane probe technology for testing wafer level packages. A novel contactor and socket were designed for high performance and low-cost for use in wafer probe or final test [11].

Figure 16 shows a socket test system overview showing a load-board and device under test (DUT) with a ball-grid-array (BGA) in contact with traditional spring pins, that is, pogo pins™. The DUT can be packaged as BGA with bumps or land grid array (LGA) and the contactor pin geometry will change depending on the pad/bump materials and contact surfaces [11].

The proposed design of new contactor is illustrated in **Figure 17** including a plunger, spring wire and the socket with a retaining plate. The contactor consists of a plunger pin made of beryllium copper and a braided stainless steel spring wire. The spring wire is typically copper over-plated. The socket materials with retaining plates were made of FR4. The overall

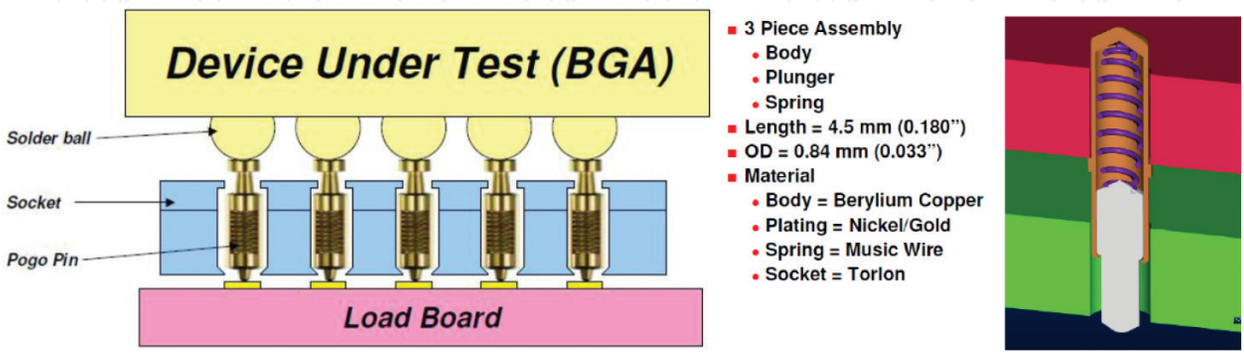

Figure 16. A pogo pin socket system overview.

diameter of the spring wire section was 0.51 mm. The contactor has a 5 mm in uncompressed total length including the plunger and the spring. The length of the spring wire section was 0.27 mm.

The measurement results in **Figure 18** show the contact resistance behavior of the spring assembly for SS304V/Cu plated with Ni/Au contacts in a 36-Pin test socket. SS304 stands for stainless steel spring wire and Cu, Ni and Au are overplating applied to the spring to improve the electrical performance characteristics. S parameter characterization has shown better results than those of traditional spring pins. **Figure 19** shows electrical simulation results for pitches of 0.8, 1.6 and 2.5 mm are shown. Insertion loss was estimated to be at −1 dB bandwidth as 5.025 GHz (A). Return loss of −16 dB at 4 GHz is illustrated at (B).

The plunger pin and stainless steel spring wire can be manufactured with MEMS processes to make them scalable to much finer pitches than these versions can support.

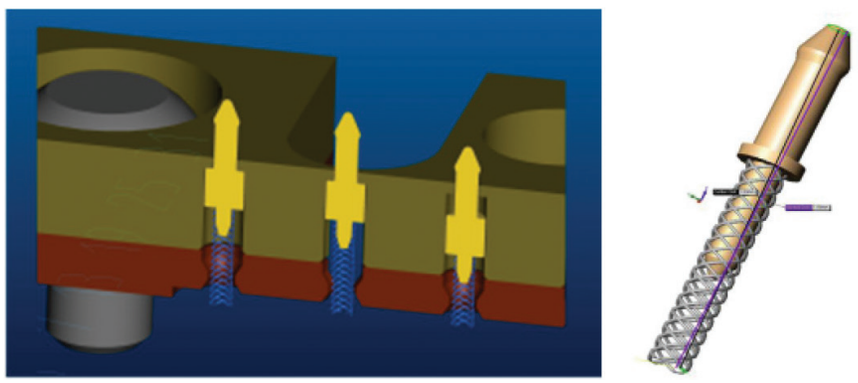

Figure 17. Prototype of new contactor design showing the plunger and the spring sections held in a retaining plate.

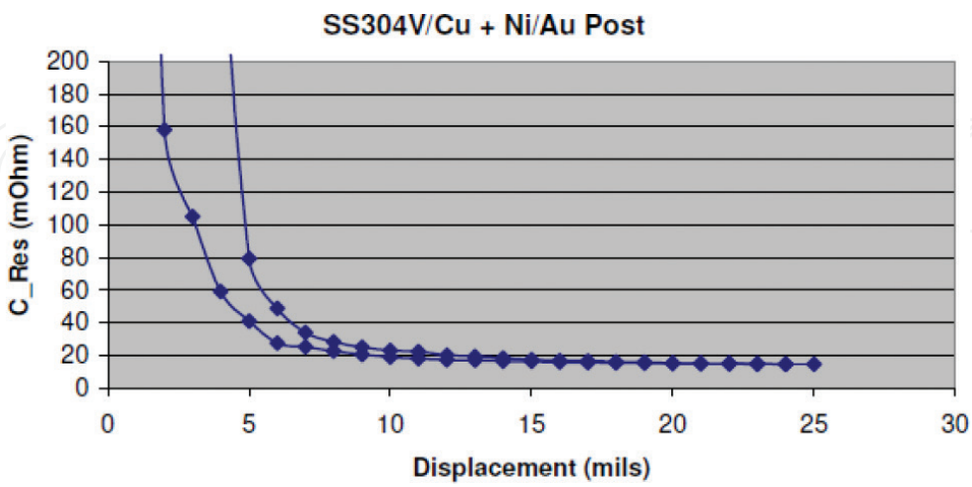

Figure 18. The contact resistance behavior if the plated spring contact.

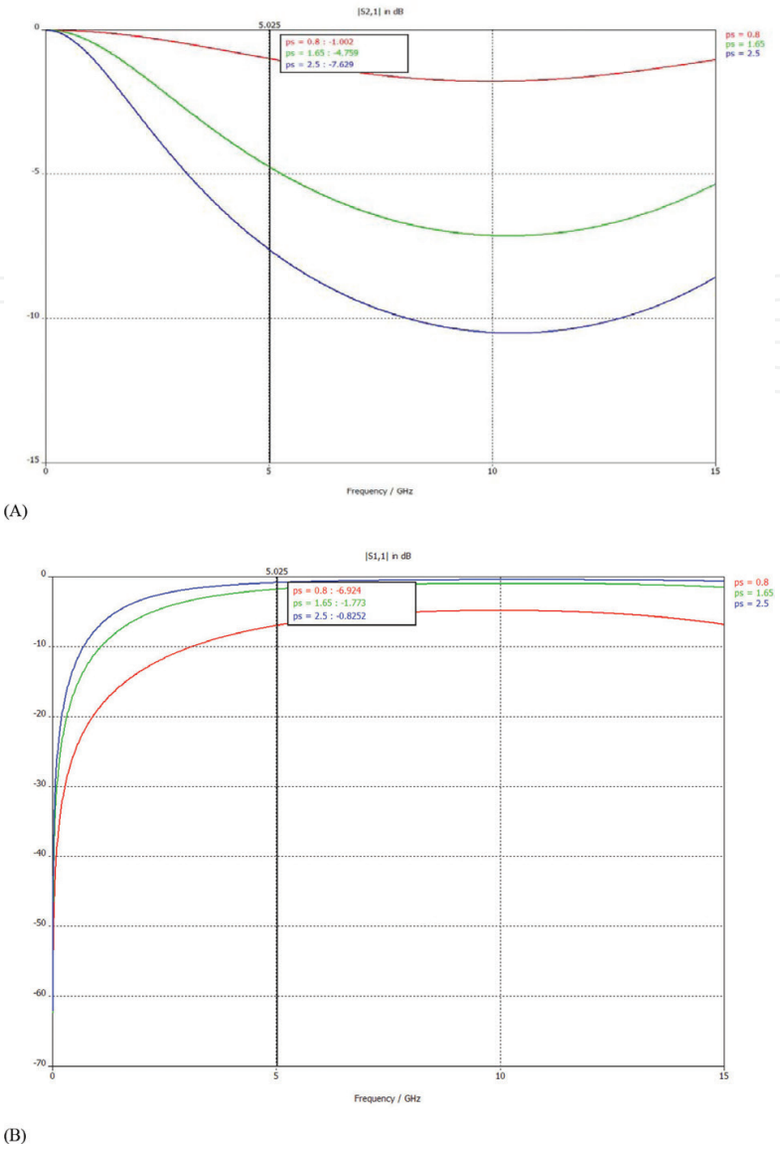

Figure 19. Simulation results for pitches of 0.8, 1.6 and 2.5 mm are shown. (A) Insertion loss, −1 dB bandwidth is 5.025 GHz (top). (B) Return loss of −16 dB at 4 GHz.

6. Conclusions

Wafer test systems and enabling requirements for effective testing of mixed signal, logic and memory ICs were reviewed. TSVs and 3D packaging are evolving and making silicon interposers available and high performance stacked die packages without wire-bonding. Silicon interposers using TSV technology based on MEMS processes can be utilized in probe card assemblies to enable next generation fine-pitch vertical probing. MEMS technologies are being developed for manufacturing of novel high density substrates and fine-pitch probes for cantilever as well as vertical probing. MEMS technologies already dominate the memory test market. It is clear though the overall market is trending toward MEMS technologies and purely vertical, cantilever, blade technology or others will shrink in probe card market and advanced MEMS technologies will win.

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