Chapter 6

Optical Proximity Correction (OPC) Under Immersion Lithography

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Additional information is available at the end of the chapter

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Abstract

As advanced technology nodes continue scaling down into sub-16 nm regime, optical microlithography becomes more vulnerable to process variations. As a result, overall lithographic yield continuously degrades. Since next-generation lithography (NGL) is still not mature enough, the industry relies heavily on resolution enhancement techniques (RETs), wherein optical proximity correction (OPC) with 193 nm immersion lithography is dominant in the foreseeable future. However, OPC algorithms are getting more aggressive. Consequently, complex mask solutions are outputted. Furthermore, this results in long computation time along with mask data volume explosion. In this chapter, recent state-of-the-art OPC algorithms are discussed. Thereafter, the performance of a recently published fast OPC methodology—to generate highly manufactured mask solutions with acceptable pattern fidelity under process variations—is verified on the public benchmarks.

Keywords: immersion lithography, optical proximity correction (OPC), mask, edge placement error (EPE), process variability band (PV band), runtime, mask manufacturability, kernel

1. Introduction

Optical microlithography provides a feasible solution in the foreseeable future for advanced technology nodes patterning with its relatively cheap equipment, if compared with other fabrication techniques. An integrated circuit (IC) design level elements are represented as a set of polygons that are carved onto a pixelated template, called the mask. Mask image is then projected onto a photoresist coating the silicon wafer through an exposure tool. If sufficient light intensity is projected onto the resist, it is chemically exposed. Exposed regions are then etched to form the target circuitry pattern onto the silicon wafer [1, 2].

Complex circuit is made up by repeating lithographic operation for each layer. With the continuous shrinkage of critical dimensions (CDs) of advanced technology nodes following Moore's law, IC dimensions are being pushed into sub-16 nm according to the International Technology Roadmap for Semiconductors (ITRS) [3]. Thus, light diffraction and interference impact becomes pronounced during circuit printing, which results in wafer image quality degradation. For example, corners are rounded and lines are shortened. Such distortions in the wafer image impact circuit functionality and performance. Besides, it could result in circuit malfunction [4, 5].

To reduce the minimum printable CD, wavelength of the illumination source of the optical system had been steadily reduced till it reached its practical limit at 193 nm due to high instability and strong birefringence of lens materials [6]. Immersion lithography has been introduced to improve the resolution through filling the gap between wafer and projection lens with purified water for higher numerical aperture. However, CD of technology nodes continues scaling down to become small fractions of the wavelength. This makes 193 nm immersion lithography insufficient for modern ICs printing [7].

Resolution enhancement techniques (RETs) aim to improve wafer image quality through manipulating the amplitude and phase of the optical wave to pre-compensate wafer image distortions [8]. Since next-generation lithography (NGL) is still not mature enough, the industry relies heavily on RETs, wherein optical proximity correction (OPC) is dominant, to print sub-16 nm technology nodes in the foreseeable future [9].

In OPC, a mask pattern is iteratively adjusted to obtain an acceptable wafer image quality. However, a lithographic process is susceptible to raw process variations, which result in lithographic yield degradation. Since finding an optimal mask solution with acceptable wafer image quality under all possible process conditions is infeasible, the industry defines a process window including a set of process conditions upon request. The most probable process condition is often defined as nominal process condition under which acceptable wafer image quality is desired with minimizing the variations between different images within the process window [10, 11].

To keep pace with advanced technology nodes, model-based OPC algorithms get increasingly more aggressive. Consequently, complex mask solutions are outputted, which results in mask manufacturability degradation along with explosion in mask data volume [12, 14].

OPC computation time forms another crucial factor. For example, brute force algorithms to find optimal mask solutions are infeasible for industrial cases, wherein, mask data have to be prepared in a matter of hours to cover the huge number of target circuitries [10, 13].

In this chapter, recent state-of-the-art OPC algorithms are discussed. Thereafter, a recently published algorithm in [15, 16] is deeply analyzed and its performance is verified in terms of pattern fidelity under process variations, mask manufacturability, and computation time.

The rest of this chapter is organized as follows: Section 2 briefly discusses recent OPC algorithms and their main shortcomings. Section 3 describes lithographic terminology and mask evaluation metrics. Sections 4 and 5 discuss intensity modeling and the to-be-evaluated OPC methodology, respectively. Experimental results are proposed in Section 6, and Section 7 concludes the chapter.

2. Recent research

Several algorithms have been proposed to minimize edge placement error (around wafer image contours) in model-based OPC. Mask error enhancement factor (MEEF) matrix has been widely adopted to guide edge shifting following EPE changes in each fragment control point [17, 18]. However, such algorithms slowly converge for advanced technology nodes. Source and mask optimization has been proposed in [19] at the cost of long computational time. A fast intensity-based algorithm has been proposed in [20]. However, this algorithm considers only sparse patterns, while recent dense patterns are more challenging. Adaptive fragments refinement has been proposed to improve wafer image quality without significantly considering process variations [21].

Process window OPC algorithms consider both EPE and process variations [22, 23]. However, wafer image has to be simulated under each process condition, which is time-consuming.

Retargeting has been adopted to improve pattern fidelity through modifying the target pattern itself along with the mask at the cost of long computation time [24]. Process variations have been effectively considered through including the intensity slope in the cost function in simultaneous mask and target optimization (SMATO) algorithm [25].

Inverse lithography technology (ILT) has been extensively exploited to find optimal mask solutions based on rigorous mathematical models [26, 27]. However, ILT masks are hard to be manufactured due to ILT pixel-based behaviors.

Sub-resolution assist features (SRAFs) insertion has been widely exploited to increase mask robustness against dose variations [28, 29]. Consideration of multiple process conditions is required upon SRAF insertion/sizing.

To improve mask manufacturability without sacrificing lithographic yield, design aware OPC algorithms include a set of restricted design rules (RDRs) in the OPC recipe. RDRs define the minimum dimensions in mask geometry [30, 31]. Although including RDRs in the OPC preserves acceptable pattern fidelity with less complex masks, long computation time is expected due to the low stability and slow convergence of the algorithm.

To accelerate OPC computation, a fast method has been proposed in [32] to simulate wafer image with less number of kernels. However, using more kernels is required in further iterations. Intensity difference map has been recently proposed in [15] and its performance has been confirmed in [33].

Recently, an effective Process Variation Aware OPC algorithm, namely PV-OPC, has been proposed with good results in terms of pattern fidelity under process variations, computational time, and with considering mask notch rule for higher manufacturability through exploiting variational EPE, and adaptive fragmentation [9]. Furthermore, PV-OPC effectively reduces the number of needed simulations. Mask Optimization Solution with Process Window Aware Inverse Correction (MOSAIC) algorithm has been recently proposed as an ILT algorithm with exploiting variational EPE under each process corner. MOSAIC has two versions: fast and exact [34]. However, complex masks are outputted from this algorithm. A robust approach for process variation OPC has been recently published in [35] at the cost of outputting complex masks.

Recently, a novel intensity-based OPC methodology has been published in [15]. This algorithm outperforms the most recent effective algorithms on the public benchmarks in terms of pattern fidelity under process variations and runtime. Besides, this algorithm has been extended to improve mask manufacturability in [16] with preserving its effectiveness. This algorithm is analyzed in this chapter and its effectiveness is numerically verified through comparing it with other recent algorithms on the most challenging public benchmarks.

3. Lithographic terminology and problem description

A lithographic process is susceptible to raw process variations resulting in lithographic yield degradation. Dose and focus variations are dominant in this context. Thus, a set of dose and focus process conditions that are requested to be considered are defined as a process window P_w.

3.1. Lithographic pattern terminology

Given a region of pixels R wherein a target pattern T is defined such that $T \subset R$. Similarly, a mask pattern M is defined in R such that $M \subset R$.

A pattern consists of a set of nonoverlapped rectilinear polygons where a polygon consists of a set of connected pixels. Let S be a polygon. If a pixel p is contained in S, it is denoted by $p \in S$. Furthermore, if $p \in S \in T$, it is denoted by $p \in T$. The same notation is applied for a pixel $p \in S \in M$, which is simply denoted by $p \in M$.

An edge on the boundary of a polygon is either a horizontal or vertical line connecting two corners. Let E_T and E_M be the set of edges along the boundary of all polygons in T and M, respectively. Let $l(e)$ denote the length of an edge e and $D(e_i, e_j)$ denote the Manhattan distance between edges e_i and e_j in a target/mask pattern.

Target pattern: A set of target design rules are defined to be satisfied. This includes: (1) minimum allowable line width, denoted by L_w. (2) Minimum spacing between different polygons, denoted by L_s. Note that, $e \in E_T$; $l(e) \geq L_w$.

A corner on the boundary of a polygon in the target is either positive or negative. A positive corner forms 90° angle outside the polygon, while a negative corner forms 270° angle inside the polygon. **Figure 1(a)** illustrates a target pattern with both types of corners [15].

Mask pattern: Mask pattern polygons are classified into three types: core-polygon, serif, and SRAF. **Figure 1(b)** shows these types. A core-polygon that corresponds to a polygon $S \in T$ is obtained from S by fragmenting its boundary to segments and shifting them. A segment located on a corner in the target pattern is said to be a corner segment. A serif on a positive corner is a squared feature added outside of the polygon, while, a serif on a negative corner is a square picked from the polygon. An SRAF (scatter bar) is a long bar parallel to an edge of a polygon in the target [15].

A notch is either peak or valley in the polygon geometry, as illustrated in **Figure 2(a)** [36]. From mask manufacturing perspective, thin notches are forbidden. A jog is the orthogonal edge between two neighboring edges in the mask boundary. Small jogs in an OPC mask typically

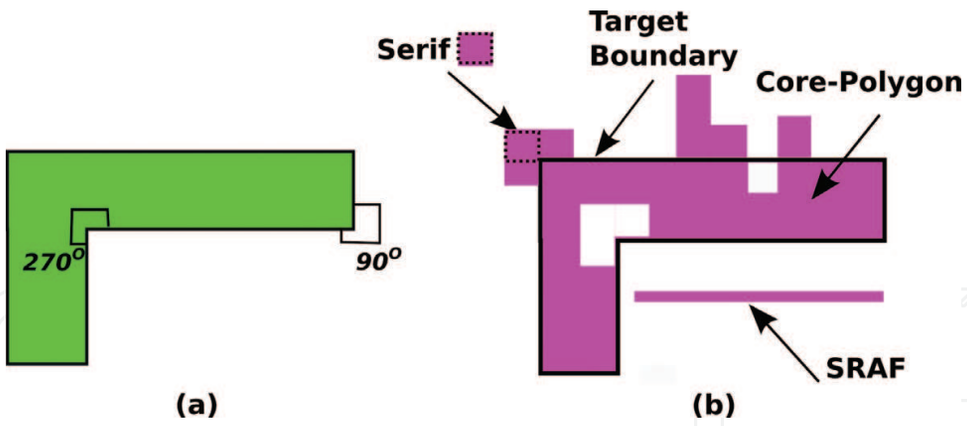

Figure 1. (a) Target pattern T. (b) Mask pattern M [15].

exist, as shown in **Figure 2(b)**. However, such small features increase shot count during mask writing [12]. Moreover, they increase mask manufacturing process variations, which turns out into pattern fidelity degradation.

Mask design rules define a set of constraints to be satisfied in a mask pattern for higher mask manufacturability. In this chapter, the following mask design rules are considered: (1) mask notch rule, which defines the minimum allowable edge length in the mask boundary, denoted by d_n. (2) Mask spacing rule, which defines the minimum allowable spacing between patterns in the mask pattern, denoted by d_s.

3.2. Lithographic model

A mask M is transformed through an optical and projection system into an aerial image. This image is an intensity map holding a set of light intensities floating onto the resist. The set of exposed pixels within the intensity map forms the image onto the silicon wafer. Let $I_{Pc}(M)$ and $G_{Pc}(M)$ represent the intensity map and wafer image of mask M under process condition $P_c \in P_w$, respectively, as illustrated in **Figure 3**.

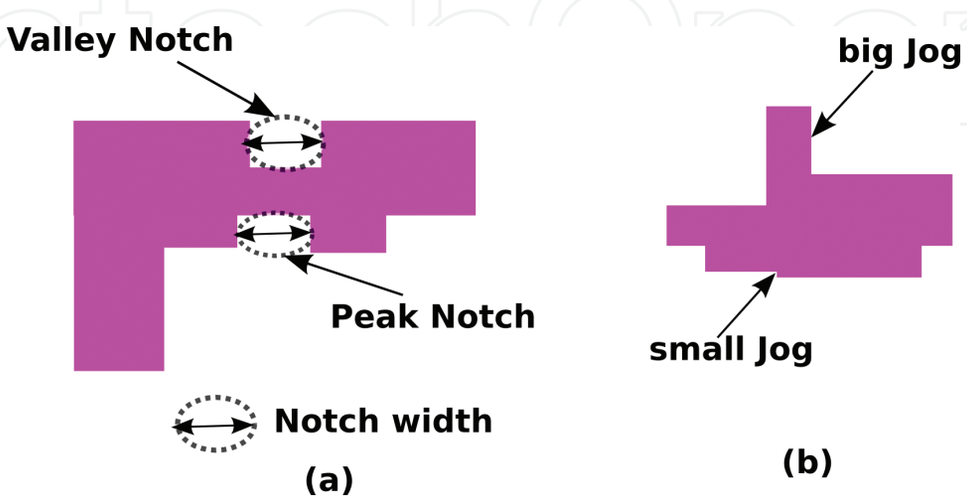

Figure 2. (a) Notch types and width and (b) jogs in the mask boundary.

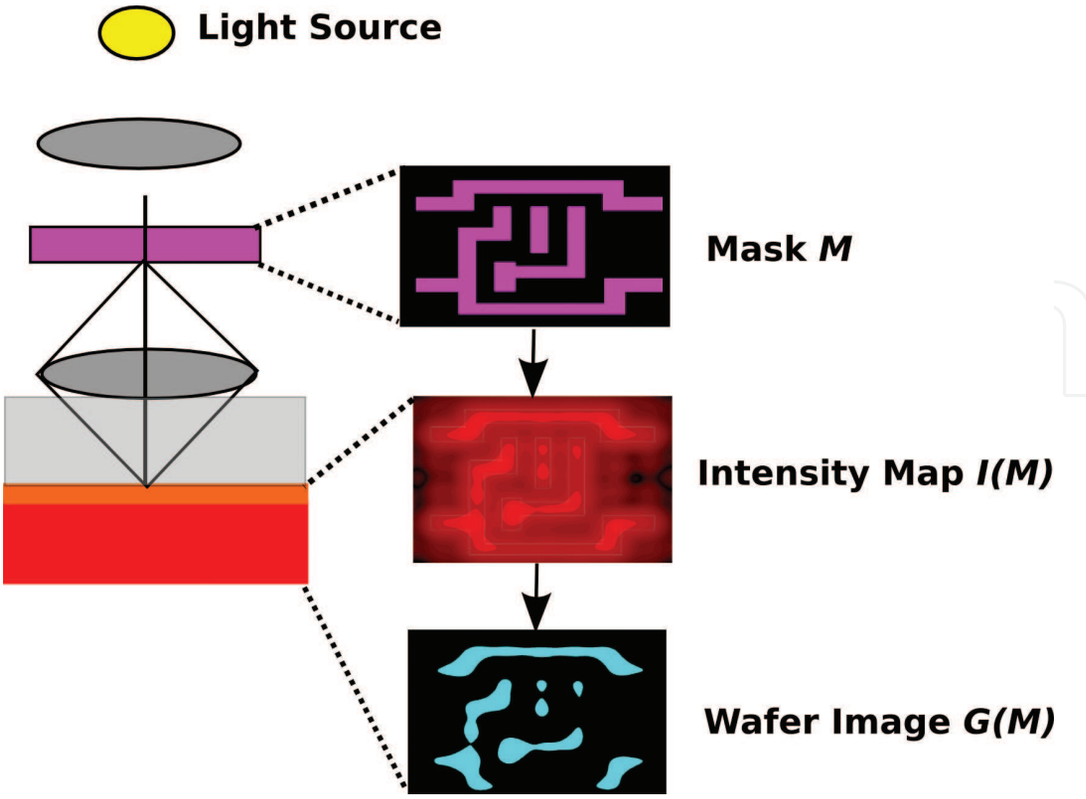

Figure 3. Intensity map and wafer image for a given mask pattern.

Sum of coherent systems (SOCS) is often used in OPC to roughly estimate the intensity map [38]. In SOCS model, the optical system is decomposed into a set of coherent kernels working as low pass filters. Each kernel has an eigenfunction, which represents its filtering behavior and eigenvalue and its weight for intensity estimation. For a mask M, intensity map, $I_{Pc}(M, K)$, under process condition P_c is defined as given in Eq. (1), where K denotes the set of all kernels in a lithographic system, ${\sigma_k}^{p_c}$ and $\phi_k^{P_c}$ represent the eigenvalue and the eigenfunction for kernels $k \in K$ under process condition P_c, respectively, and $\otimes$ denotes convolution operation.

$$I_{p_c}(M) = \sum\nolimits_{k \in K} {\sigma_k}^{p_c} \left| \phi_k^{P_c} \otimes M \right|^2 \tag{1}$$

Once intensity map is obtained, it undergoes resist modeling. Constant threshold resist (CTR) is one of the commonly used resist models, wherein intensity threshold of exposure I_{th} is predefined. Wafer image $G_{Pc}(M)$ is the set of pixels whose intensities are greater than or equal to I_{th}, as given in Eq. (2), where $I_{Pc}(M, p)$ represents the intensity in pixel p by mask M.

$$G_{P_c}(M) = \{p \in R | I_{P_c}(M) \geq I_{th}\} \tag{2}$$

3.3. Representative lithographic process conditions

Wafer image gets wider with higher positive dose values. On the other hand, it gets thinner with negative values. Defocus impact causes wafer image to be thinner than its form under

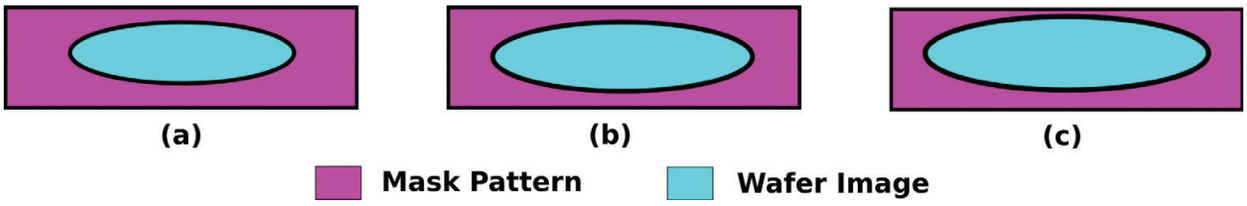

Figure 4. Representative wafer images: (a) innermost, (b) nominal, (c) outermost.

nominal focus condition [9]. Thus, for a process window P_w, three representative process conditions are defined as follows (illustrated in **Figure 4**):

1. Innermost process condition: Includes the maximum negative dose value and defocus under which innermost intensity map $I_i(M)$, is defined. Innermost wafer image $G_i(M)$ is extracted from $I_i(M)$.
2. Outermost process condition: Includes the maximum positive dose and in-focus under which maximum intensity map $I_o(M)$, is defined. Outermost wafer image $G_o(M)$ is extracted from $I_o(M)$.
3. Nominal process condition: Includes average dose and in-focus under which nominal intensity map $I_n(M)$, is defined. Nominal wafer image $G_n(M)$ is extracted from $I_n(M)$.

3.4. Mask evaluation metrics

A mask pattern is evaluated in terms of the pattern fidelity under nominal process condition, robustness against process variations, mask manufacturability, and the computation time required to find that mask solution.

Pattern fidelity evaluation: Edge placement error (EPE) is often used for pattern fidelity evaluation under nominal process condition. EPE is the geometrical distance between a point on the target boundary and its corresponding point onto wafer image contour. Let $epe(M, t)$ denote the EPE for a point $t \in T$, as shown in **Figure 5**. As long as no electric violations occur in the circuit functionality, EPE evaluation can be relaxed. Let EPE_{max} be the maximum allowable EPE distance [10].

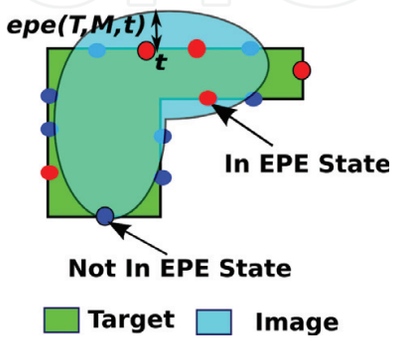

Figure 5. EPE evaluation [15].

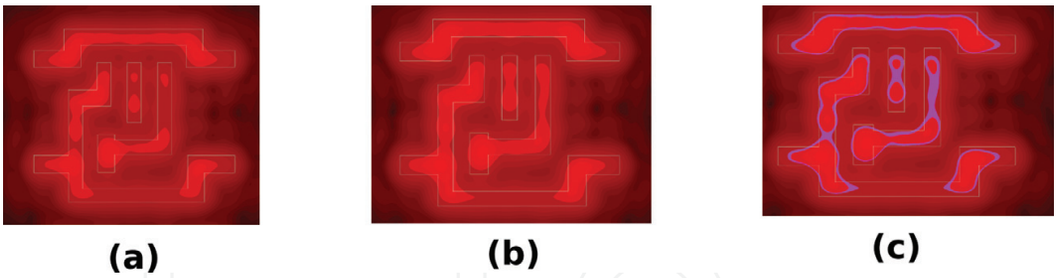

Figure 6. (a) Innermost intensity map, (b) outermost intensity map and (c) PV band area.

For fast evaluation, EPE is statically measured among a set of tap points defined on the boundary of *T*, as given in **Figure 5**. Let *A* denote the set of defined tap points. For each $t \in A$, let $t^+ \in T$ be a point whose distance from *t* is EPE_{max} pixels, which is on the line that passes *t* and perpendicular to its edge in the target. Similarly, $t^- \in T$ is defined but inside the polygon in *T*. For a tap point $t \in A$, it is said to be not in EPE state if $I_n(M, t^-) \geq I_{th}$ and $I_n(M; t^+) < I_{th}$. Otherwise, *t* is said to be in EPE state. The number of EPE violations for mask M, denoted by $\#EPEV(M)$, is the number of tap points in EPE state. Pattern fidelity of a mask *M* is assumed to be inversely proportional to $\#EPEV(M)$ [15].

Process variability evaluation: Process variability (PV) band area is a commonly used metric for process variations. PV band area is the area denoted by XORing wafer images under all process conditions within process window P_w.

Innermost and outermost wafer images are exploited to provide a fast and roughly sufficient estimation for PV band area. For a mask *M*, PV band area, denoted by $PV(M)$, is the XOR area between $G_i(M)$ and $G_o(M)$. The less the PV band area, the more is the mask robustness against process variations. **Figure 6** illustrates PV band area for a given mask [17].

Mask manufacturability evaluation: Mask manufacturability is evaluated in terms of satisfying mask notch and spacing design rules. The more the rule violations, the lower is the manufacturability of the mask. **Figure 7(a)** illustrates examples of design rule violations. Mask notch rule defines the minimum allowable edge length in the mask polygons, denoted by d_n. Thus, the number of mask notch rule violations of mask *M*, denoted by $\#NotchV(M)$, is formulated as in Eq. (3):

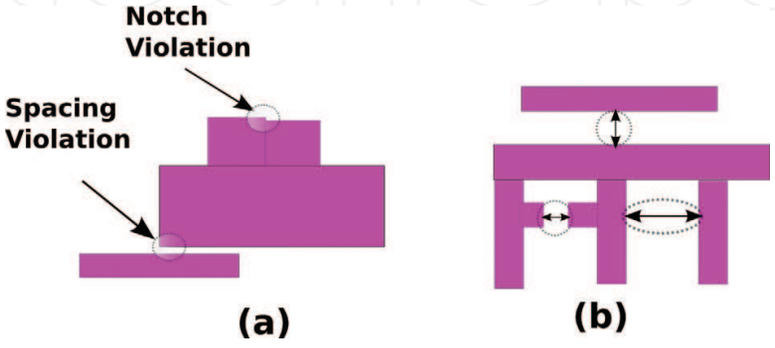

Figure 7. (a) Design rule violations and (b) comparison pair examples [16].

$$\#NotchV(M) = |\{e|e \in M; l(e) < d_n\}| \tag{3}$$

Two edges in the mask boundary violate mask spacing rule if the Manhattan distance between them is less the minimum allowable spacing distance d_s. However, both edges should either belong to two different polygons or belong to the same polygon without overlapping between them, as illustrated in **Figure 7(b)**. Such edges are said to be a comparison pair. Consequently, the number of spacing rule violations, denoted by $\#SpaceV(M)$, is given in Eq. (4), where C_p represents the set of comparison pairs in M. Comparison pairs of a mask can be retrieved by bounding techniques [16].

$$\#SpaceV(M) = |(e_i, e_j)|(e_i, e_j) \in C_p, D(e_i, e_j) < d_s| \tag{4}$$

4. Tap point intensity estimation

The purpose of the proposed intensity modeling in [17] is to roughly estimate the intensity map of a mask using SOCS model within a short time. As lower weight kernel contribution in intensity value is typically small [32], such contribution in intensity value for each pixel does not dramatically change much if a mask pattern is slightly modified. On the other hand, top weight kernel contribution is significantly affected by such mask modifications. Thus, by utilizing lower weight kernel intensity information of some reference mask, the intensity map of a general mask can be estimated using only top weight kernel, followed by proper compensation with exploiting the intensity information of the reference mask.

4.1. Top weight kernel intensity modeling

Let $F_1(d)$ and $F_2(d)$ be the functions that represent the intensity impact induced by a segment to its own tap point and to the neighbor tap point, respectively, where d represents the shifting distance of that segment from its original position in the target T. The differences of intensity impact to a segment tap point and to neighbor tap point between cases when the shifting distances of that segment are d and d' are represented by $F_1(d, d')$ and $F_2(d, d')$, respectively. Let $B(w)$ represent the intensity impact induced by a serif feature on a corner to tap point t located on a corresponding corner segment, where w represents the width of the serif. The differences of intensity impact between cases when the widths of the serif are w and w' are represented by $B(w, w')$ [15].

With assuming the linearity of F_j as proposed in [15], $F_j(d, d') = F_j(d') - F_j(d) = \alpha_j$ (d′ − d), where α_j is a constant ($j = 1, 2$) obtained by regression. Additionally, it is assumed that B is a quadratic function such that $B(w, w') = B(w') - B(w) = \beta\ (w' - w)^2 + \gamma\ (w' - w)$, where β and γ are constants obtained through regression.

Let $(s_0, s_1, \ldots, s_m)$ be a sequence of segments defined along the edge between corner c_0 and c_1 on the boundary of a polygon in T by fragmentation, and t_i be the tap point of s_i ($0 \geq i \geq m$). Let d'_i and d_i be the shifting distances from the boundary in the target T for segment s_i in masks M and M_{ref}, respectively. In addition, let w_j' and w_j be the widths of serif feature on a corner c_j in masks M and M_{ref}, respectively ($0 \geq i \geq m$, $0 \geq j \geq 1$). **Figure 8** depicts the given situation. With exploiting

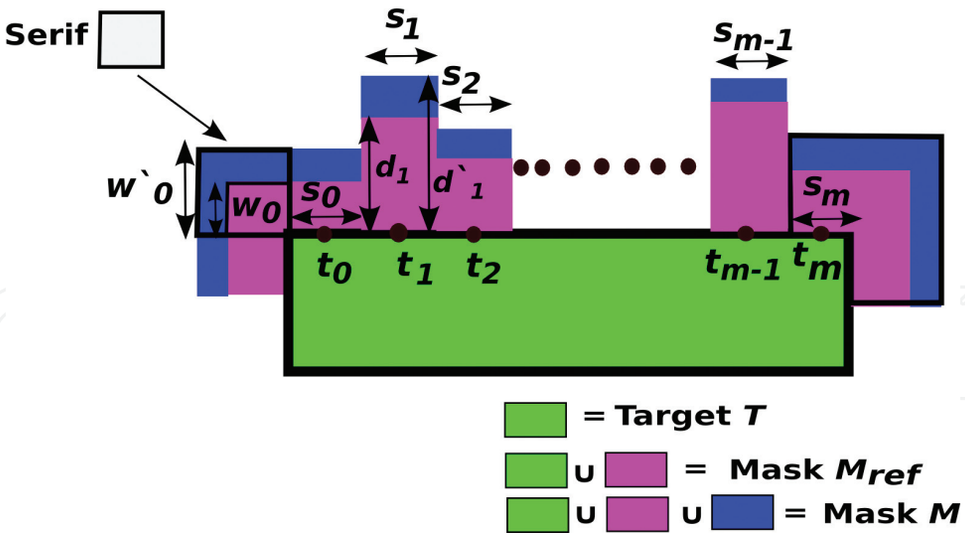

Figure 8. Top weight kernel modeling situation [17].

top kernel modeling, the intensity I_{Pc} (M, t_i) of tap point t_i under process condition P_c is given in Eq. (5) for corner segment and in Eq. (6) for non-corner segment, where $\Delta x = x' - x$ [17].

$$\begin{aligned} I_{P_c}(M,t_0) &\approx I_{P_c}(M_{\text{ref}},t_0) + B(w_0,w\prime_0) + F_1(d_0,d_0') + F_2(d_1,d_1') \\ &\approx I_{P_c}(M_{\text{ref}},t_0) + B(w_0,w_0') + \alpha_1\triangle d_0 + \alpha_2\triangle d_1 \end{aligned} \tag{5}$$

$$\begin{aligned} I_{P_c}(M,t_i) &\approx I_{P_c}(M_{\text{ref}},t_i) + F_2(d_{i-1},d_{i-1}') + F_1(d_i,d_i') + F_2(d_{i+1},d_{i+1}') \\ &\approx I_{P_c}(M_{\text{ref}},t_i) + \alpha_1\triangle d_i + \alpha_2(\triangle d_{i-1} + \triangle d_{i+1}) \end{aligned} \tag{6}$$

4.2. Lower weight kernel intensity modeling

Intensity difference map (IDM) is introduced as the mathematical difference between two intensity maps obtained using two sets of kernels [33]. Let I_{diff} (M, K, K') be the IDM between intensity maps $I(M, K)$ and $I(M, K')$, where $I(M, K)$ denotes the intensity map obtained using set of kernels K and $K' \subset$ K, respectively, as formulated in Eq. (7).

$$I_{diff}\left(M,K,K`\right) = I_{P_c}(M,K) - I_{P_c}\left(M,K`\right) \tag{7}$$

Typically, there is a trade-off between intensity map accuracy and the number of kernels used to obtain that map. However, with relaxed EPE evaluation, a set of top weight kernels in a lithographic system can be sufficient to be used for in intensity estimation, and thus, to guide the OPC response. Let K denotes the set of all kernels and $K_{suff} \subset$ K denote the set of top weight kernels roughly sufficient for optimization. Besides, let $k_0 \in$ K denote the top weight kernel [15].

In lower weight kernel modeling, intensity map for a mask M is roughly estimated through using a reference mask M_{ref} (both M and M_{ref} have been derived from the same target) as follows: The IDM of mask M_{ref} under a certain process condition is obtained using K_{suff} and

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$\{k_0\}$. To estimate the intensity map of mask M, IDM works as a compensative map to the top weight kernel intensity map as given in Eq. (8). This modeling reduces effectively the simulation time since only one convolution operation is required [15].

$$I_{P_c}(M) \approx I_{P_c}(M, \{k_0\}) + I_{diff}\left(M_{ref}, K_{suff}, \{k_0\}\right) \tag{8}$$

5. OPC engine framework

Figure 9 illustrates the general framework of the OPC engine proposed in [15, 16]. Before performing the actual OPC algorithm, a preprocessing phase, wherein, the parameters that guide OPC algorithm are found through regression. The input of the OPC algorithm is a target pattern and the output is a mask solution. This algorithm consists of initialization phase, input intensity modeling, mask correction phase, mask evaluation, and post-OPC phase.

5.1. Initialization phase

This phase aims to accelerate the algorithm convergence through finding an initial mask solution whose pattern is not much deviated from the final mask solution. Initialization phase includes the following:

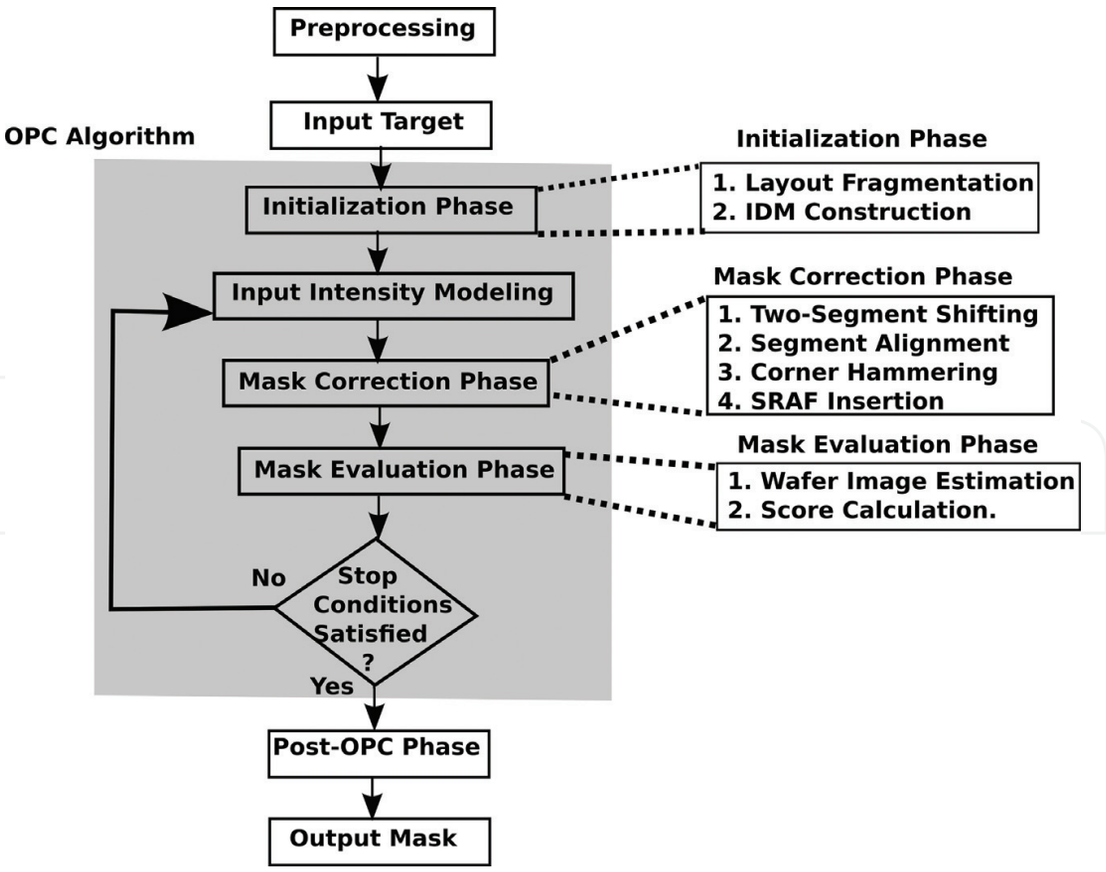

Figure 9. OPC engine framework.

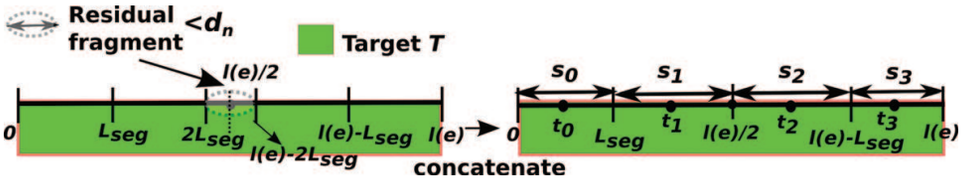

Figure 10. Fragmentation process [15].

Layout fragmentation: Edges along the boundary of target T are fragmented into segments. Segment length L_{seg} is predefined such that L_{seg} is greater than the minimum allowable notch width d_n. If a segment length is less than d_n, it is equally concatenated with its neighbors. The center for each segment s_i on the target is defined as a tap point t_i, as illustrated in **Figure 10** [15].

Intensity Difference Map (IDM) construction: One extra mask correction step is applied to generate a mask $M^{[0]}$ whose features are printable around target boundaries. With setting $M_{ref} = M^{[0]}$ and $K = K_{suff}$, IDM is constructed and exploited as in Eq. (9) to estimate intensity map of a mask M, where k_0 represents the top weight kernel in K [15].

$$\begin{aligned} I_{\text{diff}}(M^{[0]}, K_{\text{suff}}, \{k_0\}) &= I(M^{[0]}, K_{\text{suff}}) - I(M^{[0]}, \{k_0\}) \\ I_{P_c}(M) &\approx I_{P_c}(M, \{k_0\}) + I_{\text{diff}}(M^{[0]}, K_{\text{suff}}, \{k_0\}) \end{aligned} \tag{9}$$

5.2. Input intensity modeling

An OPC algorithm typically tries to make the nominal intensity curve of a given tap point crossing the target boundary at I_{th}, as depicted in **Figure 11(a)**. The distance from the target boundary to the cross-point of innermost intensity at which $I_i = I_{th}$ contributes to PV band as

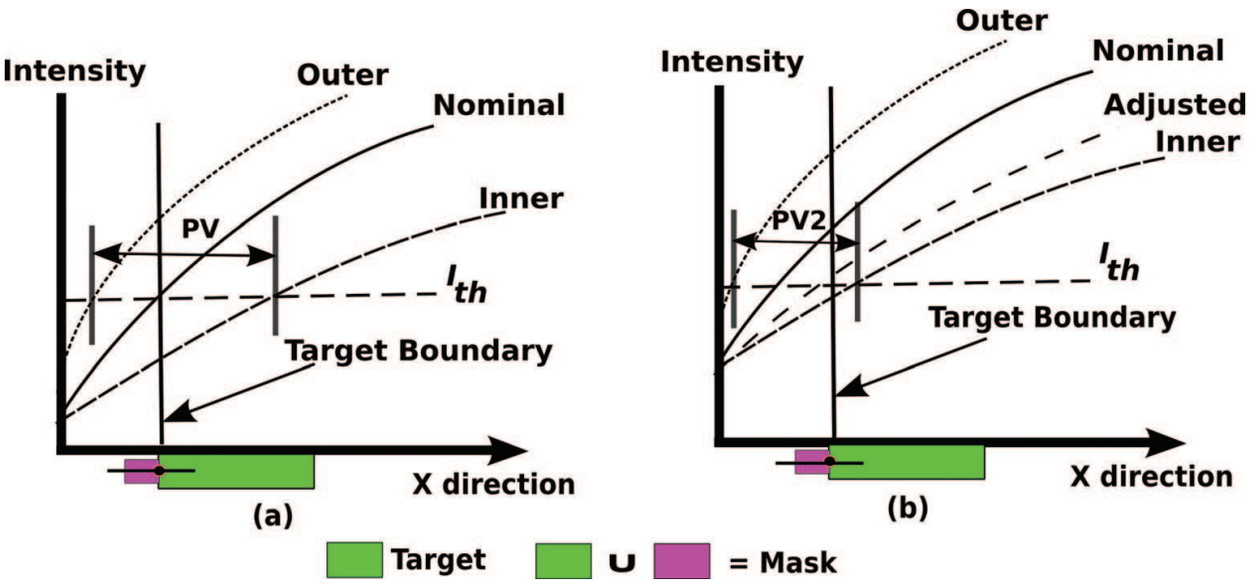

Figure 11. (a) Nominal intensity is considered to reach I_{th}, resulting in PV as PV band area indicator. (b) Adjusted intensity is considered to reach I_{th}, resulting in $PV2 < PV$ as PV band reduction [17].

well as distance from target boundary to the cross-point of outermost intensity. However, the innermost intensity cross-point to I_{th} is typically larger from the target boundary than the outermost intensity cross-point.

With making the cross-point of nominal intensity with I_{th} slightly outside the target boundary, PV band area can be reduced (as shown in **Figure 11b**). This is reasonable because the innermost intensity cross-point to I_{th} reaches close to the target boundary, which results in lesser PV band, since outermost intensity has already been saturated and its cross-point distance from target boundary is not expected to change significantly.

As an implementation, let $I_{def}(M)$ denote the intensity map under nominal dose and defocus. $I_n(M)$ denotes the nominal intensity under nominal dose and best-focus. In [15], the adjusted intensity map is defined, denoted by $I_{adj}(M)$, as the intensity map obtained by averaging both $I_n(M)$ and $I_{def}(M)$, as given in Eq. (10).

$$\forall p \in R, I_{adj}(M,p) = \frac{I_n(M,p) + I_{def}(M,p)}{2} \tag{10}$$

5.3. Mask correction phase

Mask correction phase applies a set of OPC steps on the input mask to optimize both EPE and PV band area with satisfying design rules. Adjusted intensity map of the input mask drives segment shifting and corner hammering, while innermost and outermost maps control SRAFs insertion.

Two-segment shifting: Let s_i and s_{i+1} be two neighboring segments with positions P_i and P_{i+1}, respectively, in mask M (see **Figure 12(a)**). The purpose is to find the new positions of those segments, denoted by P'_i and P'_{i+1}, such that the estimated intensities of their tap points become I_{th}. With exploiting top weight kernel model, the objective is to find (ΔP_i, ΔP_{i+1}) in Eq. (11) such that $\Delta P_i = P'_i - P_i$, $\Delta P_{i+1} = P'_{i+1} - P_{i+1}$. With solving Eq. (11), the new positions P'_i and P'_{i+1} are given in Eq. (12). **Figure 12(b)** illustrates two-segment shifting subroutine [15].

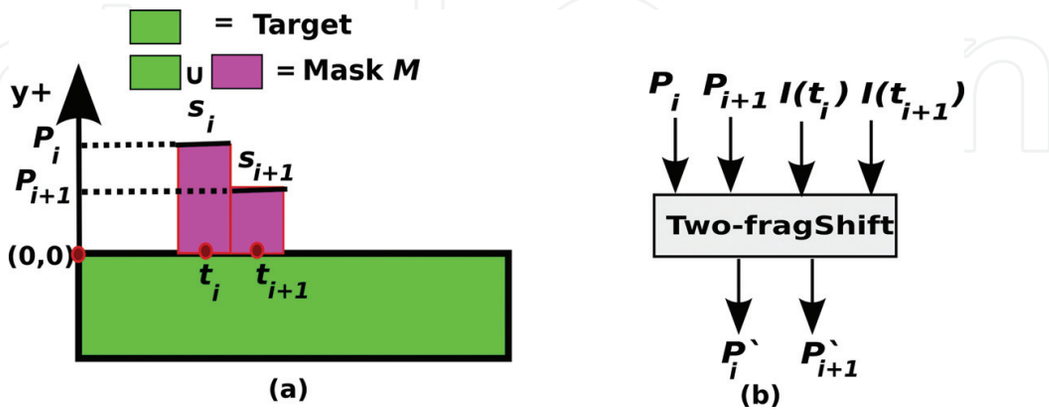

Figure 12. Two-fragment shifting: (a) current situation and (b) subroutine.

$$\begin{bmatrix} I(t_i) + \alpha_1 \triangle P_i + \alpha_2 \triangle P_{i+1} \\ I(t_{i+1}) + \alpha_1 \triangle P_{i+1} + \alpha_2 \triangle P_i \end{bmatrix} = \begin{bmatrix} I_{\text{th}} \\ I_{\text{th}} \end{bmatrix} \tag{11}$$

$$\begin{aligned} P_i' &= P_i + \frac{\alpha_1 (I_{\text{th}} - I(t_i)) - \alpha_2 (I_{\text{th}} - I(t_{i+1}))}{\alpha_1^2 - \alpha_2^2} \\ P_{i+1}' &= P_{i+1} + \frac{\alpha_1 (I_{\text{th}} - I(t_{i+1})) - \alpha_2 (I_{\text{th}} - I(t_i))}{\alpha_1^2 - \alpha_2^2} \end{aligned} \tag{12}$$

Consider the situation of non-corner segments s_{i-1}, s_i, s_{i+1} in mask M shown in **Figure 13(a)**. As illustrated in **Figure 13(b)**, Two-fragShift subroutine is applied first to s_{i-1} and s_i, followed by setting their tap point intensities to I_{th}. $I(t_{i+1})$ change due to s_i shifting is linearly estimated according to top weight kernel modeling. These data are inputted to Two-fragShift subroutine, which is then applied to s_i and s_{i+1} [15].

Corner hammering: Let c be a corner wherein corner segments a_c and b_c meet (in target T). A hammer is formed on c by shifting both a_c and b_c outside the polygon with distance w_c. This shifting amount is equivalent to the serif width as depicted in **Figure 14(a)**. Thus, the purpose

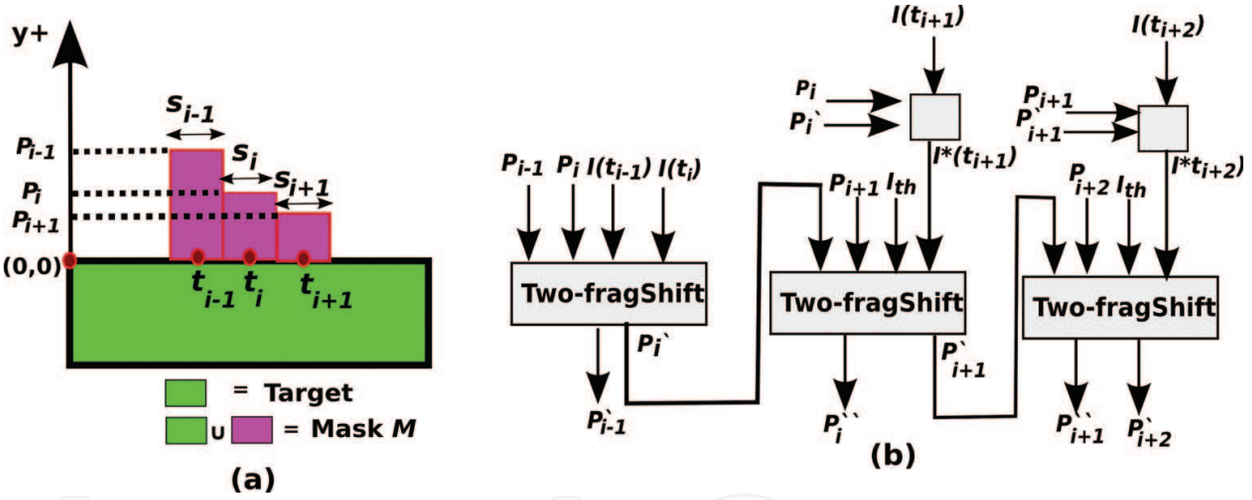

Figure 13. Edge non-corner fragments shifting: (a) situation and (b) subroutine [15].

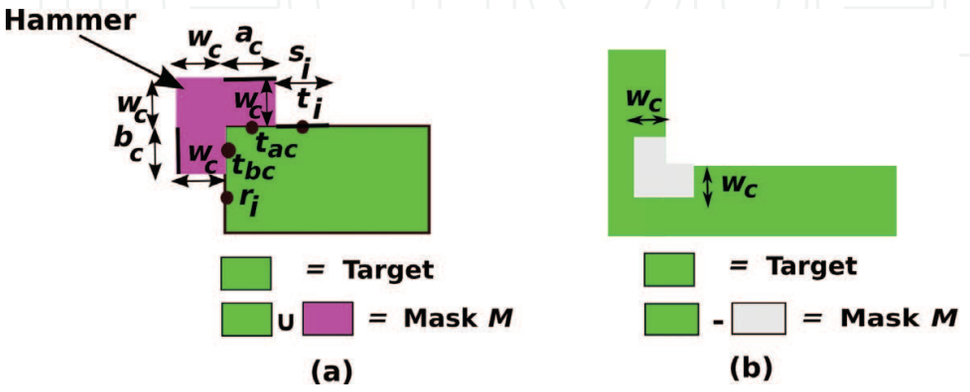

Figure 14. (a) Hammer insertion and (b) negative corner hammering [17].

is to find the serif width w′$_c$ such that the average intensity of both corner segments tap points, denoted by t_{ac} and t_{bc}, becomes equivalent to I_{th} [15]. For a negative corner, both corner segments are shifted inside and a squared serif is picked from T, as shown in **Figure 14(b)**.

However, due to the nonlinearity of the hammering problem, several solutions might exist. However, w′$_c$ is chosen within the interval [w_{min}, w_{max}], which represents the minimum and maximum allowable serif width, where $w_{min} \geq d_n$ to satisfy notch rule and w_{max} is predefined to neglect oversized serif solutions. This problem is formulated in Eq. (13) [15].

$$\textbf{Solve for } w^*\textbf{: } (I(t_{ac}) + I(t_{bc}))/2 + (B(w^*) - B(w_c)) + \alpha_1 w^* = I_{\text{th}}$$
$$w'_c = \begin{cases} w^*; & w_{\min} \leq w^* \leq w_{\max} \\ w_{\max}; & w^* > w_{\max} \\ 0; & \text{Otherwise} \end{cases} \tag{13}$$

Segment alignment: Alignment aims to ensure satisfying notch rule during segment shifting. Thus, a number of parallel lines to each edge in the target are created with d_n spacing between each two consecutive lines. In this way, each segment is aligned to the closest line parallel to it after shifting, as shown in **Figure 15** [16].

SRAF insertion: With increasing the distance between an SRAF and a tap point t, the difference between outermost intensity and innermost intensity of t does not monotonically decrease. Therefore, global minimal values of this difference within the decaying intervals are SRAF candidate locations to ensure reducing $I_o(M, t)$ - $I_i(M;$ t), which turns out into lesser PV band area. SRAF candidate locations are determined during preprocessing stage [15].

5.4. Post-OPC phase

Post-OPC phase aims to improve mask manufacturability through reducing mask data volume and spacing rule violations resolution. This phase consists of the following:

Segment concatenation: Reducing the segment numbers along the mask boundary helps in reducing mask data volume along with reducing the shot-count. This is achieved through two-segment concatenation. However, ad hoc concatenation of neighboring segments badly impacts pattern fidelity.

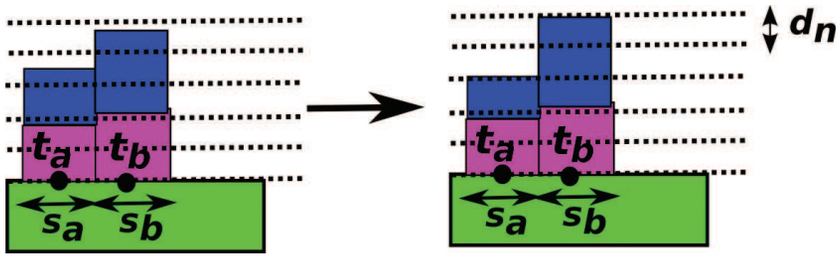

Figure 15. Segment alignment [16].

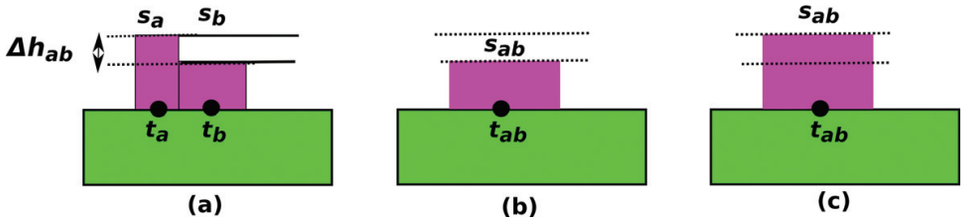

Figure 16. Concatenation process [16]: (a) before concatenation, (b) s_a is moving, and (c) s_b is moving.

Let s_a and s_b be two neighboring segments with Δh_{ab} orthogonal distance between them (**Figure 16(a)**). Let epe_{prea} and epe_{preb} denote the predicted EPE in tap points t_a and t_b, respectively, after concatenation. Concatenation process is performed as follows [16]:

- If $epe_{prea} < epe_{preb}$ and $epe_{prea} \geq epe_{max}$, shift s_a to concatenate with s_b (**Figure 16(b)**).
- if $epe_{preb} < epe_{prea}$ and $epe_{preb} \geq epe_{max}$, shift s_b to concatenate with s_a (**Figure 16(c)**).
- If the predicted EPE causes violation, no concatenation is performed.
- If concatenation is done, s_a and s_b become one segment s_{ab}.

Feature movement: Segment/SRAF extra movement aims to resolve spacing violations in the mask pattern outputted from concatenation process. This is strictly subjected to the constraint that no additional EPE violations occur, as illustrated in **Figure 17** [16].

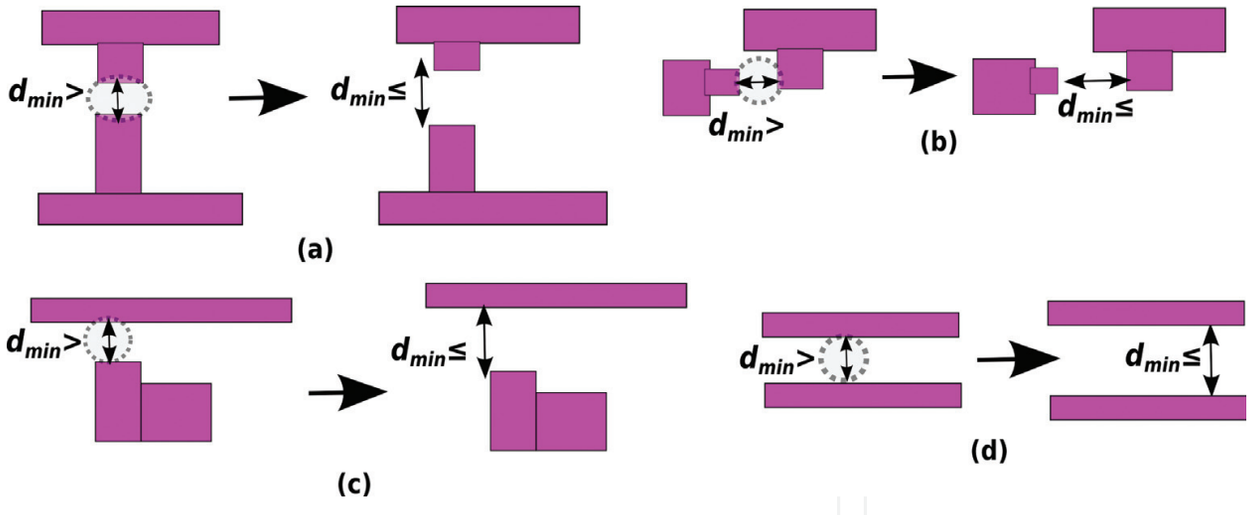

Figure 17. Spacing violation resolution cases [16]: (a) two parallel features, (b) two orthogonal features, (c) SRAF and segment, and (d) two SRAFs.

6. Experimental results and discussion

6.1. Experimental setup

Simulation environment: Lithosim uses industrial optical models with 193 nm immersion lithography. CTR model is used with intensity threshold of 0:225. Layout patterns are defined

in 1024 × 1024 pixels region, where each pixel represents 1 nm × 1 nm. A set of 24 SOCS kernels forms the optical model in Lithosim [11].

OPC algorithm parameters: The proposed OPC algorithm in [16] has been implemented on top of Lithosim. The algorithm was executed on 4 cores 3.6 GHz Linux machine with total memory of 1,986,912 kB. Segment length has been chosen as 20 nm; minimum allowable mask notch has been set practically to 5 nm. The maximum allowable hammer width is 80 nm; maximum allowable SRAF width is 60 nm. The maximum number of iterations has been set to 10.

Testing benchmarks: Testing benchmarks have been provided by IBM for ICCAD 2013 CAD contest. Each benchmark is an M1 layout pattern for 32 nm technology nodes. The CD of those benchmarks ranges from 20 to 80 nm. The number of patterns (polygons) in those benchmarks ranges between 4 and 34 polygons with layout density ranges from 0.3 to 0.46 due to the pitch spacing design rules for realistic industrial cases [11].

Mask evaluation: The score function used in ICCAD 2013 CAD contest is used for evaluation [37]. Given a mask M, the score of M, denoted by $\varphi(M)$, is given in Eq. (14), where τ denotes the computation time to find a mask and ζ represents the number of hole shapes in the corrected mask. α, β, and γ are set to 5000, 4, and 10,000 following the contest.

$$\varphi(M) = \alpha^{*}\#EPEV(M) + \beta^{*}PV(M) + \gamma^{*}\zeta(M) + \tau \tag{14}$$

6.2. Comparison with recent algorithms

The proposed algorithm in [16] has been compared with recently published algorithms executed on the same benchmarks. **Table 1** shows a comparison between the proposed algorithm and state-of-the-art algorithms including: MOSAIC fast [36], MOSAIC exact [36], and PV-OPC [11].

The proposed algorithm in [16] outperforms MOSAIC fast in the overall score and it is 3.76 times faster. MOSAIC fast is effective in terms of PV band area due to its pixel-based behavior in finding the mask solution under each process condition. However, it has lack of estimation accuracy, which turns out into pattern fidelity degradation. MOSAIC exact effectively optimizes both EPE and PV band area since it simulates wafer image under each process condition using all kernels. However, this algorithm slowly converges. While the proposed algorithm in [16] has almost the same cost of MOSAIC exact in terms of EPE and PV band area, it is 22 times faster. PV-OPC is an effective algorithm as it exploits variational EPE under representative process conditions with satisfying mask notch rule. Keep out zone (KOZ) concept is exploited as well to avoid pinching and bridging errors between patterns. Thus, PV-OPC algorithm outperforms [16] in terms of EPE while [16] has less PV band area due to input intensity modeling and SRAFs insertion. Additionally, the proposed algorithm in [16] is 1.65 times faster. Note that PV-OPC does not consider spacing rule violations and mask data volume reduction.

Generally, it seems obvious that the proposed algorithm in [16] outperforms other recent algorithms, specifically in OPC runtime as it is 1.65 times faster than the fastest algorithm among others. Exploiting intensity difference map concept is the main reason, which turns out into minimizing the number of kernels needed for simulation during optimization.

Benchmark	MOSAIC fast				MOSAIC exact				PV-OPC				Proposed algorithm [16]			
	#EPEV	PV	Time	Score	#EPEV	PV	Time	Score	#EPEV	PV	Time	Score	#EPEV	PV	Time	Score
B1	6	58,232	318	263,246	9	56,890	1707	274,267	2	58,269	164	243,240	6	61,474	78	275,974
B2	10	47,139	256	238,812	4	48,312	1245	214,493	0	52,674	130	210,826	5	48,925	84	220,784
B3	59	82,195	321	624,101	52	84,608	2522	600,954	47	81,541	203	561,367	44	98,257	81	613,109
B4	1	28,244	322	118,298	3	24,723	1269	115,161	0	26,960	190	108,105	2	26,853	80	117,492
B5	6	56,253	315	255,327	2	56,299	2167	237,363	4	61,820	62	267,342	0	61,810	79	247,319
B6	1	50,981	314	209,238	1	49,285	2084	204,224	0	55,090	54	220,414	1	50,227	82	205,990
B7	0	46,309	239	185,475	0	46,280	1641	186,761	0	51,977	74	207,982	0	42,547	80	170,268
B8	2	22,482	258	100,186	2	22,342	663	100,031	0	22,869	65	91,541	0	22,078	69	88,381
B9	6	65,331	322	291,646	3	62,529	3022	268,138	0	70,713	55	282,907	0	65,047	75	260,263
B10	0	18,868	231	75,703	0	18,141	712	73,276	0	17,846	41	71,425	0	17,328	62	69,374
Ratio	1.57	0.96	3.76	1.04	1.31	0.95	22.12	1.0	0.91	1.01	1.65	1.0	1.0	1.0	1.0	1.0

Table 1. Comparison with state-of-the-art.

Benchmark	Algorithm published in [35]							Proposed algorithm in [16]						
	#EPEV	PV	Time	Score	#NotchV	#SpaceV	Volume	#EPEV	PV	Time	Score	#NotchV	#SpaceV	Volume
B1	0	66,218	278	265,150	186	67	10,695	6	61,474	78	275,974	0	9	5863
B2	0	53,434	142	213,878	175	68	9139	5	48,925	84	220,784	0	8	4739
B3	18	146,776	152	677,256	215	83	12,013	44	98,257	81	613,109	0	15	6902
B4	0	33,266	307	133,371	77	84	7096	2	26,853	80	117,492	0	4	2328
B5	1	65,631	189	267,713	214	124	13,582	0	61,810	79	247,319	0	8	5356
B6	0	62,068	353	248,625	224	127	13,692	1	50,227	82	205,990	0	11	5592
B7	0	51,069	219	204,495	120	134	13,019	0	42,547	80	170,268	0	3	3172
B8	0	25,898	99	103,691	109	68	7285	0	22,078	69	88,381	0	4	3027
B9	1	75,387	119	306,667	227	132	15,426	0	65,047	75	260,263	0	13	6047
B10	0	18,141	61	72,625	78	31	4934	0	17,328	62	69,374	0	0	2246
Ratio	0.36	1.21	2.50	1.10		12.24	2.36	1.0	1.0	1.0	1.0	1.0	1.0	1.0

Table 2. Mask manufacturability comparison with state-of-the-art algorithm.

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To verify the effectiveness of the proposed OPC algorithm from mask manufacturability perspective, the algorithm published in [35] and the proposed algorithm in [16] have been compared in terms of mask notch and spacing rule violations, in addition to the mask data volume. **Table 2** shows this comparison, in which pattern fidelity, process variability, and computation time are included.

As shown **Table 2**, the algorithm in [35] effectively tackles pattern fidelity under nominal process condition. However, it has a relatively large PV band area. Algorithm in [16] outperforms the overall score of the algorithm published in [35] by 9%. Additionally, it is 2.5 times faster. Mask notch violations have been totally eliminated due to alignment stage while spacing violations have been reduced by 92% on average due to features movement. Mask data volume has been reduced by around 57.6% on average due to segments concatenation and alignment.

Figure 18 illustrates a target pattern, its generated mask solution using the proposed algorithm in [16], nominal wafer image, and PV band.

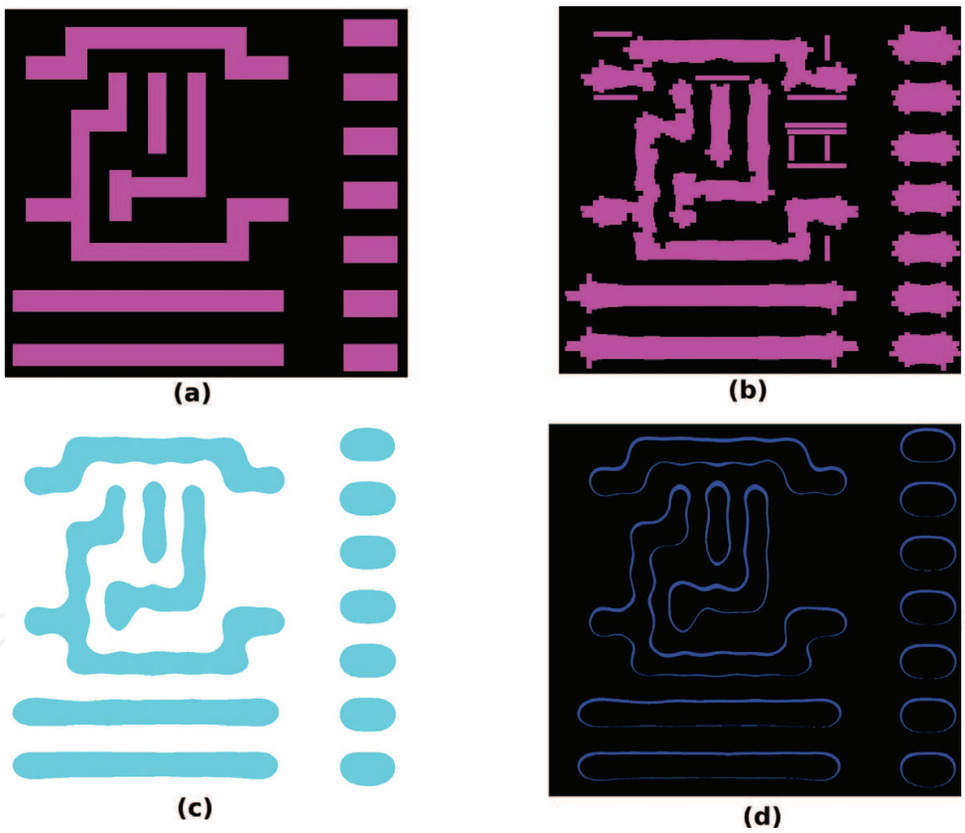

Figure 18. (a) Target pattern, (b) mask solution using [18], (c) nominal wafer image, and (d) PV band.

7. Conclusions

In this chapter, we have discussed the recent state-of-the-art OPC algorithms to tackle mask optimization problem for advanced technology nodes patterning through optical system.

Then, we have analyzed the algorithm published in [17, 18] as fast, recent OPC methodology to generate mask solutions. The analyzed algorithm outperforms other state-of-the-art algorithms in terms of EPE and PV band area reduction due to OPC adjustments guided by adjusted intensity in addition to SRAFs insertion/sizing. Computation time reduction is evident due to the fast novel intensity estimation model exploited in the OPC engine. Mask manufacturability has been significantly improved due to the post-OPC stages, wherein EPE prediction models are exploited to preserve acceptable pattern fidelity and robustness against process variations while respecting mask design rule constraints.

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