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Plastic Optical Fibre Sensor System Design Using the Field Programmable Gate Array

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Abstract

Extrinsic optical fibre sensor (OFS) systems use a fibre optic cable as the medium for signal propagation between the sensor and the sensor electronics using light rather than electrical signals. A range of different optical fibre sensors have been developed and electronic hardware system designs interfacing the sensor with external electronic systems devised. In this chapter, the use of the field programmable gate array (FPGA) is considered to implement the circuit functions that are required within a portable optical fibre sensor system that uses a light emitting diode (LED) as the light source, a photodiode as the light receiver and the FPGA to implement the system control, digital signal processing (DSP) and communications operations. The capabilities of the FPGA will be investigated and a case study sensor design introduced and elaborated. The OFS system will be based on the FPGA and will provide wireless communications to an external supervisory system. The chapter will commence with an overview of OFS systems and the typical architecture of the system. Then the FPGA will be introduced and discussed as a hardware alternative to a software programmed processor that is currently widely used. A case study will then be presented with a discussion into design considerations.

Keywords: optical fibre sensor, field programmable gate array, electronic system design, SPR sensor, Python

1. Introduction

Recent advances in optical fibre sensing technology have been rapid and widespread stimulated through achievements in developing sensors for applications such as environmental monitoring, mechanical structure stress and strain monitoring, and biomedical [1–4]. Advances in sensor fabrication, sensitivity enhancement and the availability of new materials have demonstrated the potential of using optical sensors in new applications. The aim is to harness the

advantages that optical components can provide over electrical component alternatives in a wide range of sensor applications. However, identifying and using suitable enabling technologies, supported through experience in achieving repeatable results from suitable experiments for new OFS industrial applications, should be recognised as key in moving forward from a research idea into application [5].

It is widely accepted that initial OFS designs were fragile, reliable only under laboratory conditions and with material costs higher than those used in other sensor technologies [6, 7]. They were also difficult to produce and this limited their ability for practical use. However, with an increase in the availability of new materials, the proliferation of inexpensive 3D printing and other additive manufacturing technologies that enable rapid prototyping and analysis, sensor design and packaging performance have been improved dramatically. These OFS packaging improvements have enabled optical fibre sensor (OFS) deployment [8] in a wide range of different applications as referenced above. An OFS system is however not complete without supporting instrumentation [9]. It requires a suitable electronic system to implement system functions that include system control, sensor stimulus generation, data acquisition (DAQ) and storage, data analysis (high-speed digital signal processing (DSP) operations) and serial communications interfacing. To date, OFS system deployment is still largely dependent on laboratory-based sub-systems, particularly the light source and optical receiver that interface to a computer through a data acquisition (DAQ) module or proprietary software via universal serial bus (USB). A typical OFS system needs to use high-cost and complex instruments to provide the necessary control and measurement capabilities, and usually depends on a human operator to set-up the light source and access the sensor results. To make optical sensors more accessible, the use of high quality but lower cost equipment is required. Some improvements have been noted in recent system designs where operations were performed using a software programmed microcontroller based arrangement [10–12]. The potential also exists to create supporting instrumentation that can harness inexpensive and physically smaller components to make an OFS system portable (i.e. a battery operated system capable of operating independently for extended periods of time, small physical size, programmable with wireless communications and ability to be carried by an individual, e.g. a first responder). The low cost aspect however must not compromise the quality of the system operation and it must also have reliable operation in the intended application. The inert nature of optical fibre also allows it to perform in-situ measurements in harsh environments whilst the sensitive electronic circuits can be shielded at an appropriate location and remotely from the environment being sensed. In addition, for complex photonic system design, photonic integrated circuit (IC) technology is a promising solution to achieve lower cost and miniaturisation, but is still not yet as mature as electronic technology [13].

This chapter will consider the electronic system design requirements for a portable OFS system based on the use of a microcontroller alternative. Specifically, the field programmable gate array (FPGA) is used to implement the necessary digital logic functions in hardware including light emitting diode (LED) (light source) switching and current control and photodiode (light receiver) signal sampling and signal conditioning. A plastic optical fibre (POF) arrangement is considered, although the focus of the chapter will be on the FPGA based electronic system design approaches and potential solutions. The chapter will consider the system design, both

analogue and digital parts, and will develop a discussion into the use of the FPGA as a hardware based alternative to a software based processor design. The available hardware resources within the FPGA will be considered and approaches to using these resources will be discussed. The FPGA, as an alternative, provides potential benefits to system design and operation by using configured hardware that provides the potential for high speed operation, parallel processing (concurrent operation), high-speed embedded DSP operations and low-voltage/-low-power capability. The available hardware resources within the FPGA, along with the capability for low-voltage and low-power operation, mean that a powerful whilst portable sensor system can be developed and deployed. This chapter will consider the potential benefits of using the FPGA in such sensor systems and the design choices required. The chapter will commence with an introduction to OFS systems and electronic system design using the FPGA. It will then discuss the use of the FPGA within an existing OFS system and the benefits the FPGA can provide before providing a conclusion.

In this chapter, the discussion will be based on a single sensor arrangement to demonstrate the use of the FPGA. However, the FPGA would be easily capable of interfacing to multiple sensors due to the availability of configurable hardware within the FPGA and the availability of a large number of programmable digital pins which can be configured to act as inputs, outputs or bi-directional pins. It would therefore be practical for the FPGA to be used in multiple (multipoint) and quasi-distributed OFS systems of the form shown in **Figure 1**. Additionally this concept may ultimately be extended to use in fully distributed systems, e.g. Rayleigh and Brillouin scattering based systems, utilising the considerable on-board capabilities of the FPGA in fulfilling the complex signal process required from these systems. However, this article is constrained to assessing the feasibility of a potential distributed OFS application where multiple 'single point' sensors are distributed in location but connected to
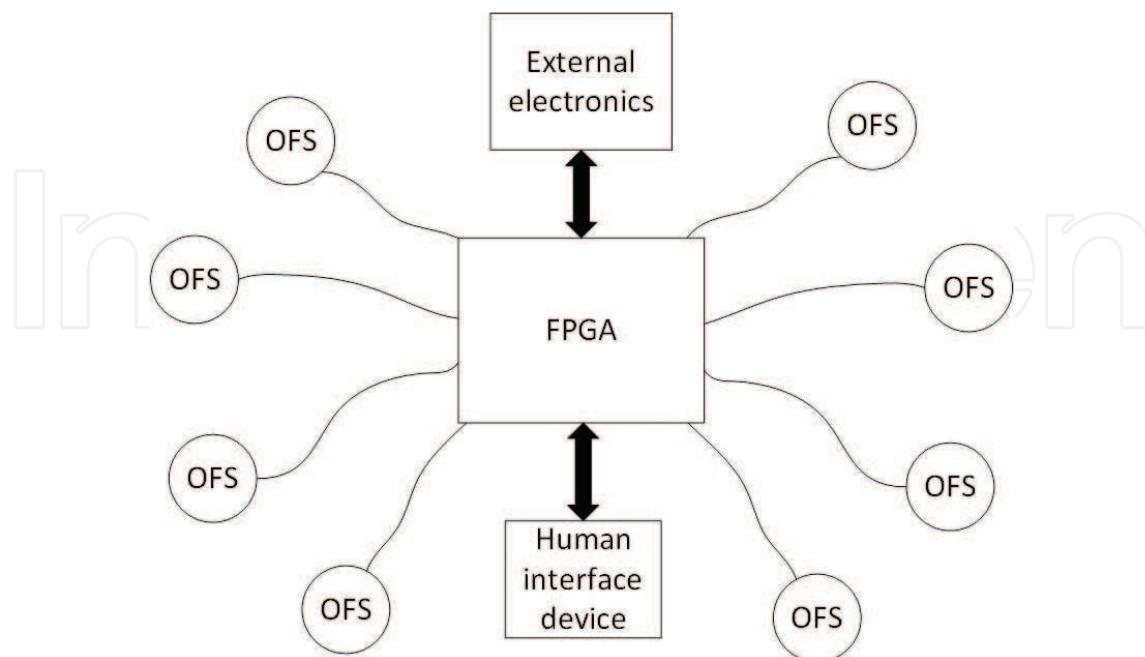

Figure 1. Distributed sensing with multiple 'single-point' sensors.

a single FPGA. The high number of available FPGA I/O pins are especially useful in allowing independent driving of multiple light sources and taking multiple light intensity measurements. Those measurements can be taken in a parallel manner and could be useful in phenomena detection [14]. Whilst the focus of this chapter is on a single 'single point' sensor, the basic design could be duplicated with other similar sensors and using the same FPGA to realise distributed sensing.

The chapter is structured as follows. Section 2 describes the OFS system operation and the design choices in the use of suitable components. Section 3 introduces the FPGA and how digital and mixed-signal electronic circuits and systems can be designed using the FPGA. This section also highlights a number of the advantages that the FPGA has over software programmed processor alternatives. Section 4 discusses the feasibility of use of the FPGA in an OFS system and Section 5 provides a real system based case study design using POF to provide an optical interface to the surface plasmon resonance (SPR) sensor. Section 6 concludes the paper.

2. Optical fibre sensor systems

2.1. Introduction

In this section, the structure and operation of a typical optical fibre sensor system is discussed. A typical OFS system essentially comprises of a light source, sensing element, optical detector and sensor data readout parts (external communications). A simplified architecture of such a system is shown in **Figure 2**. Light is guided from the light source to the optical receiver using an optical fibre. The sensing element is the part that transforms a change in the monitored parameter into a corresponding change in one or more of the physical properties of the guided light. Those properties include purely intensity, wavelength, polarisation orientation and phase. A change in the properties of the transmitted light through the sensor can be created by different physical mechanisms. For example, the chemical properties of a material being sensed. To capture the change in the propagated light properties, an appropriate light source
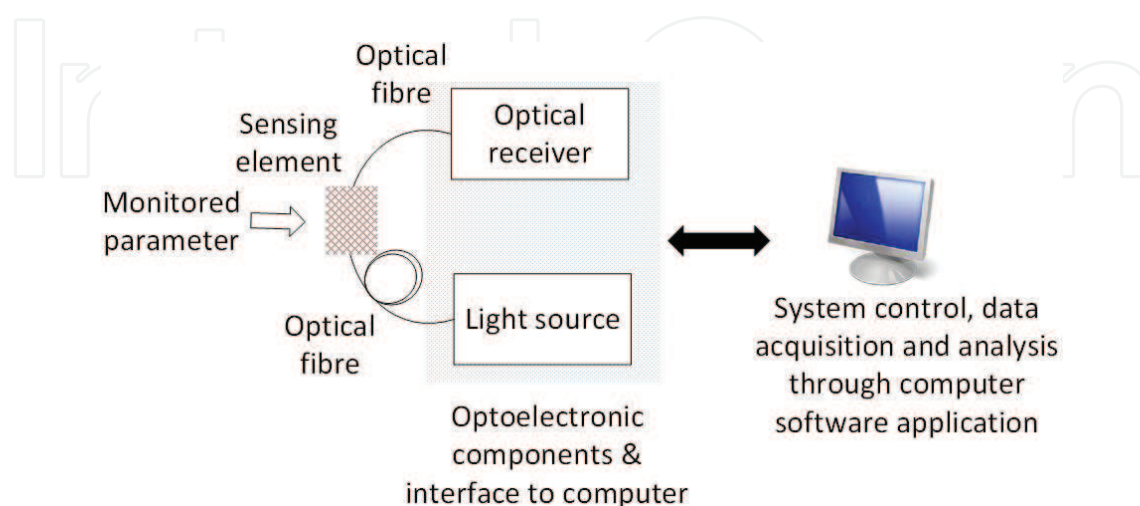

Figure 2. Simplified architecture of an OFS system (either intrinsic or extrinsic).

and matching optical receiver are required. The light source provides the sensor light stimulus of a particular wavelength or band of wavelengths to propagate to the sensing element. This light is modulated by the sensor and the resulting signal is captured by optical receiver. The optical parts of the system are linked together using an optical fibre cable. POF is becoming an increasingly popular choice in many sensors when compared to glass optical fibre (GOF) due to its low-cost, ease of connection and flexibility (allowing it to be mechanically bent and shaped to the requirements of the sensor housing and location). The source and receiver are electrically connected to the computing device that provides an optical-electrical interface, system control, communications and data analysis. The complexity of an OFS system is usually dependent on light modulation method used, the type of sensor and whether a single or multiple sensors are required. For example, distributed sensing requires complex light sources, coupling optics and receivers to obtain a sufficiently high-resolution result [14]. Distributed sensing ideally enables the measurement of any point along the optical fibre and is used in applications such as temperature, strain and acoustic sensing. Other OFS types include multi-point sensing or single point sensing [15, 16]. A multipoint sensor is similar to distributed sensing and therefore often also requires complex instrumentation although the cost of the interrogator unit is often much less than the fully distributed sensor. On the other hand, a single point sensor usually is the simplest form that requires less complex instrumentation. In all cases, the sensors may be classified as being either intrinsic or extrinsic. An intrinsic sensor uses the fibre itself as the sensor whilst in an extrinsic sensor, the fibre is used only used for light propagation to and from the sensor element which is therefore an external device. Clearly in the case of distributed sensors, e.g. Rayleigh or Brillouin, these are examples of intrinsic sensors.

The individual components of the OFS system are considered in the following sections.

2.2. Optical fibre

An optical fibre is a flexible optically transmitting waveguide that is drawn from glass or plastic [7]. In its simplest form, it is composed of three parts. Referring to **Figure 3**, these are the core, cladding, and coating. Both the core and cladding are made of a suitable dielectric
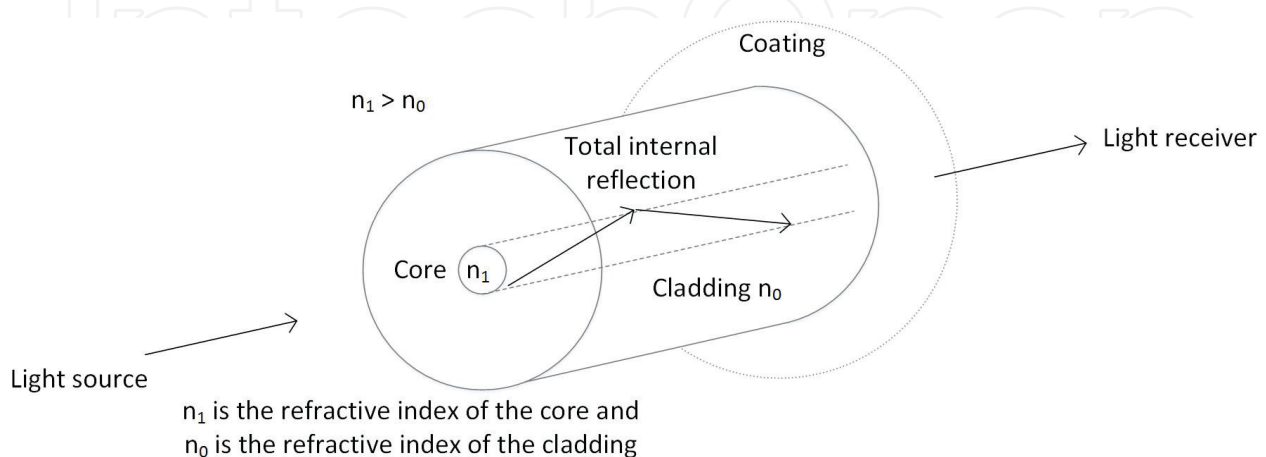

Figure 3. Optical fibre structure.

material, usually doped silica glass or a polymer. The core usually has a cylindrical cross-section and has higher refractive index (*n*) than the cladding that surrounds it. The coating is an additional layer of material, often a toughened polymer that provides protection from physical damage whilst maintaining flexibility. The interface of the core and cladding can be considered as a perfect abrupt but completely smooth boundary and the refractive index difference between the materials allows for total internal reflection to occur whilst minimising scattering losses [17]. In the case of total internal reflection, all of the light energy is ideally preserved within the core and allows the light to transmit through the fibre not only when the fibre is straight, but also when bent (up to a limit known as the minimum bend radius) as would be typically seen with a flexible fibre [7].

A number of fibre types are commercially available for different purposes and can be broadly categorised into two basic types: silica (glass) fibre or polymer (plastic) fibre. Glass fibre has widespread use in communications applications [18] due to its low-cost and material proper-ties. It allows for extremely low loss long distance transmission of data with the need for fewer repeaters to boost signal strength due to losses in the transmission medium than would be required with electrical signal transmission. POF has found use in relatively short distance light transmission, e.g. in local area networks and, due to its flexibility, in situations that involve bending of the fibre, e.g. as in the case of automotive based networks. POF is generally large core fibre (i.e. a large fibre diameter, being typically 0.25 to 2 mm in diameter) that can bend into a smaller radius than can a silica fibre. There are some exceptions with much recent research being focused on single mode POF, e.g. for strain sensing [19]. Despite the material differences, both types of fibre operate under same principle of allowing the transmission of light. A major advantage of all optical fibres is that due to their material properties, an optical fibre is immune to external electrical interference. For example, unlike copper wiring, there is no cross-talk between signals in different close-proximity cables and no pickup of environ-mental noise, e.g. from proximal electrical machines or faulty electrical equipment. Recently, the application of the optical fibre has been extended from primarily a communications medium to the use as a sensor. An OFS introduces the idea of the modulation of a transmitted light signal as it propagates through a fibre and through different physical phenomena that are aimed to be measured [20]. Other specialist fibre types are available which result from novel structures or alternative materials. Photonic Crystal or Photonic Bandgap Fibres (PCF or PBF) rely on hollow or honeycomb (or many other sophisticated designs) patterned cores but currently their use is confined to some specialist applications, e.g. Supercontinuum Light sources [21]. Other specialist fibre materials are also available, e.g. Chalcogenide and ZBLAN for mid-infrared (MIR) operation, but again their use has been confined to some specialist sensing activities e.g. gas sensing [22].

2.3. Light source and optical detector

The light source and optical detector are fundamental parts of an OFS system. Both are required to have the necessary operating characteristics to be useful, are required to operate reliably over a long periods of time and to provide trustworthy data to the user. Light sources used to support low-cost optical fibre sensors are LED based and in some cases low-cost semiconductor laser diodes. Other systems use a broadband white light source and spectrometer

arrangement. The choice of which light source to use depends on the required application. For example, the laser provides a very narrow wavelength range, whereas the white light source provides a wide band of wavelengths. LEDs also provide a relatively small band of wavelengths (broader than laser diodes) that is governed by the semiconductor material band gap energy. The light source can also be categorised as either a directional or diffused light source. A directional light source emits the majority of the light in one direction and with a narrow angle of spread. A diffused light source emits light in a wide range of directions equally and requires optical components to efficiently couple it into waveguide. Some OFS applications may be able to utilise an unpolarised light source, others may need a polarised light source. In addition, there may be a requirement to the use a coherent rather than an incoherent light source. The most commonly used optical detectors for low-cost optical fibre sensors are the photodiode, the avalanche photodiode and the phototransistor. These optical detectors translate optical intensity into an electrical signal (a current proportional to the intensity of the light that the device is sensitive to). In addition, the light dependent resistor (LDR) can sometimes be used which converts input light intensity to generate a change in electrical resistance. However the LDRs tend to be inefficient and slow compared to the photodiode/phototransistor type detectors. A single current output is produced which corresponds to an integral result of the intensities at all the detected light wavelengths. If a system is to be able to discriminate signals at discrete spectral values, an optical detector needs to be used in conjunction with an optical grating or filter [23]. The spectral bandwidth of the detector must also be aligned with the light source spectrum and the spectral transmission of the sensor. Other parameters to consider in choice of detector include response time and the noise figure.

In considering the use of the LED and photodiode based arrangement, the digital sub-system must provide the necessary digital-analogue-digital signal interface. A typical system arrangement is shown in **Figure 4**. On the transmission side, the LED requires a drive current to output a specific light intensity. This is produced by a voltage-to-current (VI) converter that receives a voltage and outputs a current proportional to the input voltage. As the signal originates from a digital sub-system, the digital output is required to be converted to its analogue equivalent
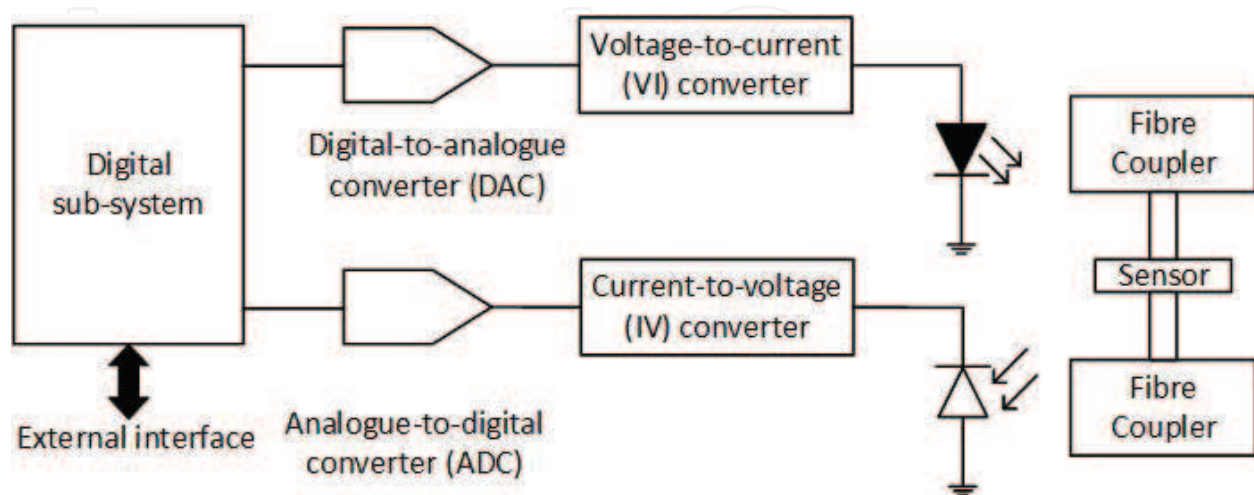

Figure 4. LED based light source current control and photodiode receiver circuit.

through a digital-to-analogue converter (DAC) with suitable speed and resolution. **Figure 4** assumes that the DAC output is a voltage rather than a current. The light is coupled to the POF and propagates to the sensor. Following transmission through and modulation by the sensor, the POF propagates the returning light signal to be received by the distal photodiode. The output of the photodiode is a current proportional to the intensity of the input light received. This is converted to a voltage though a current-to-voltage (IV) converter and applied to the input of an analogue-to-digital converter (ADC) with suitable speed and resolution. This set-up assumes that the ADC is a voltage input rather than a current input device. The digital sub-system captures and processes the digitised value. Results can then be processed and transmitted to a user or an external electronic system. The photodiode characteristics (light intensity range and range of wavelengths that can be detected) must be matched to the LED light source, otherwise the measurements do not accurately reflect the behaviour of the measured quantity.

2.4. Referencing

The accuracy of an OFS measurement depends on how reliably the value of the modulated signal reflects the behaviour of physical quantity being measured. However, other effects may cause the signal to change and therefore, their influence must ideally be isolated and removed in order to focus solely on the physical quantity being measured. In practice, this condition is not easy to achieve due to various factors. For example, the propagating light suffers from multiple attenuation factors in its propagation path which include losses from optical components and uncertainty introduced by optoelectronic component variability. To compensate for known effects that the system can be calibrated to account for, potential deviations from the ideal should be recognised and recorded. A common method is to apply an additional light signal that is used as a reference and is subjected to the same environmental influence as for measurement signal. Thus, the reference signal can calibrated to the measurement signal. There are different techniques that can be used to introduce a reference signal into system including spatial, spectral, temporal, frequency separation or through a combination of these methods [24]. Such an approach also requires some form of signal processing, analogue or digital, and hence this must be factored into the design. Increasingly, digital signal processing (DSP) techniques are used and in the case of software based processors or hardware configured programmable logic devices (PLDs), can readily be included in order to provide for programmable and local sensor signal conditioning.

2.5. Wavelength and intensity interrogation

Some sensing elements react only to a narrow band of wavelengths. These sensor systems use a simple intensity interrogation technique where light is collected as a single value regardless of wavelength in order to provide a single light intensity reading. This technique is normally used with narrow bandwidth or monochromatic light sources. A low-cost choice for the light source in intensity interrogation based systems includes the LED and semiconductor laser diode. However, the LED is less complex to use from the viewpoint of driver circuitry and does not have the safety concerns that exist with some laser diodes. The optical receiver can be a photodiode or phototransistor. Referring to **Figure 5**, this represents the main choices to be made. The light source (**Figure 5**) is either an LED, low-cost laser diode (a) or a white light
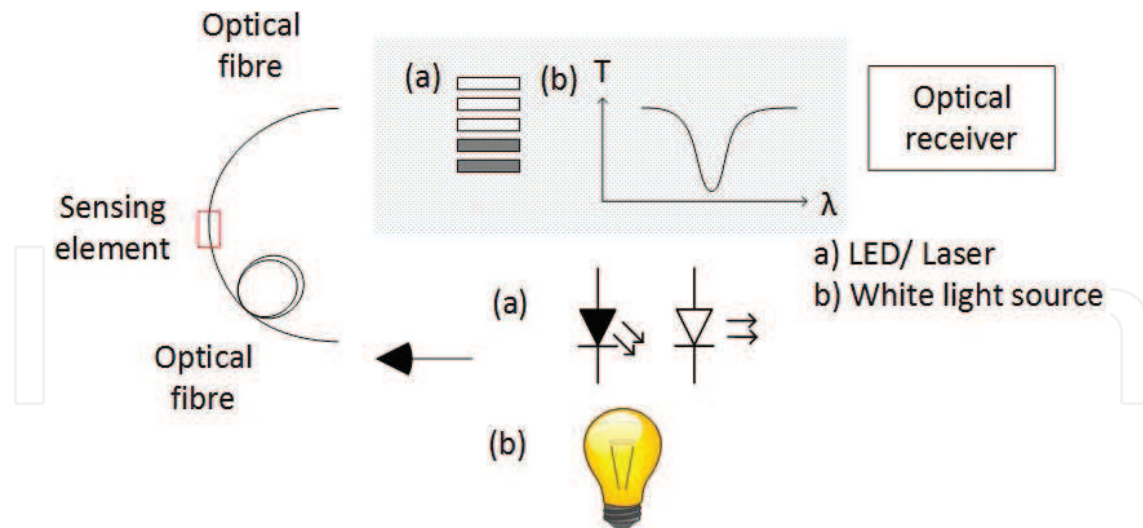
Figure 5. OFS system using a white light source and spectrometer or laser/LED and photodiode/phototransistor.

source (b). The choice of receiver is based on the light source. For the LED or laser diode, the receiver (**Figure 5**) provides only intensity interrogation (a) and for the white light source, either intensity or wavelength resolved interrogation (b).

It should also be noted and considered that some information can only be captured by observing at the signal spectrum instead of the cumulative intensity integrated across the whole spectrum. To extract such information, the signal needs to be spectrally resolved with adequate (spectral) resolution that will enable the desired measurand to be accurately determined and recorded. This technique, also known as wavelength interrogation, usually requires the use of a white light source and spectrometer as a detector.

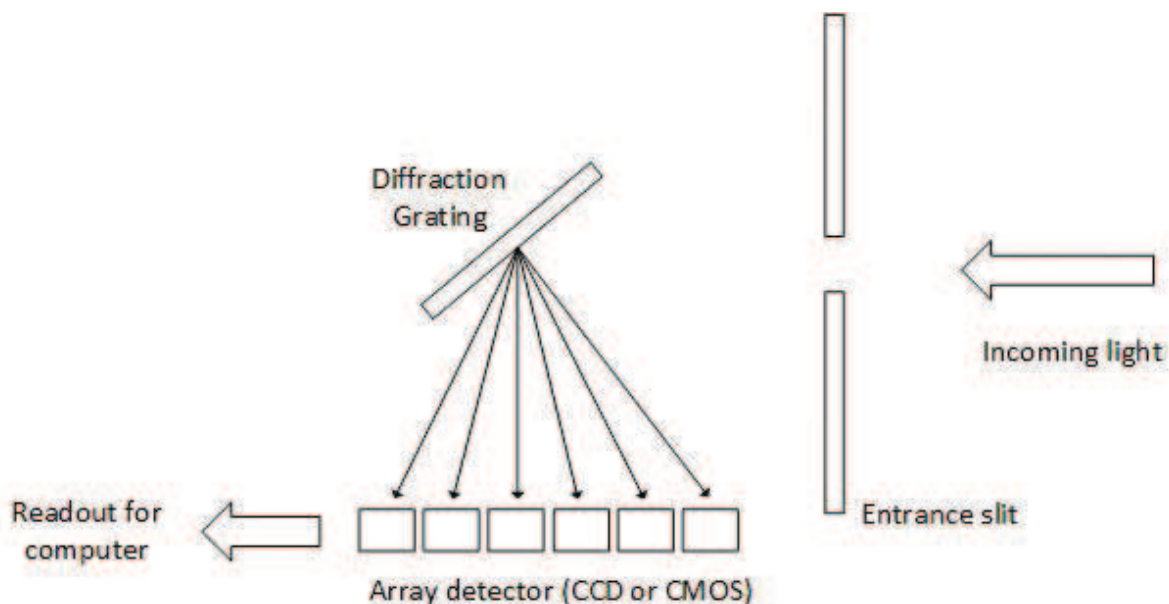**Figure 6** shows the principle of operation of the spectrometer.

Figure 6. Principle of operation of the spectrometer.

The spectrometer is becoming increasingly widely used as an optical receiver. It receives a collimated input and disperses it into spectral components by an optical component such as a diffraction grating. The different spectral components are then registered by an array detector such as a charge-coupled-device (CCD) or complementary metal oxide semiconductor (CMOS) camera. To read out the spectral data as a digital representation of the captured optical signal, the spectrometer normally incorporates a suitable computer interface. The whole series of tasks require high precision optical elements and the spectrometer often needs to be recalibrated at regular intervals by a qualified technician. The cost of a spectrometer system is a factor that normally prohibits its use in situations with limited (financial) resources [25], although their cost and robustness is rapidly improving. Different parameters are best measured using the optimum combinations of suitable light sources and optical receivers. For example, surface plasmon resonance (SPR) sensing typically usually uses a white light source and spectrometer to measure a shift of wavelength. For purely light intensity interrogation sensing, it is possible to use a variety of light sources including the LED and laser diode, and optical receivers including the photodiode, phototransistor or the LDR. To access the information gathered by an OFS, the sensor information needs to be read out and displayed. A common acquisition module for light intensity interrogation is the DAQ module with micro-controller control. For other more complex instruments, the DAQ module is usually built into the instrument. A computer is universally used for data read-out using a common serial interface such as a wired USB or general purpose interface bus (GPIB), or a wireless interface such as Wi-Fi, Bluetooth or ZigBee. Software such as *LabVIEW*™ from National Instruments or *MATLAB*™ from The Mathworks company are commonly used to implement system control and data analysis. To identify examples of developed systems, **Table 1** provides a summary of the attributes of five reported systems. These arrangements use a variety of approaches, but are currently only suitable for use in a laboratory environment.

System configuration is generally similar for all sensor system implementations and this structure is shown in **Figure 7**. Each part can be implemented using different technologies and the choice of implementation is dependent on the requirements of the application. The required

Authors	Jiang et al. [26]	Zhao et al. [27]	Di et al. [28]	Mahanta et al. [29]	Stupar et al. [30]
Sensing mechanism	Surface plasmon resonance	Surface plasmon resonance	Intensity interrogation	Intensity interrogation	Intensity interrogation
Light source	White light source	White light source	LED	He-Ne laser source	LED
Optical receiver	Spectrometer	Spectrometer	Phototransistor	Light dependent resistor	Photo Darlington transistor
Data acquisition	Data acquisition card	Spectrometer	Data acquisition card	Data acquisition card	Microcontroller
Computer interface	USB	USB	DB37 cable	USB	ZigBee
Data readout	Computer	Computer	Computer	Computer	Computer
Data analysis	LabVIEW	–	WaveScan 2.0	LabVIEW	LabVIEW

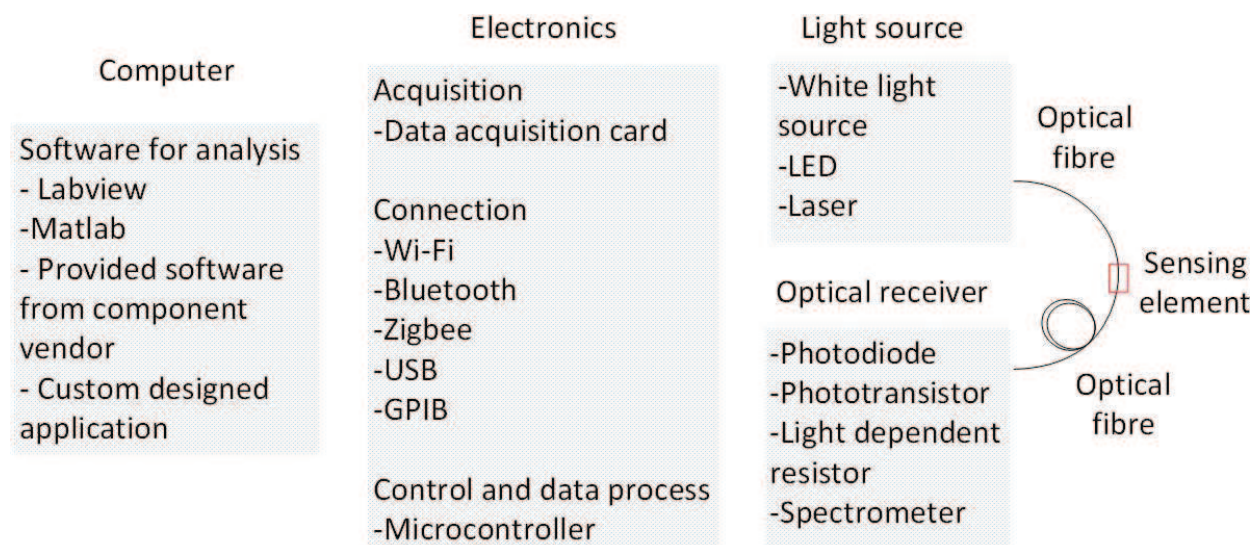**Table 1.** Examples of reported OFS system operation.

Figure 7. Typical sensor system – choice of sub-system components.

resources are identified in terms of the computing (PC), the electronics (electronic-optical-electronic signal interfacing), the light source and the optical receiver.

3. The field programmable gate array

3.1. Introduction

A programmable logic device (PLD) is a device with configurable logic and flip-flops linked together with programmable interconnect. Unlike a processor [microprocessor (μP), microcontroller (μC) or digital signal processor (DSP)] which is programmed to implement a software program, the PLD is configurable (programmable) in hardware. It is configured to implement different digital logic hardware circuits. The architecture provides flexibility in use and re-programmability to quickly re-target the same device to a different application. Early PLDs were based on the architecture of the simple PLD (SPLD) which could implement basic combinational logic and synchronous sequential logic (counter and state machine) circuits. Development of the SPLD led to the complex PLD (CPLD) which essentially is an array of SPLDs with programmable interconnect within a single device and hence, can implement more sophisticated functions. The CPLD has found uses in applications such as instrumentation and control. An alternative to the CPLD is the FPGA. This has a different architecture which allows for high-speed digital signal processing (DSP) operations which would not be possible in a CPLD. An advantage of the PLD is that it the same device can be configured and reconfigured in a short time, thus saving resources in terms of time and money to the need to develop new digital hardware. Any new update or correction can be simply done by downloading a new configuration bit stream into it.

3.2. The FPGA architecture

The FPGA is an integrated circuit (IC) that can be electrically configured to implement a digital hardware design. It consists of a matrix of configurable logic blocks (CLBs) connected via

programmable interconnects and through input/output blocks to interface with other devices. The logic blocks consist of look-up tables (LUTs) constructed using simple memories that store Boolean functions to perform logic operations. The LUT can handle any kind of logic function, but the complexity of the LUT depends on the manufacturer. In addition to the LUT, and with the growing demands to create more complex digital circuits and systems using the FPGA, special purpose blocks such as the DSP slice, embedded memory (Block RAM in FPGAs from Xilinx Inc.) and other functions have been introduced into FPGA. Today, a range of FPGAs from different vendors are available. **Table 2** provides a summary of the devices available from the key programmable logic vendors. The key differences between CPLD and the FPGA are in the device architectures and the complexity of functions that its basic unit is able to perform. The basic unit of CPLD is known as macro cell, using simple sum-of-products combinatorial logic functions and an optional flip-flop.

For a particular design, the configuration pattern is stored in memory within the device or external to the device. The configuration would initially be downloaded into the FPGA memory from an external circuit in the form of a bit stream file. Depending on the particular FPGA, the internal memory may non-volatile memory [electrically erasable programmable read only memory (EEPROM) or Flash] or volatile memory [static read only memory (SRAM)]. When using volatile memory, the configuration will need to be loaded from external memory into FPGA every time it powered on in order to set-up the FPGA. Currently, SRAM based FPGA dominate the market, however the availability of Flash memory based FPGAs is increasing and these provide lower power consumption and no boot time (i.e. the time to start operating once the device power supply is provided).

3.3. FPGA design flow

In many sensor designs, a software programmed processor, typically a μC, is programmed to provide the necessary digital sub-system operations (referring to **Figure 4**). The design flow for

Vendor	FPGA families	SPLD/CPLD	Other relevant devices	Notes
Xilinx Inc.	Virtex, Kintex, Artix and Spartan	CoolRunner-II, XA CoolRunner-II and XC9500XL	3D ICs, Zync PSoC	PSoC – Programmable system on a chip
Intel Corporation	Stratix, Arria, MAX, Cyclone and Enpirion	–	Stratix SoC FPGA	FPGAs were formerly from Altera. Altera MAX family also included CPLDs.
Atmel Corporation	AT40Kxx family FPGA	ATF15xx and ATF75xx CPLD families, ATF16xx and ATF22xx SPLD families	–	–
Lattice Semiconductor	ECP, MachX and iCE FPGA families	ispMACH CPLD family	–	–
Microsemi	PolarFire, IGLOO2 and RTG4 FPGA families	–	SmartFusion2 SoC FPGA	FPGAs were formerly from Actel

Table 2. Summary of key FPGAs and vendors (including SPLD and CPLD devices).

processor based design is well-known to many people and would be chosen based on existing knowledge and experience. However, hardware configured devices such as the FPGA can provide advantages to the system capabilities and operation if the capabilities of the FPGA were known and the ability to design with the FPGA existed. There are a number of advantages of using an FPGA within the digital sub-system and these include:

- High speed DSP operation capabilities such as digital filtering and FFT (fast Fourier transform) operations.

- Concurrent operation which means that operations in hardware can be run in parallel.

- A high number of digital input and output pins for connecting to peripheral devices.

- Programmable I/O standards such as LVTTL, LVCMOS, HSTL and SSTL.

- In-built memories for temporary data storage.

- In-built hardware multipliers for DSP operations.

- In some FPGAs, in-built ADCs are available for analogue input sampling.

- Availability of macros such as FFT blocks for high-speed DSP operations.

- Ability to develop custom architectures suited to the particular application which does not restrict the designer to using the capabilities and limitations of existing processor architectures.

'But how is a design created using programmable logic, specifically with reference to the FPGA?' is an important question to ask. Details of the design flow would be specific to a particular device vendor and each vendor would provide an integrated development environment (IDE) for their devices. The terminology used also differs between vendors. However, **Figure 8** shows a
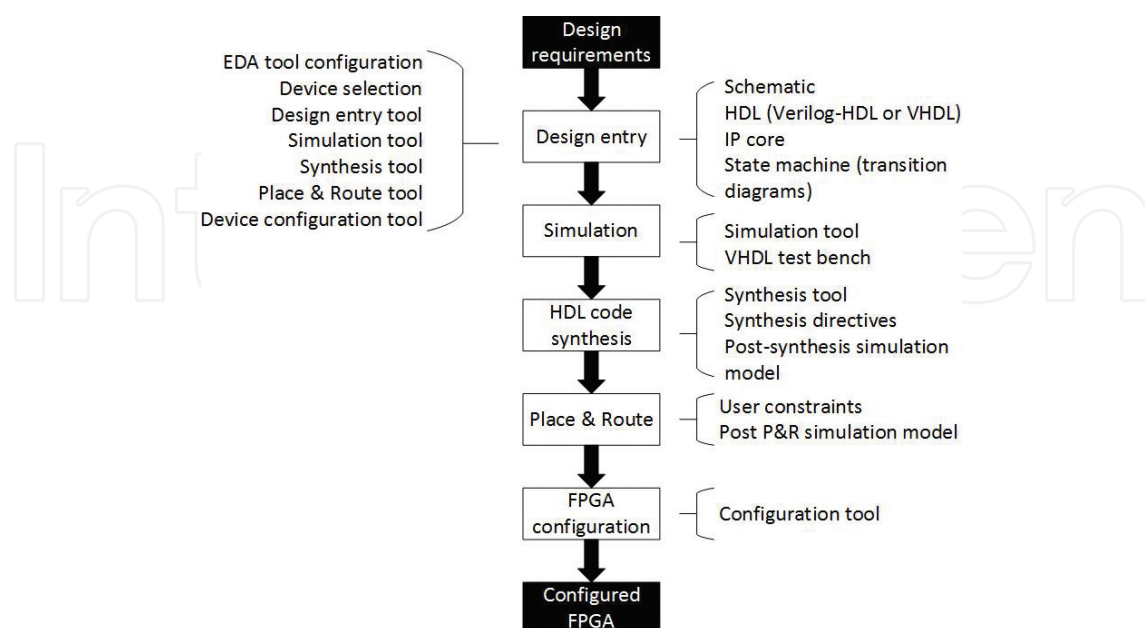
Figure 8. Simplified FPGA design flow.

simplified view of a typical FPGA design flow. Starting with the design requirements and understanding of the capabilities of the target FPGA, the FPGA design tool is used and the design description created. This can be in the form of a circuit schematic, hardware description language (HDL) description, a predesigned IP core or a FSM state transition diagram. An advantage of using an HDL is that the design description is in the form of an ASCII text file and if suitably written, is independent of any particular target device. This means that the HDL code can be synthesised to a different device and this allows for flexibility in design choice and the ability to update designs in the future if so required. The design is initially simulated using a suitably defined test bench (also referred to as a test fixture) before synthesis into logic and implementation within the FPGA (design place and route (P&R) into the FPGA hardware). After synthesis and P&R, timing details in terms of additional signal delays due to logic and interconnect propagation delays can be identified and included in the simulation studies. This is particularly important for high-speed operation as the timing of the signals propagating through the hardware need to be taken into consideration otherwise incorrect circuit operation may occur. Finally, the design can be configured into the FPGA and physical testing of the hardware can then be undertaken. At each step, depending on the simulation and test results, it may be necessary to modify aspects of the design in order to achieve correct circuit operation.

4. FPGA based OFS system

4.1. Introduction

Within an OFS system, the operation of the system in the majority of solutions is controlled by the deployment of one or more software programmed processors. There would be many reasons for adopting such an approach, particularly designer understanding and experience. Using programmable logic as an alternative requires a different design approach and a different set of designer skills. The design philosophy must be switched from '*how can I achieve the required functionality using the available sequential software functions?*' to '*how can I achieve the required functionality in concurrent hardware?*'. When considering the use of the FPGA, there must be benefits for adopting such an approach. The FPGA can:

- Provide the ability to handle real-time system operation with a high sampling rate of sensor data and other DSP operations that other, traditional microcontroller only based approaches would have problems in undertaking. For example, [31] discusses the use of the FPGA within wireless sensor networks (WSNs). In Ref. [32], a phase-sensitive optical time-domain reflectometer using the FPGA is discussed.

- Undertake high-speed DSP operations in hardware using embedded macros.

- Be readily reconfigured in the field for system upgrades.

- Allow the user to rapidly prototype the design in the same way as software programmed microcontroller while provide concurrent processing capability that overcome processor performance and precision limitations.

- Adapt its hardware configuration to a target application needs. As the FPGA does not have a fixed architecture, it is not limited to a predefined set of possible operations and this allows for a custom design which matches the operating requirements of the target application (speed, power consumption, circuit size) to be developed.

In this section, the use of the FPGA is considered as a digital core (sub-Section 4.2) to integrate functions (sub-Section 4.3) for optically based sensor systems.

4.2. The FPGA as a digital core

With reference to the digital sub-system in **Figure 4**, this can be considered in terms of the functions it needs to implement. Specifically the required functions can be considered as:

- Sensor interfacing.

- Control.

- Storage (memory).

- DSP.

- Communications to an external electronic system.

- User interfacing.

Figure 9 shows a simplified block diagram for an FPGA based design that implements the above functions. The FPGA operation control signal timing is determined by the external clock it uses (e.g. a 100 MHz clock) and control signals from external peripheral devices (e.g. an external power-on reset circuit) as well as user control which has been configured into the
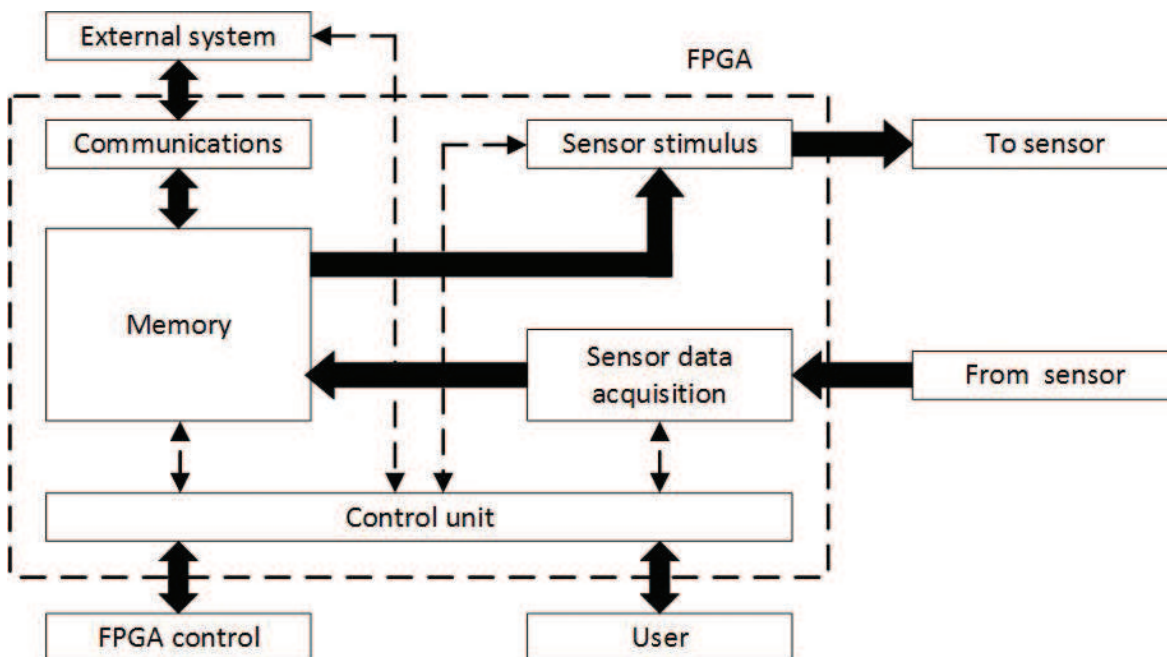

Figure 9. FPGA core functions example.

device. User control can come from an external electronic system using wired or wireless communications and from human interaction devices such as a keypad or touch-screen device. This requires a suitable *Control unit* to be designed for controlling the other circuits configured into the FPGA. Signals to/from an external system would be via a suitable *Communications* circuit that allows both control signal and data transfer. Local memory, bistables (latches and flip-flops) and SRAM are used for temporary storage. *Memory* may be internal to the FPGA only, or external. Output to the sensor in the form of *Sensor stimulus* would be in the form of a voltage that may need translating to a current. For example, an LED may be driven by a DC current level or by a modulated signal using a signal encoding scheme such as pulse-width modulation (PWM). Sensor response would be sampled using a *Sensor data acquisition* circuit. Building on this architecture, additional operations, such as DSP, can be included.

4.3. Integrating functions into the FPGA

An OFS system based on a digital core within an FPGA will need to ensure that the circuit configured into the FPGA meets the system requirements. A simple implementation would consist of a basic communications protocol, along with a basic signal generator (LED current control) and a signal capture (photodiode current sampling) along with memory for temporary storage of values (where the memory requirements are small then latches and flip-flops would be sufficient, whereas where the memory requirements are larger, static random access memory (SRAM) and Flash memory would be required). Such a basic system would not utilise many of the available hardware resources within the FPGA and in such a case, a smaller and simpler CPLD would probably be sufficient. The power of the FPGA however becomes apparent where higher operating frequencies and embedded DSP functions are introduced. For example, analogue signal measurements are influenced by external parameters such as ambient temperature and noise introduced into the signal from surrounding electronic circuitry and the ambient environment. This would be particularly noticeable where low-level signal measurements are required. To improve system performance, signal processing techniques such as oversampling, averaging and correlation can be used as well as digital filtering and the FFT. For these functions to operate in an application such as a real-time system, the calculations to be performed need to operate at high frequency and utilise high-speed memories for temporary storage. All these requirements map effectively to modern FPGAs and so can make the FPGA the natural choice for a high performance embedded sensor arrangement. With the increased interest and use of the FPGA in DSP operations, recent FPGA architectures have evolved with high-speed operation and complex DSP in mind. Generally, FPGAs today incorporate the following circuitry. With reference to the Xilinx FPGA families, these can include:

- CLB: The configurable logic block is a basic building block of the FPGA and incorporates circuitry such as the look-up table (LUT), a flip-flop and a multiplexer.

- Distributed RAM: Small RAM within the LUT.

- Slices: Slices are groups of LUTs and flip-flops.

- Block RAM (dedicated two-port memory), first-in first-out (FIFO) and error correction checking (ECC) cores.

- Singled-ended and differential input/output cells (I/O): For higher speed signals, differential signals are preferred and the programmable I/O cells can be configured for single-ended or differential signal operation and with different I/O standards.

- DSP slices: Essentially high-speed cells that can be used to create DSP operations.

- Analog(ue) mixed-signal (AMS) core: XADC, in-built ADC.

- Configuration bit stream encryption blocks incorporating methods such as AES, HMAC and DNA.

Although the discussion into the use of the FPGA has so far concentrated on the development of custom hardware designs, with hardware architectures suited to a target application needs, it is possible and in some cases preferable to utilise a software programmed processor. A processor itself is simply hardware with logic gates and memory connected in such a way to implement a processor architecture. The FPGA therefore can be used to implement a processor core and so be configured to act as a software programmed processor. Either a pre-defined processor architecture can be implemented within the FPGA as an intellectual property (IP) core with a description provided in Verilog-HDL or VHDL, or the designer can develop their own architecture processor. Therefore, the FPGA can implement a design which is based on hardware logic only, be based on a processor only or, and where the benefits of using the FPGA can be truly seen, can implement a hardware-software co-design within a single device. In addition, with the hardware resources available in many FPGAs, multiple processors can be implemented within a single FPGA and so architectures consisting of arrays of interconnected processors operating concurrently with hardware only based designs for high-speed computations can be developed.

5. Case study design

5.1. Introduction

Modern OFS systems are becoming ever more sophisticated as such systems today are targeting more complex problems than previously considered [33]. This includes the need for more sophisticated and computationally intensive data analysis methods. Today, an OFS system that uses a personal computer (PC) and software data analysis software such as *LabVIEW™* or *MATLAB™* has little difficulty to undertake such analysis tasks. However, the PC may not necessarily be an ideal data processing unit for in-field measurements or real time monitoring in remote areas due to its size and power consumption requirements. To make this system portable for personnel to carry, and for remote deployment over extended periods of time, it has to be physically small, lightweight, low-power and battery powered. The system should be as easy as possible for operator personnel to use as they should not be expected to understand the detailed electronic circuit operation or the arrangement that forms the system. It would also be better if it is capable of real-time data processing that provides timely and useful information via modern telemetry. Real-time data processing also reduces storage and transmission requirements that both consume precious resources in a portable system [34].

This section provides a case study into an OFS system using the surface plasmon resonance (SPR) principle. The objective of this case study was to demonstrate integration of the FPGA into an OFS system based on SPR. SPR is a popular sensing mechanism for biomedical optical sensors as it is sensitive to a change in the refractive index of a surrounding medium. It is a phenomenon that occurs when photon momentum is matched with plasmon momentum and thus photon energy efficiently transfers to the surface plasmon. This results in absorption of specific wavelengths of light that are then visible in the resulting light spectrum and the absorption wavelengths are then used to determine the properties of the measurand. The surface plasmon effect exists only in p-polarised (transverse magnetic) waves, so it is a requirement that a p-polarised wave is generated that oscillates in the same orientation in order to be excited. A propagating photon in vacuum or air does not have enough momentum to excite SPR [35]. The common technique to excite SPR optically is by using total internal reflection to create an evanescent wave that has a higher momentum. The matching condition depends heavily on the surrounding environment which makes it suitable for use as a sensor. **Figure 10** shows the principle of operation for the sensor used.

The electronic system design was also created to be modular in order to accommodate different sensing mechanisms. This is readily managed using POF as the interface medium since the sensor housing can be changed by simply removing and inserting the transmitting and receiving fibres. The system architecture developed is discussed and the strategy to implement refractive index measurement using a combination of the FPGA with a tri-colour (RGB: red, green, blue) LED and photodiode is proposed. The FPGA functionality is identified in a later section. System control and data acquisition with a host PC was created using the Python open
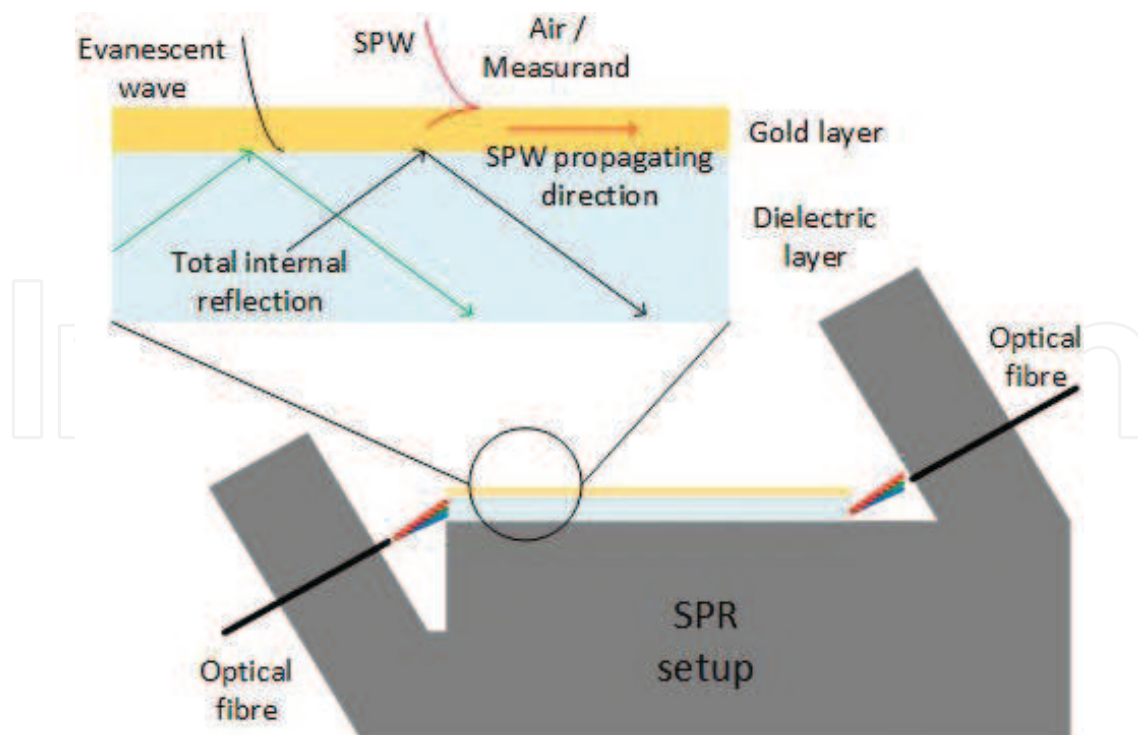

Figure 10. Surface plasmon sensor. Schematic diagram of total internal reflection and surface plasmon wave (SPW) generated during SPR.

source programming language. However, the FPGA operation does not rely on a PC connection to work. The FPGA used was the Xilinx Artix-7 [36] FPGA and this was embedded within the Arty development board from Digilent [37]. The FPGA operates on a 100 MHz clock frequency on this particular development board, so all digital signals were timed to this master clock. Connections to an external printed circuit board (PCB) with additional hardware was made using the available PCB header connections. This supports the capability to readily configure the FPGA as well as enabling the FPGA to be powered from the USB port +5 V power supply for development. In the final set-up, a battery pack provides the power supply for the FPGA. The digital logic operating within the FPGA was developed using VHDL design entry and synthesised to the Artix-7 architecture. Design entry and simulation using VHDL test benches were undertaken using the Xilinx Vivado toolset.

5.2. System architecture

The circuit hardware design, as shown in **Figure 11**, was separated into five sub-systems: OFS, power supply, digital core, light signal generation and sensing module. The power supply module comprises a low-dropout linear voltage regulator circuit for providing the necessary power supply to the light signal generation and sensing modules. A separate linear voltage regulator is used to isolate the photodiode circuit from digital noise which could be present on the power supply from the FPGA board. These regulators also provide the system flexibility to accommodate different battery voltage levels.

The light signal generation and sensing modules are additional circuits that support the opto-electronic components and their corresponding circuits. For light signal generation, a current source was designed to control the light through a digital signal (two level voltage) from the FPGA. As a tri-colour LED was used, the FPGA was required to provide a sequential series of
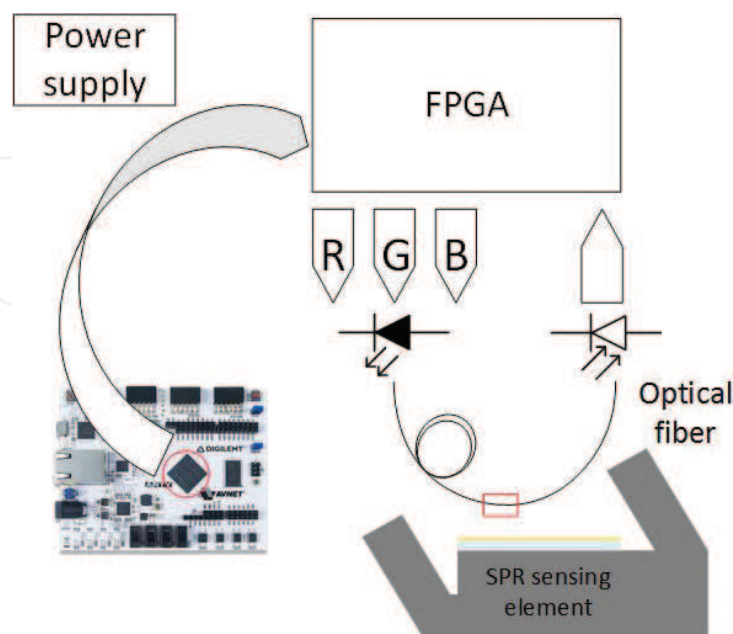

Figure 11. Case study system architecture.

red, green, and blue light pulses in a current range from 0 mA to 20 mA for each LED. With the receiver, the analogue response from photodiode circuit as a voltage was sampled using the in-built 12-bit 1 MSPS (mega sample per second) ADC (XADC) and the sampling of the responses were synchronised with the XADC conversion timing within the FPGA. Therefore, the intensity of the individual colour pulses could be recorded separately. The on-chip ADC is then used to translate the voltage reading into a 12-bit digital signal. The photodiode current is initially converted to a voltage using a high-gain transimpedance amplifier and then amplified. For a high attenuation sensing mechanism, the received light intensity is low and a high-gain transimpedance amplifier using an operational amplifier (op-amp) hence required. However, this leads to noise related issues and so the choice of a suitable op-amp along with the use of noise reduction techniques are required in the realised electronic circuit. To reduce noise in this design, PCB ground planes and an aluminium shield fixed on top of the receiver circuit was required. Although these additions reduced the resulting noise levels, additional noise reduction should also be considered. A 3D printed cap for the LED allowed a bare-end of the POF to collect light immediately from LED without any focus aid and coupled the light into the sensor housing without the need for a connector. A photodiode that requires no connector was also chosen to be the optical receiver for the modulated light. The OFS is an extrinsic sensor; gold film coating on top of a glass slide and mounted on top of a 3D printed housing to position the fibre at an angle facing the edge of the glass slide. It was designed to excite SPR for different measurands with minimum change in the blue light region.

The digital output from the FPGA is fed into an op-amp based current driver circuit. The digital logic 1 and 0 values from the FPGA are represented by two voltage levels of 3.3 V and 0 V. It is assumed in this discussion that the voltage levels produced are exactly 3.3 V and 0 V. The voltage-to-current conversion is achieved using an op-amp as a unity gain amplifier with a transistor in the feedback loop as shown in **Figure 12**. The transistor is included in this configuration as a current amplifier as it can achieve higher current output than the op-amp alone. A 20 mA current was allowed to flow when a logic 1 output is given and no current otherwise (logic 0). A current sensing resistor, R_E, is used to provide a voltage input for the op-amp. The average current then can be controlled using the pulse width modulation (PWM) control technique which is generated using a PWM generator circuit within the FPGA. The FPGA then receives an analogue output from a transimpedance circuit that translates the generated current into a voltage.
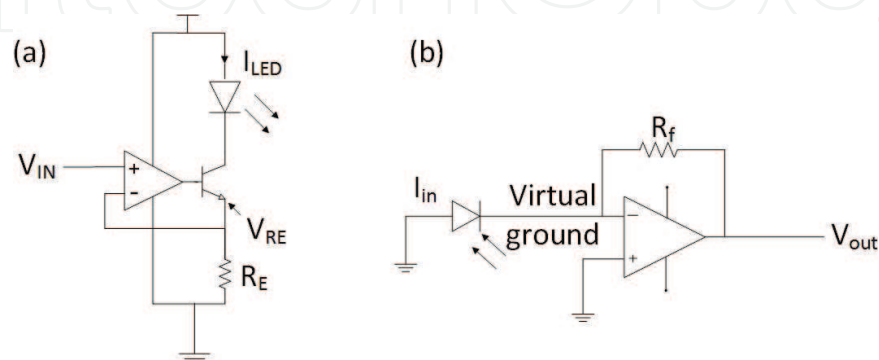

Figure 12. (a) Current source and (b) transimpedance amplifier circuit.

The Artix-7 FPGA board used also has some additional and useful features which include external SRAM, external Flash memory and the ability to be powered from the USB connector or any 7–15 V power supply voltage source. The Artix-7 FPGA operates with a core voltage of 1 V, with 3.3 V I/O and a 100 MHz master clock. The XADC has access to nine external analogue input channels and is capable of performing self-calibration in order to correct for offset and gain errors, provided that the ADC reference voltage is reliable (i.e. an accurate and stable value). On-board peripherals include a USB-UART (UART: universal asynchronous receiver transmitter) integrated circuit that allows a computer to communicate with FPGA for configuration and data transfer during normal operation. This wired communication is especially useful during development and testing. However, in the realised system and once the FPGA has been configured, a ZigBee wireless interface is used for normal data transmission and this allows the sensor hardware to be operated at a distance from the computer. This FPGA board undertakes multiple functions including system control, data processing, communication, LED control and analogue-to-digital conversion (ADC) for sensing module. Its functionality is discussed detail in the next section.

5.3. FPGA functions

To support the system operation as previously discussed, the FPGA function as a digital core (sub-system) that itself is composed of different sub-systems. The circuit configured within the FPGA is shown diagrammatically in **Figure 13**. This is a block diagram representation of the VHDL code. These sub-systems include data acquisition, control system, communication, LED pulse generation. All these sub-systems were initially described in VHDL and operate concurrently. The control system includes an XADC acquisition control unit that keeps the timing of the XADC and LED pulse generation units in synchronisation. It allows the user to set the
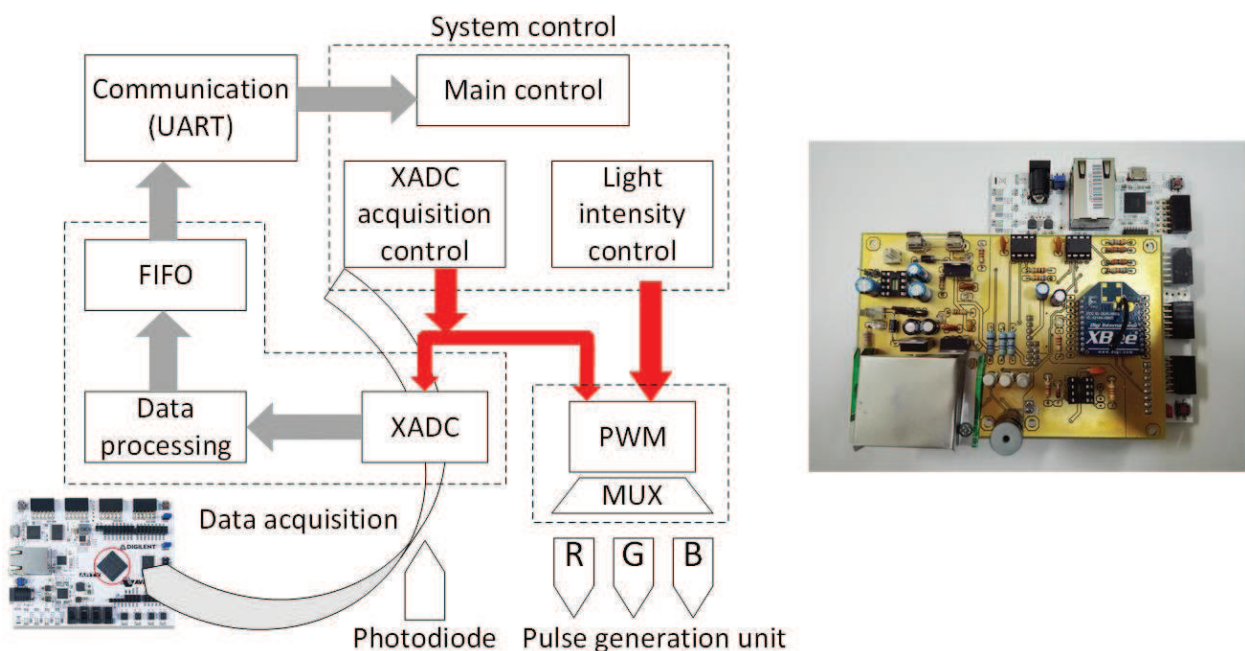

Figure 13. Schematic of the digital design implemented within the FPGA.

number of measurement to be taken. The light intensity control unit is tasked to regulate the duty cycle of the PWM output for each LED. The generated signal is then passed to the digital pin output set by multiplexer. The data acquisition system involves the use of the XADC that is capable to sample voltage reading from 0 to 3.3 V into 12-bit digital signal and can be controlled in order to accommodate different settling times for the signal conditioning circuit or different sampling rates. The acquired data bit size is bigger than the UART protocol (with eight bit data, one start bit and one stop bit), and so is required to be separated into two parts. A protocol was developed for data transmission which included a header to indicate each different light colour. Within the FPGA, sampled data is processed and the processed data stored in memory storage before transmitted to PC when requested to do so. Serial communication is implemented using UART protocol with a Baud rate of 115,200 baud. At this stage, the data is then processed with computer.

5.4. Control and data acquisition using Python

In order to interface the PC to the FPGA and then to the user, a USB or ZigBee serial interface is used. The FPGA and the computer then communicate using UART protocol so that the computer can send commands to the FPGA and the FPGA can respond with sensor data results. Therefore, a suitable programming language was required to achieve the computer-to-FPGA and computer-to-user communications. In this work, the Python open source language is used to implement system control, data acquisition and data presentation. A graphical user interface (GUI) was built using *Tkinter* and *Matplotlib* modules for Python which enabled live data presentation. The GUI is shown in **Figure 14** with left graph showing all red, green, and blue intensities plotted together and three smaller graph at the right side shown three
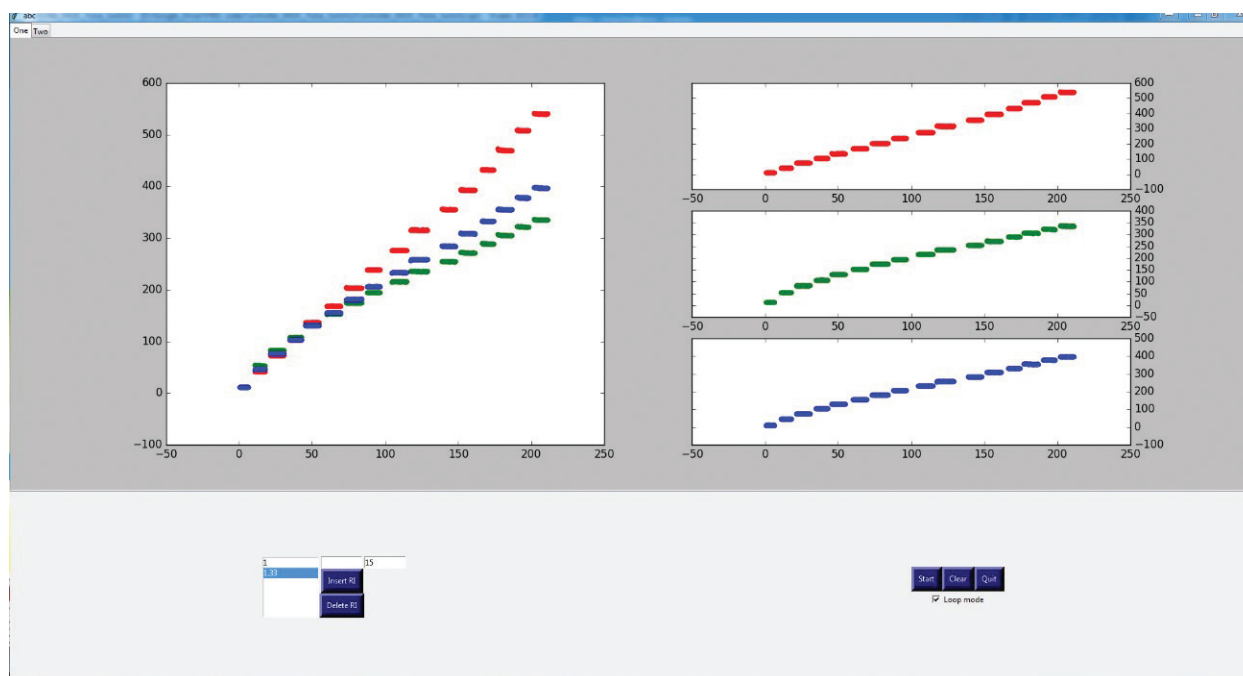

Figure 14. GUI created from Python.

individual colour intensity plots. Data labels for data frame are selected at lower left region of GUI. The lower right region are for system control: measurement initiation and process termination. The *Pyserial* module was used for communication with the FPGA by using the computer COM port in order to carry out FPGA control and sensor data acquisition. The acquired data stream is then formatted using the *NumPy* and *Pandas* modules. The data structure used was a data frame using the *Pandas* module. This data frame was considered as it allowed the sensor data to be serialised into a minimal and useful *JSON* format that could then be stored in a database or readily transferred elsewhere. In addition, a *MySQL* database was set up for data storage and management.

Test results are shown in **Figure 15**. The top plot shows the sensor results with air as the measurand and the bottom plot with water. A comparison is made between the spectrometer measurement using an Ocean Optic QE65000 and the Industrial Fiberoptics IF-D91 photodiode output. The spectrometer integration time was set to 500 ms. The line plot showing the spectrometer reading is shown on the left y-axis and the overlap bar plot showing the photodiode measurement for intensity reading is shown on the right y-axis. The wavelength x-values are only for the spectrometer reading while the photodiode just overlap with it for comparison. In this view, both the spectrometer and photodiode's y-values are represented in plot using arbitrary units. The photodiode measurement and spectrometer readings for different measurands has shown good agreement in terms of the trend of the signal during the measurand change. However, the magnitude of the changes are not exactly the same for the spectrometer and photodiode and this can be attributed to different spectral responsivity. The plot shows that the blue colour measurement is relatively stable for both the photodiode and spectrometer. The blue colour measurement shows a weak response to both measurands and it is therefore suitable for use as the reference signal. It provides the system with a self-calibration capability which can be built in hardware within the FPGA.
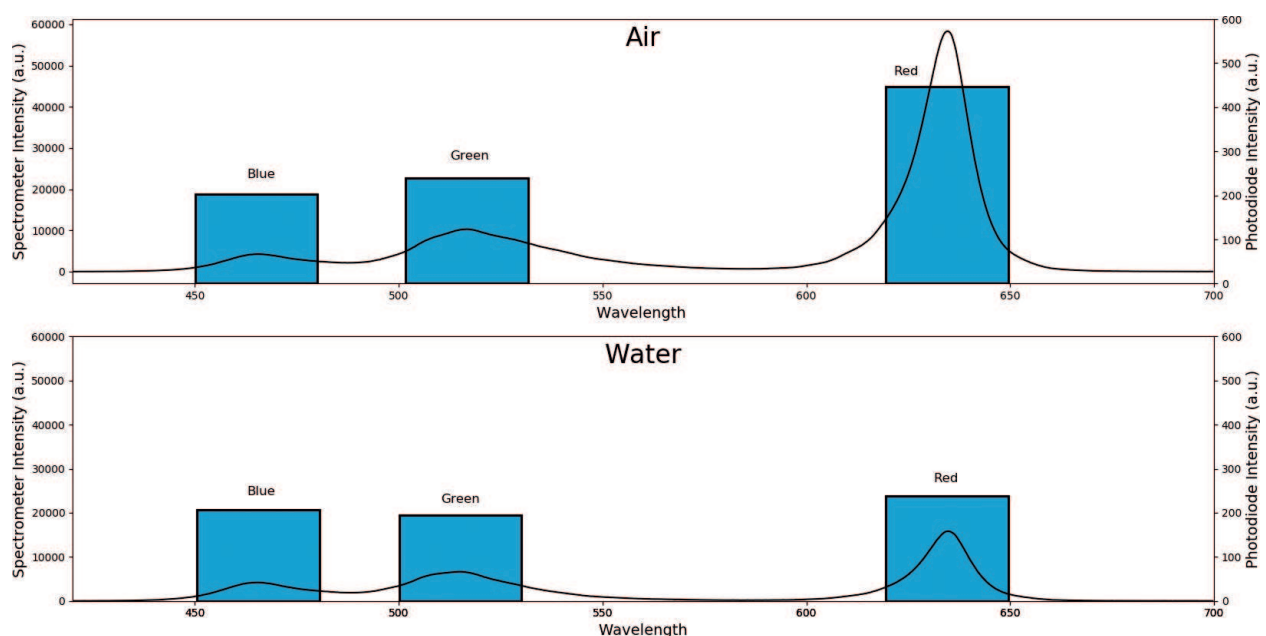

Figure 15. OFS test results visualisation.

6. Conclusions

In this chapter, the use of programmable logic has been discussed in relation to the design and implementation of OFS systems using POF technology. Specifically, the focus of the discussion was based on the use of the FPGA to provide hardware functionality as a complement to a software based processor approach. In this case, the necessary digital operations were performed in hardware using a synthesised VHDL description of the digital logic functions. The FPGA provided the necessary signals to control the output light intensity of a LED source using current control. An RGB LED was used, and hence three wavelengths of light could be created and combined. The light was propagated to a SPR sensor using standard 1 mm diameter POF and was received by a photodiode detector, also using POF. The chapter has included a case study of a SPR sensor based on POF, and the system has been designed, built and characterised when tested in air and submersed in water. With the functions created in this particular application, the building blocks of the FPGA based sensor systems capable of measurement of a wide range of parameters could be developed. FPGA control, data capture and visualisation was achieved on PC using the Python open source language.

Acknowledgements

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