Chapter 3

Redox-Active Molecules for Novel Nonvolatile Memory Applications

Hao Zhu and Qiliang Li

Additional information is available at the end of the chapter

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Abstract

The continuous complementary metal-oxide-semiconductor (CMOS) scaling is reaching fundamental limits imposed by the heat dissipation and short-channel effects, which will finally stop the increase of integration density and the MOSFET performance predicted by Moore's law. Molecular technology has been aggressively pursued for decades due to its potential impact on future micro-/nanoelectronics. Molecules, especially redox-active molecules, have become attractive due to their intrinsic redox behavior, which provides an excellent basis for low-power, high-density, and high-reliability nonvolatile memory applications. This chapter briefly reviews the development of molecular electronics in the application of nonvolatile memory. From the mechanical motion of molecules in the Langmuir-Blodgett film to new families of redox-active molecules, memory devices involving hybrid molecular technology have shown advantageous potential in fast speed, low-power, and high-density nonvolatile memory and will lead to promising on-chip memory as well as future portable electronics applications.

Keywords: molecular electronics, redox-active molecules, self-assembled monolayer, nonvolatile memory, high-density, high-endurance, flash-like memory

1. Introduction

1.1. CMOS scaling challenges and impact on nonvolatile memory

The complementary metal-oxide-semiconductor (CMOS) scaling has deviated from the trends predicted by Moore and the scaling rules set forth by Dennard et al. due to both fundamental physical and technical limitations [1, 2]. This will inevitably slow down the pace of current CMOS scaling when approaching atomic dimension. Scaling limitations such as

ultrathin gate oxide, channel length modulation, and off state leakage have become growing concern, and there are urgent needs to develop new semiconductor technology and solutions toward CMOS scaling challenges. For example, barriers such as doping, carrier transport, and series resistance scaling have been effectively avoided by innovations such as source/drain process upon silicon-on-insulator (SOI) structure, multigate field-effect transistor (FET), and SiGe BiCMOS technologies [3–6].

Currently, computing architectures and electronic systems built on CMOS components are still pursuing without signs of slowing down of requirements for low-power, fast speed, and high-density alternatives [7, 8]. Various scenarios of fundamentally new technology with advanced materials and structures have been proposed and investigated such as quantum computing, DNA computing, single electron device, spin transistor, and molecular electronics for both logic and memory applications. However, these new approaches still need in-depth studied before they can be considered for application in real-world device applications.

In modern electronic systems, the main functions lie in the data computing and data storage, which take up more than half of the semiconductor market. Solid-state mass storage occupies a large portion of this market; the demand is still growing explosively in areas such as portable electronic devices, due to their compatibility with CMOS scaling, suitability for harsh environment, and the fact that most types of memory are nonvolatile, which means that the data information can be maintained even without power supply. Currently, main types of nonvolatile memory technology that have been investigated include phase-change memory (PCM), ferroelectric random access memory (FeRAM), resistive random access memory (RRAM), magnetic random access memory (MRAM), and flash memory [9–13]. However, these nearer term new technologies have inherent disadvantages that may limit their implementations. For instance, even though FeRAM, PCM, and MRAM are currently in commercial production, they are still many years away from competing with dynamic RAM (DRAM) and NAND (Not-AND) flash for industry adoption [14, 15]. On the other hand, the retention time of floating-gate DRAM decreases with scaling, and the relatively poor endurance of the flash memory ($\sim 10^5$) is the critical limitation for its further application.

1.2. Molecular electronics

1.2.1. Introduction

Molecular technology has been aggressively pursued for its potential impact on nanoelectronics since the early 1970s due to its inherent scalability and intrinsic properties [16–18]. Molecular electronics has been considered to replace the conventional silicon-based computing even before hitting the fundamental limits [19–21]. Molecular electronic devices are typically fabricated by forming a self-assembled monolayer (SAM) or multiple layers on different surfaces using inexpensive and simple processing methods. Such device functions by the controlling of fewer electrons at a molecular scale, and therefore, has potential for fast speed, low-power, and ultrahigh-density device and circuit applications.

Molecular electronics are typically achieved through two fundamentally different approaches, which are graphically termed as "top-down" and "bottom-up". The top-down approach includes

making nanoscale structures by machining and etching techniques. Molecular electronics relying on the bottom-up approach takes advantage of molecule self-assembly, building organic or inorganic structure by atom-by-atom or molecule-by-molecule techniques. In the past decades, the cross-disciplinary publications in the field of molecular electronics have dramatically increased by chemists, physicists, engineers, and other researchers. Various novel molecular device architectures and electronic systems have been introduced and explored. Nevertheless, most of the molecular electronics has been implemented by top-down approaches, and recently, the combination of top-down device fabrication (mainly lithography) with bottom-up molecule self-assembly has attracted more and more interest.

1.2.2. Advantages and challenges of molecular electronics

Molecular electronics competes to a large extent with conventional microelectronics based on traditional metal-oxide-semiconductor (MOS) structures. Molecular electronics has been expected to possess the following advantages [22]. First, the inherent scalability of molecules enables functional structures and ultrahigh device density with atomic control over a diversity of physical properties. Second, molecules can be self-assembled through intermolecular interaction to form nanostructures, and further for desired molecular devices and circuits. Third, molecular properties can be tailored with choice of composition and geometry, including electrical transport, binding, and structural properties. Fourth, a variety of molecules have multiple distinct stable electrical and geometric structures, therefore, molecular switching devices and circuits can be achieved through the transitions between different structures under electrical or chemical stimulus.

The major challenges molecular electronics are facing lie in the unknown reliability at high temperature, volatile environments, and electrical stress. The instability at high temperature makes most molecules incompatible with current CMOS process integration. The retention time is the biggest challenges for most of the molecular memory devices as at least >10-year retention time is necessary in order to be considered as a candidate technology for universal memory applications. Some specific condition and environment need to be taken care of when integrating molecular electronics in conventional CMOS devices and circuits. Furthermore, molecular technology development requires advancement in both molecular properties and device integration processes.

1.2.3. Redox-active molecules

Redox-active molecules have attracted more and more interest recently, due to their intrinsic and reliable redox behavior, which can be readily utilized for charge-storage memory applications. Physically, a redox-active molecule contains a redox component acting as the charge-storage center surrounded by insulators/barriers formed by the linkage and the surface group. The electrons tunnel through the barrier during the oxidation and reduction processes. Typically, the application of an oxidation voltage will cause electron loss in the redox molecules; reversely, the electrons will be driven back to the molecules by applying a reduction voltage. Generally, the redox molecules have multiple stable states. The switching between these states is dynamically reversible through the loss or capture of a charge, that

is, oxidation and reduction of the redox centers. Distinct charged or discharge states can be deemed as logic on and off states, at different voltage with very fast write and erase speeds. It has been demonstrated that the redox molecules attached on silicon structures are stable and can endure more than 10^{12} program/erase cycles [23]. Such advantageous properties of redox molecules make them very attractive for future applications of fast speed, low-power, high-endurance, and high-density nonvolatile memory.

There have been great efforts to effectively integrate molecules as the active component for future micro-/nanoelectronic devices. The following sections will review the attachment and characterization of redox molecules on active surfaces, and the strategies to involve such attractive medium in low-power and high-density nonvolatile memory applications.

2. Redox molecules, attachment, and characterization techniques

2.1. Redox-active molecules

As described above, the generic structure of a redox-active molecule consists of redox-active components, linkage components, and surface attachment groups. **Figure 1** illustrates two examples of redox molecules with different components [24, 25]. α-Ferrocenylethanol (referred as ferrocene) molecule shown in **Figure 1a** has one Fe redox center and -OH linker component. $Ru_2(ap)_4(C_2C_6H_4P(O)(OH)_2)$ (referred as Ru_2) possesses two Ru redox centers, and the phosphonic acid component functions as the linker part. Such redox molecules have discrete energy states, which are accessible with relatively low, distinct, and quantized voltages. Ferrocene has a single cationic-accessible state and, therefore, can exhibit two states: neutral and monopositive. Ru_2 has two Ru metal atoms as redox centers; thus, it has two cationic states leading to three charge states: one neutral and two positive states. This is very attractive for multibit memory storage applications.

Despite the redox-active and linker components shown in **Figure 1**, a variety of different redox-active and linkage parts can be specifically designed and engineered for purposes including more redox states and attachment on desired surfaces via covalent bonds [26–29]. The molecules reviewer here are more focused on the attachment on Si and oxide structures with specific tethers and linkers, due to the prevalence of silicon in current microelectronic devices and the subsequent implementation in CMOS compatible nonvolatile memory devices.

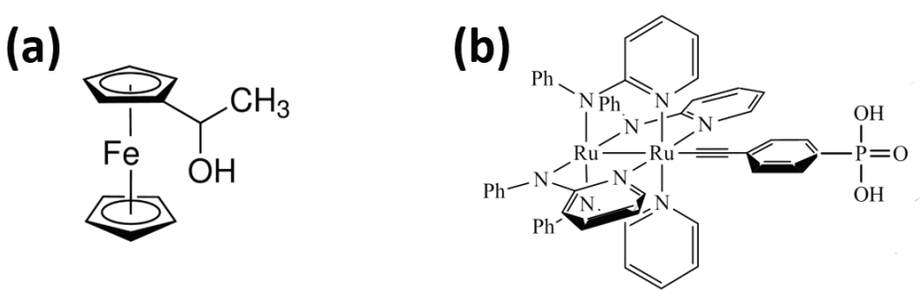

Figure 1. Structure of redox-active molecules (a) α-ferrocenylethanol and (b) $Ru_2(ap)_4(C_2C_6H_4P(O)(OH)_2)$ [24].

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2.2. Molecule attachment and characterization techniques

2.2.1. Attachment methods

The attachment of well-ordered and tightly packed layers of molecules on active surfaces is important for the application of redox molecules in electronic devices. The attachment technique reviewed here is by using the self-assembled monolayers (SAMs) [24, 30–33]. SAMs are formed on active surfaces via covalent bonds to the atoms on the surface, and specific tether groups can be designed such that they can only attach to specific surfaces. The attachment of SAMs of redox molecules is via the use of chemical solution deposition [30]. A layer of 110 nm SiO_2 was first thermally grown on the Si substrate followed by the definition of square-shaped active areas (100 μm wide) using photolithography and wet etching. Then, a thin layer of SiO_2 was grown in the active area for the molecule attachment on the oxide surface, and it will also function as part of the tunnel barrier in the memory device. The solutions for deposition are prepared by dissolving redox molecules in organic solvents. The SAMs were then formed by placing droplets of the solution on the active areas with each drop kept in place for 3–4 min. The samples were held at elevated temperature in an N_2 environment during the attachment process. Saturated SAMs will be formed after ~30 min. An alternative approach to form SAMs is by immersing the substrate into the solution under same condition for a certain period of time. During the attachment process, redox molecules are covalently bonded to the desired surface through the linkage component. After the self-assembly process, the same organic solvent and the cleaning organic solvent were used to rinse the substrates in order to remove any residual molecules that are not bonded to the surfaces.

2.2.2. Characterization techniques

After the molecule attachment, cyclic voltammetry (CyV) was used to characterize the attachment quality and measure the molecule surface density. **Figure 2** shows the schematic of the CyV characterization setup [24]. The measurements were performed in a standard probe

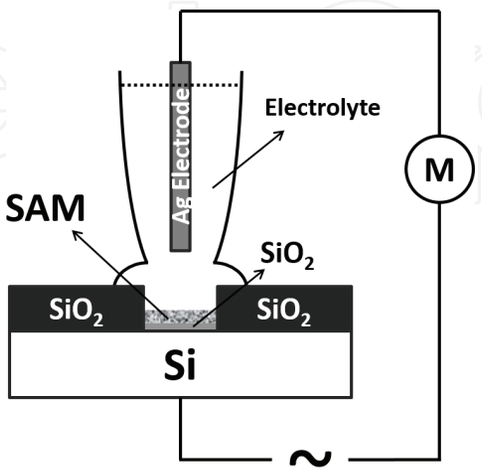

Figure 2. Schematic of the CyV characterization setup. "~" represents the voltage source and "M" represents the electrometer [24].

station, with the backside contact made via the probe station chuck. A solution of 1.0-M tetrabutylammonium hexafluorophosphate (TBAH) in propylene carbonate (PC) was used as the conducting gate electrolyte. Polypropylene micropipette tip containing the silver counter electrode and the electrolyte was lowered until only a small amount of electrolyte was spread across the active area. During the measurement, the voltage was applied on the substrate, and the CyV curves were obtained using a CHI600 electrochemical analyzer.

3. Redox molecules for nonvolatile memory applications

In this section, the early logic forms of molecular memory—molecular logic switching devices will be reviewed. The integration of redox molecules in a liquid electrolyte-involved nonvolatile memory device will be discussed where we also consider the device-related issues and limitations.

3.1. Introduction

3.1.1. CMOS memory technology

The continuous CMOS scaling and the impact on memory scaling has pushed for the investigation of alternative storage technologies, and many solutions have been proposed and studied. Solid-state mass-storage memory is getting a large part of the market, as introduced in the first section, due to its consolidated technology, better reliability, nonvolatility, and tolerance to harsh environment. Currently, the main solid-state reprogrammable nonvolatile memory is based on the floating-gate structure, which is also known as flash memory. Flash memory has fast read access times, good retention and reliability, and CMOS compatible fabrication process [34, 35]. However, physical limitations related to the difficulty in shrinking the tunnel and interpoly dielectric layer have further reduced the margins for the memory cell size reduction predicted by Moore's law. The floating-gate memory will suffer short-channel effects when the channel length is scaled below 100 nm. Leakage current will be significant during program/erase operations due to both drain-induced barrier lowering (DIBL) and subsurface punch-through effects.

In recent decades, charge-trapping nonvolatile memory has attracted intensive attention to replace the conventional floating-gate memory due to its advantages such as better scalability, lower power consumption, improved reliability, and simpler structure and fabrication process [36–38]. In a charge-trapping memory, the electrons are stored in a trapping layer, instead of the conducting floating gate in the conventional floating-gate memory. Different charge-storage media have been well studied, including conventional nitride material, various nanocrystals, and high-k dielectric materials. Incorporating redox-active molecules as the charge-storage medium in a Si-based nonvolatile memory is very interesting, as it will leverage the advantages afforded by a molecule-based active medium with the vast infrastructure of traditional metal-oxide-semiconductor (MOS) technology.

3.1.2. History of molecular memory

Memory application of molecules has been widely investigated, and one of the most common approaches in the molecular memory devices has been the bistable conductance switching devices. There are two major device architectures based on these devices: molecular crossbar circuit and nanocell molecular circuit.

In a crossbar circuit, the switching element is a metal/molecule/metal sandwich junction, wherein the molecules are located at the cross-section of two nanoscale metal wires [39–41]. The early demonstration of such a junction-switching device utilized the bistable rotaxane molecule that consists of two mechanically interlocked rings [39]. The molecular monolayers were deposited as a Langmuir-Blodgett film. The mechanical motion of such a molecule is an activated redox process, and the two stable mechanical states can exhibit different tunneling currents, representing logic on and off states. Note that ~100 on/off current ratio has been reported, but with limited endurance cycles. By taking advantage of the fabrication simplicity and high nanowire density, large-scale crossbar circuit has been realized [42]. However, the controlling of metal-molecule interface is the major challenge, upon which a new theory was put forward with experimental evidence indicating that the conductance switching in the metal/molecule/metal junction is independent of molecules, but attributed to the electrode reactions with molecules [43, 44].

Nanocell molecular circuit is a two-dimensional network of self-assembled metallic particles connected by molecules [45, 46]. The active component in a nanocell is also metal/molecule/metal switch. The molecules in a nanocell can show reprogrammable negative differential resistance which was initially believed to be originated from the redox center in the molecules. However, experimental results suggested that the electron transport phenomena is more likely due to the nanofilamentary metal switching, which is correlated with the similar metal-molecule interface problems as the crossbar circuit [46].

In addition to the two-terminal metal/molecule/metal junction devices, molecules have also been tested as the channel material in a standard three-terminal metal-oxide-semiconductor (MOSFET) architecture [47–49]. Even though organic field-effect transistors (OFETs) with low-power and low leakage current have been demonstrated, such OFETs suffer from the slower switching speed and limited device lifetime as compared with conventional silicon transistors. Moreover, the poor stability in a harsh environment is another disadvantage of these OFETs. Thus, the direct integration of molecules in advanced silicon CMOS technology is still under question and needs further research efforts.

3.2. Electrolyte/molecule/Si capacitors for memory application

3.2.1. Introduction

Based on the molecular logic switching devices, appropriate modifications of the molecular structures and switching elements have been designed to change the switching kinetics with enhanced memory performance. Different device platforms have been engineered to interface

with molecules such as oxides, dielectrics, nanowires, and so forth. The memory effect achieved by integrating redox-active molecules is very promising, due to the intrinsic redox behavior of the molecules giving birth to fast speed, low operation voltage, and high-reliability memory devices.

Hybrid CMOS/molecular memory devices were proposed and studied by incorporating redox-active charge-storage molecules into Si structures through the self-assembly process [32, 33, 50–52]. Different redox-active components can be designed or synthesized for multiple redox states, thus for complex and high memory density. The memory retention properties can be effectively tuned through the engineering of the linkage component. The redox component such as the Fe in 4-ferrocenylbenzyl alcohol (referred as Fc-BzOH) and Zn in 5-(4-hydroxymethylphenyl)-10,15,20-trimesitylporphinatozinc(II) (referred as Por-BzOH) as shown in **Figure 3a** and **b**, respectively, can be in neutral and positively charged states through losing electrons [32, 51]. The molecular components surrounding the redox center function as the barrier against charge loss. Such an alternative scenario replacing the conventional tunneling, charge-trapping, and blocking layers in a charge-trapping memory with molecular components provides a smooth transition from CMOS technology to molecular electronics technology.

3.2.2. Characterization and performance discussion

The SAM attachment of the two redox molecules to the silicon surface was carried out by using the similar chemical solution deposition as described in the previous section. Benzonitrile was used as the organic solvent in the attachment process [32, 51]. The sample was placed in the solution for 80 min at 100°C. **Figure 3c** shows the structure of a fabricated electrolyte/molecule/Si capacitor memory cell. **Figure 4a** and **b** shows the CyV curves of Fc-BzOH and Por-BzOH molecular structures, both exhibiting oxidation and reduction peaks. Fc-BzOH shows one pair of redox peaks because the redox center Fe has only one neutral and one

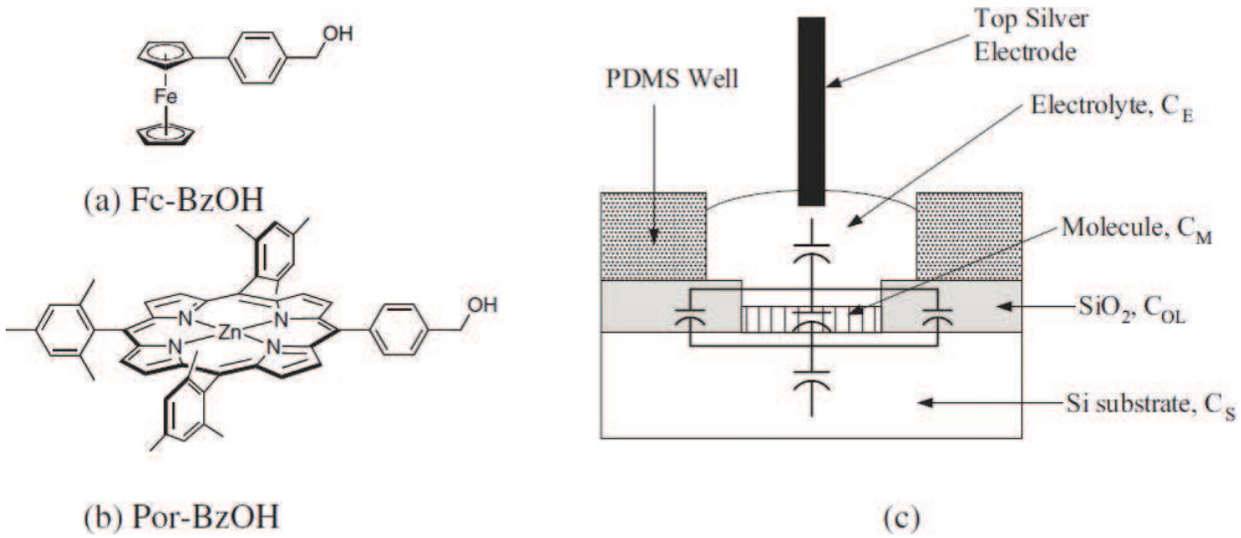

Figure 3. Molecular structure of redox molecules (a) Fc-BzOH and (b) Por-BzOH. (c) Schematic structure of the electrolyte/molecule/Si capacitor for memory application with a simplified equivalent circuit [32, 51].

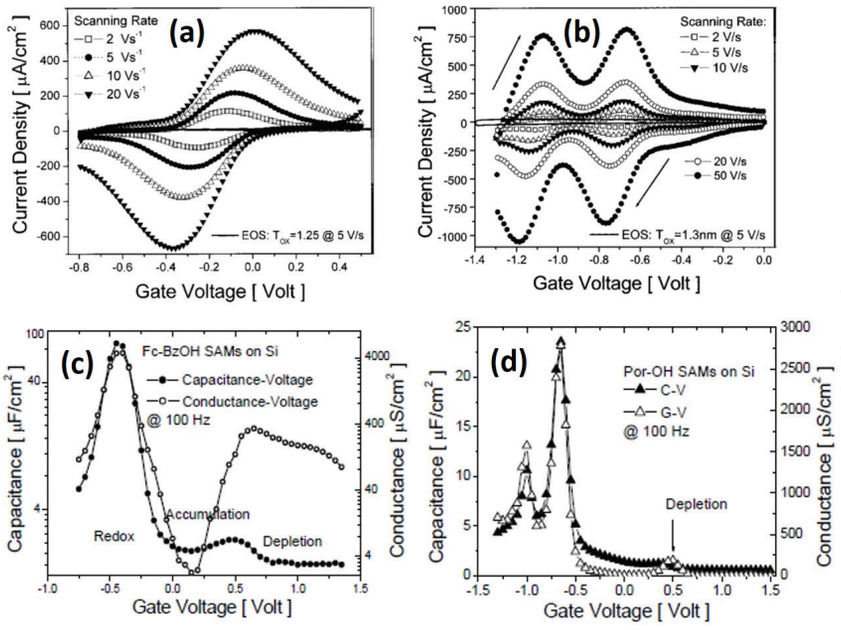

Figure 4. CyV of the electrolyte/molecule/Si structures with (a) Fc-BzOH and (b) Por-BzOH molecules at different voltage scan rates. *C-V* and *G-V* curves of the capacitor structures involving (c) Fc-BzOH and (d) Por-BzOH molecules at 100 Hz [31, 33, 52].

monopositive state. The Zn redox center in Por-BzOH exhibits one neutral and two (mono- and di-) positive states, thus, two pairs of redox peaks were observed.

Clear capacitance and conductance peaks related to the oxidation and reduction processes have been observed from the capacitance-voltage (*C-V*) and conductance-voltage (*G-V*) characteristics, as shown in **Figure 4c** and **d**, respectively [33, 52]. The *C-V* and *G-V* curves can be divided into three regions: depletion, accumulation, and redox regions. The depletion and accumulation are associated with the Si substrate, in a similar manner as MOS capacitors. The characteristics in the redox regions are due to the charging and discharging of molecules, resembling the CyV characteristics. Capacitance and conductance peaks were also observed at higher frequencies up to 5 kHz, but with lower capacitance peaks and higher conductance peaks. The lower capacitance peak at higher frequency is attributed to a lower effective capacitance of the electrolyte in series, while the higher conductance peak is due to the increasing frequency.

3.2.3. Multibit molecular memory in one cell

One of the simple yet effective approaches to increase the memory density is to employ charge-storage element containing molecules with multiple redox states. There are different approaches to realize multiple redox states, including mixed or stacked SAMs of different redox-active molecules with distinct voltage levels, and synthesis of molecule with multiple redox centers. Here, we review the first method by mixing the Fc-BzOH and Por-BzOH molecules in one memory cell [51]. The second approach will be reviewed in the following section.

Mixed SAMs of Fc-BzOH and Por-BzOH on silicon surfaces to achieve a four-state memory element were achieved by using the chemical deposition method of a mixture solution of Fc-BzOH and Por-BzOH in benzonitrile [51]. Molar ratios (Fc-BzOH/Por-BzOH) of 1:0.35, 1:1.4, and

1:3.5 were selected. The CyV curves of the mixed molecules are shown in **Figure 5a**. The results from the nonmixed pure molecules were also illustrated for comparison. One pair of Fc-BzOH peaks and two pairs of Por-BzOH peaks were clearly observed for the three mixed SAMs. With decreasing Fc-BzOH molar percentage, the corresponding peak height decreased substantially due to the changing surface coverage density. The coverage of Fc-BzOH was higher than that of Por-BzOH in the pure SAMs and even mixed SAMs with 1:1 molar ratio, because of the smaller size and the faster attachment of smaller molecule of Fc-BzOH. The redox peaks exhibited a scan rate-dependent peak separation, as shown in **Figure 5b**. Such phenomena could arise from either an increasing resistive drop in the electrolyte or limitations imposed by the intrinsic electron-transfer rate of redox centers on the Si substrate [51]. **Figure 5c–e** shows the *C-V* and *G-V* characteristics of the SAMs at 100 Hz. Each of the mixed SAMs shows three pairs of peaks corresponding to the charging and discharging behaviors of the Fc-BzOH and Por-BzOH molecules. As the molar ratio decreases, the capacitance and conductance peaks of Por-BzOH increase while those of Fc-BzOH decrease. This is also in agreement with the CyV measurement results.

Such a mixed SAM approach is very attractive owing to its simpler synthesis and more distinct potential of the redox states, as compared with a single molecule with multiple redox

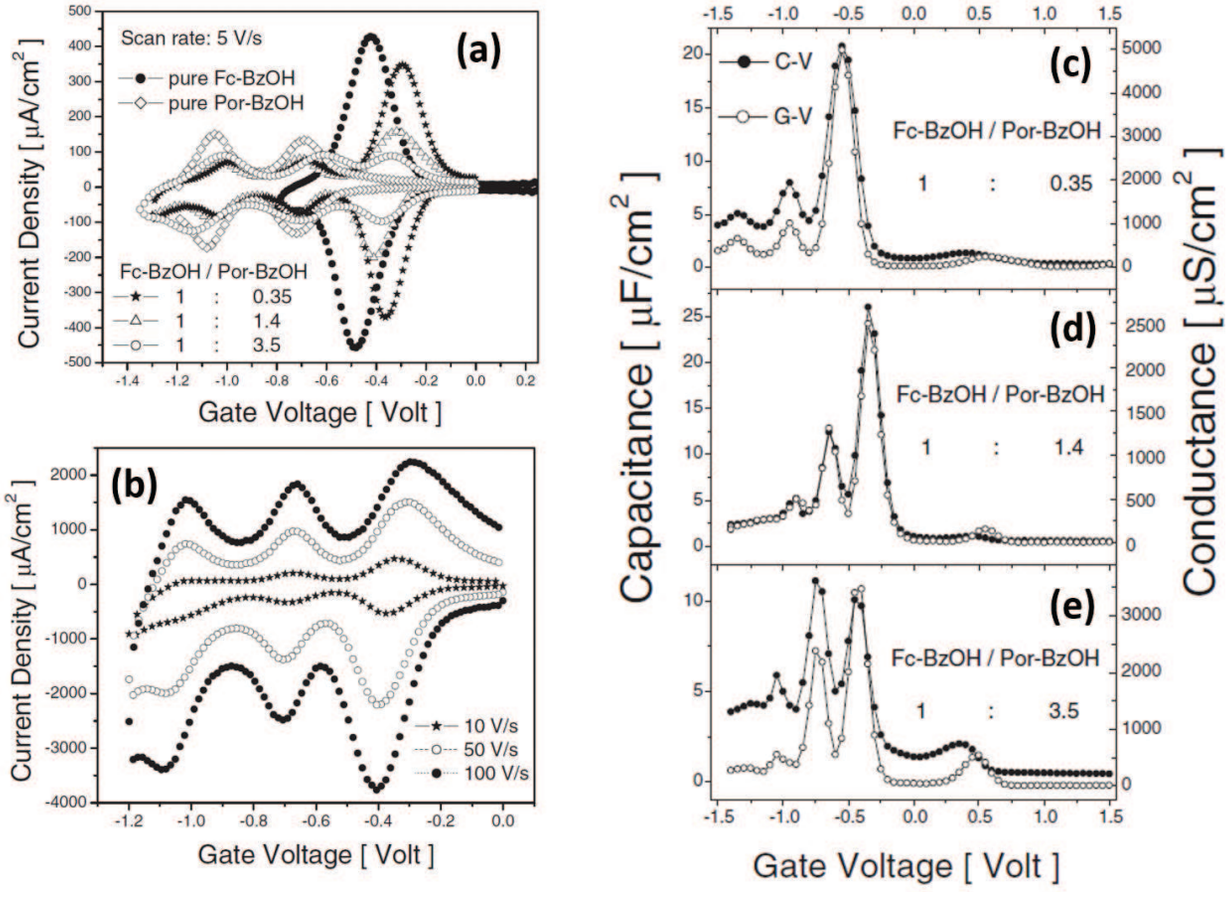

Figure 5. (a) CyV of SAMs of pure and mixed Fc-BzOH and Por-BzOH with different molar ratios. The scan rate was 5 V/s. (b) CyV at increasing scan rates of 10, 50, and 100 V/s. *C-V* and *G-V* characteristics with mixed SAMs with molar ratios of (c) 1:0.35, (d) 1:1.4, and (e) 1:3.5 [51].

states. However, the disadvantage of this method is that the density of a given peak goes down. Nevertheless, this approach still paves the way for constructing multibit information storage devices.

4. Solid-state molecular nonvolatile memory

4.1. Introduction

CMOS and semiconductor nonvolatile memory scaling have create huge demands for alternative memory technologies with higher scalability and better performance. The well-studied charge-trapping memory relies on hot electron injection from the channel into the charge-trapping medium through a tunneling layer. By attaching redox-active molecules onto silicon structures as the charge-storage medium can further enhance the memory density and enable further cell scaling [30, 53–55]. The previous section has introduced the implementation of redox molecules for nonvolatile memory applications. However, the liquid electrolyte-involved structure lacks effective protection for the molecules leading to deteriorated memory performance. By integrating redox molecules in a solid-state molecular memory cell with a solid-state insulating barrier deposited on both sides of the molecules, the possibility of orbital hybridization from the gate can be lessened. The structure of the solid-state molecular memory can be engineered with the material and layer thickness as well as the molecules, whose linker also works as the tunnel barrier and can be optimized by variation in structure and connectivity to obtain the desired tunneling probability, redox potential, and retention time. Such an integration of redox molecules in a solid-state memory provides an excellent platform to study the electrical behavior of the molecules and the devices with universal microelectronic characterization metrologies.

In this section, we first review a solid-state capacitor structure incorporating embedded redox molecules as the charge-trapping medium for high-endurance memory applications. Then, a Si nanowire FET-based molecular flash-like memory with faster operation speed, lower operation voltage, better reliability, and multibit charge storage will be introduced.

4.2. Metal/dielectric/molecule/oxide/Si capacitors for memory application

4.2.1. Device fabrication

Figure 6a shows the structure of the ferrocene molecule and the schematic of a metal/Al_2O_3/ferrocene/SiO_2/Si (MAFOS) solid-state capacitor structure [30]. The most important fabrication process steps are the molecule attachment on SiO_2 and the formation of Al_2O_3 encapsulating the molecules. After the 100 μm × 100 μm active areas were defined by photolithography and wet etching, a ~1.5 nm SiO_2 was grown in the active area by rapid thermal oxidation at 850°C for 2 min. The SAM was formed by placing the substrate in a solution of 3 mM ferrocene in dichloromethane at 100°C for 20 min. After the attachment, dichloromethane was used again to rinse the substrate to remove any physisorbed residuals on the surface.

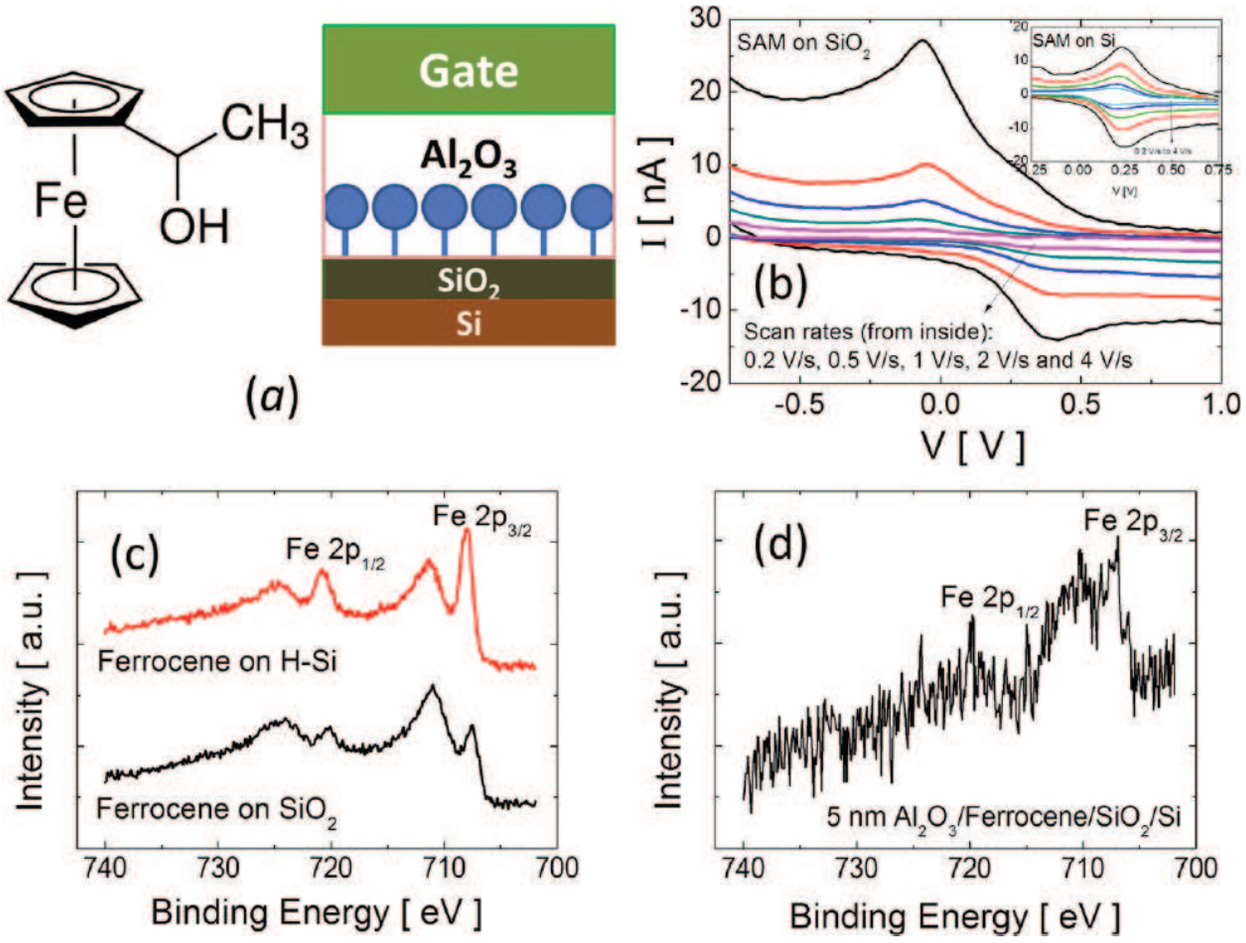

Figure 6. (a) Molecule structure of α-ferrocenylethanol (ferrocene) and the schematic of the MAFOS capacitor memory cell. (b) CyV curves of ferrocene-attached capacitor at different scan rates. Inset: CyV curves of the reference sample with ferrocene attached on the Si surface. (c) XPS spectra of the samples with ferrocene attached on Si and SiO_2 surfaces. (d) The XPS spectrum of the ferrocene-attached SiO_2 substrate with 5 nm Al_2O_3 covered on the top [30].

CyV was performed after the attachment of molecule. Other substrates were immediately loaded into the atomic layer deposition (ALD) vacuum chamber to deposit 20 nm Al_2O_3 at 100°C. Trimethyl aluminum (TMA) and H_2O were used as precursors. In the final step, a layer of 80 nm Pd was deposited and patterned on Al_2O_3 as the top gate. Three reference samples were fabricated for comparison: metal/Al_2O_3/ferrocene/Si (MAFS), metal/Al_2O_3/SiO_2/Si (MAOS), and metal/Al_2O_3/Si (MAS). For the ferrocene attachment on the Si surface in MAFS device, a hydrogen-terminated Si surface was obtained by dipping the substrate into 2% hydrofluoric acid for 30 s prior to the attachment [30].

4.2.2. Electrical characterization

Figure 6b shows the CyV curves of the electrolyte/ferrocene/SiO_2/Si structure at various scan rates. Oxidation and reduction peaks were observed at negative and positive gate voltage (V_G), respectively, through losing and restoring electrons from the SAM. By comparing the CyV curves with the results from the electrolyte/ferrocene/Si structure (inset in **Figure 6b**),

the clear peak separation is due to the tunneling barrier (~1.5 nm SiO_2) and the molecular linker. The ferrocene surface coverage can be calculated from the oxidation peak, and the coverage was found to be 5.23×10^{13} and 3.14×10^{13} cm^{-2} for ferrocene attachment on Si and SiO_2 surfaces, respectively. X-ray photoelectron spectroscopy (XPS) was carried out before and after the ALD to examine the viability of ferrocene during the deposition. From the XPS spectra shown in **Figure 6c** and **d**, the ferrocene SAMs were well attached on both Si and SiO_2 surfaces, and the SAM survives the deposition of Al_2O_3.

The memory behavior was characterized by measuring the *C-V* hysteresis at 1 MHz. As shown in **Figure 7a**, large memory window was observed with the MAFOS device, and the counterclockwise hysteresis loop indicates the charge storage in ferrocene SAM. **Figure 7b** shows the flat-band voltage shift (ΔV_{FB}) of the MAFOS and three control samples as a function of applied programming/erasing (P/E) operations. The much smaller ΔV_{FB} observed from MAOS and MAS devices indicates the negligible charge storage at the dielectric interface traps. The asymmetric behavior observed from the MAFS device suggests the difficulty of

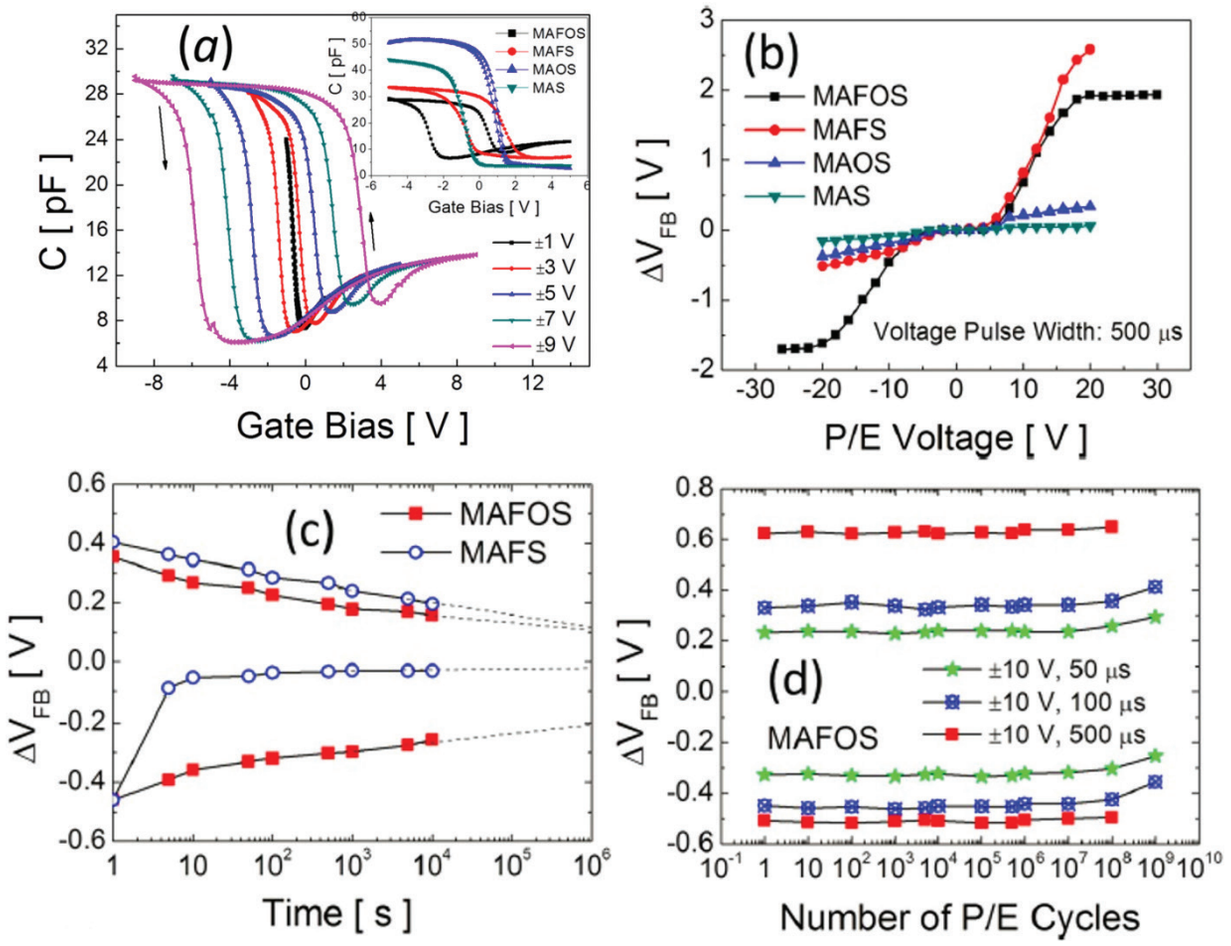

Figure 7. (a) *C-V* hysteresis curves of the MAFOS device at 1 MHz with different gate voltage scan ranges. Hysteresis of MAFOS and three control samples with ±5 V scan range were compared in the inset. (b) ΔV_{FB} of MAFOS and three control samples versus P/E voltage with 500 μs pulse width. (c) Retention properties of MAFOS and MAFS at room temperature. (d) Endurance properties of MAFOS with ±10 V P/E voltage but different pulse width [30].

maintaining molecules positively charged without the SiO_2 tunnel barrier. The stable and symmetric staircase ΔV_{FB} of MAFOS device originated from the reliable charging/discharging behavior of ferrocene and the effective charge separation by the SiO_2 tunnel barrier [30]. The charge density of the ferrocene SAM was calculated by using the following equation [30]:

$$\Delta V_{FB} = \frac{e \cdot n}{C} = e \cdot n \cdot \left(\frac{T_{Al_2O_3}}{\varepsilon_0 \varepsilon_{Al_2O_3}} \right) \quad (1)$$

where e is the elementary charge, n is the number of stored electrons, T_{Al2O3} and ε_{Al2O3} are the thickness and relative dielectric constant of Al_2O_3, respectively. The charge density was calculated to be 4.82×10^{12} cm^{-2}, which is only a small portion (~15%) of the coverage density obtained from the CyV results. Nevertheless, effective memory can still be realized and the charge density of the solid-state molecular memory is sufficiently high [30].

The room temperature retention of MAFOS and MAFS devices is shown in **Figure 7c** [30]. Note that ~60% charge loss was observed after 10^6 s retention time for MAFOS. Such fair retention is due to the relative thin SiO_2, and the oxide quality by rapid thermal oxidation is not satisfactory. The endurance property of the MAFOS device was measured with ±10 V P/E voltages and different pulse width. The memory device continues to behave well after 10^9 P/E cycle with the same memory window and a slightly upshift which is due to the accumulation of electron in deep traps [30]. Such excellent endurance characteristics are naturally derived from the intrinsic redox properties of the redox molecules, which have been well protected by the device structure design and fabrication.

4.3. Nanowire/nanotube-based flash-like molecular memory

Semiconductor nanowires and nanotube MOSFETs have been regarded as the building blocks for nanoelectronics and circuits [56, 57]. The quasi-one-dimensional nanowires have a larger surface-to-volume ratio as compared with the bulk materials. Therefore, less stored charges are needed to induce a same memory window. In addition, the nanowire or nanotube can enable a gate-surrounding structure, allowing excellent electrostatic gate control. The integration of redox molecules in semiconductor nanowire FET for solid-state flash-like memory can be expected to significantly enhance the memory performance by taking advantages of the inherent properties of redox molecules [24, 58–60].

4.3.1. Device fabrication

Figure 8 illustrates the fabrication process of a molecular flash memory based on a so-called "self-aligned" silicon nanowire FET [24, 61]. A thin film of Au catalyst (2–3 nm) was first sputtered at predefined locations by photolithography on a 300-nm SiO_2/Si substrate. The Si nanowires were then grown from the catalyst following the vapor-liquid-solid (VLS) mechanism in a low-pressure chemical vapor deposition (LPCVD) furnace at 440°C for 2 h with an ambient SiH_4 stream under a pressure of 500 mTorr. Immediately after the growth, the nanowires were oxidized at 750°C for 30 min by dry oxidation to form a 3-nm SiO_2 on which the SAM will be attached [24]. As compared with the SiO_2 grown by rapid thermal oxidation, the SiO_2 formed here is of much better quality by using the dry oxidation technique [30]. Therefore, enhanced memory retention can be expected. The next step is to pattern the source/drain

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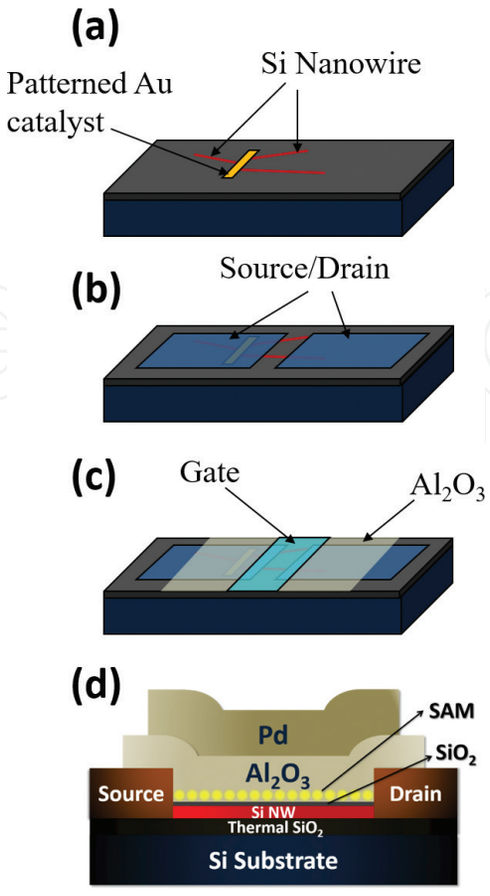

Figure 8. Schematic of the fabrication process of a molecular flash memory. (a) Au patterning on SiO_2, synthesis of Si nanowires and nanowire oxidation. (b) Formation of S/D electrodes and SAM attachment. (c) Deposition of Al_2O_3 by ALD and fabrication of top gate electrode. (d) Schematic structure of a completed molecular flash memory [24].

(S/D) electrodes with photolithography. A 2% HF wet etch was applied to remove the oxide from the nanowire at the patterned S/D area before 5/100 (unit:nm) Ti/Pt was deposited and lift-off to form S/D electrodes.

The SAM of ferrocene and Ru_2 redox molecules (**Figure 1**) were then formed on the SiO_2/Si nanowire channel by placing droplets of a solution of dichloromethane with 3-mM ferrocene and 2-mM Ru_2 on active areas separately [24]. Each drop was in place for 3–4 min and the substrates were held at 100°C in an N_2 environment during attachment. Saturated SAMs were formed after ~30 min. Dichloromethane solvent was used to rinse the substrates to remove the residual molecules. The samples were then immediately loaded into the ALD chamber for a layer of 25 nm Al_2O_3 deposition at 100°C with TMA and H_2O as precursors. The final step is the fabrication of 100-nm Pd top gate with the same photolithography and lift-off process as S/D electrodes. A reference sample without redox molecules was fabricated for comparison [24].

4.3.2. Electrical characterization

Figure 9 shows the transmission electron microscopy (TEM) image of the cross-section of a ferrocene-attached molecular flash memory device [24]. Clear gate-surrounding structure has been achieved, with a ~6-nm "intermixed" region observed.

Figure 10a and **b** shows the out characteristics, drain current (I_{DS}) versus drain voltage (V_{DS}) of the ferrocene molecular flash memory in linear and log-scale, respectively. Smooth and well-saturated I_{DS}-V_{DS} curves have been observed with negligible contact resistance. The leakage-affected and the weak, moderate, and strong inversion operation regions are shown in **Figure 10b**. From the transfer characteristics shown in **Figure 10c** and **d**, counterclockwise hysteresis loops have been observed at different gate voltage (V_{GS}) sweep ranges for both ferrocene and Ru_2 memory devices, suggesting the charge-trapping mechanism. From the log-scale I_{DS}-V_{GS} curves shown in the insets of **Figure 10c** and **d**, clear off states were achieved, and the on/off current ratio was as high as ~10^7 [24].

The P/E speed characteristics of the molecular memory (ferrocene) are shown in **Figure 11a** and **b**, demonstrated by the threshold voltage shift (ΔV_{TH}) under different P/E gate voltage pulses [24]. The P/E operations were performed by applying top gate voltage pulses while the substrate, S/D electrodes were all grounded. As shown in **Figure 11a**, with accumulative +10 V programming pulses, the threshold voltage showed a clear shift toward positive direction, indicating that the electrons were injected from the nanowire channel through the tunnel barrier and stored in the redox centers of the molecules. Erasing operations with −10 V gate voltage pulses back shifted the threshold voltage toward the negative direction, suggesting hole injection from the nanowire channel during erasing operations. The P/E speed characteristics of ferrocene and Ru_2 memory are summarized in **Figure 11c** and **d**, respectively. Both devices showed fast P/E speed, which arises from the intrinsic fast speed of the charging behavior of the redox molecules. The slightly faster erasing speed over programming speed was attributed to the more favorable hole injection in the Si/SiO_2/molecule/Al_2O_3/gate interface states, though the amount charge is very small even with ±10 V, 1 s stressing [24].

Figure 12a shows the ΔV_{TH} of the ferrocene molecular memory and the reference sample as a function of P/E voltages at a fixed pulse width of 500 μs. Negligible ΔV_{TH} was observed for

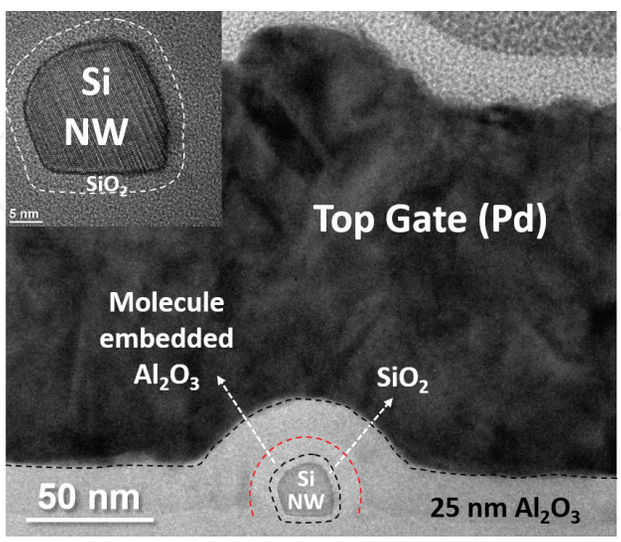

Figure 9. TEM image of the cross-section of a ferrocene-attached molecular flash memory device. The red-dashed line indicates the ferrocene-embedded region. Inset: cross-section of the nanowire channel, with the SiO_2 layer indicated by the dashed line [24].

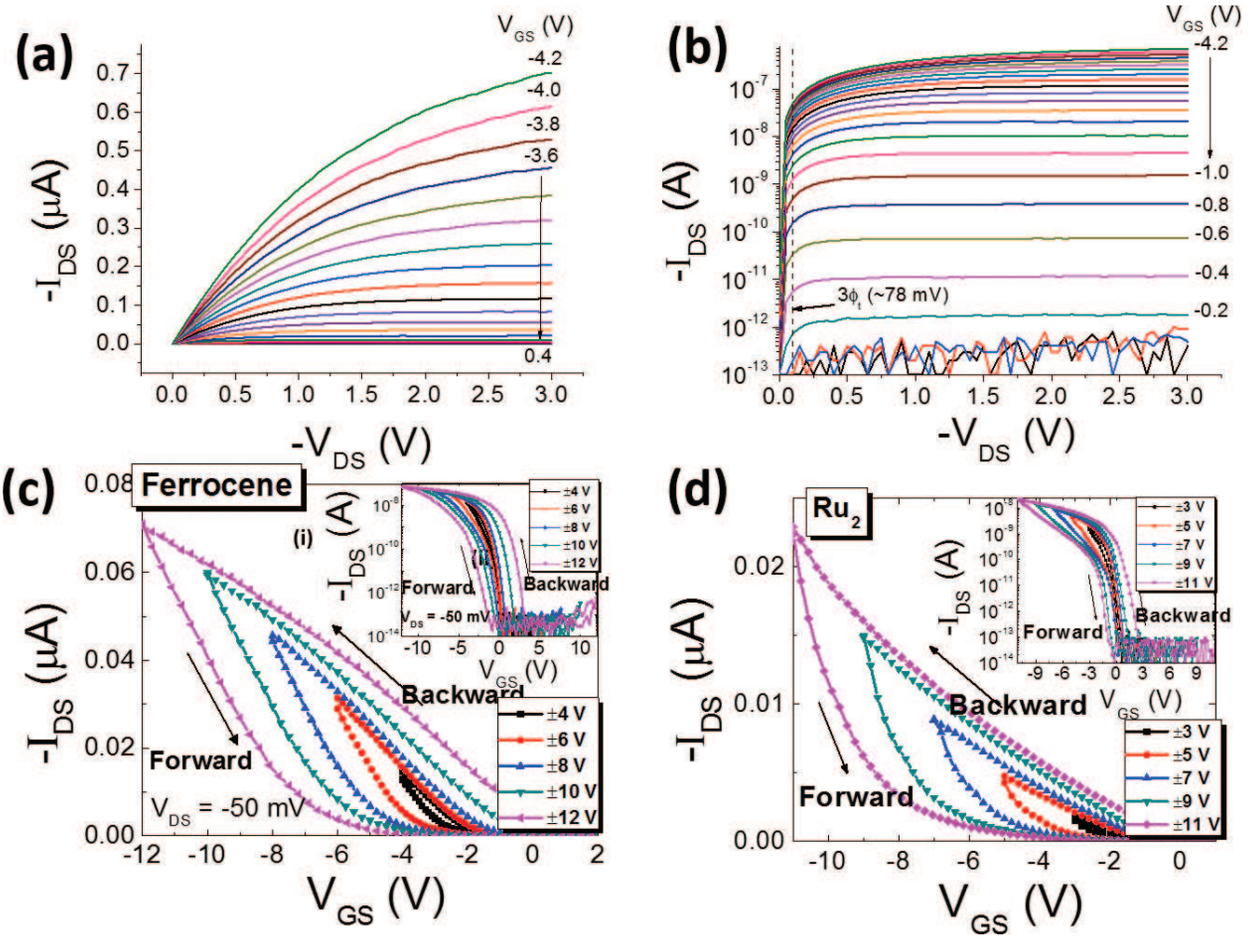

Figure 10. Output characteristics of ferrocene molecular memory in (a) linear and (b) log-scale. Transfer characteristics of (c) ferrocene and (d) Ru_2 molecular memory with different gate voltage sweep ranges. V_{DS} was set to −50 mV [24].

the reference sample, indicating the fact that the dominant charge-storage location lies in the molecules, rather than the solely traps within the gate dielectric interface or a dielectric interface. Clear staircase behavior was observed for the ferrocene memory, demonstrating discrete energy levels corresponding to various molecular orbitals. A saturated ΔV_{TH} was observed beyond ±26 V gate voltage, suggesting that all the available redox centers in the SAM have been occupied by injected charges. The charging density in the SAM can be thus calculated by

$$\Delta V_{TH} = \frac{qN}{C_{Redox}} \cong \frac{qN}{C_{AlO}} = qN \frac{\ln\left(\frac{t_{AlO\text{-}out}}{t_{AlO\text{-}in}}\right)}{2\pi \varepsilon_0 \varepsilon_{AlO} L} \quad (2)$$

where q is the elementary charge, N is the total charge stored in the redox centers, C_{Redox} is the total capacitance arising between the redox centers and the metal gate, C_{AlO} and $\varepsilon;_{AlO}$ are the capacitance and relative dielectric constant of the Al_2O_3 layer, respectively, L is the channel length, $t_{AlO\text{-}out}$ and $t_{AlO\text{-}in}$ are the distances from the center of nanowire channel to the outside and inside surfaces of the Al_2O_3 layer. The charging density was found to be 6.96×10^{12} cm^{-2}, which is about 22% as compared with the coverage density from the CyV results [24]. This indicates that effective memory can be realized even

with a partial (i.e., non-continuous) ferrocene SAM. Two-step charge-storage behavior was observed in the Ru_2 molecular memory due to the two redox centers in the Ru_2 molecule which can exhibit stable and distinct charged states at different voltage level. As shown in **Figure 12b**, with increasing programming gate voltage, the first step charged state was found at 10 V, with 0.8 V ΔV_{TH}. This means that the Ru_2 redox centers with lower voltage level have been occupied by electrons. Further increasing the programming voltage led to a second charged state, which was observed beyond 14 V V_{GS}, with 1.95 V ΔV_{TH}. Up to now, all the redox centers in Ru_2 SAM have been filled with injected electrons. Similarly, the overall charging density of Ru_2 SAM was calculated, and was found to be 1.12×10^{13} cm^{-2}, which is about 44% of the freshly attached SAM before Al_2O_3 deposition [24]. Such discrete charging behavior in Ru_2 molecules with multiple redox centers is very attractive for discrete multibit memory applications.

Figure 12c and **d** shows the room temperature retention properties of the ferrocene and Ru_2 molecular memory devices, respectively [24]. The devices were initially programmed/erased by ±10 V gate voltage with 500 and 100 μs pulse width. Only ~20% charge loss was observed with a projected 10-year memory window. As compared with the previous capacitor structure molecular memory, the improved retention shown here is attributed

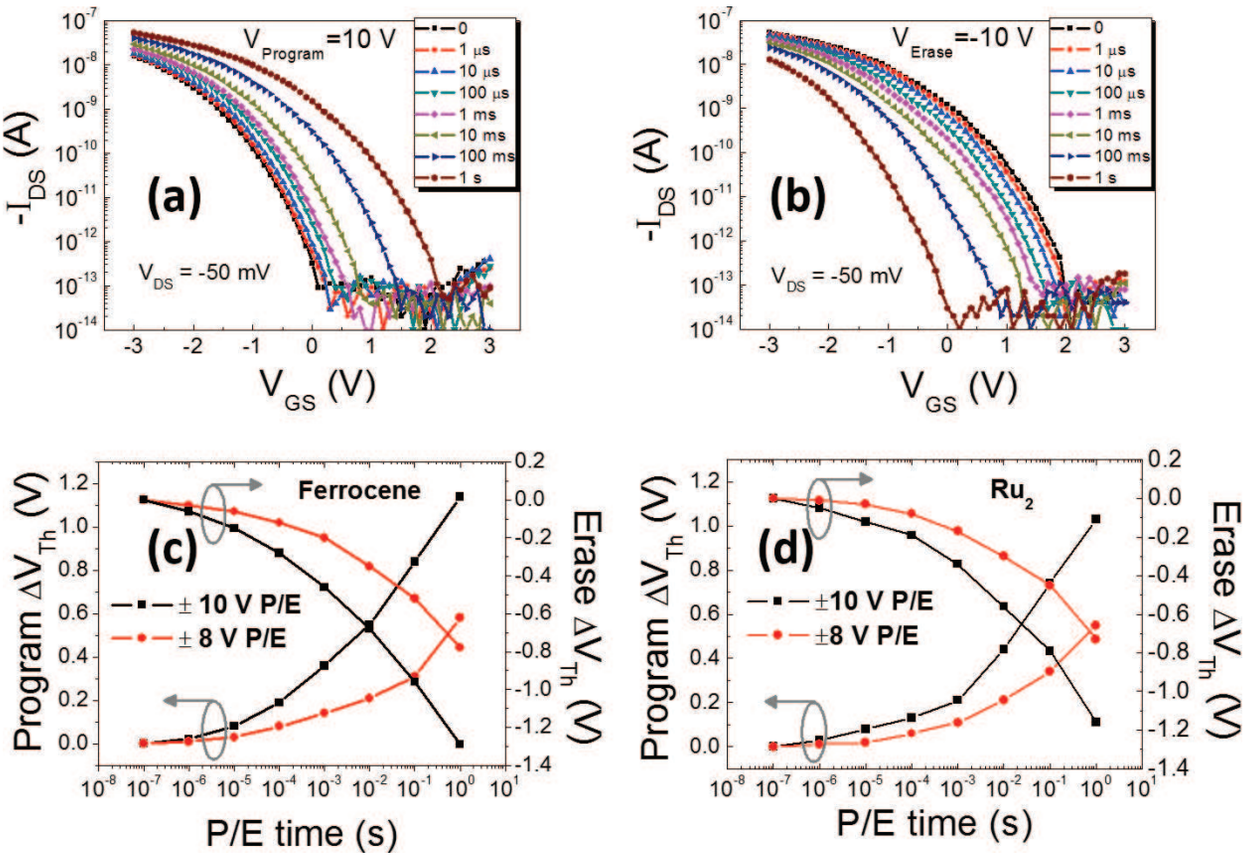

Figure 11. (a) Programming and (b) erasing operations of the ferrocene molecular memory under ±10 V P/E gate voltage pulses with accumulative time. P/E speed characterization of (c) ferrocene and (d) Ru_2 molecular memory devices, respectively [24].

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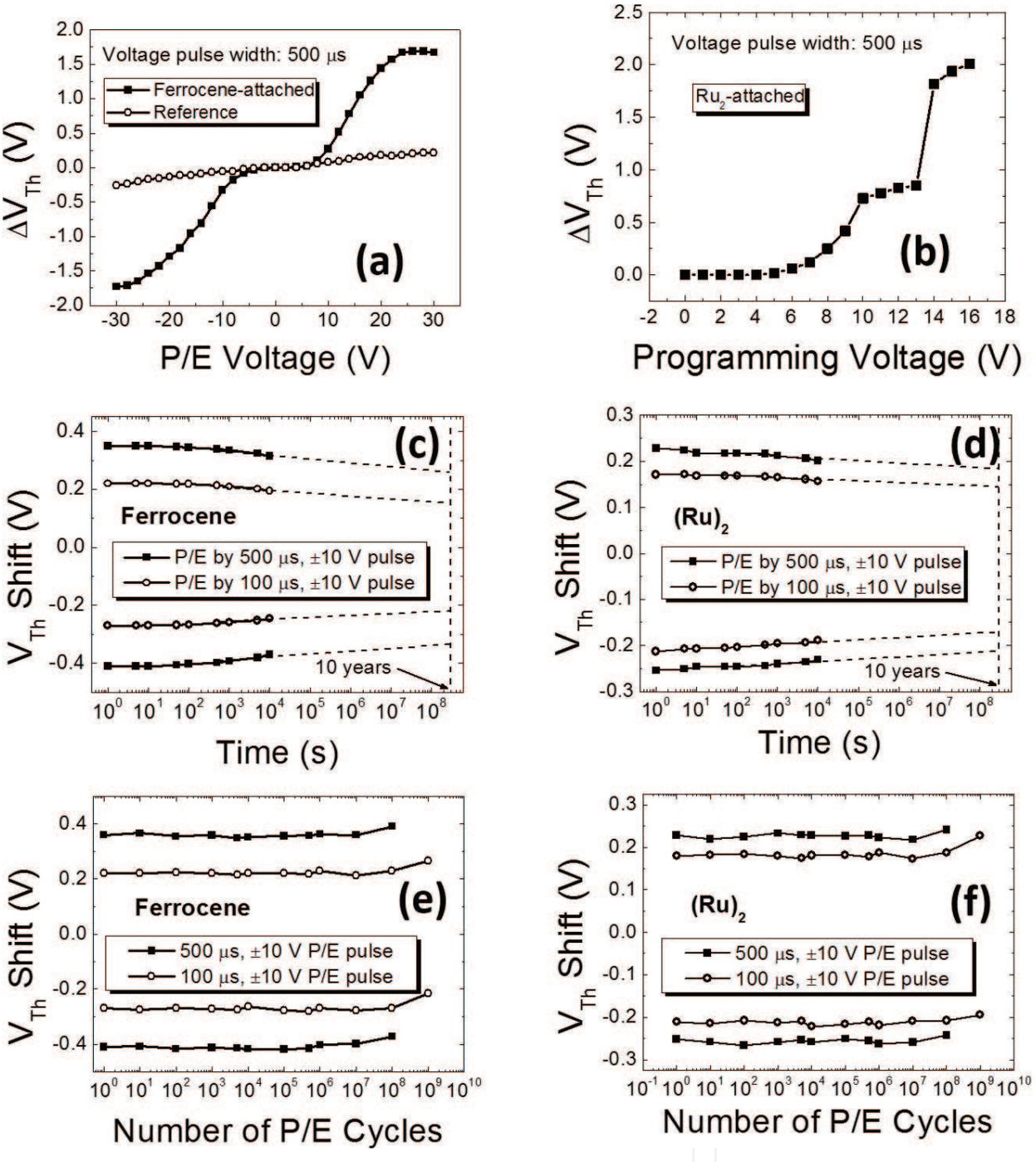

Figure 12. ΔV_{TH} of (a) ferrocene and reference sample and (b) Ru_2 molecular memory as a function of P/E gate voltage with 500 μs pulse width and increasing pulse height. Room temperature retention properties of (c) ferrocene and (d) Ru_2 molecular memory. The initial P/E pulses were ±10 V gate voltage with 500 and 100 μs pulse width, respectively. Endurance properties of (e) ferrocene and (f) Ru_2 molecular memory. Note that ±10 V gate voltage with 500 and 100 μs pulse width was applied [24].

to the high-quality tunnel oxide with clean solid/molecule and dielectric interfaces during the fabrication process. This further supports the mechanism of dominant charge storage located in the redox centers instead of interface states, since the recovery process of

the interface states is quite fast leading to a poor retention. The endurance properties of the molecular memory devices are shown in **Figure 12e** and **f** [24]. Both devices exhibited excellent endurance characteristics with ±10 V P/E gate voltages and 500 and 100 μs pulse width. Negligible memory window degradation was observed after 10^8 P/E cycles by applying 500 μs P/E voltages. With shorter P/E voltages (100 μs), both devices still functioned perfectly after 10^9 P/E operation cycles. Such excellent endurance is 10,000 times better than that of the conventional floating-gate memory, and is resulted from the excellent reliability of the redox properties of the ferrocene and Ru_2 molecules [24]. However, less than 50% of the molecules in the SAM were effectively involved in the redox process, though the portion is slightly higher than that of the capacitor structure memory cell. Further research efforts are needed to increase the redox efficiency so as to lower the operation voltage and improve the operation speed. The memory density can be further increased with more carefully engineered molecules, and the demonstrated multibit memory concept is more reasonable and feasible than by just modulating the voltage level, as precise controlling of the charged states can be clearly defined and monitored with the physically discrete redox states.

5. Conclusions

The properties of redox-active molecules and the integration of molecular electronics in nonvolatile memory technology have been systematically discussed. So far, redox-active molecules have already shown their potential and advantageous properties for future low-power, high-density, and high-reliability nonvolatile memory. Solid-state integration of the redox molecules in flash-like nonvolatile memory devices enables the extension of the advantages afforded by the molecules to advanced electronic devices combined with universal semiconductor metrologies. Due to the intrinsic redox behavior of the molecules, large memory window with sufficient charge-trapping density can be achieved, and the $>10^9$ endurance cycles is about 10,000 times better than that of the conventional floating-gate memory. Furthermore, discrete multibit charge storage can be enabled by mixing various redox molecules or using molecules with multiple redox states. The current main barriers are the CMOS compatibility and the process issues introduced with the molecular integration. The realization of future molecular memory applications still requires a combination of empirical fabrication and rational designs for particular molecular electronics devices toward sophisticated application. Upon this, the molecular electronics will no doubt be shedding more new lights on the micro-/nanoelectronics society for creating next generation nonvolatile memory with enhanced performance.

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Author details

Hao Zhu[1]* and Qiliang Li[2]

*Address all correspondence to: hao_zhu@fudan.edu.cn

1 School of Microelectronics, Fudan University, Shanghai, PR China

2 Department of Electrical and Computer Engineering, George Mason University, Fairfax, VA, USA

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