Chapter 6

Memristor Emulator Circuit Design and Applications

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http://dx.doi.org/10.5772/intechopen.69291

Abstract

This chapter introduces a design guide of memristor emulator circuits, from conceptual idea until experimental tests. Three topologies of memristor emulator circuits in their incremental and decremental versions are analysed and designed at low and high frequency. The behavioural model of each topology is derived and programmed at SIMULINK under the MATLAB environment. An offset compensation technique is also described in order to achieve the frequency-dependent pinched hysteresis loop that is on the origin and when the memristor emulator circuit is operating at high frequency. Furthermore, from these topologies, a technique to transform normal non-linear resistors to inverse non-linear resistors is also addressed. HSPICE numerical simulations for each topology are also shown. Finally, three real analogue applications based on memristors are analysed and explained at the behavioural level of abstraction.

Keywords: memristor, pinched hysteresis loop, current conveyor, non-linear resistor, behavioural modelling

1. Introduction

Memristors have turned out to be of considerable importance in several areas of research and application, such as analogue circuits, non-linear (chaotic) circuits, sensors, control systems, storage systems, cellular neural networks, logic circuits, power systems, neuromorphic circuits, etc. [1]. In order to research all those applications, the first step is understanding and modelling the behaviour of a memristor. In this scenario, there are, basically, three approaches:

behavioural modelling, SPICE type models and emulator circuits. In the former case, smooth continuous cubic non-linear functions [2], square non-linear functions [3], piecewise linear models [4] and hyperbolic sine models [5, 6] have been proposed to emulate the Hewlett-Packard (HP) memristor behaviour. Examples of this type of modelling are TEAM model [7], VTEM model [8] and Simmons tunnelling model [9]. Although these models are approaching the HP memristor behaviour with a level of error relatively low, a full custom software is required for solving the mathematical models [10]. Furthermore, this task becomes cumbersome when applications with several memristors are addressed, since a large set of equations must first be established according to the topology, and next, the system of equations must be numerically solved. In the second approach, SPICE models have also been developed in order to model the HP memristor, principally [11–16]. It is worth mentioning that the memristive effect is not limited to TiO_2, and this effect has also been glimpsed on nickel oxide [1], Ag-loaded Si films [17], TiO_2 sol-gel solutions [18], and other materials. Although this type of modelling is interesting, since the capabilities of commercially available tools are exploited, its major disadvantage is that numerical simulations of circuits based on memristors can only be done. In the latter, several emulator circuits have been proposed in the literature, which use different design methodologies and different topologies. In this way, grounded and floating memristor emulator circuits working at incremental or decremental mode and built with operational amplifiers and analogue multipliers have been proposed in [19–24]. Other interesting topologies were reported in [25, 26], where digital and analogue mixed circuits were used. More recently, other active devices such as current feedback operational amplifiers, positive second-generation current conveyors (CCII+) and differential difference current conveyor, see [27–33] and the references cited therein, have also been used to design a memristor emulator circuit. However, some of them not only become complex and bulky, requiring rigid conditions to operate, but also some emulators do not exhibit those fingerprints that are useful to affirm that the emulator circuit is a memristor or memristive device. With this in mind and depending on the application, any emulator circuit must accomplish some properties, some of them are: the frequency-dependent pinched hysteresis loop for any kind of flux- or charge-controlled incremental or decremental memristor/memductor, in its version grounded or floating, must pass through the origin for any periodic signal with any amplitude, operating frequency and initial conditions; the possibility for controlling the initial state of the emulator circuit, i.e. adjust of the initial conditions, non-volatility, memristive/memductive behaviour at high-frequency and without offset, etc. All in all, the design of memristor emulator circuits is also important in order to study and research real applications as those mentioned above. As a consequence, a lot of emulator circuits using off-the-shelf components have been developed to imitate not only the real behaviour of a memristor but also the real behaviour of meminductors and memcapacitors [1].

In this chapter, we discuss the design of three memristor emulator circuits. The aim is to show the conceptual idea on the design of an emulator, passing for numerical simulations and until experimental tests. Each behavioural model is derived and programmed at SIMULINK under MATLAB environment. From a circuit-design perspective and of the knowledge gained, a design guide is described in order to design a memristor emulator circuit in a systematic way. Then, we introduce a novel technique for achieving the frequency-dependent pinched hysteresis loop associated to a memristor emulator circuit that is operating at high frequency, and the

crossing point does not deviate of the origin. Since a memristor is basically a charge- or flux-controlled resistor, we describe how to transform a non-linear resistor with its normal pinched hysteresis loop to an inverse behaviour. Therefore, the main difference of an inverse non-linear resistor with respect to normal resistors is that the behaviour of frequency-dependent pinched hysteresis loop becomes a straight line when the operating frequency of the signal source decreases. Finally, some real analogue applications are described.

2. Analogue memristor emulators

Unlike behavioural models and SPICE type models, an emulator circuit is very useful, since real applications based on memristors can be researched and built. In this section, we describe three memristor emulator circuits.

2.1. Floating memristor emulator circuit

The topology shown in **Figure 1(a)** was reported in [28]. By a straightforward analysis, the behaviour equation is given by:

$$\frac{v_{\mathrm{m}}(t)}{i_{\mathrm{m}}(t)} = M(\varphi_{\mathrm{m}}(t)) = R_1 \pm \frac{R_1 R_4}{10 R_2 R_3 C_z} \int_0^t v_{\mathrm{m}}(\tau) d\tau \tag{1}$$

From **Figure 1(a)**, the ***S*** switch is connected to ***I*** to obtain a memristor emulator circuit operating at incremental mode, whereas if ***S*** is connected to ***D***, then a decremental behaviour is obtained. These behaviours correspond to the signs + and − at Eq. (1), respectively. Assuming that

$v_{\mathrm{m}}(t) = A_{\mathrm{m}} \sin(\omega t)$, where A_{m} is the amplitude and $\omega = 2\,\pi f$ in rad/s, we obtain:

$$\frac{v_{\mathrm{m}}(t)}{i_{\mathrm{m}}(t)} = R_1 \pm \frac{R_1 R_4 A_{\mathrm{m}}}{10 R_2 R_3 C_z \omega} \cos(\omega t - \pi) \tag{2}$$

From Eq. (2), one can observe that the memristance is composed by a linear time-invariant resistor and a linear time-varying resistor. The relationship between both resistors is described by the ratio of their amplitudes, given as

$$k_{\mathrm{n}} = \frac{R_4 A_{\mathrm{m}}}{R_2 R_3 C_z \omega 10} = \frac{1}{\tau f} = \frac{T}{\tau} \tag{3}$$

where $\tau = \frac{20\pi R_2 R_3 C_z}{R_4 A_{\mathrm{m}}}$ is the time constant of the emulator circuit and $T = \frac{1}{f}$ is the period of $v_{\mathrm{m}}(t)$. In order to hold the pinched hysteresis loop in several operating frequencies, one can observe in Eq. (3) that τ must be updated according to f, since k_{n} will decrease as the frequency increases. Thus, the numeric value of τ can be updated by R_3 or C_z. On the other hand, Eq. (3) reveals that:

1. $k_{\mathrm{n}} \to 0$ when $f \to \infty$ or $A_{\mathrm{m}} \to 0$. Hence, Eq. (1) is dominated by its linear time-invariant part.

2. $k_n \rightarrow 1$ when $f \rightarrow 1/\tau$ or A_m is monotonically increased. Therefore, the maximum pinched hysteresis loop is obtained.

3. $k_n \rightarrow \geq 1$ when $f \leq 1/\tau$ or A_m increases too much. Here, the hysteresis loop is lost.

In order to ensure the behaviour of the frequency-dependent pinched hysteresis loop, the numerical value of k_n must be in the interval (0, 1). Once the behavioural model of the memristor has been deduced, numerical simulations can be realized. The numerical value of each element of **Figure 1(a)** used during numerical simulations and experimental tests can be found in [28]. Therefore, **Figure 2(a)** (solid line) shows only the incremental pinched hysteresis loop behaviour obtained of **Figure 1(b)** when a sinusoidal waveform operating to 16 Hz is applied. For this case and that follows, the direction of the hysteresis loop is clockwise, whereas for a decremental mode, the direction is counterclockwise. Therefore, a similar behaviour is obtained for the decremental case, as illustrated in **Figure 2(a)**.

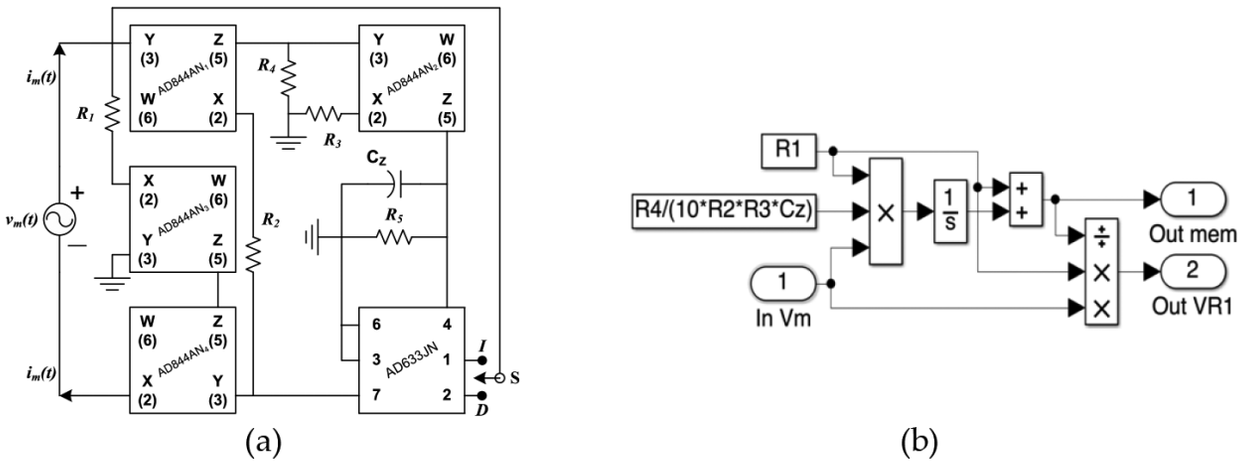


Figure 1. (a) Flux-controlled floating memristor emulator circuit taken from [28] and (b) SIMULINK model of Eq. (1).

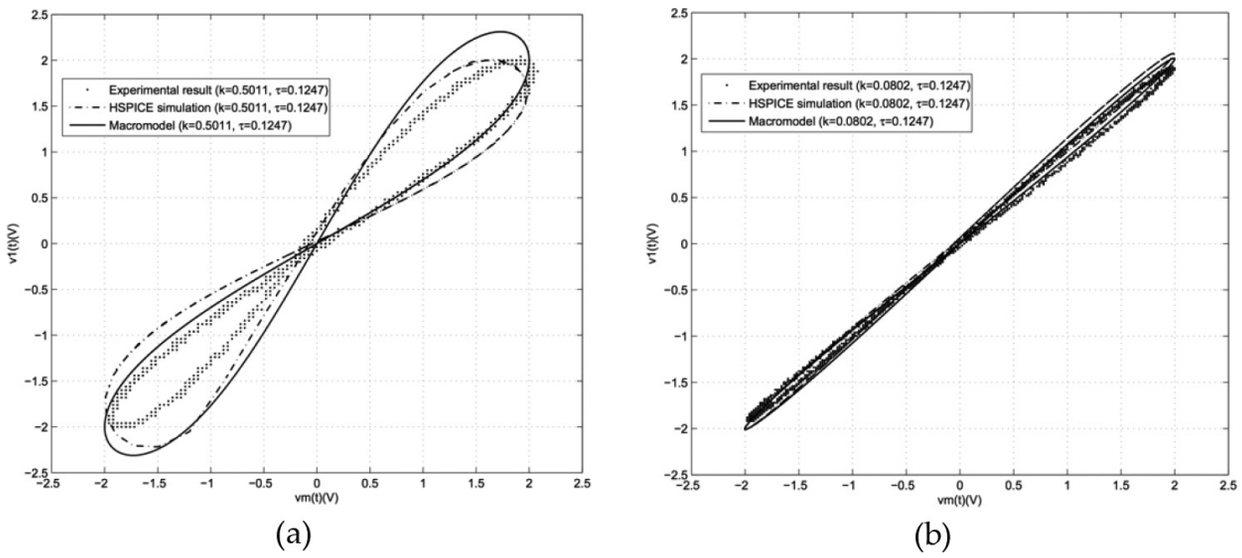


Figure 2. Numerical, HSPICE and experimental results of **Figure 1(a)** operating at: (a) 16 Hz and (b) 100 Hz.

Figure 1(a) was also simulated at HSPICE by using the macro-models associated to each active device and numerical results are shown in **Figure 2(a)** (dash-dot line). In order to validate the previous results, **Figure 1(a)** was experimentally tested, and the results are shown in **Figure 2(a)** (dot-dash line). On the other hand, when the operating frequency increases, the pinched hysteresis loop is gradually lost and the memristor behaviour becomes a straight line for all cases, as depicted in **Figure 2(b)**. Furthermore, the frequency-dependent pinched hysteresis loop is a necessary condition but not sufficient for claiming that the emulator circuit is emulating the real memristor behaviour. In this case, tests of non-volatility are necessary. Since capacitors and inductors are the solely elements that are storing energy, the non-volatility property is indirectly measured across C_z of **Figure 1(a)**. Thus, **Figure 3** shows experimental tests of non-volatility of **Figure 1(a)** when a narrow pulse train of 1.2 V of amplitude and 2.4 μs of pulse width (yellow line) is applied. According to **Figure 3**, one can observe that once programmed the incremental and decremental memristance, its value is keeping when the input signal is not applied. Note that during non-pulse period, the memristance is non-volatile, and its variation is negligible. For incremental topology, the memristance increases according to the amplitude and pulse width, as depicted in **Figure 3** (pink line), whereas for the decremental topology, the memristance decreases (blue line). It is important to point out that memristive behaviour in each operation mode can be reverted to its last value, when a negative pulse of the same size is applied.

2.2. Grounded memristor emulator circuit I

Recently in [28, 31, 32], floating and grounded memristor emulator circuits based on CCII+ were proposed. In this way, the behavioural model of the charge-controlled grounded memductor emulator circuit described in [32] and shown in **Figure 4(a)** is given by

$$\frac{i_{\mathrm{m}}(t)}{v_{\mathrm{m}}(t)} = W(q_{\mathrm{m}}(t)) = \frac{1}{R_1 + R_x} \pm \frac{A_v A_i}{10(R_{\mathrm{m}} + R_{\mathrm{x}})(C_{\mathrm{m}} + C_{\mathrm{a}})} \int_0^t i_{\mathrm{m}}(\tau) d\tau \tag{4}$$

where R_{x} and C_{a} are the parasitic resistance and capacitance connected in x- and z-terminal,

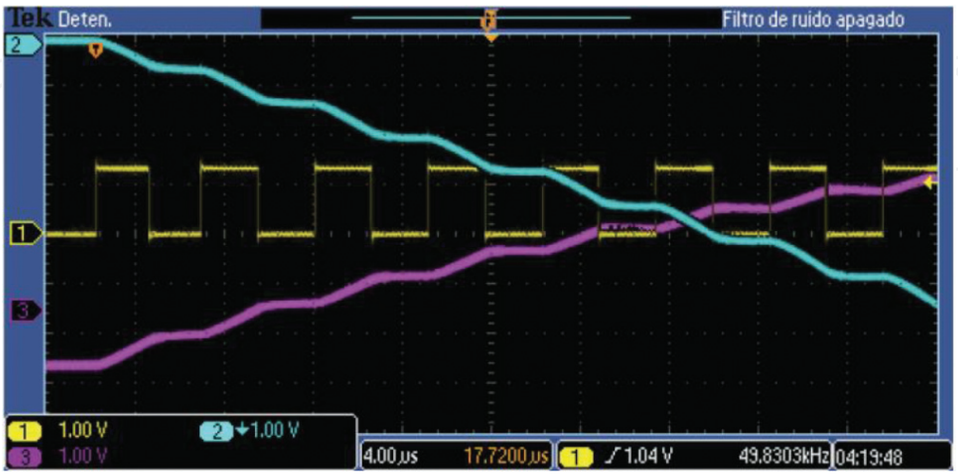


Figure 3. Experimental results of non-volatility property for incremental (pink line) and (blue line) decremental memristor. Pulse signal at yellow line.

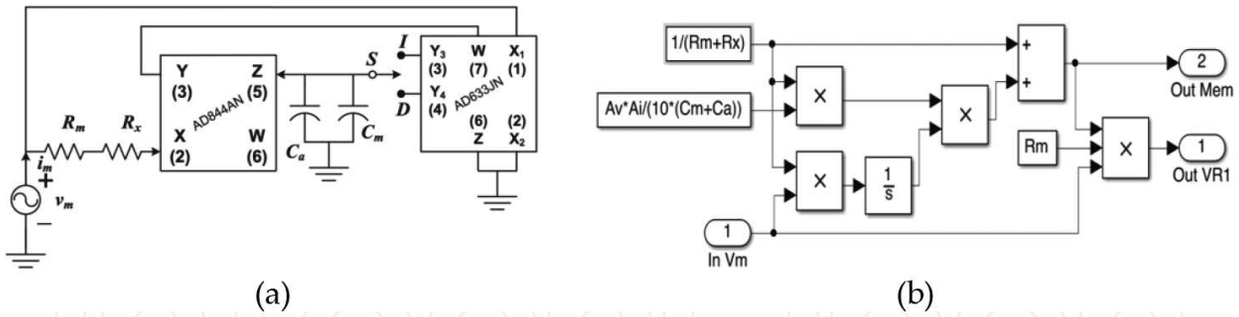


Figure 4. (a) Charge-controlled grounded memductor emulator circuit taken from [32] and (b) SIMULINK model of Eqs. (4) and (5).

respectively; A_v and A_i are the voltage and current gains between *y*- and *x*-terminal and *x*- and *z*-terminal of CCII+. Similarly as in Subsection 2.1, an incremental behaviour is obtained when the ***S*** switch is connected to ***I*** and a decremental behaviour is obtained if ***S*** is connected to ***D***. Each behaviour corresponds to the sign + and − at Eq. (4), respectively. According to the behaviour of the frequency-dependent pinched hysteresis loop, this is composed by two lobes with symmetric areas. Since the hysteresis loop is represented on the *v*-*i* plane, the average current occurs when the area of both lobes is zero, and hence, the hysteresis loop tends to be a straight line as $f \to \infty$. This last effect is achieved when the linear time-varying part of the memductor is zero, and hence, from Eq. (4), we get

$$i_m(t) = \frac{v_m(t)}{R_m + R_x} \tag{5}$$

From Eqs. (4) and (5), a SIMULINK model can be easily built, as shown in **Figure 4(b)**. Note that to obtain a decremental memductor, the input-terminal second of the block, shown in **Figure 4(b)**, must be negative. Considering $v_m(t) = A_m \sin(\omega t)$ and substituting Eq. (5) in Eq. (4), we get

$$\frac{i_m(t)}{v_m(t)} = \frac{1}{R_m + R_x} \pm \frac{A_v A_i A_m}{10\omega(R_m + R_x)^2(C_m + C_a)} \cos(\omega t - \pi) \tag{6}$$

and the k_n parameter is given by

$$k_n = \frac{A_v A_i A_m}{10\omega(R_m + R_x)(C_m + C_a)} = \frac{1}{\tau f} = \frac{T}{\tau} \tag{7}$$

where $\tau = \frac{20\pi(R_m + R_x)(C_m + C_a)}{A_v A_i A_m}$. From Eq. (7), one can intuit that k_n will decrease as the frequency increases, but Eq. (7) also reveals that

1. $k_n \to 0$ when $f \to \infty$ or $A_m \to 0$. Therefore, Eq. (6) becomes dominated by its linear time-invariant admittance.
2. $k_n \to 1$ when $f \to 1/\tau$ or A_m is monotonically increased. Hence, the maximum frequency-dependent pinched hysteresis loop is obtained.
3. $k_n \to \geq 1$ when $f \leq 1/\tau$ or A_m increases too much. For this case, the hysteresis loop is lost.

In this manner, the behaviour of the frequency-dependent pinched hysteresis loop can be kept over a broad range of frequencies and amplitude A_m, when the numerical value of k_n is in the interval (0, 1) [32]. This means that τ must be updated according to f and A_m, respectively. The numerical value of each element of **Figure 4(a)** for different operating frequencies and amplitudes can be found in [32].

According to [32], **Figure 4(a)** was configured for working at 16 Hz in both operation modes. Henceforth, numerical results of the incremental topology will be shown below in the left side, whereas the decremental topology will be shown in the right side. From **Figure 4(b)**, numerical results for each topology are depicted in **Figure 5(a)** and **(b)** (solid lines). Let us now increase monotonically the operating frequency of $v_m(t)$ until $f = 500$ Hz. As depicted in **Figure 5(c)** and **(d)** (solid lines), the frequency-dependent pinched hysteresis loop for both topologies becomes dominated by the linear time-invariant admittance. In this stage, for widening the hysteresis loop of each topology and keeping $f = 500$ Hz, C_m or R_1 must be adjusted. Afterwards, each topology shown in **Figure 4(a)** was simulated at HSPICE and numerical results are illustrated in **Figure 5(a)** and **(b)** (dash-dot lines) operating at 16 Hz, respectively. Similarly as above, the operating

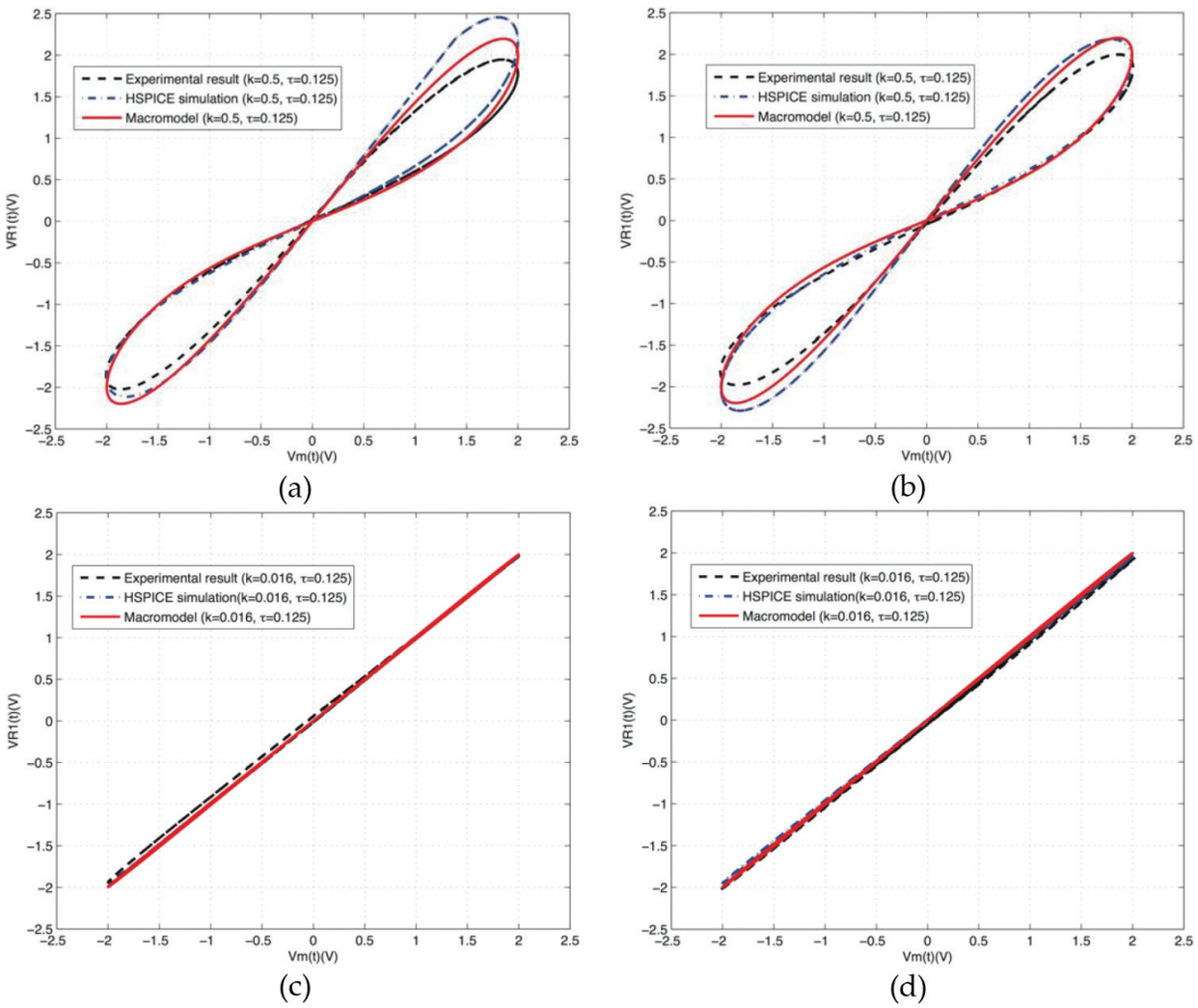


Figure 5. Numerical, HSPICE and experimental results of **Figure 4(a)** operating at: (a) 16 Hz and (c) 500 Hz, for incremental mode; (b) 16 Hz and (d) 500 Hz, for decremental mode.

frequency was increased until 500 Hz and, as a consequence, both pinched hysteresis loops become a straight line, as depicted in **Figure 5(c)** and **(d)** (dash-dot lines). In order to demonstrate the real behaviour of the memductor emulator circuit, **Figure 4(a)** was built with off-the-shelf devices.

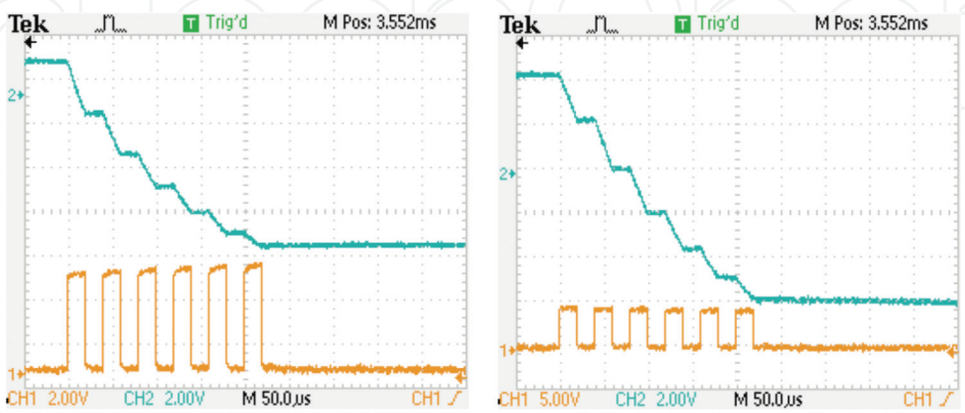
In this way, **Figure 5(a)** and **(b)** (dashed lines) illustrate the pinched hysteresis loops for both operation modes and the upper and lower lobe area of both hysteresis loops becomes zero when the operating frequency increases and hence the hysteresis loop tends to be a straight line, as illustrated in **Figure 5(c)** and **(d)** (dashed lines), confirming the theory described before. To experimentally test the non-volatility of the memductor emulator circuit, the voltage across C_m of **Figure 4(a)** was measured for each incremental and decremental configuration. In both cases, a rectangular pulse train of 5 V of amplitude with 82 μs was applied in the input of **Figure 4(a)**. Therefore, **Figure 6(a)** shows the behaviour of $v_{Cm}(t)$ for the incremental case, whereas **Figure 6(b)** shows the decremental case. From **Figure 6**, one can observe that the variation of $v_{Cm}(t)$ is more pronounced for the decremental case. Observe, also, that the voltage is kept during non-pulse period. Again, the memductive behaviour in each operation mode can be reverted to its last value, whether a negative pulse of the same size is applied [32].

2.3. Grounded memristor emulator circuit II

As last example, we discuss the charge-controlled grounded memristor emulator circuit reported in [31] and illustrated in **Figure 7(a)**. Simple analysis of **Figure 7(a)** allows us to obtain the memristive behaviour given by

$$\frac{v_m(t)}{i_m(t)} = M(q_m(t)) = R_1 \pm \frac{R_2}{40C_1}\int_0^t i_m(\tau)d\tau \tag{8}$$

It is notable to point out that the positive sign in Eq. (8) correspond to the ***S*** switch connected to ***I*** in **Figure 7(a)** and hence, an incremental behaviour is obtained; whereas the negative sign is obtained when ***S*** is connected to ***D*** and hence a decremental behaviour. Again, following the idea described in previous subsections and reported in [28, 31], a frequency analysis can be



(a) (b)

Figure 6. Experimental results of non-volatility property for: (a) incremental mode and (b) decremental mode.

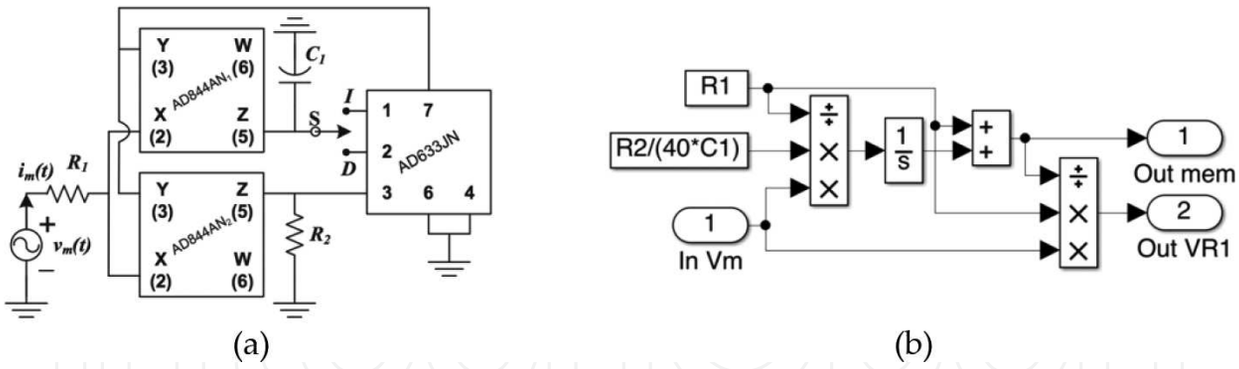


Figure 7. (a) Charge-controlled grounded memristor emulator circuit taken from [31] and (b) SIMULINK model of Eqs. (8) and (9).

done. According to Eq. (8), the average current will occur when the linear time-varying resistor is zero and hence from Eq. (8) we get:

$$i_{\mathrm{m}}(t) = \frac{v_{\mathrm{m}}(t)}{R_1} \tag{9}$$

By merging Eqs. (8) and (9), a SIMULINK model can be built, as depicted in **Figure 7(b)**. In this figure, the input-terminal second of the adder block must be negative to obtain a decremental behaviour. Assuming $v_{\mathrm{m}}(t) = A_{\mathrm{m}}\sin(\omega t)$ and substituting Eq. (9) in Eq. (8), we obtain

$$\frac{v_{\mathrm{m}}(t)}{i_{\mathrm{m}}(t)} = R_1 \pm \frac{R_2 A_{\mathrm{m}}}{40 R_1 C_1 \omega} \cos(\omega t - \pi) \tag{10}$$

It follows from Eq. (10) that

$$k_{\mathrm{n}} = \frac{R_2 A_{\mathrm{m}}}{40 R_1^2 C_1 \omega} = \frac{1}{\tau f} = \frac{T}{\tau} \tag{11}$$

where $\tau = \frac{40\pi R_1^2 C_1}{R_2 A_{\mathrm{m}}}$ is the time constant of the emulator circuit and $T = \frac{1}{f}$ is the period of $v_{\mathrm{m}}(t)$. In the same way as in previous subsections, k_{n} will decrease as the operating frequency increases, and for holding the hysteresis loop at a particular frequency, the numeric value of τ must be updated by C_1. Analysing Eq. (11) for both configurations, we have

1. $k_{\mathrm{n}} \to 0$ when $f \to \infty$ or $A_{\mathrm{m}} \to 0$. Therefore, Eq. (10) becomes dominated by R_1.
2. $k_{\mathrm{n}} \to 1$ when $f \to 1/\tau$ or A_{m} is monotonically increased. Thus, we see that the maximum pinched hysteresis loop is achieved.
3. $k_{\mathrm{n}} \to \geq 1$ when $f \leq 1/\tau$ or A_{m} increases too much. For this case, the hysteresis loop is lost.

According to [31], the memristor emulator circuit was configured to operate at 16 Hz in both operation modes. By using **Figure 7(b)**, the hysteresis loop for each topology shown in **Figure 7(a)** is obtained, as depicted in **Figure 8(a)** and **(b)** (solid lines), respectively. By monotonically increasing the operating frequency of $v_{\mathrm{m}}(t)$ until 100 Hz, both hysteresis loops become dominated by R_1,

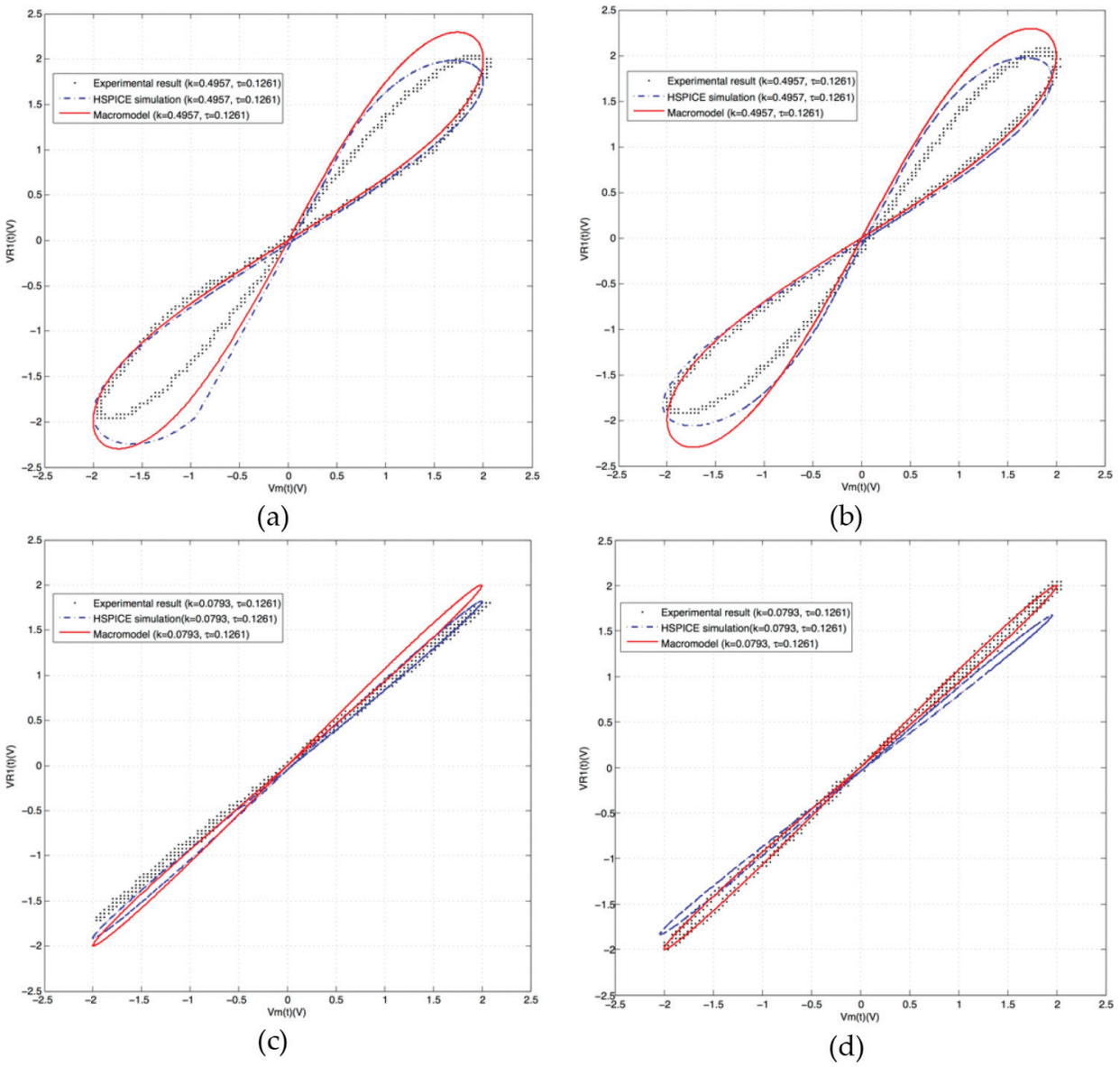


Figure 8. Numerical, HSPICE and experimental results of **Figure 7(a)** operating at: (a) 16 Hz and (c) 100 Hz, for incremental mode; (b) 16 Hz and (d) 100 Hz, for decremental mode.

as illustrated in **Figure 8(c)** and **(d)** (solid lines). It is worth stressing that to obtain the pinched hysteresis loops shown in **Figure 8(a)** and **(b)** (solid lines) but at $f = 100$ Hz, the numeric value of C_1 must be adjusted. Therefore, one can insight that by scaling down C_1, the hysteresis loop behaviour, for both topologies, can be pushed for operating at higher frequencies. On the other hand, **Figure 7(a)** was also simulated at HSPICE by using the numerical value of each element described in [31] and for both topologies. Simulation results are illustrated in **Figure 8(a)** and **(b)** (dash-dot lines), respectively; whereas the linear behaviours are depicted in **Figure 8(c)** and **(d)** (dash-dot lines).

To validate the results derived and demonstrate the real behaviour of the emulator circuit, **Figure 7(a)** was built and experimentally tested by using commercially available active

devices. Therefore, **Figure 8(a)** and **(b)** (dot-square lines) show the experimental results for each topology and at each fundamental operating frequency; whereas **Figure 8(c)** and **(d)** (dot-square lines) show that the hysteresis loops become dominated by R_1, confirming the theory described above. A notable fingerprint of any memristor emulator circuit is the non-volatility of its memristance. This means that the memristance once programmed, its last value must be kept for a long time. In order to verify this property, the voltage across C_1 was first experimentally measured and next, by using Eq. (8), a post-processing was done for getting the memristance variation for each topology, as depicted in **Figure 9** (top figure). The memristance variations were obtained when a pulse train of 5 V of amplitude and 0.5 ms of pulse width was applied to **Figure 7(a)**, as illustrated in **Figure 9** (lower figure).

As one can observe in **Figure 9**, the memristance range for both emulator circuits is 7 kΩ, and although the pulse train is applied indefinitely, the maximum memristance achieved is 19 kΩ; whereas the minimum memristance for the decremental case is 5 kΩ. On the other hand, if the pulse train with −5 V of amplitude and same pulse width is applied, then the memristive behaviour is inverted for each topology shown in the top of **Figure 9** [31].

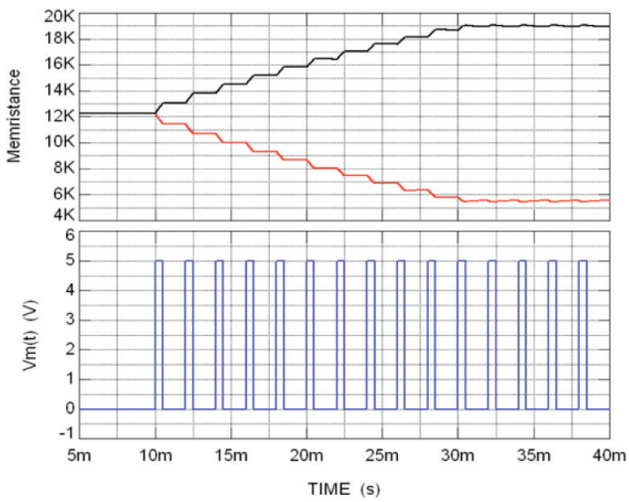


Figure 9. Experimental results of non-volatile memristance for incremental mode (black line) and decremental mode (red line). In the figure below, $v_m(t)$ as pulse train.

3. Design guide

According to Section 2, one can observe that Eqs. (1), (4) and (8) have the form

$$y_n(t) = x(t)\left(a_n \pm b_n \int_0^t z(\tau)d\tau\right) \tag{12}$$

where $y_n(t)$ is the current or voltage output signal, $x(t)$ is the voltage or current input signal and $z(t)$ is the voltage or current control signal; a_n represents the linear time-invariant gain and b_n represents the linear time-varying gain, which is associated with the time constant of the emulator circuit [28, 31, 32]. Assuming that $z(t) = A_m\sin(\omega t + \theta)$, where θ is the phase in degrees, we obtain

$$\int_0^t z(\tau)d\tau = -\frac{A_{\mathrm{m}}}{\omega}\cos(\omega t+\theta) = \mp\frac{1}{\omega}\sqrt{A_{\mathrm{m}}^2 - z^2(t)} \tag{13}$$

therefore, Eq. (12) becomes

$$y_{\mathrm{n}}(t) = x(t)\left(a_{\mathrm{n}} \mp \frac{b_n}{\omega}\sqrt{A_{\mathrm{m}}^2 - z^2(t)}\right) \tag{14}$$

According to [28, 31, 32], the linear time-varying gain can be computed in function of ω and A_{m} given by

$$b_{\mathrm{n}} = \frac{a_{\mathrm{n}}\omega k_{\mathrm{n}}}{A_{\mathrm{m}}} \tag{15}$$

where $k_{\mathrm{n}} \in (0, 1)$ is a parameter that is used to ensure the behaviour of the pinched hysteresis loop.

In order to design a memristor emulator circuit, the following four-step design procedure is proposed

Step 1. For all memristor emulator circuit that has the form given by Eq. (12) and to ensure the pinched hysteresis loop, we choose $k_{\mathrm{n}} = 0.5$.

Step 2. Given an operating frequency and A_{m}, use Eq. (15) to find the relation between b_{n} and a_{n}.

Step 3. Select the numeric value of a_{n}, which is associated to the linear time-invariant resistor/conductor. As a consequence, the numeric value of b_{n} is derived from Eq. (15).

Step 4. For each topology, b_{n} is related with those parameters of the emulator circuit and τ. Therefore, the numeric value of each resistor and capacitor can be deduced.

If the above procedure is followed, it is most likely that a memristor emulator circuit with good features will result and with a frequency-dependent hysteresis loop with relatively symmetrical lobes.

4. Offset compensation

Some properties that any emulator circuit must satisfy to be considered as memristor were described in Section 1. One of them is the frequency-dependent pinched hysteresis loop observed on the voltage-current plane, which must pass through the origin for any periodic signal with any amplitude, operating frequency and initial conditions [1]. Thus, whether a periodic signal is applied to the memristor emulator circuit, both the voltage and current are zero when any of them is zero. Therefore, any device is a memristor or a memristive device when it has a current-voltage hysteresis curve with identical zero crossing. However, until today, all the memristor emulator circuits reported in the literature [19–32] are operating in low-frequency and some of them present a deviation of the crossing point on the origin. This behaviour is more evident when the operating frequency of the stimulus signal increases, and

hence, the emulator circuit does not only stop mimicking the behaviour of the memristor, but also reduces its application range. Note that below a certain critical frequency, the emulator circuit mimics well the behaviour of a memristor and beyond that of critical frequency, the circuit becomes a memristive device with an additional battery in series.

In order to overcome this shortcoming and achieve a pinched hysteresis loop operating at high frequency, an offset compensation technique must be applied. Such techniques have been reported in [33]. Basically, the technique involves adding two DC voltage sources in the analogue multiplier to vertically and horizontally control the offset of the hysteresis loop. However, as described in [33], this offset reduction technique is only applicable to floating and grounded memristor emulator circuits whose design is based on analogue multipliers. In this manner, let us consider the topologies shown in **Figure 1(a)** and **7(a)**, including the voltage sources, as depicted in **Figure 10(a)** and **(b)**, respectively. According to Eq. (1), **Figure 10(a)** and [28, 33], the controlled incremental and decremental memristance is modified as

$$M\left(\varphi_{\mathrm{m}}(t), V_{\mathrm{H}}, V_{\mathrm{V}}\right) = R_1 \pm \frac{R_4(R_1 - V_{\mathrm{V}})}{10R_2R_3C_{\mathrm{z}}}\int_0^t v_{\mathrm{m}}(\tau)d\tau - V_{\mathrm{H}} \tag{16}$$

Similarly for Eq. (8), **Figure 10(b)** and [31, 33], the memristance becomes:

$$M(q_{\mathrm{m}}(t), V_{\mathrm{H}}, V_{\mathrm{V}}) = R_1 \mp \frac{R_2}{20}V_{\mathrm{V}} \pm \frac{R_2}{40C_1}\int_0^t i_{\mathrm{m}}(\tau)d\tau \pm V_{\mathrm{H}} \tag{17}$$

where V_{H} is a DC voltage source to control the horizontally offset and V_{V} is other DC voltage source to control the vertical offset of the frequency-dependent pinched hysteresis loop on the voltage-current plane. Note that if $V_{\mathrm{H}} = V_{\mathrm{V}} = 0$, then Eqs. (16) and (17) are reduced to Eqs. (1) and (8), respectively. For both topologies shown in **Figure 10**, two switches, S_1 and S_2, are used to interchange the kind of memristor and to connect the V_{V} voltage source in each case. To validate the offset reduction method, **Figure 10(a)** was configured at decremental mode and operating to 14 kHz. In a first step, $V_{\mathrm{H}} = V_{\mathrm{V}} = 0$ were considered and simulation results are depicted in **Figure 11(a)** (solid line). Note that the pinched hysteresis loop deviates of the origin. In a second step, the DC voltage sources were monotonically decreased until $V_{\mathrm{H}} = -60.59$ mV and $V_{\mathrm{V}} = -160.3$ mV, and as a consequence, the offset was reduced, as shown

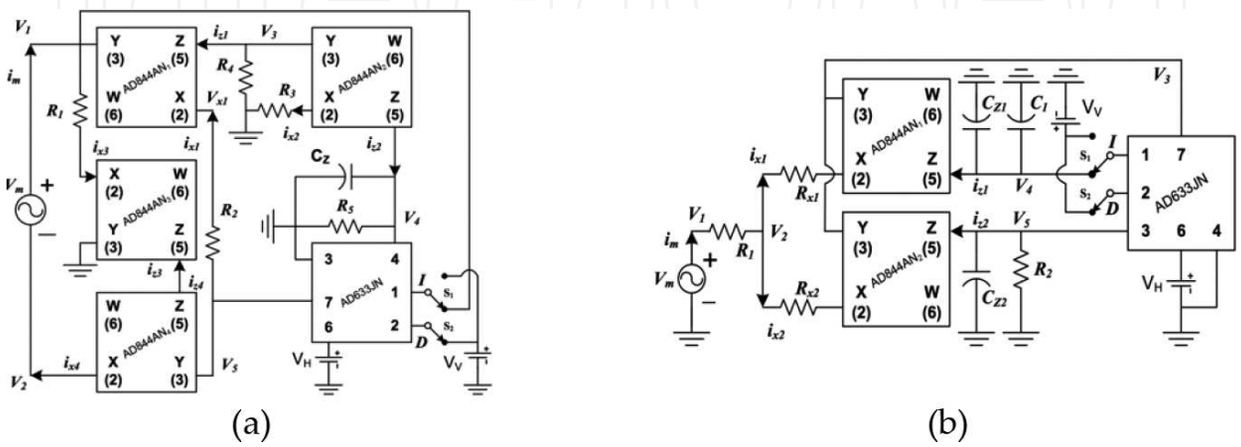


Figure 10. Offset compensated memristor emulator circuits: (a) **Figure 1(a)** and (b) **Figure 7(a)**.

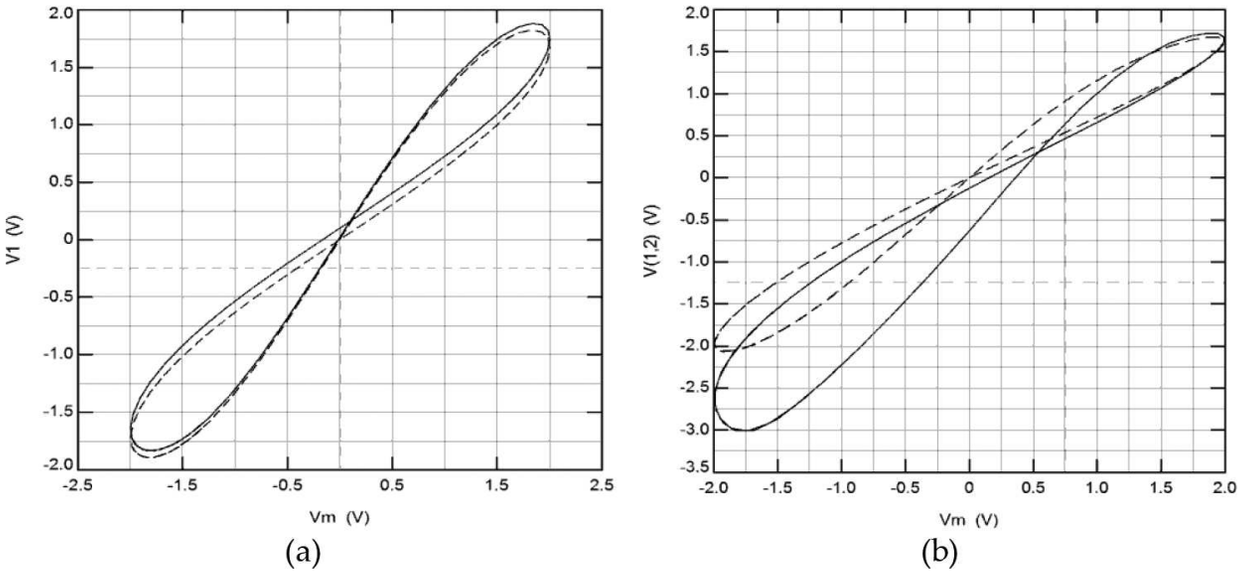


Figure 11. HSPICE results for: (a) decremental topology of **Figure 10(a)** and (b) incremental topology of **Figure 10(b)**. For both figures: offset uncompensated (solid lines) and compensated (dashed lines).

in **Figure 11(a)** (dashed line). A similar analysis procedure was realized to the topology depicted in **Figure 10(b)** but operating to 160 kHz. In this manner, the grounded memristor emulator circuit was connected as incremental mode and considering $V_H = V_V = 0$. HSPICE simulations were obtained and shown in **Figure 11(b)** (solid line). In order to reduce the offset in **Figure 11(b)** (solid line), the DC voltage sources were updated to $V_H = -195.5$ mV and $V_V = 1.568$ V, and hence, the crossing point was pulled towards the origin, as shown in **Figure 11(b)** (dashed line). It is worth to stress that the value of each DC voltage source associated to each topology was derived to trial and error, and it should slightly be updated for each operating frequency. Hence, an open question is how to automatically compute the numeric value of each DC voltage source associated to each topology and operation mode. Moreover, in **Figure 11(b)** (solid lines), one can observe that each frequency-dependent pinched hysteresis loop becomes slightly deformed, resulting at an asymmetrical behaviour with regards to the origin, and hence, the hysteresis lobe area is not equal. Nonetheless, after of the offset compensation, the hysteresis lobe area for all frequency-dependent pinched hysteresis loops become relatively equal as depicted in **Figure 11(b)** (dashed lines). As a result, it is predicted that the frequency behaviour of the pinched hysteresis loops for both memristor emulator circuits can be pushed for operating in higher frequencies and holding a symmetrical behaviour, since the offset voltage glimpsed can again be reduced by updating the DC voltage sources.

5. Transformation of normal non-linear resistors to inverse

A memristor/memductor is basically a resistor/conductor whose resistance/conductance can be changed by applying a voltage across its terminals or by applying a flow of current. The type of control signal depends on the type of memristor/memductor, i.e. flux- or charge-controlled. In any case, the frequency-dependent pinched hysteresis loop of a normal non-linear resistor/conductor will become a straight line if the operating frequency increases. This

effect is because a normal non-linear resistor/conductor uses an integrator block and, in general, its behaviour can be modelled by Eq. (12). Since the inverse operation of an integral is the derivate, the hysteresis loop behaviour of a normal non-linear resistor can be inverted whether a differentiator block is used instead of an integrator block. Under this assumption and following the idea presented in Section 3, we have modified Eq. (12) as

$$y_{\mathrm{i}}(t) = x(t)\left(a_{\mathrm{i}} \pm b_{\mathrm{i}}\frac{dz(t)}{dt}\right) \tag{18}$$

where $y_{\mathrm{i}}(t)$ is the inverse current or voltage output signal, $x(t)$ is the voltage or current input signal and $z(t)$ is the voltage or current control signal; a_{i} represents the linear time-invariant gain and b_{i} is the linear time-varying gain. Assuming $z(t) = A_{\mathrm{m}} \sin(\omega t + \theta)$, we obtain

$$\frac{dz(\tau)}{dt} = A_{\mathrm{m}}\omega\cos(\omega t + \theta) = \pm\omega\sqrt{A_m^2 - z^2(t)} \tag{19}$$

and Eq. (18) becomes

$$y_{\mathrm{i}}(t) = x(t)\left(a_{\mathrm{i}} \pm b_{\mathrm{i}}\omega\sqrt{A_m^2 - z^2(t)}\right) \tag{20}$$

Comparing Eqs. (14) and (20), one can observe that the sole difference is the position of ω. According to Section 3 [28, 31, 32], the linear time-varying gain can be computed in function of ω and A_{m} given by

$$b_{\mathrm{i}} = \frac{a_{\mathrm{i}}\omega k_{\mathrm{i}}}{A_{\mathrm{m}}} \tag{21}$$

where $k_{\mathrm{i}} \in (0, 1)$. In Section 2, the behavioural model of normal flux- or charge-controlled resistors was derived and one can observe that each model has an integrative part. As first approximation and for obtaining an inverse flux- or charge-controlled resistor from a normal resistor, the integrator circuit of the latter must be replaced by a differentiator circuit in the former. This task can be done by simply interchanging C_1 by R_2 in **Figure 1(a)**, as depicted in **Figure 12(a)**, and analysing this figure we obtain

$$\frac{v_{\mathrm{m}}(t)}{i_{\mathrm{m}}(t)} = R_1 \pm \frac{R_1R_3R_4C_z}{10R_2}\frac{dv_{\mathrm{m}}(t)}{dt} \tag{22}$$

Considering $v_{\mathrm{m}}(t) = A_{\mathrm{m}}\sin(\omega t + \phi)$, where ϕ is the phase in degrees and by using Eqs. (14) and (20), Eqs. (1) and (22) are rewritten as

$$\frac{v_{\mathrm{m}}(t)}{i_{\mathrm{m}}(t)} = R_1 \pm \frac{R_1R_4}{10R_2R_3C_z\omega}\sqrt{A_{\mathrm{m}}^2 - v_{\mathrm{m}}^2(t)} \tag{23}$$

$$\frac{v_{\mathrm{m}}(t)}{i_{\mathrm{m}}(t)} = R_1 \pm \frac{R_1R_3R_4C_z\omega}{10R_2}\sqrt{A_{\mathrm{m}}^2 - v_{\mathrm{m}}^2(t)} \tag{24}$$

Comparing Eqs. (23) and (24) with Eqs. (14) and (20), respectively, one obtains

$$a_{\mathrm{n}} = a_{\mathrm{i}} = R_1, b_n = \frac{R_1 R_4}{10 R_2 R_3 C_z}, b_i = \frac{R_1 R_3 R_4 C_z}{10 R_2} \tag{25}$$

At this point, our results indicate that by selecting adequately the numerical values of each element of Eq. (25) for a particular operating frequency, the emulator circuits of **Figures 1(a)** and **12(a)** are able to generate normal and inverse pinched hysteresis loops, respectively. It is worth to stress that the transformation methodology is only applicable for those topologies where the integrator circuit is clearly defined, and when it is replaced by a differentiator circuit, the behaviour of the resulting emulator circuit, in general, is not modified. However, floating and grounded non-linear resistor emulator circuits without this requirement have also been reported in the literature [27–33]. One example of them was shown in **Figure 7(a)**. However, whether C_1 is replaced by an inductor L_1 as shown in **Figure 12(b)**, we get

$$\frac{v_{\mathrm{m}}(t)}{i_{\mathrm{m}}(t)} = R_1 \pm \frac{R_2 L_1}{40} \frac{di_{\mathrm{m}}(t)}{dt} \tag{26}$$

Afterwards assuming that $i_{\mathrm{m}}(t) = A_{\mathrm{m}}\sin(\omega t + \phi)$ and by considering Eqs. (14) and (20), Eqs. (8) and (26) take the form

$$\frac{v_m(t)}{i_{\mathrm{m}}(t)} = R_1 \pm \frac{R_2}{40 C_1 \omega} \sqrt{A_{\mathrm{m}}^2 - i_{\mathrm{m}}^2(t)} \tag{27}$$

$$\frac{v_{\mathrm{m}}(t)}{i_{\mathrm{m}}(t)} = R_1 \pm \frac{R_2 L_1 \omega}{40} \sqrt{A_{\mathrm{m}}^2 - i_{\mathrm{m}}^2(t)} \tag{28}$$

Comparing Eqs. (27) and (28) again with Eqs. (14) and (20), respectively, one obtains

$$a_{\mathrm{n}} = a_{\mathrm{i}} = R_1, b_{\mathrm{n}} = \frac{R_2}{40 C_1}, b_{\mathrm{i}} = \frac{R_2 L_1}{40} \tag{29}$$

Note that although the behaviour of the inductor can be emulated by using gyrators, the resulting circuit becomes bulky and complex. Hence, this transformation technique does not

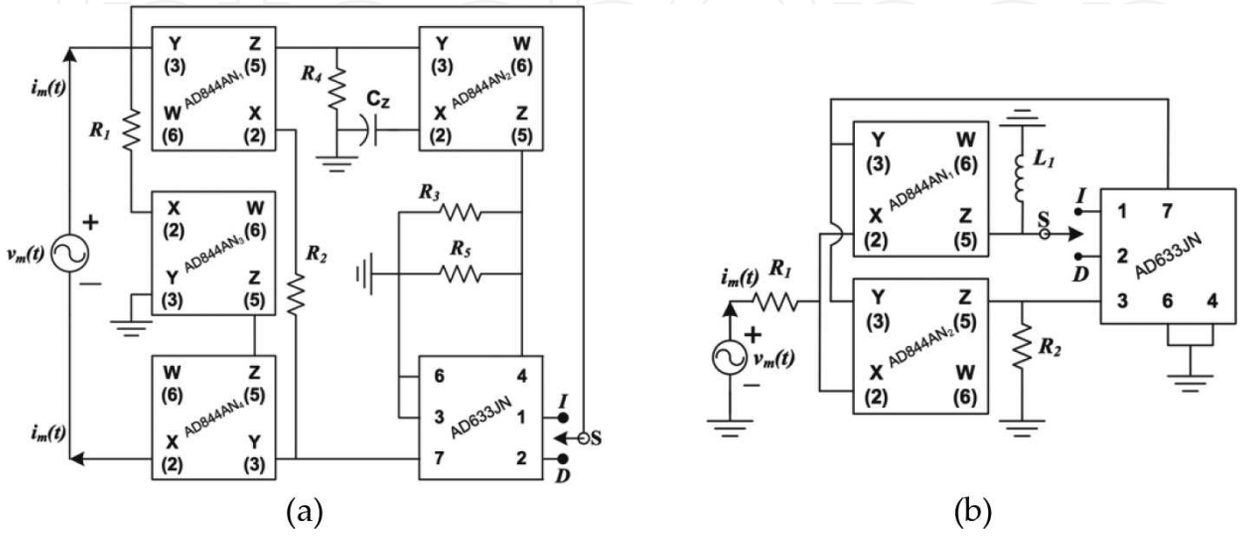


Figure 12. Inverse versions of: (a) **Figure 1(a)** and (b) **Figure 7(a)**.

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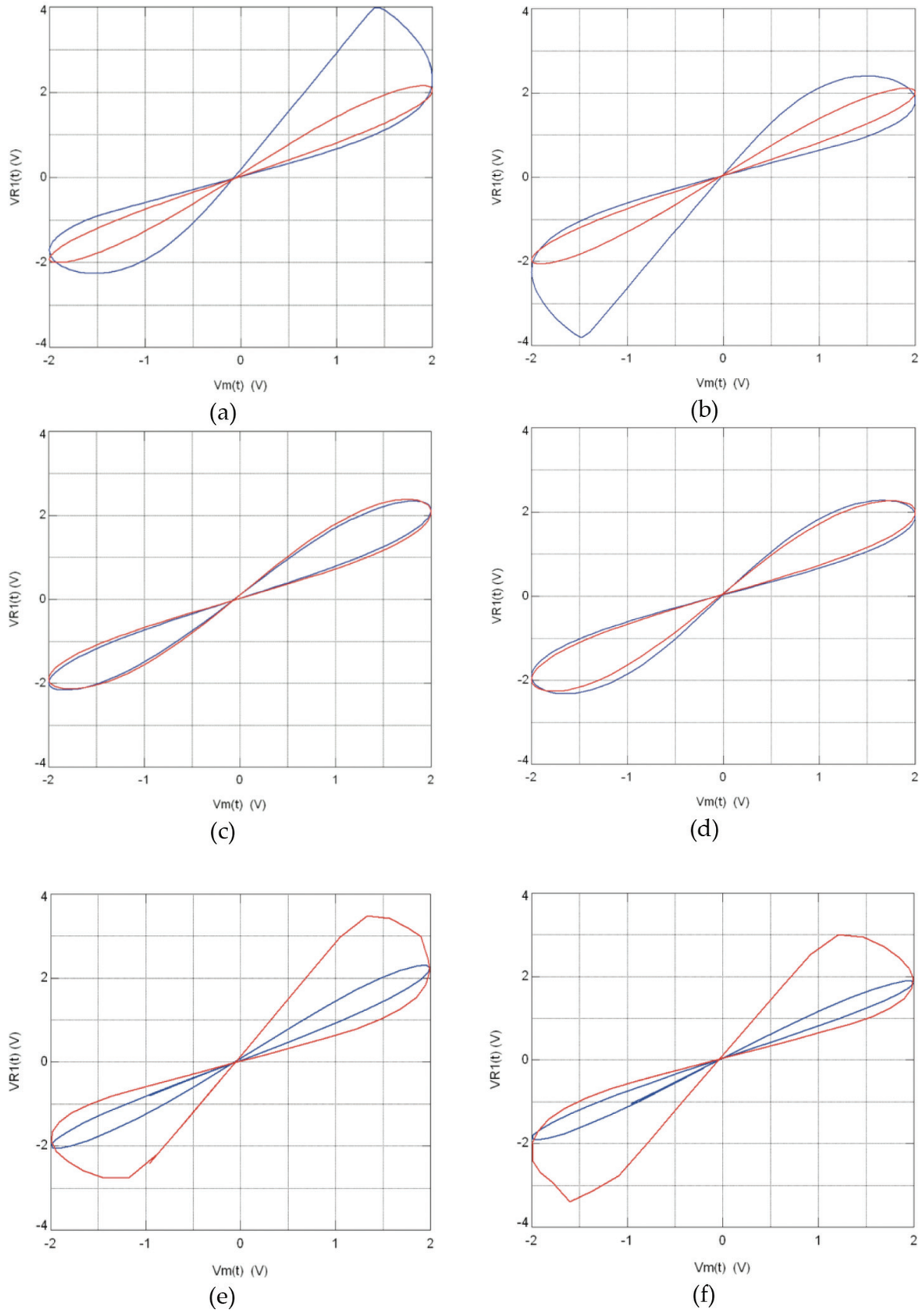

Figure 13. Frequency-dependent hysteresis loop of **Figure 1(a)** (blue line) and **Figure 12(a)** (red line) operating to: 1 kHz for (a) incremental and (b) decremental mode; 2 kHz for (c) incremental and (d) decremental mode; 4 kHz for (e) incremental and (f) decremental mode.

show any advantage with respect to the methodology mentioned above. Without loss of generality, only HSPICE results of **Figures 1(a)** and **12(a)** configured at incremental mode will be shown on the left side of **Figure 13**, whereas that for the decremental configuration will be shown on the right side. In a first step, both emulator circuits were configured to f = 2 kHz. HSPICE results are illustrated in **Figure 13(c)** and **(d)** and it is evident that these hysteresis loops are almost similar. Later, the operating frequency was decreased to f = 1 kHz, and as one can observe in **Figure 13(a)** and **(b)**, the hysteresis loops present the behaviour forecasted. Finally, the operating frequency of $v_m(t)$ was increased to f = 4 kHz, and hence, the behaviour of the hysteresis loops was inverted, as depicted in **Figure 13(e)** and **(f)**. From all these figures, we can observe that for inverse non-linear resistors, the hysteresis loop becomes a straight line when the operating frequency decreases, whereas for normal non-linear resistors, this behaviour is achieved when the operating frequency increases. Note that although the topology of an inverse non-linear resistor shows a frequency-dependent pinched hysteresis loop, this cannot be considered as memristor emulator circuit, since the property of non-volatility is not satisfied. **Table 1** gives the numerical value for each passive element.

Variable	A_m	$a_n = a_i$	b_n	b_i	k_n	k_i
F = 1 kHz	2	10e3	3.14e7	0.19	0.99	025
F = 2 kHz					0.5	0.5
F = 4 kHz					0.25	0.99
Element	R_1	R_3	R_2	R_4	R_5	C_z
Figure 1(a)	10 kΩ	3.18 kΩ	100 kΩ			10 nF
Figure 12(a)		20 kΩ				

Table 1. Numerical variables of Eq. (25) and component list of **Figures 1(a)** and **12(a)**.

6. Analogue applications based on memristor emulator circuits

This section discusses three examples at the behavioural level of abstraction on the use of memristor emulator circuits in real analogue applications.

6.1. Frequency-shift keying (FSK) modulator

Modulator circuits are important blocks in digital communications since they are used to convert a unipolar bit sequence in an appropriate form for modulation and transmission [34]. Among the modulator circuits, frequency-shift keying (FSK) modulation is a frequency modulation scheme in which digital information is transmitted through discrete frequency changes of a carrier wave. Thus, the higher frequency of the modulator is assigned to signal **1** and the lower frequency is assigned to signal **0** [35]. This behaviour can be achieved by using a single-memductor controlled sinusoidal oscillator (SMCO), as shown in **Figure 14(a)**. Through routine analysis, we get

$$s^2 + \frac{1}{C_1}\left(\frac{1}{R_1} - \frac{1}{R_3}\right)s + \frac{W_2}{R_3 C_1 C_2} \tag{30}$$

From Eq. (30), the condition of oscillation (CO) is: $R_3 = R_1$ and the frequency of oscillation (FO) is: $f_0 = \frac{1}{2\pi}\sqrt{\frac{W_2}{R_3 C_1 C_2}}$. It is seen that CO and FO can independently be controlled by R_1 and W_2, respectively. By merging **Figure 4(b)** with Eq. (30), a SIMULINK model can be built. Such model is depicted in **Figure 14(b)** where the voltage and current gains are unitary (i.e. $A_v = A_i = 1$). Note that the SMCO along with an incremental memductor is depicted in the upper part of **Figure 14(b)**, whereas the SMCO along with a decremental memductor is illustrated in the bottom. More detailed analysis of Eq. (30) is found in [36]. For this application, the SMCO was designed with an oscillation centre frequency of $f_0 = 577$ kHz and hence, $R_1 = 1$ kΩ, $R_3 = 942$ Ω, $C_1 = C_2 = 140$ pF and $W_2 = 0.33$ mS. In order to vary the incremental memductance, a pulse train with 2 V of amplitude and pulse width of 3 μs is used to increase W_2; whereas for the decremental memductance, a pulse of 0.3 V of amplitude and with the same pulse width mentioned before is used to decrease W_2. For both cases, when negative pulses with the same amplitudes mentioned before are applied, both memductances return to their last state [32]. By applying these control signals in **Figure 14(b)**, one obtains an FSK signal, as shown in **Figure 15 (a)** and **(b)**. On these last figures and into the interval [0, 2 ms], the operating frequency of the FSK modulator is the same as SMCO. Next, when a positive digital signal is applied to the incremental and decremental memductor, the memductance increases or decreases, respectively. As a consequence, the FO of the SMCO also increases or decreases, as shown in **Figure 15(a)** and **(b)** into the interval [2 ms, 4 ms], approximately. Afterwards, by applying a negative digital signal to the memductors, the FSK modulator returns to its original FO.

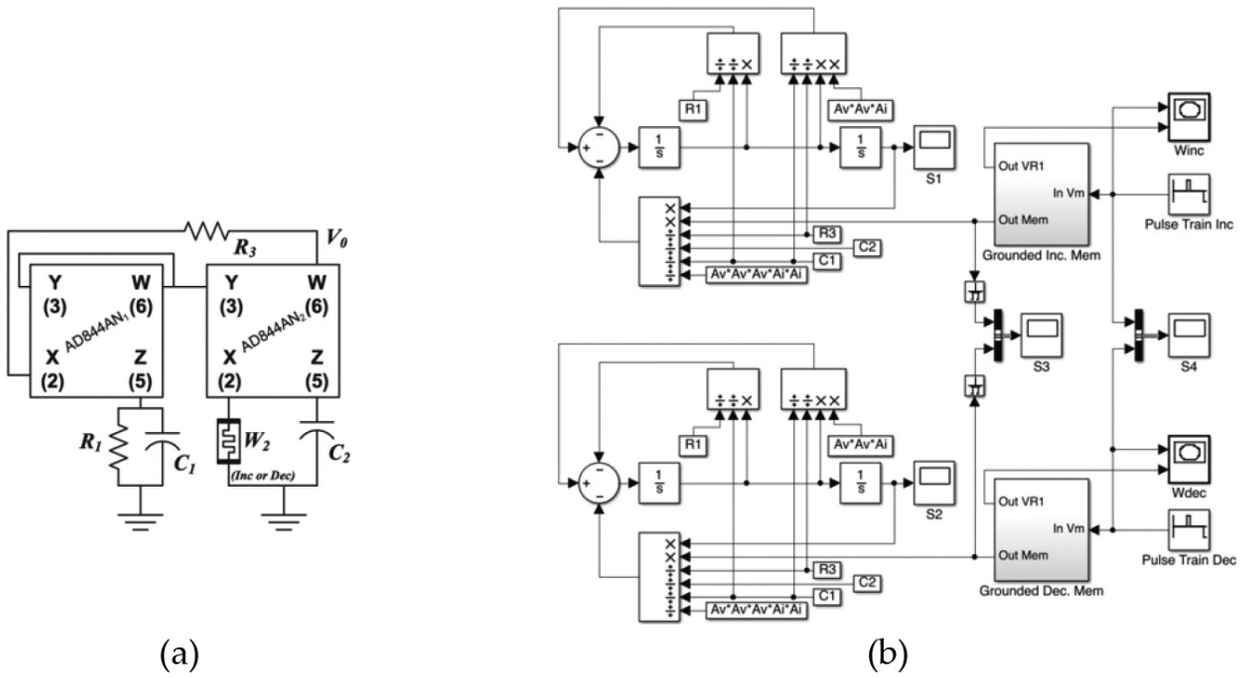

Figure 14. (a) FSK modulator based on SMCO by using **Figure 4(a)**; and (b) SIMULINK model of Eq. (30).

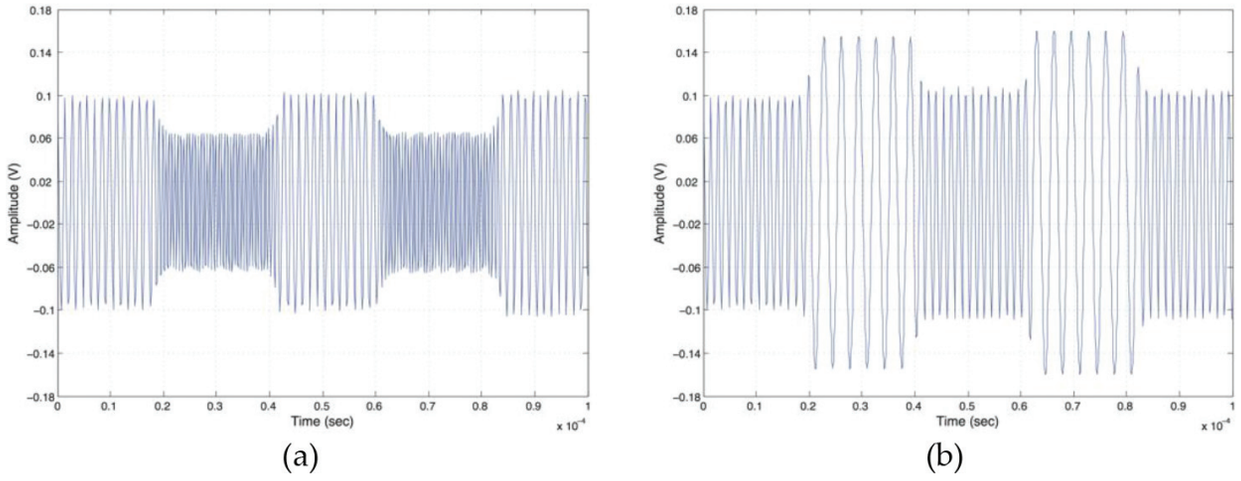

Figure 15. Time response of the FSK modulator using: (a) incremental memductor and (b) decremental memductor.

Therefore, we can observe that a memductor (or memristor) device is useful for controlling the FO of a SMCO and they can be used to design an FSK modulator.

6.2. Proportional-integral-derivative (PID) controller

Proportional-integral-derivative (PID) control has been used successfully for regulating processes in industry for more than 60 years, due to its simple and easy design, low cost and wide range of applications. A PID controller involves three parts: proportional part, integral part and derivative part, and its target is to minimize the error between the set point and the measured output. It is worth mentioning that for a complex or non-linear process, sometimes it is very difficult to find the optimal parameters of the PID controller.

In this sense, the oldest and simplest method was proposed by Ziegler and Nichols [37]. However, this tuning method provides a large overshoot and settling time, and hence, the PID parameters must subsequently be refined. Other methods that can also be used for choosing the parameters of PID controller were reported in [38]. However, this method presents drawbacks when applied to certain types of plants. Furthermore, the PID parameters are always constant and almost without knowledge of the process to control. Therefore, an efficient and effective online tuning mechanism is widely demanded. This last task can be achieved by using a memristor/memductor, since its memristance/memductance can be kept even when the current flow in the memristor/memductor is stopped [1, 28–33, 35]. This property asserts that it is possible to update the parameters of a continuous PID controller online, i.e. the proportional gain (k_p), integral gain[1] (k_i) and derivative gain (k_d). In order to illustrate this idea, the transient response of a second-order low-pass filter is controlled by a PID controller [39]. The transfer function of the filter is given by

$$H(s) = \frac{\frac{1}{LC}}{s^2 + \frac{s}{RC} + \frac{1}{LC}} \tag{31}$$

The numeric value of each element of Eq. (31) is R = 100 Ω, L = 0.475 mH, and C = 1 μF. At this point, the PID controller parameters, k_p = 80, k_i = 1e5 and k_d = 2e-3, were obtained according to [37].

[1]This parameter should not be confused with k_i parameter associated to the inverse nonlinear resistor.

Since the integral and derivative parts of the continuous PID controller are, in practice, designed with R-C elements and active devices [27], one can obtain $R_i = R_d = 2\ k\Omega$, $C_i = 5\ nF$ and $C_d = 1\ \mu F$. Under this assumption, **Figure 4(b)**, the PID controller and Eq. (31) are merged to build a SIMULINK model. It is worth mentioning that the memductor shown in **Figure 4(b)** was configured to operate at 300 Hz. Thus, **Figure 16** shows all feedback systems to be simulated [39]. In the upper part of **Figure 16**, the plant with feedback is illustrated. In the second block, the PID controller with fixed parameters along with the plant is depicted. The third block is the PID controller based on incremental memductor along with the plant; and finally, the fourth block depicts the PID controller based on decremental memductor along with the plant. For the last two cases, the memductance is varied by applying a pulse train, and a square signal with 5 V of amplitude and $f = 200$ Hz is applied to all feedback systems. **Figure 17** shows all the transient responses of **Figure 16**. As a first step, the square signal (magenta line) is applied to the feedback plant, and its transient response is underdamped (green line), as shown in **Figure 17(a)**. Hence, the plant needs to be controlled. In a second step, the transient response of the second block is obtained and shown in **Figure 17(a)** (black line). Here, the rise- and fall-time are symmetric and cannot be modified online. In order to get that effect, the incremental and decremental memductor is used [39]. For both memductances, the pulse train was adjusted to get the following cases:

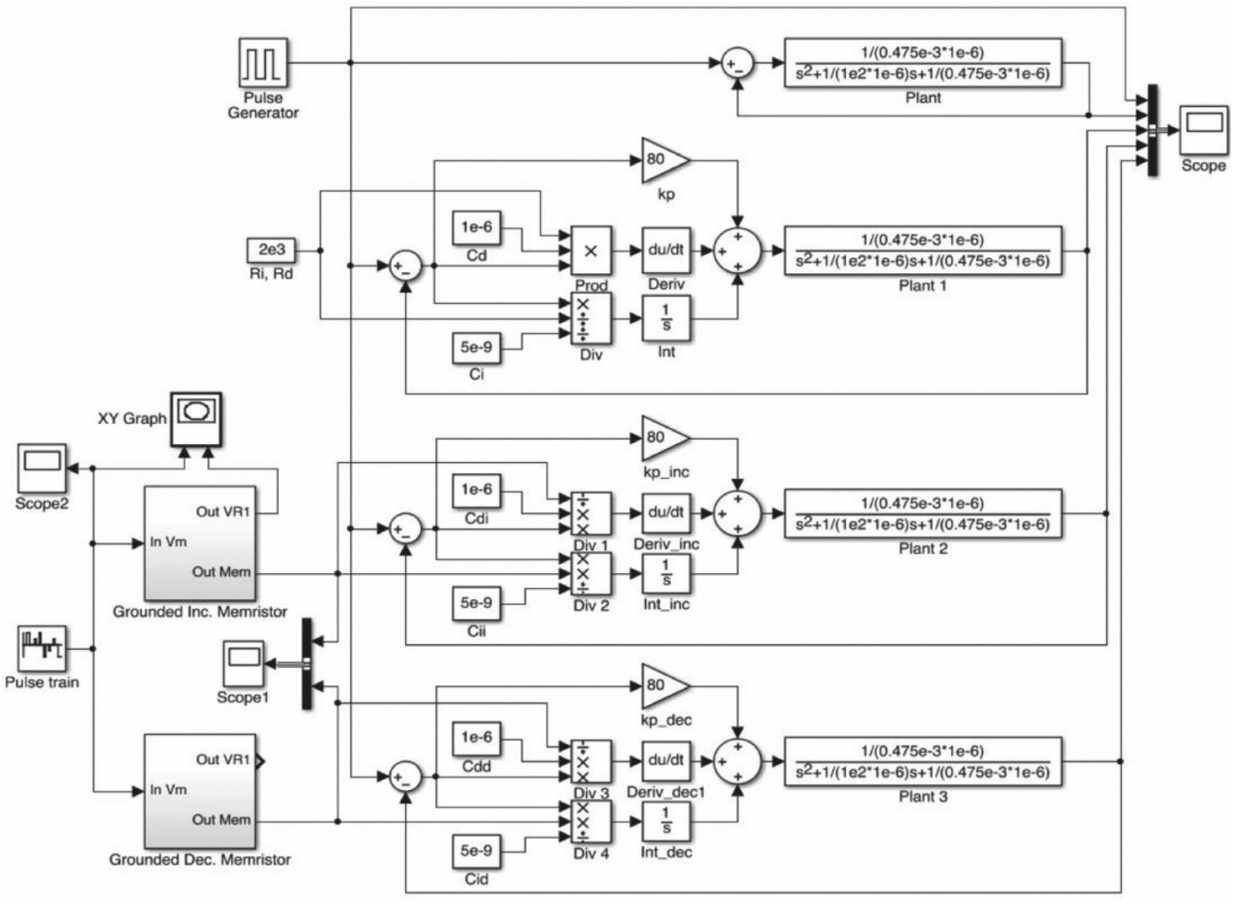

Figure 16. PID controller based on memductors.

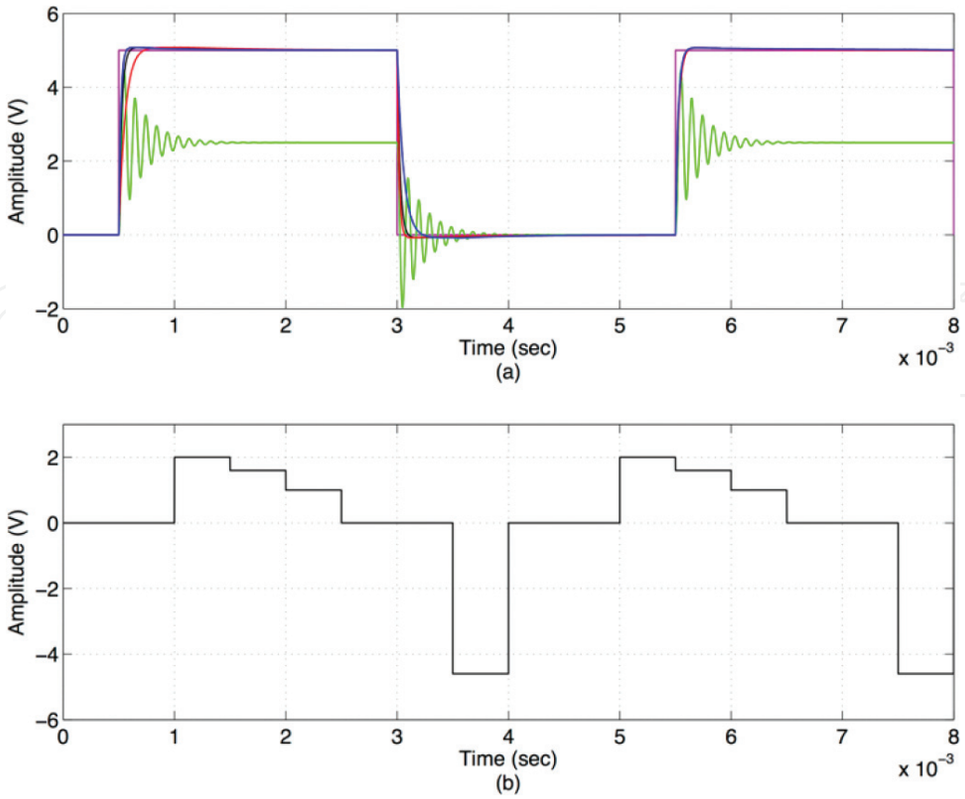

Figure 17. (a) Transient response of the plant and PID controllers. (b) Pulse train for controlling the incremental and decremental memductance.

1. By using an incremental memductor, the rise-time (red line) of the system is largest than the rise-time gotten with fixed parameters (black line) and those obtained with the decremental memductor (blue line). In fact, the rise-time of the latter is the shortest, as depicted in **Figure 17(a)**.
2. By using a decremental memductor, the fall-time (blue line) of the system is largest than the fall-time gotten with fixed parameters (black line) and those obtained with the incremental memductor (red line). In fact, the fall-time of the latter is the shortest, as shown in **Figure 17(a)**.
3. In order to get the same rise-time in all cases, both memductances were adjusted by using the pulse train shown in **Figure 17(b)**, and the result can be observed in **Figure 17(a)** at 5.5 ms, approximately.

Therefore, we can observe that memristors/memductors are useful for controlling the rise- and fall-time of the transient response of a feedback system.

6.3. Memristive synapses

As a last example, but not the least important, we describe the analysis and design of a synaptic circuit based on memristors. Basically, synapses are specialized sites where several neurons are connected, which receive and send information from other cells; this junction is the foundation of

complex brain tasks and functions related to learning and memory. Emulation of biological synapses is the basis to build large-scale brain-inspired systems [40]. A key property of the brain is its ability to learn, this process lies in the plasticity of the synapses that allows the nervous system to adapt. Memristor is a candidate suitable to emulate a synapse, due to its non-volatility property and programmable device. But a single memristor cannot accomplish this task; in fact, there are several topologies that enable this behaviour, depending on the approach used for artificial neural network, i.e. cellular neural networks (CNN) [41], spiking neural networks (SNN) [42, 43], feed-forward neural networks (FFNN) [44] and recurrent neural networks (RNN) [45]. Few architectures based on memristors are focused on feed-forward artificial neural networks, which completely satisfies the requirements of an artificial synapse. On the other hand, there are several requirements that must be met for a synaptic learning [46]:

1. The weight must be stored always in the absence of learning.
2. The synapse must be computed as an output, i.e. the product of the input signal with the synaptic weight also called synaptic weighting.
3. Each synapse must occupy a reduced area.
4. Each synapse must operate with low power dissipation.
5. Each synapse must be capable of implementing a learning rule such as Hebbian or Back propagation [1, 40, 46].

Table 2 shows a comparison among the most recent memristive neural networks. Thus, the third column of the table shows whether design meets the five rules mentioned before, such that the synapse can be considered as *learning synapse*. Design of [41] does not meet rule 5, since to change a negative weight to positive not only additional circuitries is required, but on line training is not also possible; [43] meets some of the properties of [46], because it is implemented through an ideal memristor model whose applications are limited to simulations; [44] uses a high number of active components (i.e. 64) for building a synapse, considering the memristor emulator reported in [49]. The fourth column is the frequency of the spikes for SNN approach and for the case of MCNN and ANN the time for weight setting from its lowest to the highest value is described. If weight setting time is too long, then weight processing will take longer which affects its performance. Thus, only [44] simulates and fully implements a synapse based on a memristor emulator. Unlike [41, 42, 47], its hardware applications are not limited to HP memristor fabrication, but the number of elements and the operating frequency are parameters that restrict its performance. However, frequency is limited and the number of active components is high. On the other hand, the proposed synaptic memristive bridge circuit begins with the analysis of memristance of the flux-controlled memristor of **Figure 1(a)**. First, memristance variation of **Figure 1(a)** is analysed, where Eq. (1) can be rewritten as

$$M(\varphi_{\mathrm{m}}(t)) = R_1 \pm R_1 \alpha \varphi_{\mathrm{m}}(t) \tag{32}$$

The maximum value of memristance for an incremental memristor is: $M_{\mathrm{inc}} = R_1 + R_1 k_{\mathrm{n}}$ and the minimum is $M_{\mathrm{inc}} = R_1 - R_1 k_{\mathrm{n}}$, as shown in **Figure 18(a)**.

Reference	Approach	Learning synapse	Frequency (Hz)	Memristor	Active devices	
					Synapse	Neuron
[44]	FFNN	Yes	142	Emulator	69	5
[47]	SNN		5		2	3
[43]			30	HP model	2	13
[42]			300		2	8
[48]			100		–	–
[41]	MCNN	No	0.71		1	1
[45]	RNN	Yes	1		–	1

Table 2. Comparison among memristive neural networks.

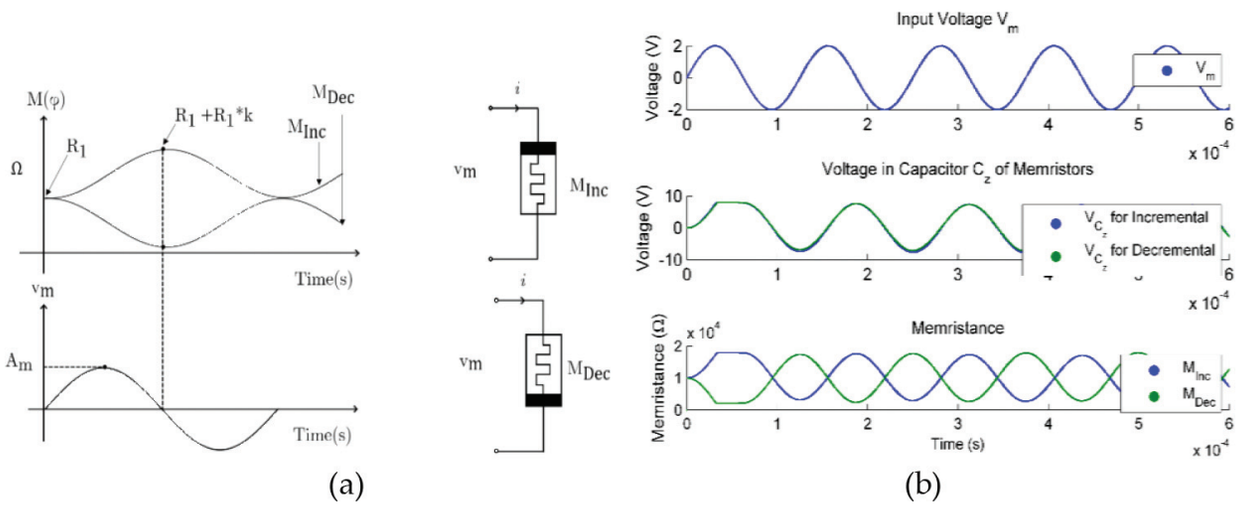

Figure 18. (a) Incremental and decremental memristance when $v_m = A_m \sin(\omega t,)$. (b) Simulation results of memristance for $A_m = 2$ V, $f = 8$ kHz and $k_n = 0.8$.

Considering that $k_n \in (0, 1)$, it is preferable to use $k_n \rightarrow 1$ to assure more range of variation; however, it is necessary to recall that memristance value is limited. In this frame of reference, several tests varying k_n were performed in HSPICE with incremental and decremental memristors tested separately and in different operating frequencies, as shown in **Figure 18(b)**. Nevertheless, secondary effects are observed when varying $k_n \rightarrow 0.8$, and therefore, the memristors have a different behaviour compared with **Figure 18(a)**, since in this case, the incremental and decremental memristance vary within the same range of memristance. In order to obtain the same behaviour of memristance from **Figure 1(a)** and for several operating frequencies, each discrete element must be updated according to **Table 3**. Note that the proposed topology takes advantage of memristance behaviour and uses only two flux-controlled floating memristor emulators, $M_1(\phi_m(t))$, configured as decremental and $M_2(\phi_m(t))$ as an incremental memristor, along with two passive resistors $R_a = R_b = 10$ kΩ, as shown in **Figure 19(a)** [50]. The analysis of **Figure 19(a)** is as follows: when a positive pulse is applied, $M_1(\varphi_m(t))$ decreases and $M_2(\varphi_m(t))$ increases. As a consequence, v_B decreases and v_A increases. Moreover, when a

Element	R_1	$R_2 = R_4$	R_3	C_z
F = 8 kHz	10 kΩ	100 kΩ	1.97 kΩ	2.5 nF
f = 10kHz				2 nF
f = 5kHz			3 kΩ	2.652 nF

Table 3. Component list of **Figure 1(a)** configured in several operating frequencies.

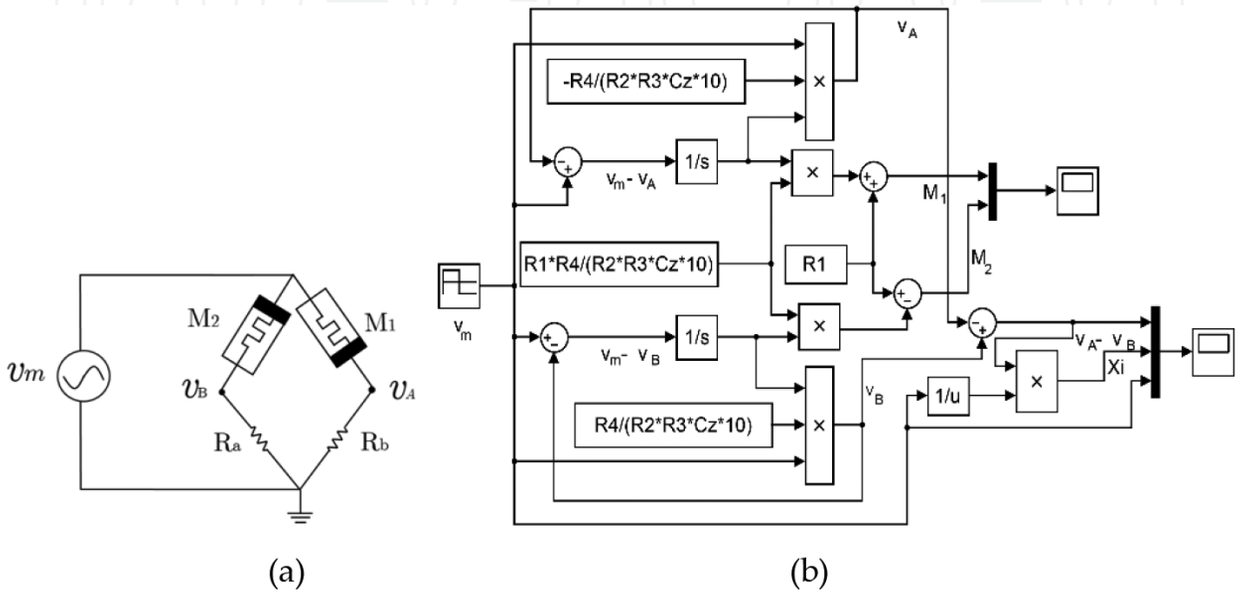

Figure 19. (a) Synaptic memristive bridge and (b) SIMULINK model of Eqs. (34)–(38).

negative pulse is applied, an inverted behaviour is glimpsed. Whether the pulse width is wide enough, the output voltage $v_{AB} = v_A - v_B$ varies gradually from negative to positive voltages and vice versa. Therefore, the memristances $M_1(\phi_m(t))$ and $M_2(\phi_m(t))$ are varied within $v_m - v_A$ and $v_m - v_B$ voltages, respectively. For synapse design, first the voltage v_2 was considered and it is described by

$$v_2 = \pm v_1 \alpha \int_0^t v_m(\tau) d\tau \tag{33}$$

Hence, considering Eq. (33), v_A and v_B are redefined as

$$v_A = -v_m(t)\alpha\varphi_{M_2}(t),\ \ \nu_A = \nu_m(t)\alpha\varphi_{M_1}(t) \tag{34}$$

where the magnetic flux of each memristor is

$$\phi_{M_1} = \int_0^t v_m(\tau) - v(\tau)_A d\tau,\ \ \phi_{M_2} = \int_0^t v_m(\tau) v(\tau)_B d\tau \tag{35}$$

Hence, v_{AB} and ξ, the weight, are obtained as

$$v_{\mathrm{AB}} = \alpha v_{\mathrm{m}}\left(\phi_{M_1}(\mathrm{t}) + \phi_{M_2}(\mathrm{t})\right),\ \ \xi = \frac{v_{\mathrm{AB}}}{v_{\mathrm{m}}} = \alpha\left(\phi_{M_1}(\mathrm{t}) + \phi_{M_2}(\mathrm{t})\right) \tag{36}$$

Memristance variation for $M_2(\phi_{\mathrm{m}}(t))$ is

$$M_2\left(\phi_{\mathrm{M}_2}(\mathrm{t})\right) = R_1 + R_1\alpha\phi_{M_2}(t) \tag{37}$$

Similarly, memristance variation for $M_1(\phi_{\mathrm{m}}(t))$ is:

$$M_1\left(\phi_{\mathrm{M}_1}(\mathrm{t})\right) = R_1 + R_1\alpha\phi_{M_1}(t) \tag{38}$$

As observed in Eqs. (37) and (38), the memristances depend on Eq. (35) and each memristor in the synapse is designed with the same parameters, so their memristances vary at same rate. From Eqs. (34)–(38), a SIMULINK model is built and depicted in **Figure 19(b)**. The synaptic memristive bridge was simulated in HSPICE and numerical simulations of **Figure 19(b)** were obtained at MATLAB. Thus, the memristance variation $M_1(\phi_{M_1}(t))$ and $M_2(\phi_{M_2}(t)$ are shown in **Figure 20**, respectively. The v_{AB} voltage for $k_{\mathrm{n}} = 0.8$ behave as sawtooth wave, as seen in **Figure 21**, and ξ is approximated by

$$\xi = \begin{cases} 49077t - 1.5338 & 0 \geq t \geq T/2 \\ -48567 + 4.5373 & T/2 \geq t \geq T \end{cases} \tag{39}$$

whose confidence level is $Q^2 = 0.996$. This value represents the linearity of ξ, if $Q^2 \rightarrow 1$ means that there is a linear relation between input pulses and ξ. To verify the behaviour of the synaptic memristive bridge, three basic steps are performed [44, 46].

1. ***Sign setting***. This stage refers to configure a positive sing or negative weight, and assures that ξ is within the desired range. Therefore, a bi-pulse signal with $v_{\mathrm{m}} = \pm 2$ V of amplitude configured at several frequencies is applied, as depicted in **Figure 22**. To configure a positive sign, it is necessary to apply a falling edge pulse, when a rising edge pulse is applied, a negative ξ is configured.

2. ***Weight setting***. Once the sign is established, it is necessary to apply a pulse width to set weight of the synapse. For the case 8 kHz, the allowed maximum pulse width is 62.5 μs, in the general case it is $T/2$. Therefore, pulse signal v_{m} with pulse width of range (0, $T/2$) is applied to set the weight to a desired ξ. In **Figure 22** a pulse v_{m} is shown whose pulse width is 2.5 μs which sets $\xi = -0.8495$.

3. ***Synaptic weight processing***. This operation refers to perform $v_s = \xi v_{\mathrm{p}}$, which is the multiplication of a narrow input pulse v_p and the pre-established ξ weight. The pulse width of v_{p} is narrow due to an effect called *memristance drifting* which is drifting of flux accumulation φ_{M_1} and φ_{M_1} caused by v_{p} [1, 40]. However, the response to that narrow pulse is governed by the settling time (*st*) and slew rate (*SR*) of multiplier AD633 used in the memristor emulator circuit, whose *st* = 2 μs at output voltage $V_0 = 20$ V and *SR* of 20 V/μs. The AD633 can be replaced by AD734 multiplier whose *SR* = 450 V/μs at $V_0 = 20$ V and *st* = 200 ns.

http://dx.doi.org/10.5772/intechopen.69291

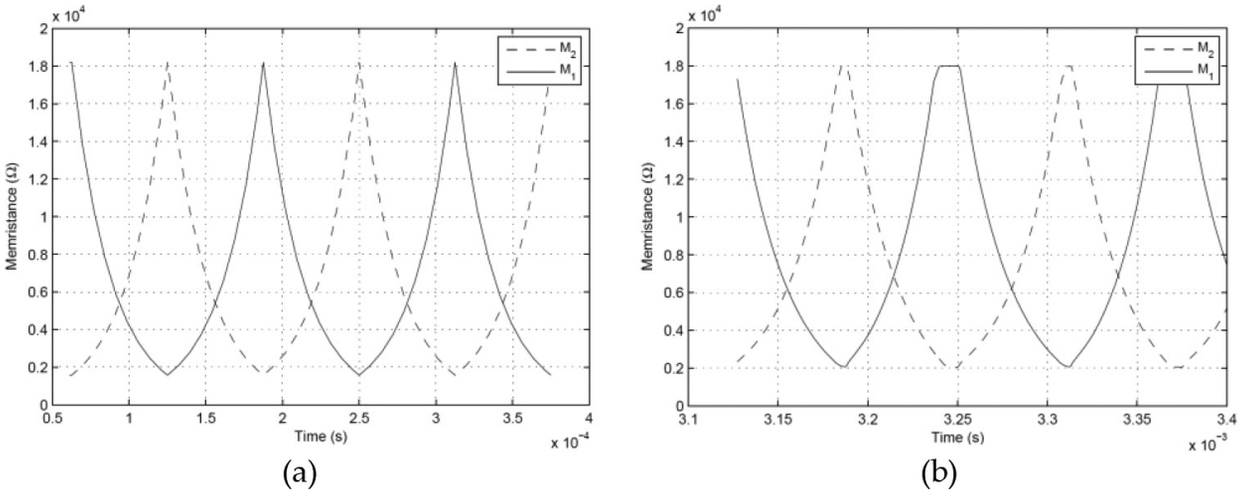

Figure 20. Memristance variations of **Figure 19(a)** when the bi-pulse signal $v_m = \pm 2$ V at 8 kHz is applied: (a) MATLAB® and (b) HSPICE®.

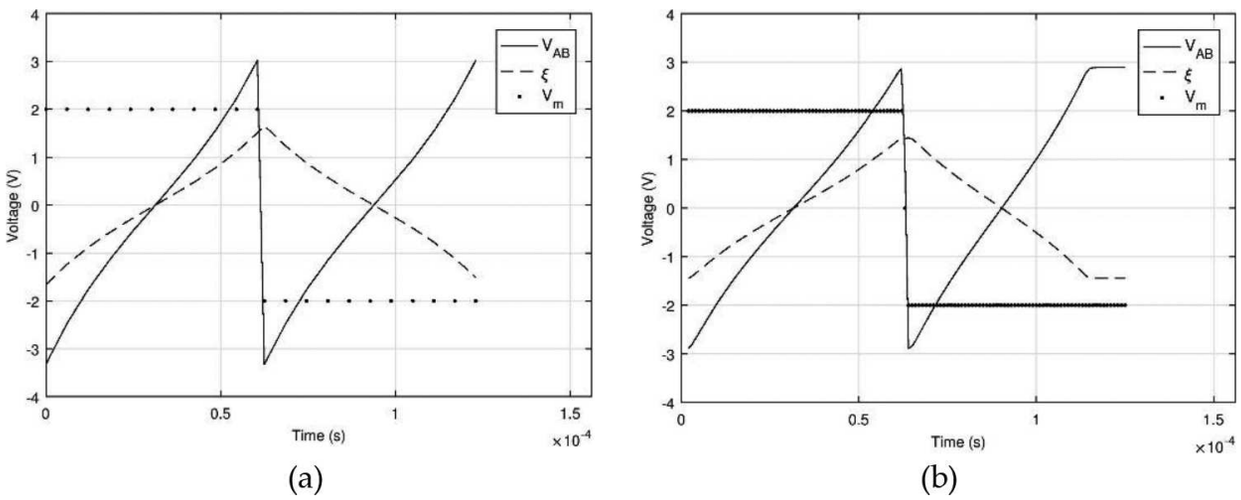

Figure 21. ξ variations of **Figure 19(a)** when the bi-pulse signal $v_m = \pm 2$ V at 8 kHz in (a) MATLAB® and (b) HSPICE®.

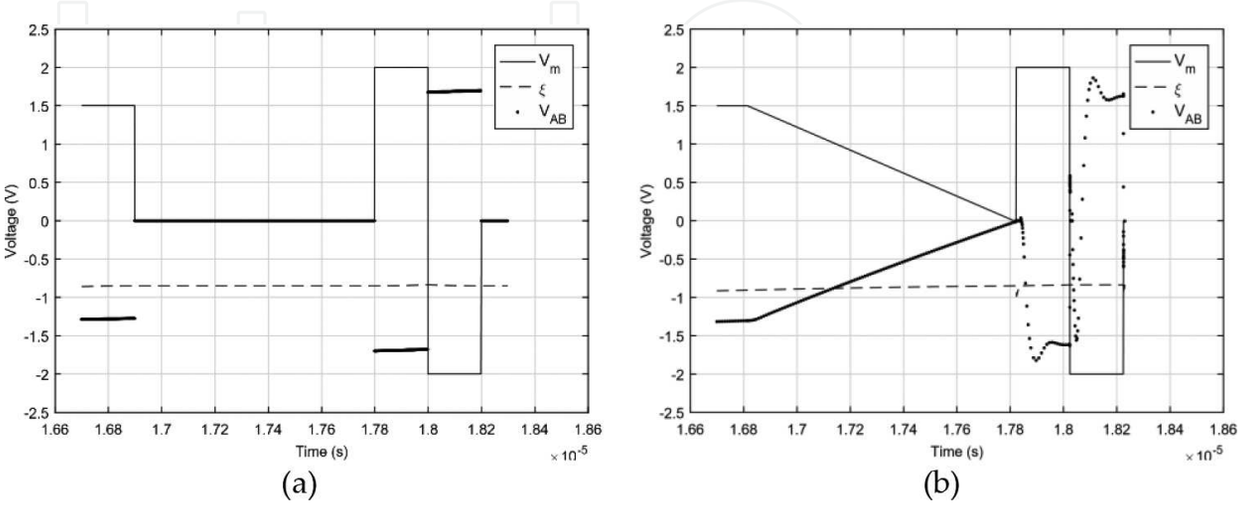

Figure 22. Synaptic multiplication when $\xi = 0.8495$ and a pulse signal $v_p = 1.5$ V of amplitude with pulse width of 200 ns is applied: (a) MATLAB results and (b) HSPICE simulations.

Finally, **Figure 22(a)** presents a MATLAB simulation of a pulse v_p = 2 V whose pulse width is 200 ns. This pulse is multiplied by ξ, obtaining $v_s = -1.699$. On the other hand, the synaptic weight processing at HSPICE shown in **Figure 22(b)** is done following the same methodology [50].

7. Conclusion

Memristor emulator circuits are useful for developing real memristor-based application circuits as well as for educational purposes. In this chapter, we have studied three memristor/memductor emulator circuits whose behaviour can be configured as incremental or decremental. Two of them are grounded versions whereas the latter is floated. The behavioural model for each topology was derived and its SIMULINK model was also programmed. The design guide suggested in this chapter provides a systematic way for designing memristor/memductor emulator circuits with good features. Further, an offset compensation technique was also described in order to achieve the frequency-dependent pinched hysteresis loop that does not deviate of the origin when the operating frequency of the input signal increases. As a result, it is predicted that the frequency behaviour of the pinched hysteresis loops of memristor/memductor emulator circuits can be pushed for operating in higher frequencies and holding a symmetrical behaviour, since the offset voltage glimpsed can again be reduced by updating the DC voltage sources. Moreover, a transformation methodology for obtaining the behaviour of inverse non-linear resistors from normal non-linear resistors has also been described, and as it was observed in Section 5, the methodology consists in replacing the integrator circuit, clearly defined in the normal topologies by a differentiator circuit, so that not only an inverse behaviour is obtained, but also the resulting topology is not drastically modified with respect to the original topology. Finally, three real analogue applications based on memristors/memductors were addressed.

Acknowledgements

This work was supported in part by the National Council for Science and Technology (CONACyT), Mexico, under Grant 222843 and in part by the Program to Strengthen Quality in Educational Institutions, under Grant C/PFCE-2016-29MSU0013Y-07-23.

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